



Automotive P-Channel 100 V (D-S) 175 °C MOSFET



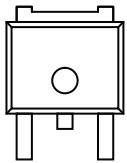
RoHS
COMPLIANT
HALOGEN
FREE

PRODUCT SUMMARY	
V _{DS} (V)	- 100
R _{DS(on)} (Ω) at V _{GS} = - 10 V	0.040
R _{DS(on)} (Ω) at V _{GS} = - 4.5 V	0.048
I _D (A)	- 38
Configuration	Single

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- Package with Low Thermal Resistance
- AEC-Q101 Qualified^d
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC

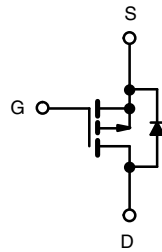
TO-252



G D S

Top View

Drain Connected to Tab



P-Channel MOSFET

ORDERING INFORMATION	
Package	TO-252
Lead (Pb)-free and Halogen-free	SQD40P10-40L-GE3

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	- 100	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current	I _D	T _C = 25 °C	- 38
		T _C = 125 °C	- 22
Continuous Source Current (Diode Conduction) ^a	I _S	- 50	A
Pulsed Drain Current ^b	I _{DM}	- 150	
Single Pulse Avalanche Current	I _{AS}	- 44	
Single Pulse Avalanche Energy	E _{AS}	96	mJ
Maximum Power Dissipation ^b	P _D	T _C = 25 °C	136
		T _C = 125 °C	45
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to + 175	°C

THERMAL RESISTANCE RATINGS			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient	R _{thJA}	50	°C/W
Junction-to-Case (Drain)	R _{thJC}	1.1	

Notes

- Package limited.
- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- When mounted on 1" square PCB (FR-4 material).
- Parametric verification ongoing.



SPECIFICATIONS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$		-100	-	-	V
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$		-1.0	-2.0	-2.5	
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}$	$V_{DS} = -100\text{ V}$	-	-	-1	μA
		$V_{GS} = 0\text{ V}$	$V_{DS} = -100\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	-50	
		$V_{GS} = 0\text{ V}$	$V_{DS} = -100\text{ V}, T_J = 175\text{ }^\circ\text{C}$	-	-	-250	
On-State Drain Current ^a	$I_{D(on)}$	$V_{GS} = -10\text{ V}$	$V_{DS} \leq -5\text{ V}$	-30	-	-	A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -10\text{ V}$	$I_D = -9.2\text{ A}$	-	0.033	0.040	Ω
		$V_{GS} = -10\text{ V}$	$I_D = -9.2\text{ A}, T_J = 125\text{ }^\circ\text{C}$	-	-	0.074	
		$V_{GS} = -10\text{ V}$	$I_D = -9.2\text{ A}, T_J = 175\text{ }^\circ\text{C}$	-	-	0.093	
		$V_{GS} = -4.5\text{ V}$	$I_D = -7.7\text{ A}$	-	0.037	0.048	
Forward Transconductance ^b	g_{fs}	$V_{DS} = -15\text{ V}, I_D = -9.2\text{ A}$		-	35	-	S
Dynamic^b							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$	$V_{DS} = -25\text{ V}, f = 1\text{ MHz}$	-	4433	5545	μF
Output Capacitance	C_{oss}			-	301	380	
Reverse Transfer Capacitance	C_{rss}			-	208	260	
Total Gate Charge ^c	Q_g	$V_{GS} = -10\text{ V}$	$V_{DS} = -50\text{ V}, I_D = -9.2\text{ A}$	-	96	144	nC
Gate-Source Charge ^c	Q_{gs}			-	8.4	-	
Gate-Drain Charge ^c	Q_{gd}			-	23.5	-	
Gate Resistance	R_g	f = 1 MHz		1.5	3.13	4.7	Ω
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = -50\text{ V}, R_L = 6.49\text{ }\Omega$ $I_D \cong -7.7\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1.0\text{ }\Omega$		-	11	17	ns
Rise Time ^c	t_r			-	11	17	
Turn-Off Delay Time ^c	$t_{d(off)}$			-	78	117	
Fall Time ^c	t_f			-	15	23	
Source-Drain Diode Ratings and Characteristics^b							
Pulsed Current ^a	I_{SM}			-	-	-150	A
Forward Voltage	V_{SD}	$I_F = -7.7\text{ A}, V_{GS} = 0\text{ V}$		-	-0.8	-1.5	V

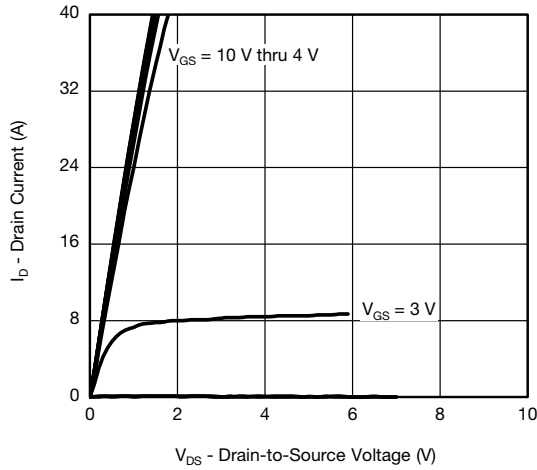
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

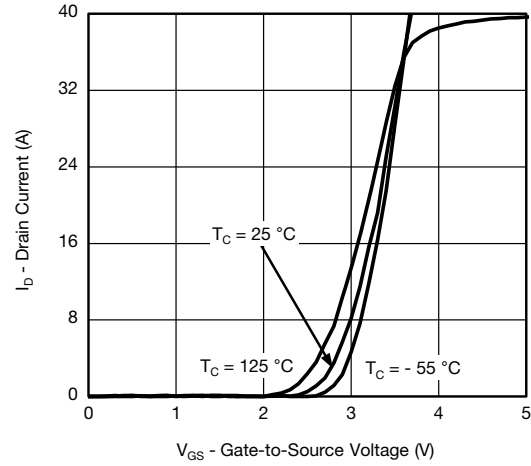
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



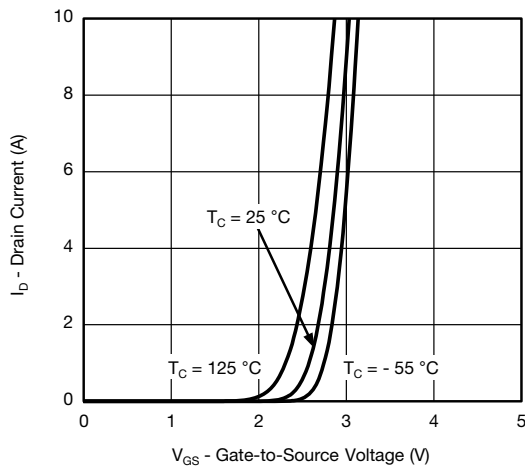
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



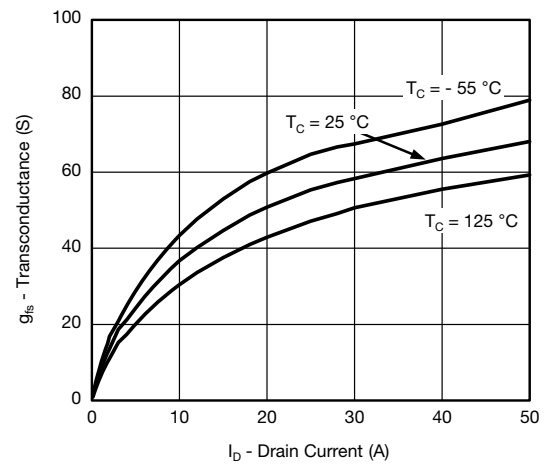
Output Characteristics



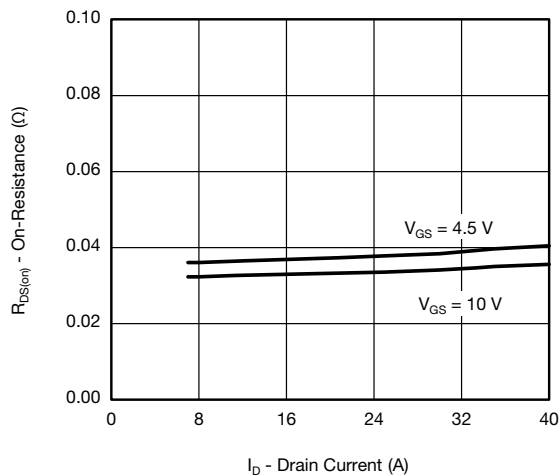
Transfer Characteristics



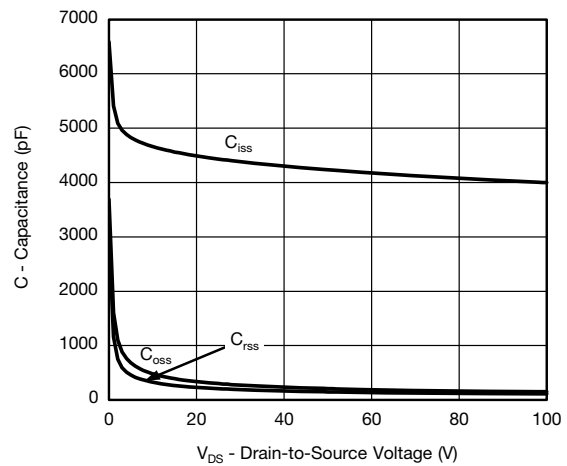
Transfer Characteristics



Transconductance

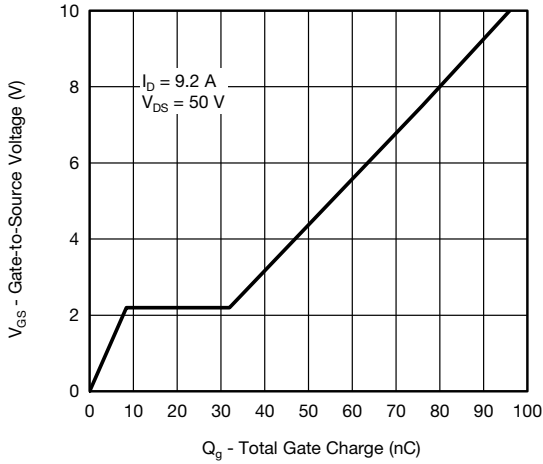


On-Resistance vs. Drain Current

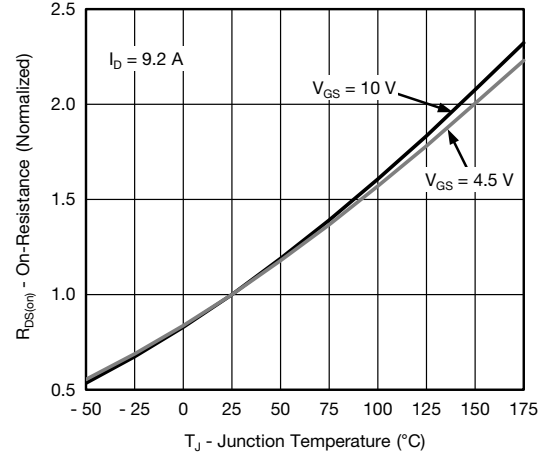


Capacitance

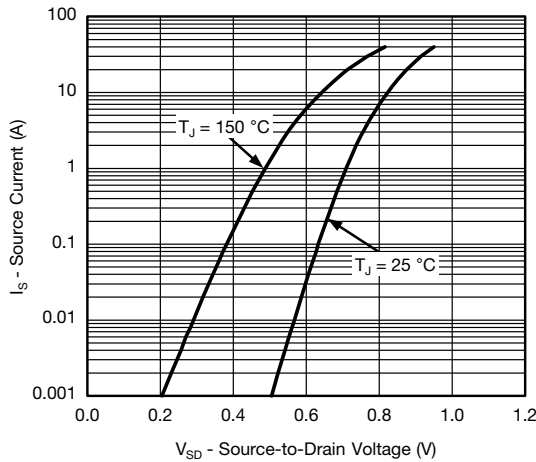
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



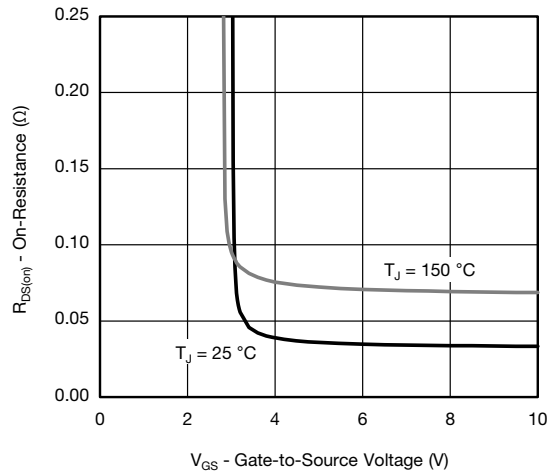
Gate Charge



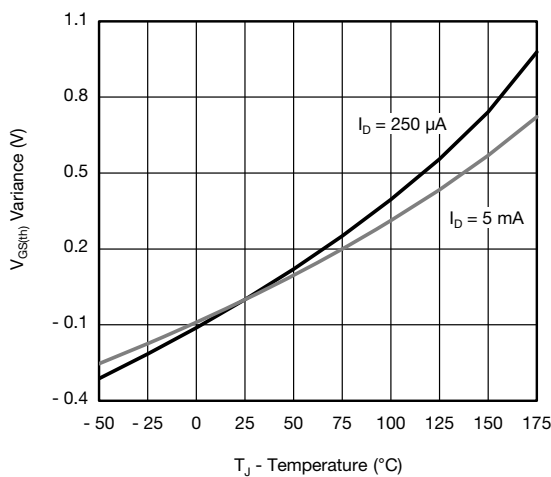
On-Resistance vs. Junction Temperature



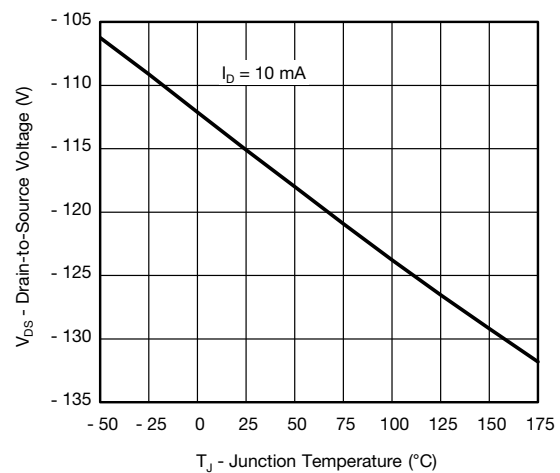
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



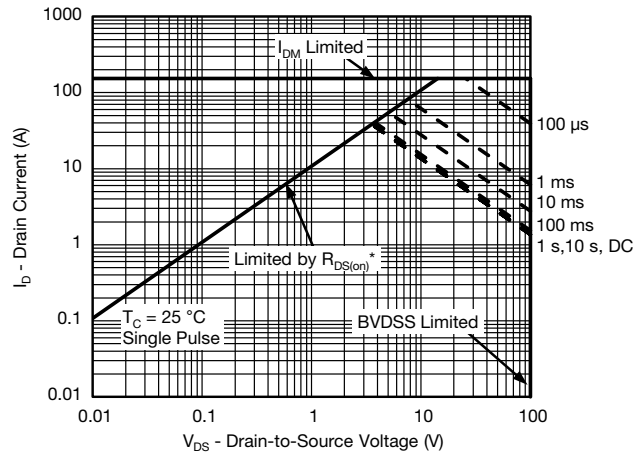
Threshold Voltage



Drain Source Breakdown vs. Junction Temperature

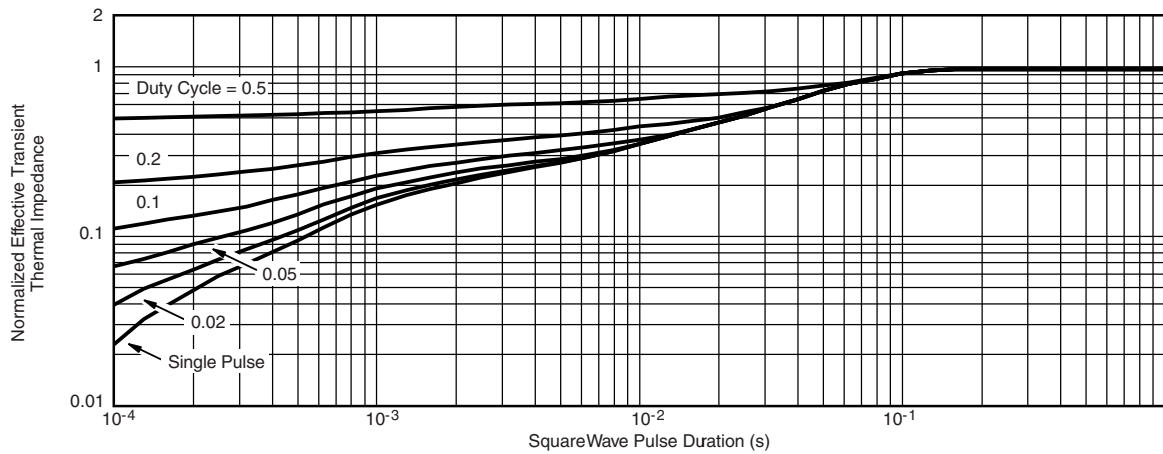


THERMAL RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)

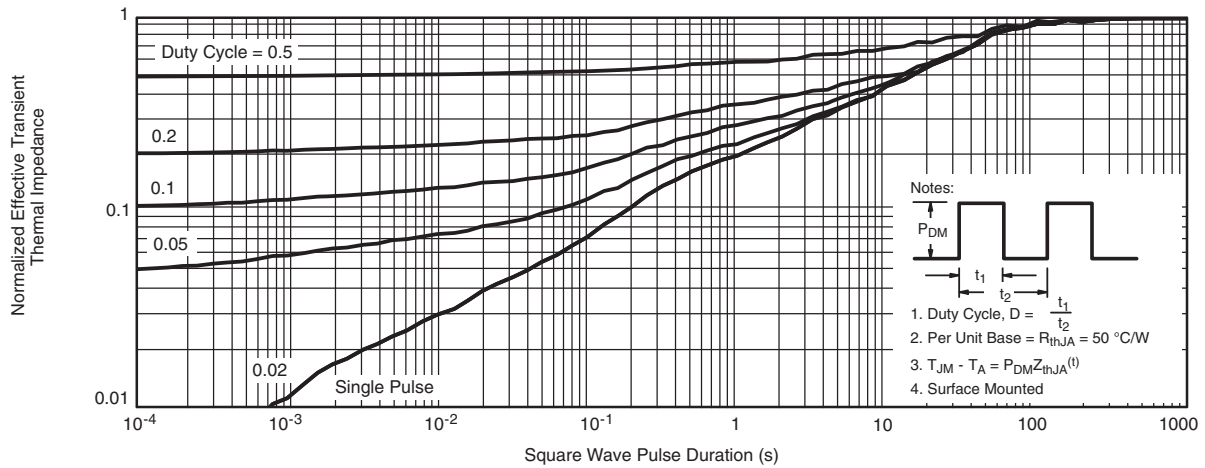


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

THERMAL RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Ambient
Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction to Ambient ($25\text{ }^\circ\text{C}$)
 - Normalized Transient Thermal Impedance Junction to Case ($25\text{ }^\circ\text{C}$)
 are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

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DPAK / TO-252 and Reverse DPAK

Ordering codes for the SQ rugged series power MOSFETs in the DPAK / TO-252 and Reverse DPAK packages:

Table with 3 columns: DATASHEET PART NUMBER, OLD ORDERING CODE a, NEW ORDERING CODE. Lists various MOSFET part numbers and their corresponding ordering codes.

Note

a. Old ordering code is obsolete and no longer valid for new orders



TO-252AA Case Outline



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060
ECN: T13-0592-Rev. A, 02-Sep-13				
DWG: 6019				

Note

- Dimension L3 is for reference only.

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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