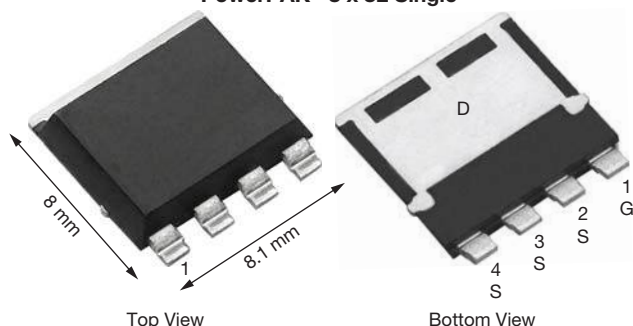


# Automotive N-Channel 40 V (D-S) 175 °C MOSFET

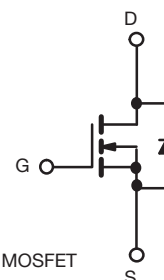
**PowerPAK® 8 x 8L Single**


## FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 %  $R_g$  and UIS tested
- Thin 1.9 mm height
- Material categorization:  
for definitions of compliance please see  
[www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**



N-Channel MOSFET

PRODUCT SUMMARY	
$V_{DS}$ (V)	40
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = 10$ V	0.0015
$I_D$ (A)	200
Configuration	Single
Package	PowerPAK 8 x 8L

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		$V_{DS}$	40	V
Gate-source voltage		$V_{GS}$	$\pm 20$	
Continuous drain current	$T_C = 25$ °C <sup>a</sup>	$I_D$	200	A
	$T_C = 125$ °C		141	
Continuous source current (diode conduction)		$I_S$	136	
Pulsed drain current <sup>b</sup>		$I_{DM}$	600	
Single pulse avalanche current	L = 0.1 mH	$I_{AS}$	70	
		$E_{AS}$	245	mJ
Maximum power dissipation	$T_C = 25$ °C	$P_D$	150	W
	$T_C = 125$ °C		50	
Operating junction and storage temperature range		$T_J, T_{stg}$	-55 to +175	°C
Soldering recommendations (peak temperature) <sup>d, e</sup>			260	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount <sup>c</sup>	$R_{thJA}$	50	°C/W
Junction-to-case (drain)		$R_{thJC}$	1	

## Notes

- Package limited.
- Pulse test; pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2$  %.
- When mounted on 1" square PCB (FR4 material).
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK 8 x 8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.



SPECIFICATIONS (T <sub>C</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0, I <sub>D</sub> = 250 μA		40	-	-	V
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.5	3	3.5	
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 40 V	-	-	1	μA
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 40 V, T <sub>J</sub> = 125 °C	-	-	50	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 40 V, T <sub>J</sub> = 175 °C	-	-	500	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> ≥ 5 V	100	-	-	A
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A	-	0.0011	0.0015	Ω
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A, T <sub>J</sub> = 125 °C	-	-	0.0021	
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A, T <sub>J</sub> = 175 °C	-	-	0.0025	
Forward transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 15 A		-	122	-	S
Dynamic <sup>b</sup>							
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 25 V, f = 1 MHz	-	11 367	14 780	pF
Output capacitance	C <sub>oss</sub>			-	6000	7800	
Reverse transfer capacitance	C <sub>rss</sub>			-	615	800	
Total gate charge <sup>c</sup>	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> = 20 V, I <sub>D</sub> = 10 A	-	125	165	nC
Gate-source charge <sup>c</sup>	Q <sub>gs</sub>			-	35	-	
Gate-drain charge <sup>c</sup>	Q <sub>gd</sub>			-	13	-	
Gate resistance	R <sub>g</sub>	f = 1 MHz		0.45	0.99	1.50	Ω
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 20 V, R <sub>L</sub> = 2 Ω I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω		-	22	32	ns
Rise time <sup>c</sup>	t <sub>r</sub>			-	8	14	
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>			-	52	73	
Fall time <sup>c</sup>	t <sub>f</sub>			-	14	20	
Source-Drain Diode Ratings and Characteristics <sup>b</sup>							
Pulsed current <sup>a</sup>	I <sub>SM</sub>			-	-	200	A
Forward voltage	V <sub>SD</sub>	I <sub>F</sub> = 50 A, V <sub>GS</sub> = 0 V		-	0.8	1.1	V

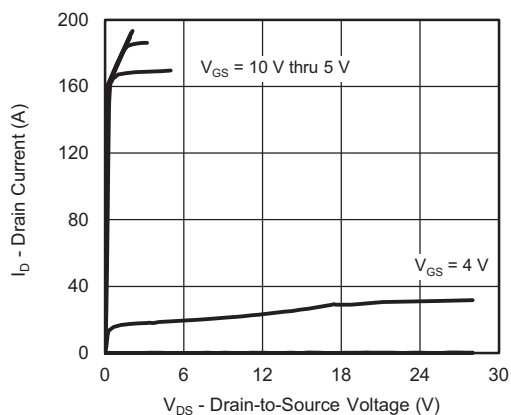
**Notes**

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.  
b. Guaranteed by design, not subject to production testing.  
c. Independent of operating temperature.

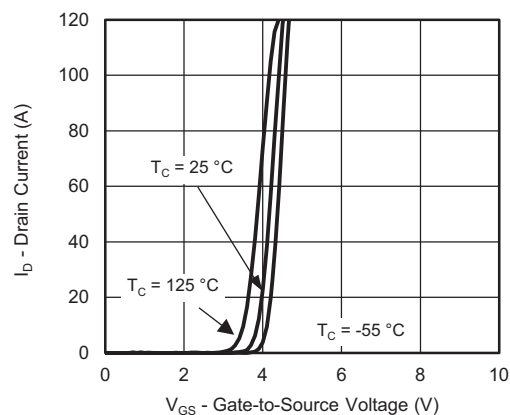
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



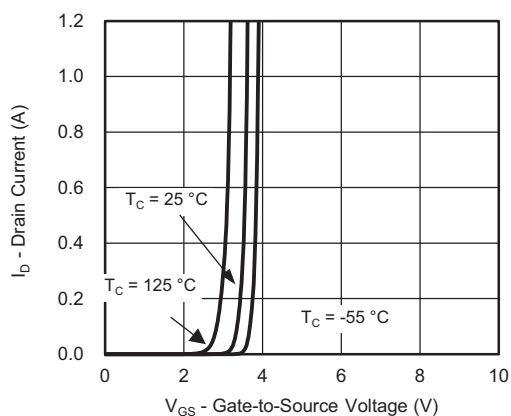
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



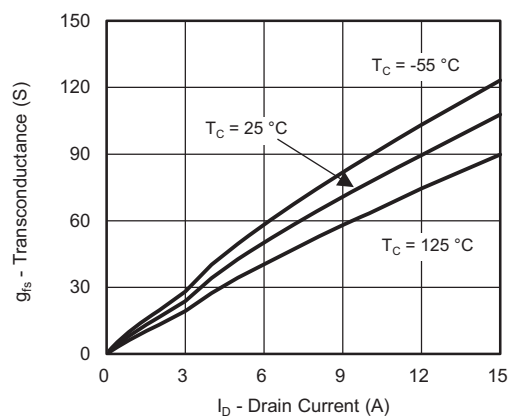
**Output Characteristics**



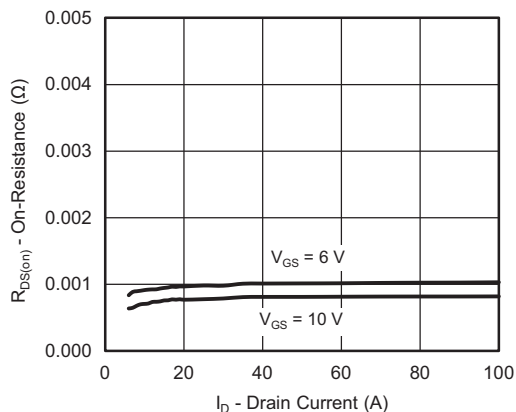
**Transfer Characteristics**



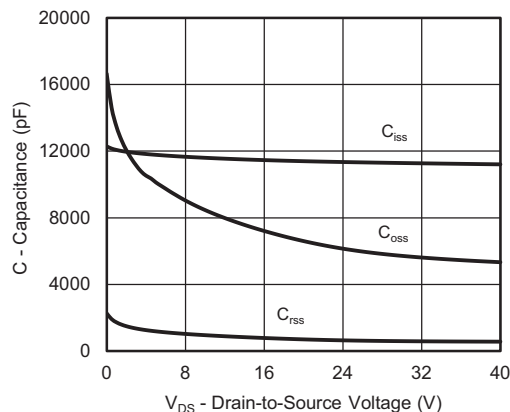
**Transfer Characteristics**



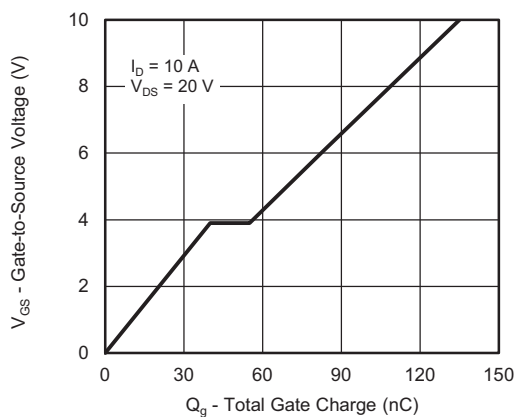
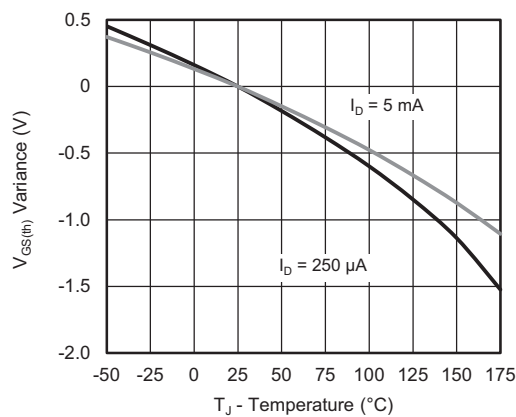
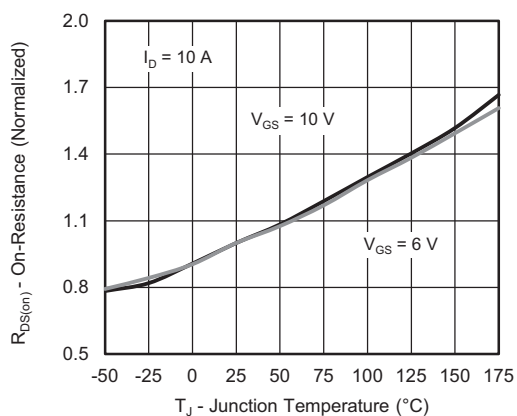
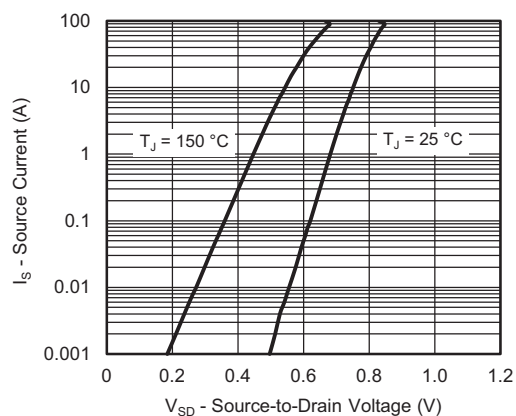
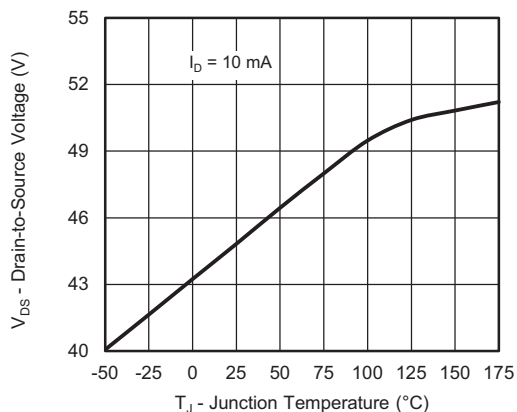
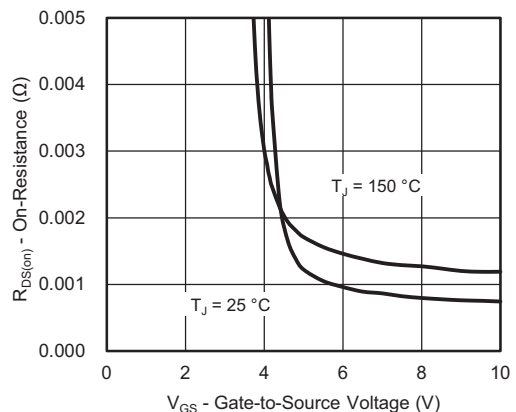
**Transconductance**



**On-Resistance vs. Drain Current**

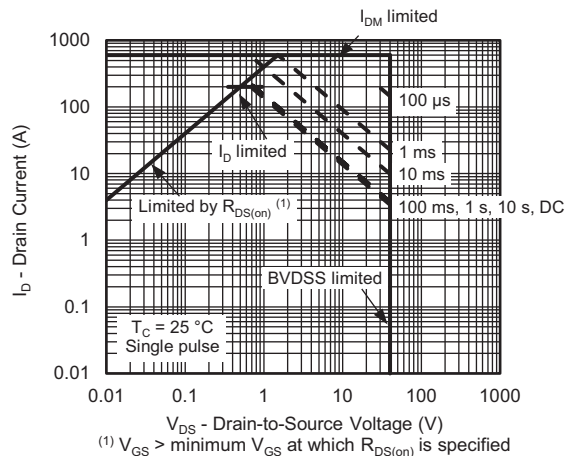


**Capacitance**

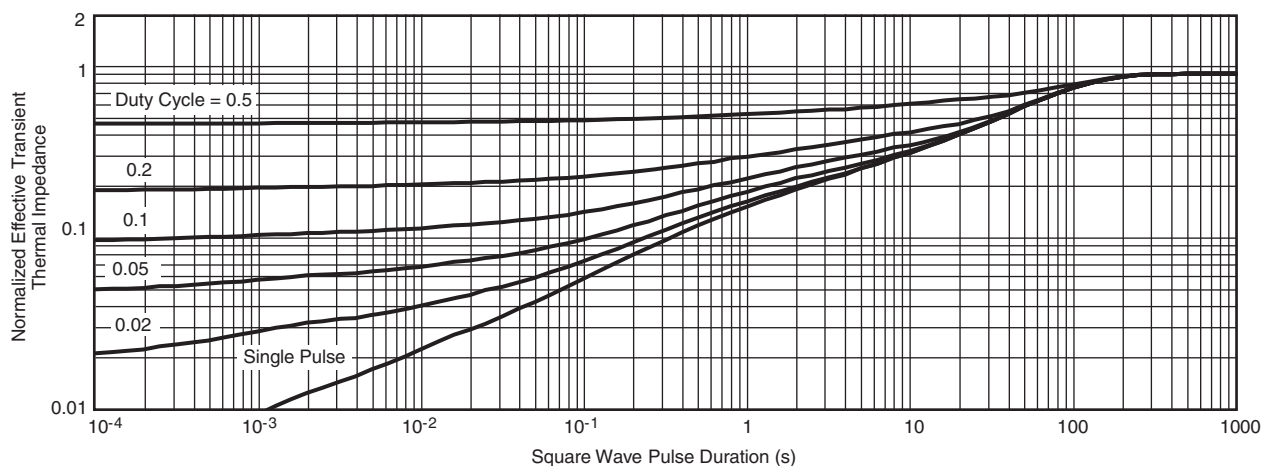
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

**Gate Charge**

**Threshold Voltage**

**On-Resistance vs. Junction Temperature**

**Source Drain Diode Forward Voltage**

**Drain Source Breakdown vs. Junction Temperature**

**On-Resistance vs. Gate-to-Source Voltage**



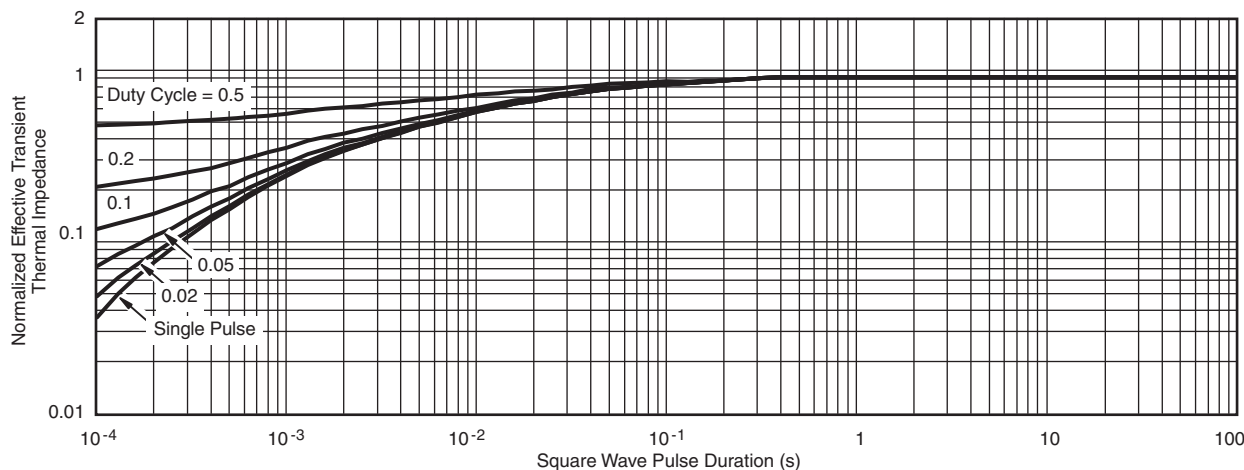
**THERMAL RATINGS** ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)



**Safe Operating Area**



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**

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