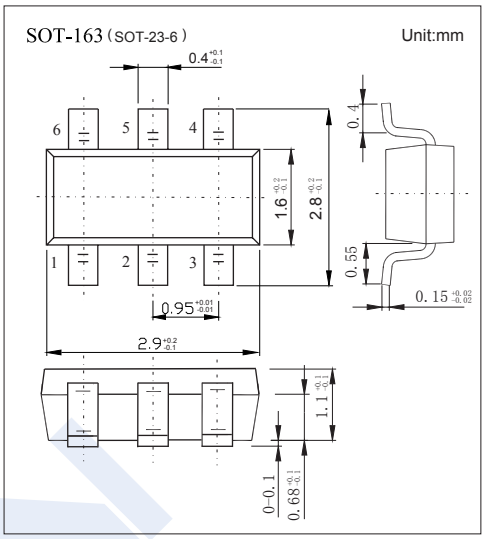
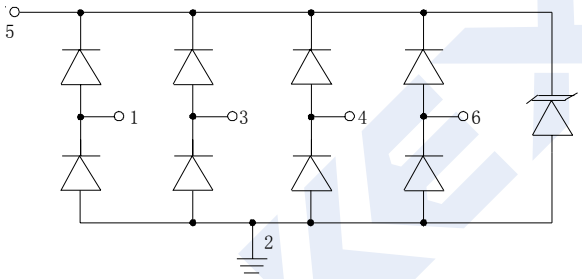
# Low Capacitance TVS Diode Array

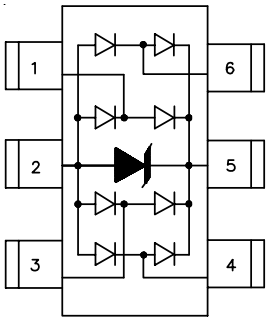
# SRV05-4




## ■ Features

- ESD protection for high-speed data lines to
  IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
  IEC 61000-4-4 (EFT) 40A (5/50ns)
  IEC 61000-4-5 (Lightning) 12A (8/20μs)
- Protects four I/O lines
- Low capacitance: 3pF typical
- Low clamping voltage
- Low operating voltage: 5V




## ■ Absolute Maximum Ratings Ta = 25℃

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| ESD per IEC 61000-4-2 (Air) | $V_{ESD}$ | 15 | KV |
| ESD per IEC 61000-4-2 (Contact) | | 8 | |
| Peak Pulse Current (tp = 8/20μs) | $I_{PP}$ | 12 | A |
| Peak Pulse Power (tp = 8/20μs) | $P_{PK}$ | 300 | W |
| Lead Soldering Temperature | $T_L$ | 260 (10 Sec) | ℃ |
| Junction Temperature | $T_J$ | 125 | |
| Storage Temperature range | $T_{stg}$ | -55 to 150 | |

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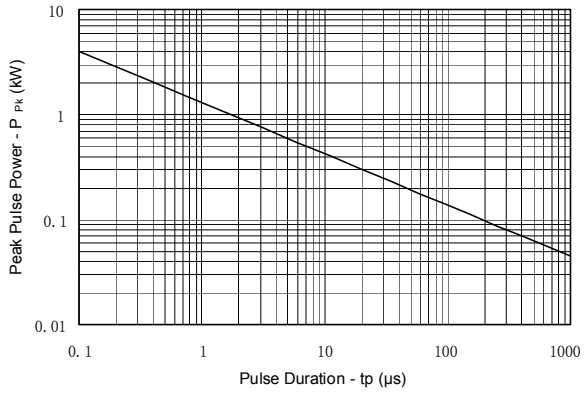
## ■ Electrical Characteristics Ta = 25℃

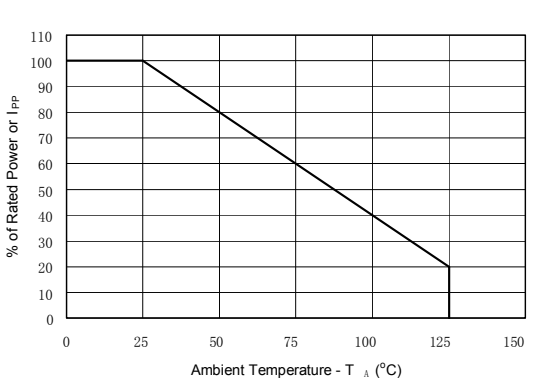
| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Reverse Stand-Off Voltage | $V_{RWM}$ | Pin 5 to 2 | | | 5 | V |
| Reverse Breakdown Voltage | $V_{BR}$ | $I_t$= 1 mA Pin 5 to 2 | 6 | | | |
| Forward voltage | $V_F$ | $I_F$= 15 mA | | | 1.2 | |
| Clamping Voltage | $V_C$ | $I_{PP}$ = 1A, tp = 8/20μs<br>Any I/O pin to Ground | | | 12.5 | |
| | | $I_{PP}$ = 5A, tp = 8/20μs<br>Any I/O pin to Ground | | | 17.5 | |
| Reverse voltage leakage current | $I_R$ | $V_{RWM}$ = 5V, T=25°C<br>Pin 5 to 2 | | | 5 | uA |
| Junction Capacitance | $C_J$ | $V_R$ = 0V, f = 1MHz<br>Any I/O pin to Ground | | 3 | 5 | pF |
| | | $V_R$ = 0V, f = 1MHz<br>Between I/O pins | | 1.5 | | |

## ■ Marking

| Marking | V05 |
|---|---|

## ■ Typical Characterisitics



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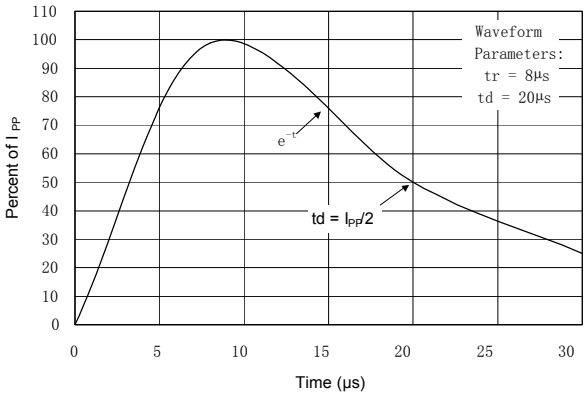
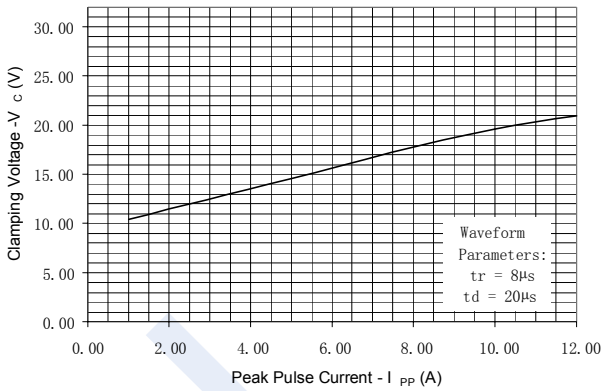
## ■ Typical Characterisitics

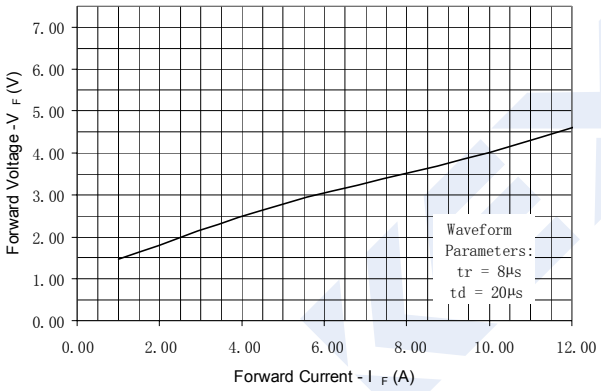
### Pulse Waveform



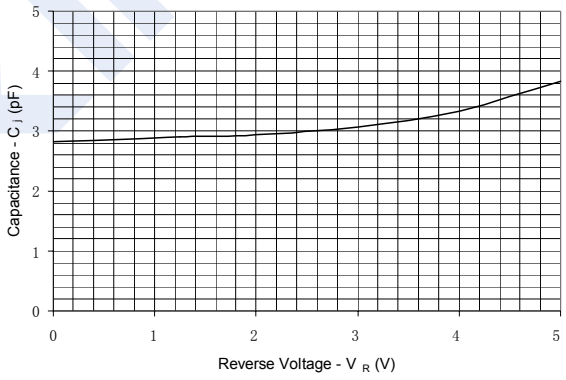

### Clamping Voltage vs. Peak Pulse Current



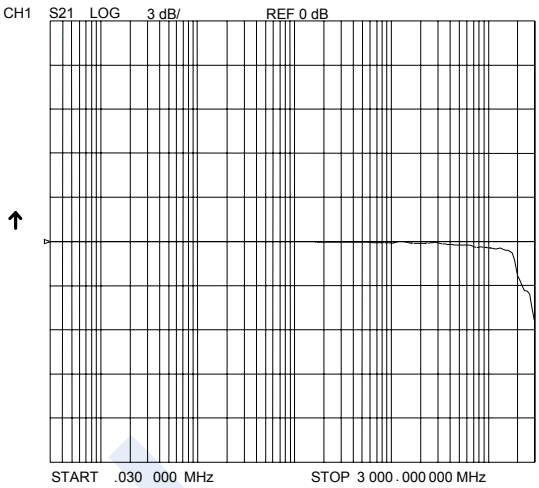

### Forward Voltage vs. Forward Current



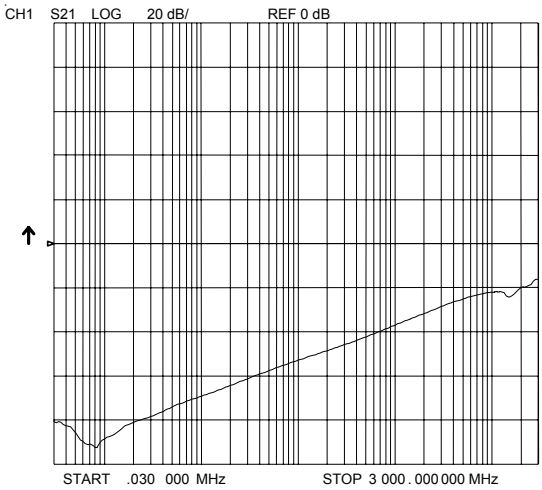

### Capacitance vs. Reverse Voltage




### Insertion Loss S21




### Analog Cross Talk



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### Device Connection Options for Protection of Four High-Speed Data Lines

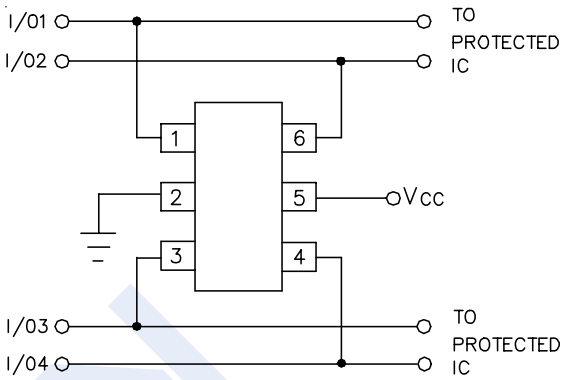
The SRV05-4 TVS is designed to protect four data lines from transient over-voltages by clamping them to a fixed reference. When the voltage on the protected line exceeds the reference voltage (plus diode $V_F$) the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. Data lines are connected at pins 1, 3, 4 and 6. The negative reference (REF1) is connected at pin 2. This pin should be connected directly to a ground plane on the board for best results. The path length is kept as short as possible to minimize parasitic inductance. The positive reference (REF2) is connected at pin 5. The options for connecting the positive reference are as follows:

1. To protect data lines and the power line, connect pin 5 directly to the positive supply rail ($V_{CC}$). In this configuration the data lines are referenced to the supply voltage. The internal TVS diode prevents over-voltage on the supply rail.
2. The SRV05-4 can be isolated from the power supply by adding a series resistor between pin 5 and $V_{CC}$. A value of 100k is recommended. The internal TVS and steering diodes remain biased, providing the advantage of lower capacitance.
3. In applications where no positive supply reference is available, or complete supply isolation is desired, the internal TVS may be used as the reference. In this case, pin 5 is not connected. The steering diodes will begin to conduct when the voltage on the protected line exceeds the working voltage of the TVS (plus one diode drop).

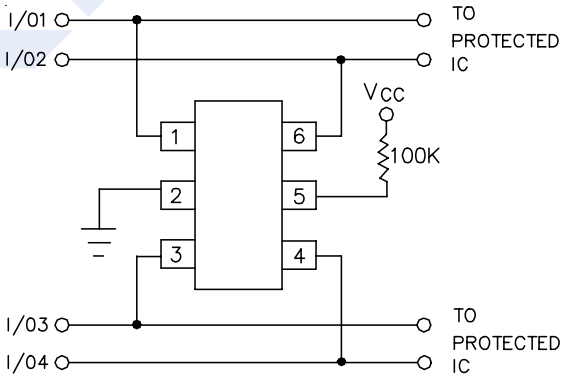
### ESD Protection With RailClamps

RailClamps are optimized for ESD protection using the rail-to-rail topology. Along with good board layout, these devices virtually eliminate the disadvantages of using discrete components to implement this topology. Consider the situation shown in Figure 1 where discrete diodes or diode arrays are configured for rail-to-rail protection on a high speed line. During positive duration ESD events, the top diode will be forward biased when the voltage on the protected line exceeds

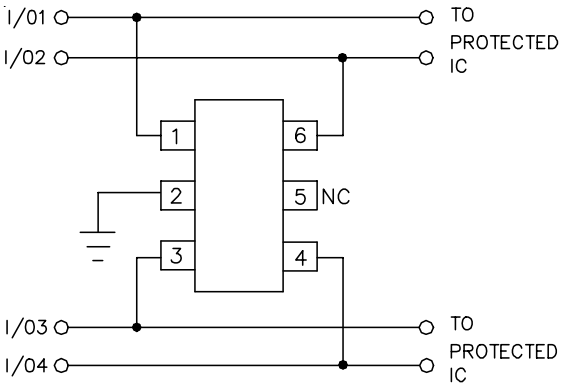
Data Line and Power Supply Protection Using Vcc as reference




Data Line Protection with Bias and Power Supply Isolation Resistor




Data Line Protection Using Internal TVS Diode as Reference



# Low Capacitance TVS Diode Array

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the reference voltage plus the $V_F$ drop of the diode. For negative events, the bottom diode will be biased when the voltage exceeds the $V_F$ of the diode. At first approximation, the clamping voltage due to the characteristics of the protection diodes is given by:

$V_C = V_{CC} + V_F$ (for positive duration pulses)
$V_C = -V_F$ (for negative duration pulses)

However, for fast rise time transient events, the effects of parasitic inductance must also be considered as shown in Figure 2. Therefore, the actual clamping voltage seen by the protected circuit will be:

$V_C = V_{CC} + V_F + L_P \, di_{ESD}/dt$ (for positive duration pulses)
$V_C = -V_F - L_G di_{ESD}/dt$ (for negative duration pulses)

ESD current reaches a peak amplitude of 30A in 1ns for a level 4 ESD contact discharge per IEC 61000-4-2. Therefore, the voltage overshoot due to 1nH of series inductance is:

$V = L_P \, di_{ESD}/dt = 1X10^{-9} (30 / 1X10^{-9}) = 30V$

Example:
Consider a $V_{CC}$ = 5V, a typical $V_F$ of 30V (at 30A) for the steering diode and a series trace inductance of 10nH. The clamping voltage seen by the protected IC for a positive 8kV (30A) ESD pulse will be:

$V_C = 5V + 30V + (10nH \times 30V/nH) = 335V$

This does not take into account that the ESD current is directed into the supply rail, potentially damaging any components that are attached to that rail. Also note that it is not uncommon for the $V_F$ of discrete diodes to exceed the damage threshold of the protected IC. This is due to the relatively small junction area of typical discrete components. It is also possible that the power dissipation capability of the discrete diode will be exceeded, thus destroying the device.

The RailClamp is designed to overcome the inherent disadvantages of using discrete signal diodes for ESD suppression. The RailClamp's integrated TVS diode

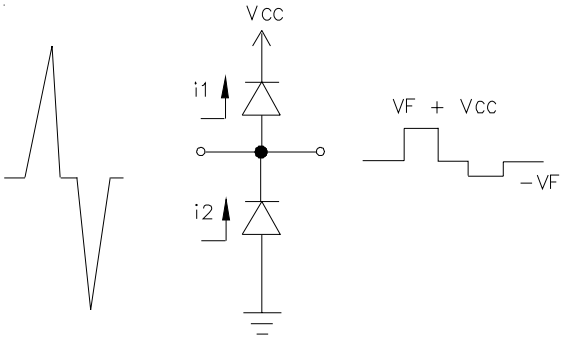


**Figure 1 - "Rail-To-Rail" Protection Topology (First Approximation)**

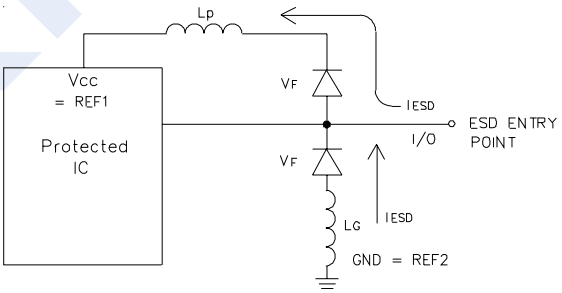


**Figure 2 - The Effects of Parasitic Inductance When Using Discrete Components to Implement Rail-To-Rail Protection**

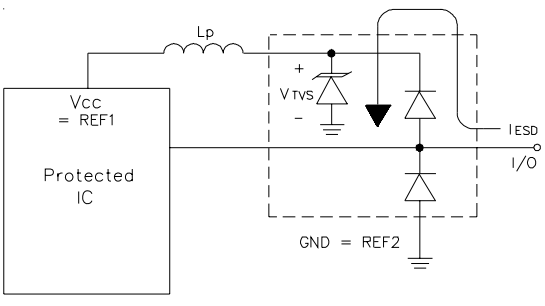


**Figure 3 - Rail-To-Rail Protection Using RailClamp TVS Arrays**

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helps to mitigate the effects of parasitic inductance in the power supply connection. During an ESD event, the current will be directed through the integrated TVS diode to ground. The maximum voltage seen by the protected IC due to this path will be the clamping voltage of the device.

Video Interface Protection

Video interfaces are susceptible to transient voltages resulting from electrostatic discharge (ESD) and “hot plugging” cables. If left unprotected, the video interface IC may be damaged or even destroyed. Protecting a high-speed video port presents some unique challenges. First, any added protection device must have extremely low capacitance and low leakage current so that the integrity of the video signal is not compromised. Second, the protection component must be able to absorb high voltage transients without damage or degradation. As a minimum, the device should be rated to handle ESD voltages per IEC 61000-4-2, level 4 (±15kV air, ±8kV contact). The clamping voltage of the device (when conducting high current ESD pulses) must be sufficiently low enough to protect the sensitive CMOS IC. If the clamping voltage is too high, the “protected” device may latch-up or be destroyed. Finally, the device must take up a relatively small amount of board space, particularly in portable applications such as notebooks and handhelds. The SRV05-4 is designed to meet or exceed all of the above criteria. A typical video interface protection circuit is shown in Figure 4. All exposed lines are protected including R, G, B, H-Sync, V-Sync , and the ID lines for plug and play monitors.

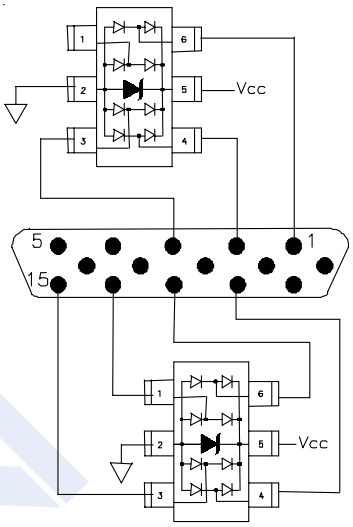


Figure 4 - Video Interface Protection

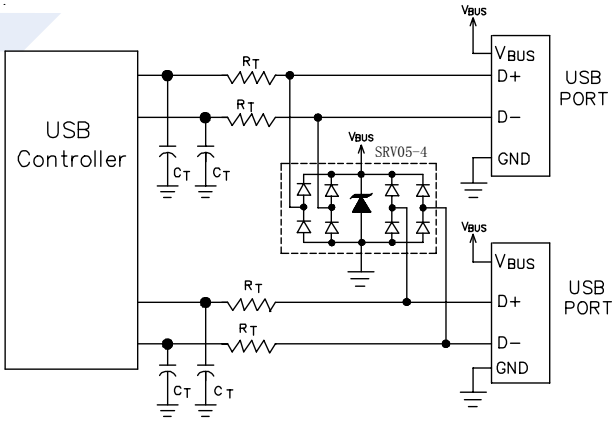


Figure 5 - Dual USB Port Protection

Universal Serial Bus ESD Protection

The SRV05-4 may also be used to protect the USB ports on monitors, computers, peripherals or portable systems. Each device will protect up to two USB ports (Figure 5). When the voltage on the data lines exceed the bus voltage (plus one diode drop), the internal rectifiers are forward biased conducting the transient current away from the protected controller chip. The TVS diode directs the surge to ground. The TVS diode also acts to suppress ESD strikes directly on the voltage bus. Thus, both power and data pins are protected with a single device.

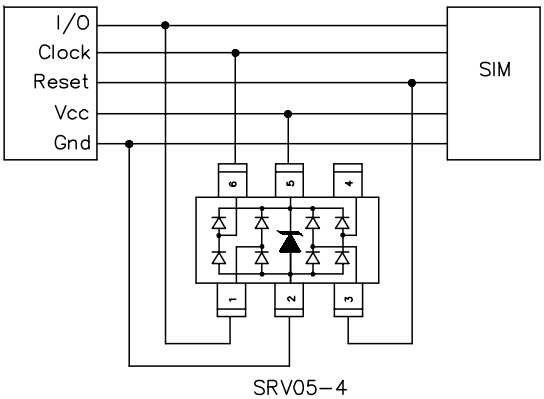


Figure 6 - SIM Port

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DVI Protection

The small geometry of a typical digital-visual interface (DVI) graphic chip will make it more susceptible to electrostatic discharges (ESD) and cable discharge events (CDE). Transient protection of a DVI port can be challenging. Digital-visual interfaces can often transmit and receive at a rate equal to or above 1Gbps. The high-speed data transmission requires the protection device to have low capacitance to maintain signal integrity and low clamping voltage to reduce stress on the protected IC. The SRV05-4 has a low typical insertion loss of <0.4dB at 1GHz (I/O to ground) to ensure signal integrity and can protect the DVI interface to the 8kV contact and 15kV air ESD per IEC 61000-4-2 and CDE.

Figure 7 shows how to design the SRV05-4 into the DVI circuit on a flat panel display and a PC graphic card. The SRV05-4 is configured to provide common mode and differential mode protection. The internal TVS of the SRV05-4 acts as a 5 volt reference. The power pin of the DVI circuit does not come out through the connector and is not subjected to external ESD pulse; therefore, pin 5 should be left unconnected. Connecting pin 5 to Vcc of the DVI circuit may result in damage to the chip from ESD current.

10/100 ETHERNET PROTECTION

Ethernet ICs are vulnerable to damage from electro-static discharge (ESD). The internal protection in the PHY chip, if any, often is not enough due to the high energy of the discharges specified by IEC 61000-4-2. If the discharge is catastrophic, it will destroy the protected IC. If it isless severe, it will cause latent failures that are very difficult to find.

10/100 Ethernet operates at 125MHz clock over a twisted pair interface. In a typical system, the twisted-pair interface for each port consists of two differential signal pairs: one for the transmitter and one for the receiver, with the transmitter input being the most sensitive to damage. The fatal discharge occurs differentially across the transmit or receive line pair and is capacitively coupled through the transformer to the Ethernet chip. Figure 8 shows how to design the SRV05-4 on the line side of a 10/100 ethernet port to provide differential mode protection. The common mode isolation of the transformer will provide common mode protection to the rating of the transformer isolation which is usually >1.5kV. If more common mode protection is needed, figure 9 shows how to design the SRV05-4 on the IC side of the 10/100

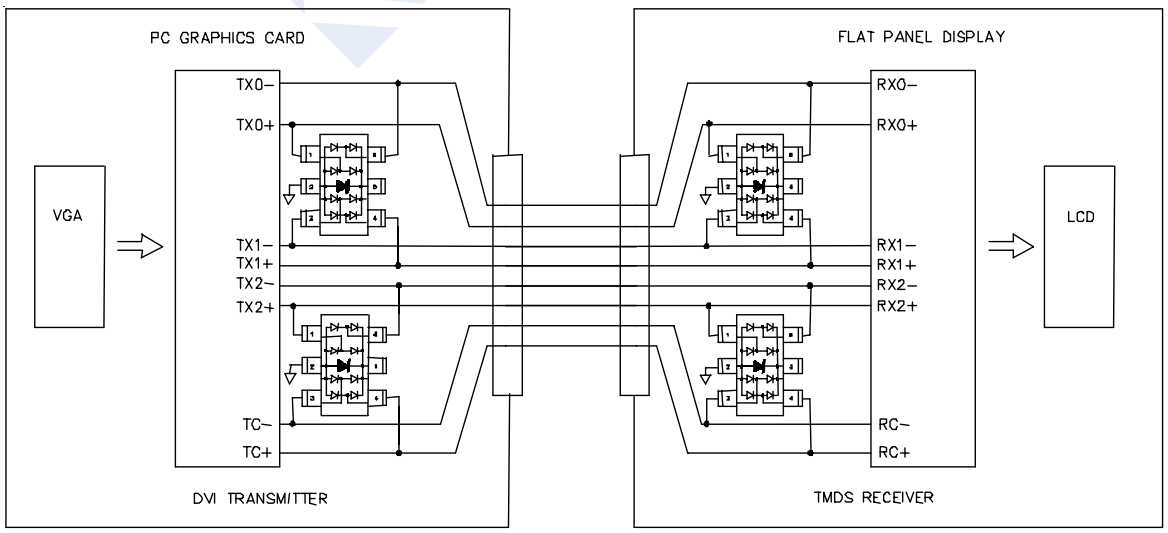


Figure 7 - Digital Video Interface (DVI) Protection

# Low Capacitance TVS Diode Array

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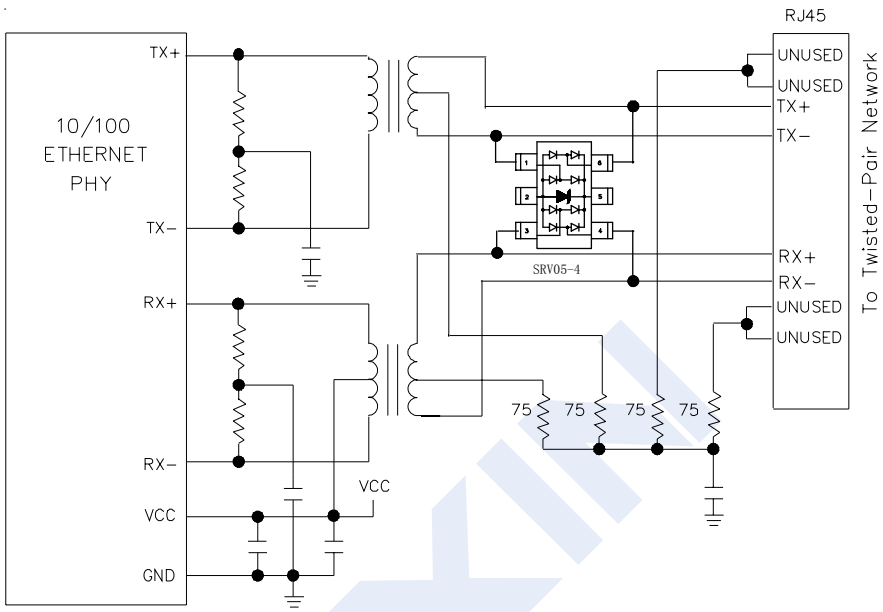


Figure 8 - 10/100 Ethernet Differential Protection

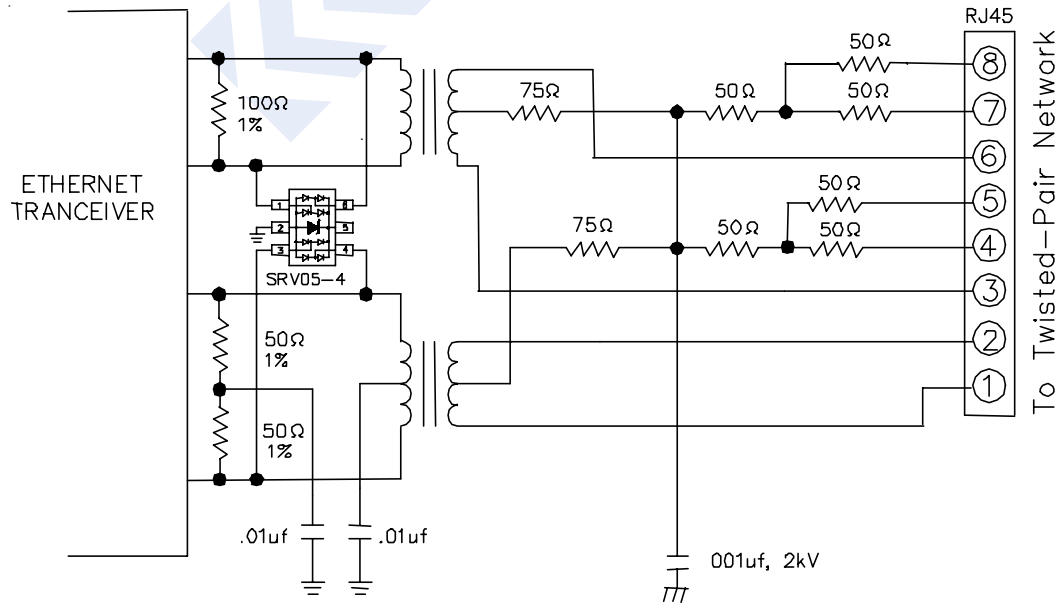


Figure 9 - 10/100 Ethernet Differential and Common Mode Protection

# Low Capacitance TVS Diode Array

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10/100 ETHERNET PROTECTION CONT'

Ethernet circuit to provide differential and common mode protection. The SRV05-4 can not be grounded on the line side because the hi-pot test requires the line side not to be grounded.

GIGABIT ETHERNET PROTECTION

The clock rate of gigabit Ethernet is the same 125MHz as the 10/100 Ethernet. However, it uses a complex five level signaling and transmits at a faster data rate that makes it more susceptible to capacitance and insertion loss. The low capacitance and low insertion loss of the SRV05-4 allow it to sit on the gigabit Ethernet line without loss of signal integrity. Figure 10 shows how to connect the SRV05-4 into a gigabit ethernet on the IC side for common and differential mode protection. Notice that pin 5 of the SRV05-4 is not connected. Some may be tempted to connect it to Vcc. In the ethernet application, the Vcc lines does not come out through the connector and does not need to be protected. Figure 10 shows the LC03-3.3 on the line side for the secondary line protection to Bellcore 1089 intrabuilding. If the designer only needs to meet ESD, CDE and low level lightning, the LC03-3.3 can be omitted.

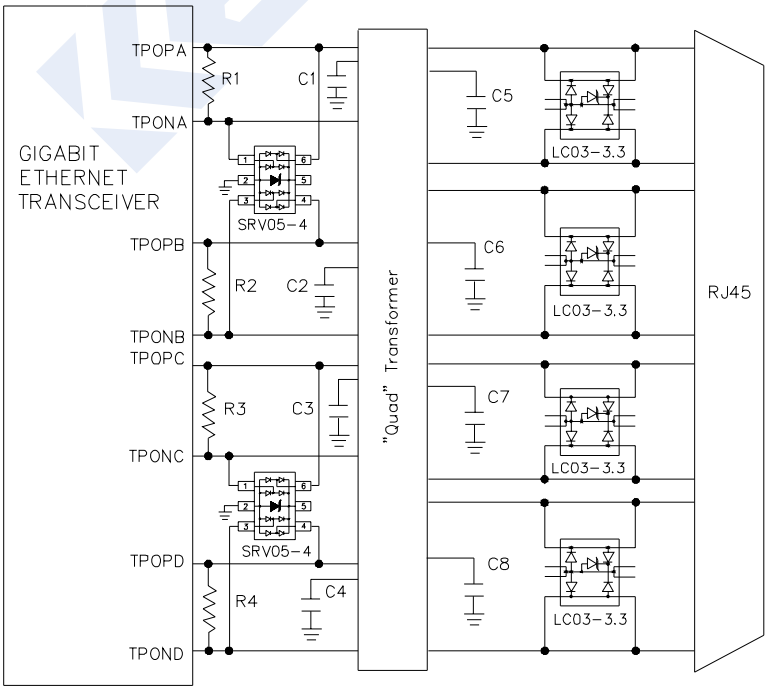


Figure 10 - Gigabit Ethernet Protection for Bellcore 1089 Intra-Building Protection