SS1101C
Integrated Spread-Spectrum Transceiver (SST)
External Specification

PRELIMINARY (V 1.1b)

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1. Introduction

Siliconians' SS1101C is a low-cost, low-power, multi-purpose spread spectrum communication chip designed to support digital voice or data communications for FCC Part 15-compliant wireless devices operating on ISM bands (USA), or on any other available frequency band (international).

The SS1101C is a very flexible chip for voice applications such as Digital Cordless Phones (DCP) for both consumer or wireless PBXs (W-PBX). In data mode, the chip is usable in acquisition and control applications (SCADA) as well as high-speed wireless LAN applications. It is implemented as a CMOS device packaged within an economic low-pin count (44-pin) surface-mounted plastic package.

1.1. Voice Mode

For operation in voice mode, the SS1101C interfaces directly with a 64 Kbps PCM CODEC for land-line quality voice in a low-cost Digital Cordless Phone. It can optionally also interface with a 32 Kbps ADPCM CODEC for high-quality compressed voice. This low-cost spread spectrum technology makes monitoring of phone calls practically impossible and greatly extends the range compared with other analog or digital phones operating in the ISM bands.

1.2. Data Mode

For operation in data mode, the SS1101C includes all of the modem baseband functions and operates in full-duplex or half-duplex modes. The on-the-air transmission is synchronous and the chip includes flexible dual FIFOs accessible by any standard microcontroller through a parallel bus and an interrupt mechanism. It provides high speed data capabilities with a maximum half-duplex rate of 400 Kbps.

In the half-duplex mode, no assumption about the higher level protocols is made, instead, the SS1101C is designed to be flexible and can be configured for a variety of uses.

1.3. General Information

The SS1101C provides constant monitoring of the link quality with an indication of the relative Signal/Noise at the baseband level. In data full-duplex and in voice modes, it also provides a low-speed signaling channel (overhead channel) independent of the main data/voice channel. The SS1101C is a 3V/5V CMOS device and contains power-saving features, including very low battery drain in standby, for battery operation.

1.4. Main features Summary

- Integrated Direct Sequence Spread Spectrum Baseband Modem
- Quaternary Baseband Modulation

- Processing Gain: 12 dB
- Data scrambler for spectral whitening and added security
- Voice Interface: 64 Kbps PCM (Mu-law, A-law) CODEC or 32 Kbps ADPCM
- Data Interface: 8-bit parallel bus with 30-byte deep dual-FIFO and interrupt signals
- Modes: Full-Duplex Voice, Full-Duplex or Half-Duplex Data
- Embedded Time-Division-Duplex (TDD) controller
- MSK on-the-air Modulation
- Differential Encoder/Decoder with Four Programmable 32-bit PN Sequences
- Programmable Station ID code
- Independent low-speed signaling channel
- Signal Quality Indicator Output (S/N)
- Power saving features
- Implementation: CMOS, 3V, 3.3V, 5V, 44-pin PQFP

2. Functional Description

The SS1101C is made up of six main functional modules. These include the parallel bus interface (PBI), the receiver, the transmitter, the time-division duplex (TDD) controller, the transmit and receive FIFOs, and the master clock generator. A block diagram is presented hereafter as Figure 1.

The PBI module supports bi-directional communication with a microprocessor. The receiver module performs all the digital signal processing required by the spread spectrum receiver, including de-spreading and demodulation. The transmit module generates the spread spectrum binary sequence for output to the RF modulator. The TDD controller includes logic implementing the time-division duplex protocol and various handshaking and interface signals. The transmit and receive FIFOs are used to buffer the transmit and receive data both in the voice and data modes. The master clock generator generates the clock signal required to drive the various modules of the SS1101C. These modules are described in more detail below.

2.1. PBI

The parallel bus interface (PBI) allows the SS1101C to communicate bi-directionally with a microprocessor. During power-on, the SS1101C should receive the programming information from the microprocessor through the PBI. The SS1101C receives and sends the signaling channel data through the PBI.

In the data mode the PBI module also provides a bi-directional data path between the microprocessor and the SS1101C.

2.2. Receiver

The receiver samples the incoming baseband signal at two samples per PN chip. The samples are correlated with four possible PN sequences in 64-bit parallel correlators.

The de-spreaded signal is demodulated via a digital phase locked loop. To reduce power consumption, the receiver is powered down while the SS1101C is transmitting and consumes peak power only during the brief period of initial acquisition. After acquisition, the receiver goes into tracking/detection mode.

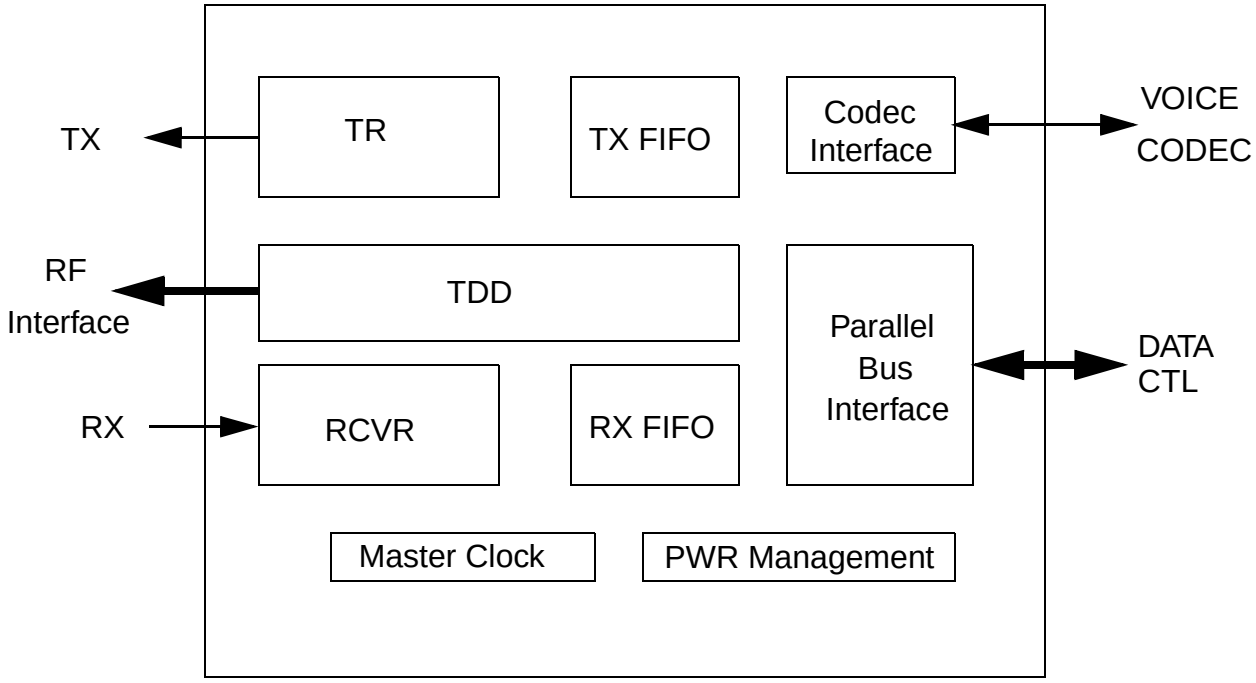


Figure 1. *SS1101C BLOCK DIAGRAM*

2.3. Transmitter

The transmitter logic encodes two consecutive bits of data into one of four possible 32-bit PN sequences. These PN sequences are programmed by the microprocessor through the PBI. The transmitted PN sequence is further randomized by modulus-2 addition with a fixed 2047-bit long PN sequence. This operation smooths the output spectrum of the transmitted signal and eliminates discrete spectral components. During TDD operation, the transmitter is powered off during the portion of the cycle when the SS1101C is in receive mode in order to save power. The transmitter output is a tri-state buffer and is at high-impedance state during a receiving period.

2.4. TDD Controller

The time-division duplex (TDD) controller implements the “ping-pong” protocol that allows a full-duplex link to be emulated by a half-duplex radio. The TDD controller also generates the appropriate clock and control signals to other modules of the SS1101C. In

full-duplex mode, the TDD controller multiplexes and de-multiplexes the overhead bits with the data or voice bit-stream. The TDD controller also uses a digital phase locked loop to maintain an equal read and write rate to the FIFOs as to avoid FIFO overflow or underflow. In addition, the TDD controller contains logic to generate the proper handshaking signals for both voice and data communication.

2.5. FIFOs

The SS1101C includes a 30-byte transmit FIFO and a 30-byte receive FIFO to buffer the input and output data. The control signals for the FIFOs are generated by the TDD controller. In the data modes the FIFOs provide the interrupt signals for the microprocessor and the microprocessor must read and write data to and from the FIFOs through the PBI.

2.6. Master Clock Generator

The master clock generator generates the various clock signals required by the modules described above. It can be disabled in power saving mode.

3. Operational Description

In this section, the operation of the SS1101C in its various modes is described.

3.1. Full-Duplex Voice and Data Operations

Although the SS1101C actually only uses a half-duplex channel for communication with the remote device, full-duplex operation is provided by using a time-division duplex (TDD) protocol. The TDD protocol basically configures the SS1101C alternatingly as a transmitter and as a receiver. When two devices are communicating with each other, one is programmed to be the master, while the other is programmed to be the slave. The TDD protocol ensures that while the master is transmitting, the slave is receiving and vice versa in a timely fashion. The end result is that as far as the user is concerned, the communication link appears to be full-duplex. In order to achieve this, it is necessary for the SS1101C to transmit at a higher rate than the actual user data rate. Ideally, for TDD operation, with 100% efficiency and 0% overhead, the SS1101C must transmit the data at twice the user data rate since the SS1101C has only half the time to transmit the user data (during the other half time period, the SS1101C is receiving from the remote station). Overhead such as preamble, unique word (UW), as well as other signaling information bits result in the SS1101C transmitting at 2.6 times the effective user data rate. The size of the FIFOs on the SS1101C is designed to provide sufficient buffer during both transmit and receive operations so that underflow or overflow of the FIFOs does not occur.

When communication between two devices first commences, the microprocessors must program one of the devices as the Master and the other device as the Slave. The master device transmits periodic bursts as soon as the reset signal, RST1_N, is released. The burst timing of the Master is derived from its internal master clock oscillator and can be computed from (EQ 1) below:

$$f_{burst} = \frac{f_{mosc}}{192} \quad \textbf{(EQ 1)}$$

In (EQ 1), f_{burst} is the burst rate and f_{mosc} is the master oscillator frequency. For a voice device using the 32 Kbps ADPCM codec, the required master oscillator frequency is 16.384 MHz with a burst rate of 85.333 Kbps or a burst period of 11.719 μsec. Note, this burst rate is the actual bit rate at which the SS1101C is transmitting during TDD operation, and is 2.667 times the user bit rate (32 Kbps). As the transmitter uses a quadrature modulation scheme, the chip rate is 16 times the burst rate or

$$f_{chip} = \frac{f_{mosc}}{12} = 16 \times f_{burst} \quad \textbf{(EQ 2)}$$

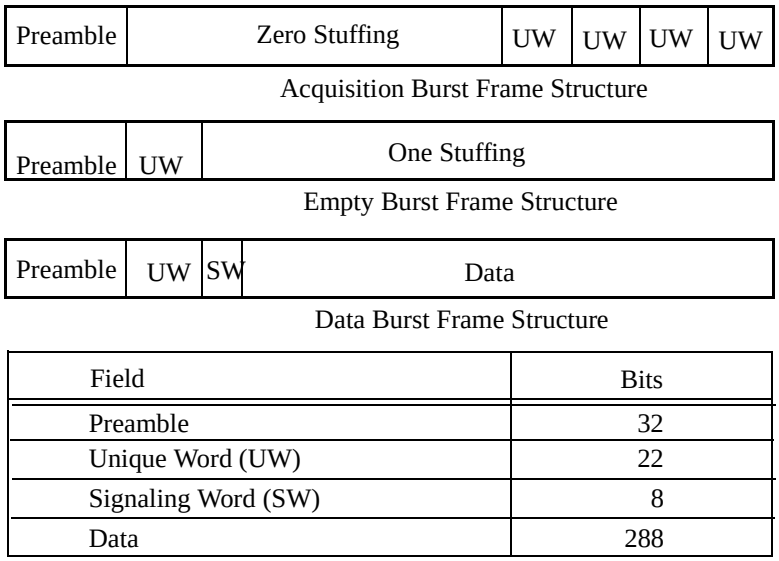
where f_{chip} is the chip rate and f_{mosc} is the master oscillator frequency. Effectively, the spread spectrum transceiver operates at 16 chips/bit or 32 bits/symbol where each symbol is composed of 2 bits.

For a voice device using the 64Kbps PCM codec the required master oscillator frequency is 32.768 MHz. The burst rate and the chip rate are also doubled in value.

The total number of bits per burst is fixed and equal for both the Master and the Slave. The Slave derives its burst timing from the Master by detecting the UW pulse transmitted by the Master.

3.1.1 TDD Protocol

Initially, the two communicating devices need to establish “sync”. The TDD protocol achieves this by using a special handshaking protocol. The Master first transmits an “acquisition burst”. The acquisition burst consists of 32 bits of preamble (binary 0’s), followed by 230 bits of “zero stuffing”, and four 22-bit unique words (UW). When the Slave receives the acquisition burst from the Master correctly (by decoding the 4 consecutive UWs), it sends an acquisition burst in response. When the Master receives the acquisition burst, it sends an “empty burst”. An empty burst contains a 32-bit preamble followed by a single 22-bit unique word, and 296-bit of “1” (One stuffing). In response to the master’s empty burst, the Slave also sends an empty burst back to the Master. When the Master receives the empty burst from the Slave, the communication link is considered to have been established and “sync” condition achieved. On the following burst, both the Master and the Slave start genuine data transmission by sending out “data bursts”. Each of the data bursts contain a 32-bit preamble, followed by a 22-bit UW, a 8-bit Signaling Word (SW), and 288 bits of user data (be it PCM/ ADPCM voice samples or data). The three different types of burst frame structures are shown in Figure 2.



Field	Bits
Preamble	32
Unique Word (UW)	22
Signaling Word (SW)	8
Data	288

Figure 2. *Burst Frame Structures*

Each burst cycle also includes 2 “Guard” times to allow for both propagation and RF transceiver switching time. More specifically, G_1 is a 28-bit delay between the time the Master stops transmission and the Slave commences transmission; G_2 is a 28-bit delay between the time the Slave stops transmission and the Master commences transmission. These guard times allow for a minimum delay of 328 µsec delay (for a master oscillator frequency of 16.384 MHz). The total burst cycle is 768 bits long, including 12 bits internal delay (the transmitter turns off 6 bits after the last data bit is latched into the transmitter, the master and slave therefore contribute a total of 12-bit internal delay).

During TDD operation, the receiver will go through several stages. Initially, when the 4 UWs of the acquisition burst has been received and decoded correctly, the receiver (either Master or Slave) declares “locked”. After the empty burst has been decoded, the receiver declares “rlocked” signifying that the remote device has locked. The behavior of the receiver after establishing the RLOCK condition depends on whether the internal state machine is turned on or not (determined by the setting of the CI_h[4] bit). When the state machine is turned off, transmission will be turned off whenever the UW is not detected. The Slave then waits for a new acquisition burst while the Master will start the acquisition cycle again by transmitting an acquisition burst. Note that the Master will continue to broadcast acquisition bursts until it has received a proper acquisition burst from the Slave in response. The Master will always revert back to the initial acquisition mode (broadcasting acquisition bursts), whenever it fails to detect the proper UWs from the slave.

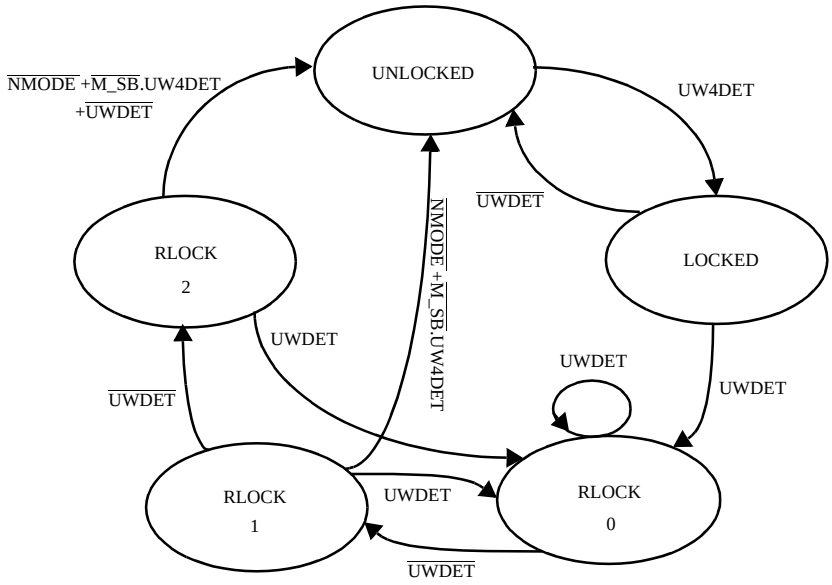


Figure 3. *Receiver Lock State Machine*

If the state machine is turned on, then the receiver will not declare LOCK loss right after UW has not been detected. Instead, it will allow for UW errors in up to two further bursts before declaration LOCK loss. The state diagram for this lock state machine is shown in Figure 3. In the figure, UW4DET indicates the condition when the four UWs have been detected during acquisition burst, UWDET indicate the condition where the single UW in empty and data bursts has been detected. M_SB is the programmed bit (CI_h[0]) which is a binary "1" when the SS1101C is programmed to be the master and a binary "0" when programmed as a slave. NMODE is a signal generated by the receive logic when the digital phase locked loop in the receiver has achieved lock, it is similar to an RSSI signal. Note that the NMODE signal is independent of the UW detection. Physically, when NMODE is asserted, it indicates that PN acquisition has been achieved. The LOCKED and RLOCK states are as described previously.

3.1.2 System Delay

To calculate the delay through the system (see Figure 3.), assume that the transmit FIFO is almost empty at the end of a burst. Then the next bit that enters the transmit FIFO will experience a system delay (excluding propagation delay but including the internal logic delay) of approximately:

$$T_{delay} = 2 \times (T_G + T_{PR} + T_{UW} + T_{SW}) + T_{DAT} + T_{\Delta} \quad \textbf{(EQ 3)}$$

where T_G is the time delay due to Guard Time (note: G = G1 = G2 = 28bits), T_{PR} is the time delay due to preamble, T_{UW} is the time delay of the UW, T_{SW} is the time delay for signaling word transmission, T_{DAT} is the time delay for data transmission, and T_{Δ} is the internal logic delay. For a 32 Kbps ADPCM voice signal, with a master oscillator (MO) of 16.384 MHz, this system delay translates into 5.625 msec.

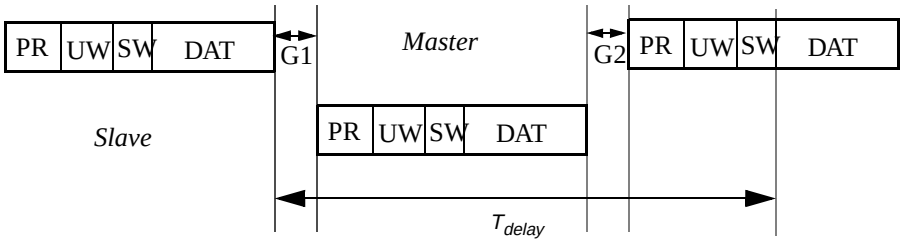


Figure 4. *System Delay*

3.2. Voice Mode Timing Information

In the voice mode the SS1101C starts transmit and receive right after the RST1_N is released (assuming the CHIPSEL_N is enabled).

The SS1101C generates the appropriate clock signals for interfacing with a 32-Kbps ADPCM or 64-Kbps PCM voice codecs. Specifically, the MHZ2_ST pin delivers the 2.048 MHz bit clock and the FCLK_RT pin delivers the 8 KHz framing or sync clock to a codec. The timing diagram for the ADPCM interface is shown in Figure 5. below. Details of the timing specification are presented in the timing section. For the PCM codec there are 8bits of data instead of 4 bits, and FCLK_RT pulse is 8 MHZ2_ST pulses long.

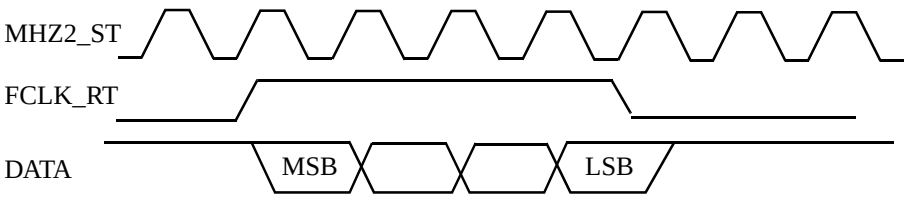


Figure 5. *ADPCM Interface Timing*

For voice operation, it is necessary to lock the average rate of writing data into the FIFOs to the average rate of reading data from the FIFOs. Since the number of bits per burst is fixed and so is the burst rate, this can be achieved by locking the sample clock onto the burst rate. For voice mode operation, the 8 Kframes/sec clock is locked onto the burst rate by a digital phase-locked loop in the TDD control module. The phase-locked loop fine tunes the 8 Kframes/sec clock delivered to the codec, so that exactly 72 frame pulses are delivered per ADPCM burst and 36 frame pulses are delivered per PCM burst. During each frame pulse, the ADPCM interface delivers and receives 4 bits of

data to and from the ADPCM codec. The PCM interface delivers and receives 8 bits of data to and from the PCM codec.

In the PCM mode operation, a MO of 32.768 MHz is required

3.3. Data Mode Timing Information

3.3.1 Full Duplex Operations

In Full Duplex mode, chips communicating with each other should have RTS_N enabled. A chip which is configured as a Master starts the acquisition procedure and data transmission. A Slave is waits for a valid spread spectrum signal to arrive.

The SS1101C transmits and receives data through TXFIFO and RXFIFO buffers. The writing and reading of data to and from the FIFOs are supported by the PBI. The synchronization of the data exchange between the microprocessor and the SS1101C is provided by the use of the interrupt signal (IRQ_N). If IE[2] and IE[3] bits of the IE register are enabled, the IRQ_N pin low indicates that either the TXshl bit from TXFIFO or RXshh bit from RXFIFO is set. TXFIFO interrupt will be active if the TXFIFO index is below the programmed TXshl and will remain active until the index is above the TXshh. The RXFIFO interrupt will be active if the RXFIFO index is above the programmed RXshh and will remain active until the index is below the RXshl. Thus the microprocessor must write data into the SS1101C for transmission when the IRQ_N is asserted by the TXFIFO, and it must read data from the SS1101C when the IRQ_N is asserted by the RXFIFO. The difference in value between thresholds high and low should be at list two bytes.

If IRQ_N low indicates that the TXshl control bit is set, data bytes should be written into the TXFIFO. To avoid the overflow of the TXFIFO and loss of data, the maximum number of bytes to be written should not be more than (30 - TXshl) bytes. The size of the burst is 288 bits or 36 bytes. If there is not enough user’s data to fill up a burst at the end of transmission of the user’s data, “0”s will be sent automatically (when there is no data and transmission is enabled, all “0”s will be sent).

If IRQ_N low indicates that the RXshh bit is set, data bytes should be read from the RXFIFO. The high level protocol should take care of the end of transmission to avoid a situation where some data can be held in the RXFIFO indefinitely or lost by a later Reset.

The timing relationship between the data and interrupt signals for transmit and receive is shown in Figure 6. below. The rate with which the MCU feeds data to the transmitter FIFO depends on the values of the thresholds and the burst rates.

3.3.2 Threshold Value Calculation

The performance of the MCU should be considered when calculating the TXshl and RXshh. The time required for transmission of TXshl bytes out of TX FIFO should be more than the time required by the MCU to write a new set of data into the TX FIFO.

Accordingly, the time for the receiving of RXshh bytes from the channel should be more than the time required by the MCU to read the data set from the RX FIFO.

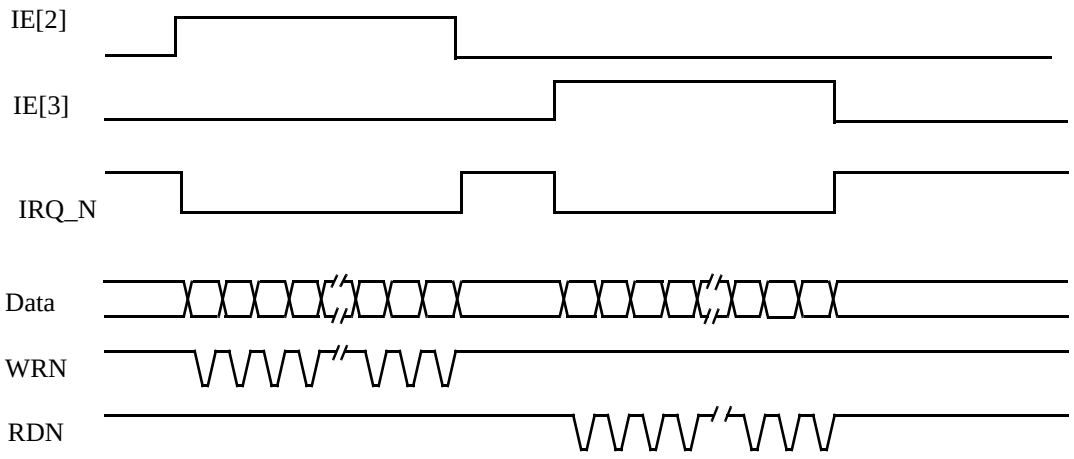


Figure 6. *Full-Duplex Data Interface Timing*

A typical start-up of the data link is also shown in Figure 7., note that the same diagram would also apply for the voice mode operation where the MHZ2_ST and FCLK_RT timing have the timing relationship previously presented in Figure 5.

In the full-duplex mode the SS1101C when programmed as a Master, starts transmission as soon as reset RST1_N is released (RTS_N is enabled). As long as the Master is powered-on the SS1101C will send out the acquisition burst and try to establish a communication link with a remote Slave. Thus, the communication channel is occupied as soon as the Master resets, and this can occur before any data becomes available for transmission. Once the communication link is established, even when there is no data to be transmitted, the Master and Slave will remain in communication with each other (sending out “0” in the data field) indefinitely or until the Master is disabled.

3.3.3 Half-duplex Operation

The half-duplex data mode is suitable for applications such as SCADA, wireless LAN or portable devices. The SS1101C does not make any assumption about the higher level protocol and relies on these higher level protocols to provide the necessary framing, error correction, and preamble. The SS1101C will transmit and deliver the data stream without multiplexing any protocol overhead bits, as it is the case for the full-duplex operation.

It is the user's responsibility to ensure that each packet transmitted contains enough preamble bits so that acquisition can be achieved prior to actual data delivery. Similarly, although the SS1101C delivers the interrupt signals to the user, the user needs to be aware that in the half-duplex mode the SS1101C in the Receiver mode (RTS_N is disabled) delivers the interrupt signals even if there is no data received. All "0"s will be read from the RXFIFO in this case.

Also, invalid received data will be present at the output due to hysteresis of the digital phase-locked loop. Thus, the user must be able to detect the end-of-packet from the data received rather than relying on the SS1101C to signify loss of the interrupt signal or loss of the lock.

The SS1101C in the Transmit mode (RTS_N is enabled) will transmit "0" if there is no data in the TXFIFO.

Because no overhead in multiplexing is required, in half-duplex mode, the highest data rate supportable is equivalent to the burst rate of the full-duplex mode. For example using a MO of 30.72 MHz this can be set at 170 Kbps. The relationship between the data rate and the required MO is as followed:

$$f_{data} = \frac{f_{mosc}}{192} \quad \textbf{(EQ 4)}$$

The data exchanges through the PBI remain unchanged from those of the full-duplex operation.

The RTS_N bit designates the direction of transmission. The transmission is directed from a chip with RTS_N enabled to a chip with RTS_N disabled. To change the direction of transmission the value of RTS_N should be reversed. Note that, in the half-duplex mode, when RTS_N changes value the SS1101C resets itself. The transmitter stops transmission as soon as RTS_N is disabled.

It is up to the user to include and detect end-of-packet information so that invalid data is not erroneously perceived as valid data. Finally, note that there is no provision for CSMA/CD type collision avoidance in the hardware, it is up to the user or the modem system to implement any desired collision avoidance schemes either in hardware and/or software. A typical timing diagram for half-duplex operation is shown in Figure 8.

Note that there is a key difference between full-duplex and half-duplex operation. In a half-duplex operation, there is no concept of Master or Slave. The SS1101C will start transmitting "0"s (if there is no data in the TXFIFO) or data once the user has asserted the RTS_N control bit. The SS1101C Receiver will receive "0"s or data, accordingly. The SS1101C Receiver will generate the interrupt signals and deliver "0"s to the MCU even if there is no transmission process at all. Those "0"s are stored in the RXFIFO

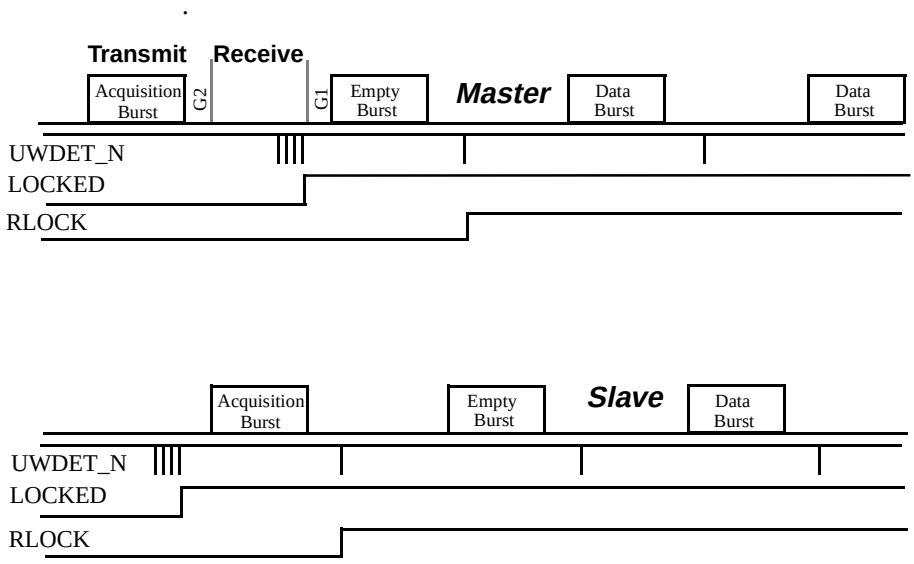


Figure 7. *Typical Communication Link Start-Up*

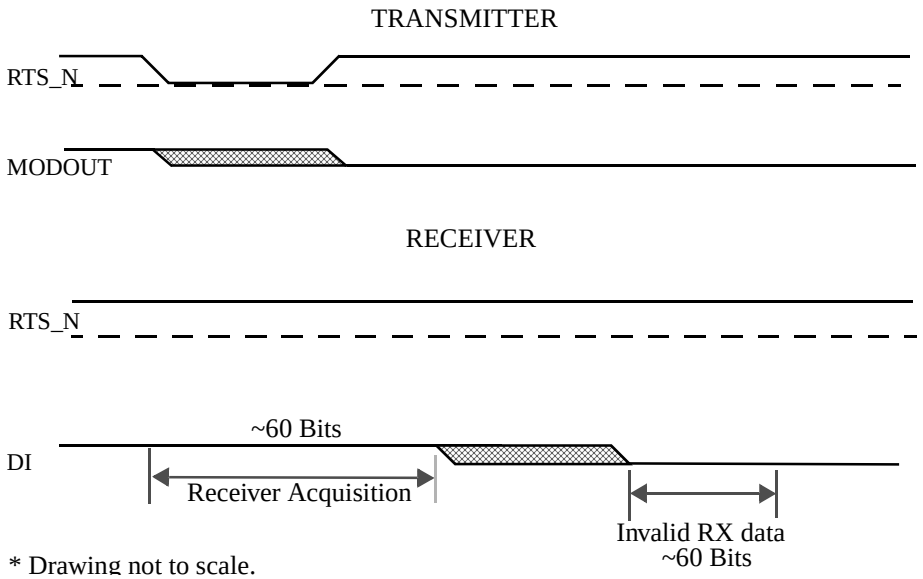


Figure 8. *Timing for half-duplex Operation*

4. The Parallel Bus Interface

The parallel bus (PBI) is designed to interface the SS1101C with a generic microprocessor. The PBI supports the loading of the SS1101C programmable data from the microprocessor, generates interrupts for remote signaling and S/N data and is used for bi-directional data transfers in data mode. In the following sections, the operation of the interface is discussed in more detail.

4.1. Read and Write Operations

The Read/Write access time of the SS1101C is less than 25ns in the worst case.

4.1.1 Write Operation

1. The microprocessor latches the data into the appropriate registers for both the address and data bus signals and by providing the WRN signal.
2. Both address and data shall be stable before WRN goes to low, and remain stable until WRN becomes inactive (“1”).

The “Write” timing diagram is shown below.

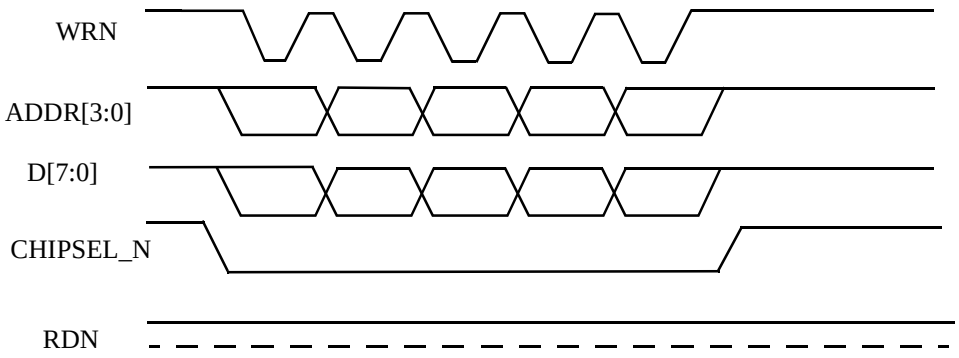


Figure 9. *PBI Write Operation*

4.1.2 Read Operation

1. The microprocessor reads the PBI data from the appropriate register on the data bus by providing data on the address bus together with the RDN signals.

2. The Address shall be stable before RDN goes to low, and remain stable until RDN becomes inactive (“1”).

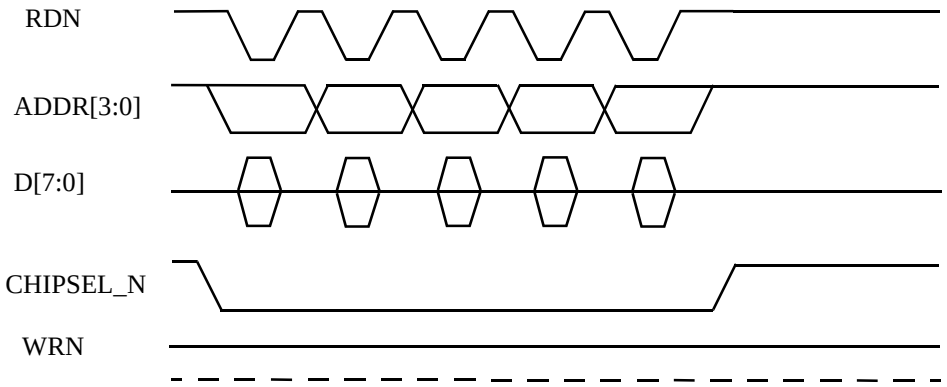


Figure 10. *PBI Read Operation*

4.2. Loading of the SS1101C Programmable Data

The microprocessor configures the SS1101C by loading the SS1101C control registers with the programmable information including PN sequences, Unique Word, configuration information bits, test bits, Signaling Word, etc. After the microprocessor selects the SS1101C by setting the CHIPSEL_N to LO, the loading of the SS1101C is done by the following steps:

1. After power up the contents of the control registers are not defined. The microprocessor writes the appropriate values into the intended register using the “Write” operation.
2. The microprocessor resets the SS1101C using RST1_N pin (Assert the system reset pin RST1_N for some time and then release it to inactive “1”)

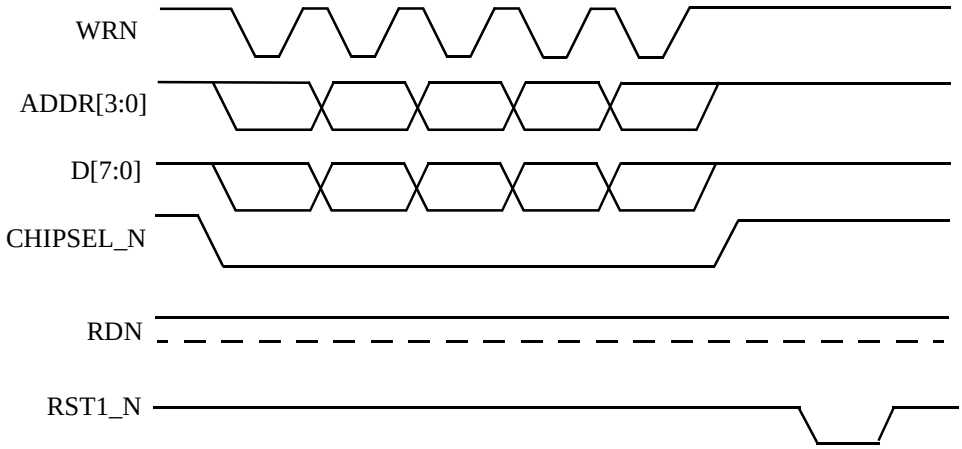


Figure 11. *Loading of the SS1101C Programmable Data*

4.3. Reading the SW and S/N Data from the PBI

The Signaling Word (SW) and S/N registers in Full Duplex Voice and Data modes are updated periodically by the SS1101C:

- The Signaling Word is updated once every burst
- The S/N data is calculated from the AGC circuit inside the SS1101C once every 128 data bits (including overhead bits)

To read the Signaling Word or the S/N value, the “PBI Read” operation needs to be performed.

4.3.1 Signaling Word (SW) Transmitting

If no SW value has been loaded at the time the communication starts (lock is achieved), the signaling word (SW) transmit register will be filled with an “FF” byte and this value will be transmitted with each burst. Once a Signaling Word has been written into the register, it is transmitted with the next burst. If there is no new Signaling Word written, the current Signaling Word value will be transmitted with each next burst, until a new SW is loaded for transmission.

4.3.2 SW Receiving

The IE[0] bit in the IE Control Register, when asserted, enables the Receive SW interrupt. If the interrupt was not enabled before the communications started, it is possible to enable it during the transmission. The SS1101C should be reset after the interrupt is enabled during the communication.

When the interrupt is enabled, once a Signaling Word has been received and loaded onto the Signaling Word receive register, the interrupt IRQ_N is asserted. If the interrupt was not serviced, a new byte will be loaded into the register on the next burst. The previous byte will be lost. If the received data is needed, the interrupt should be serviced between bursts.

5. Control, SW, and FIFO Registers

A total of thirty-one registers are available for storing and retrieving the various programming parameters and data through the PBI. They are listed below:

TABLE 1. *Control, SW, and FIFO Registers*

Name	Address	Index	Bank Select CI_l[1]	Write/ Read	Functions
CI_l	0000	[7:0]	0 Low	WR/ RD	CI_l[0]: Normal Mode CI_l[1]: High/Low Bank Select CI_l[3:2]:Width of ESD Window CI_l[4]: Set the Width of “Central Region” CI_l[5]: DPLL Accumulator 1 Reset CI_l[7:6]: Set the Width of “Detection Window”
CI_h	0001	[7:0]	0 Low	WR/ RD	CI_h[0]: Master/Slave Selection bit CI_h[3:1]:Number of errors allowed in the UW CI_h[4]:LockSMon CI_h[5]:Data/Voice Mode Selection CI_h[6]: 64/32Kbit Select in Voice Mode, Semi/Full Duplex Select in Data Mode CI_h[7]:RTS_N bit (0 to enable)
FIFO	0010	[7:0]	0 Low	WR/ RD	Write data for TXFIFO Read data for RXFIFO
IE	0011	[3:0]	0 Low	WR	IE[0]: Enable the RXSW received interrupt IE[1]: Enable the S/N interrupt IE[2]: Enable the TXFIFO interrupt IE[3]: Enable the RXFIFO interrupt
IS	0011	[3:0]	0 Low	RD	IS[0]: RXSW interrupt pending IS[1]: S/N interrupt pending IS[2]: TXFIFO interrupt pending IS[3]:RXFIFO interrupt pending

TABLE 1. *Control, SW, and FIFO Registers*

Name	Address	Index	Bank Select CI_l[1]	Write/ Read	Functions
TXSW	0110	[7:0]	0 Low	Write	Signaling Word to be transmitted
RXSW	0110	[7:0]	0 Low	Read	Signaling Word received
S/N	0111	[7:0]	0 Low	Read	Signal/Noise indicator
PNA0	1000	[7:0]	0 Low	WR/ RD	PNA[7:0]
PNA1	1001	[7:0]	0 Low	WR/ RD	PNA[15:8]
PNA2	1010	[7:0]	0 Low	WR/ RD	PNA[23:16]
PNA3	1011	[7:0]	0 Low	WR/ RD	PNA[31:24]
PNB0	1100	[7:0]	0 Low	WR/ RD	PNB[7:0]
PNB1	1101	[7:0]	0 Low	WR/ RD	PNB[15:8]
PNB2	1110	[7:0]	0 Low	WR/ RD	PNB[23:16]
PNB3	1111	[7:0]	0 Low	WR/ RD	PNB[31:24]
UW0	0001	[7:0]	1 High	WR/ RD	UW[7:0]
UW1	0010	[7:0]	1 High	WR/ RD	UW[15:8]
UW2	0011	[7:0]	1 High	WR/ RD	UW[21:16]

TABLE 1. *Control, SW, and FIFO Registers*

Name	Address	Index	Bank Select CI_I[1]	Write/ Read	Functions
TXshh	0100	[4:0]	1 High	WR/ RD	Transmitting FIFO interrupt threshold high
TXshl	0101	[4:0]	1 High	WR/ RD	Transmitting FIFO interrupt threshold low
RXshh	0110	[4:0]	1 High	WR/ RD	Receiving FIFO interrupt threshold high
RXshl	0111	[4:0]	1 High	WR/ RD	Receiving FIFO interrupt threshold low
PNC0	1000	[7:0]	1 High	WR/ RD	PNC[7:0]
PNC1	1001	[7:0]	1 High	WR/ RD	PNC[15:8]
PNC2	1010	[7:0]	1 High	WR/ RD	PNC[23:16]
PNC3	1011	[7:0]	1 High	WR/ RD	PNC[31:24]
PND0	1100	[7:0]	1 High	WR/ RD	PND[7:0]
PND1	1101	[7:0]	1 High	WR/ RD	PND[15:8]
PND2	1110	[7:0]	1 High	WR/ RD	PND[23:16]
PND3	1111	[7:0]	1 High	WR/ RD	PND[31:24]

5.1. Configuration Information Bits

The configuration information bits are used to set the various programmable parameters in the SS1101C:

CI_I[0] *Should be set to LO.*

CI_I[1] *Selects High/Low Bank. High= High Bank; Low= Low Bank*

CI_I[3:2] *PLSL. Sets the width of the ESD window. CI_I[2] is LSB, CI_I[3] is*

MSB. See Application Section.

PLSL	Width of ESD window
0	8 samples wide
1	10 samples wide
2	12 samples wide
3	14 samples wide

CI_l[4] — *CNTLR. Sets the width of the "Central Region". (**NOTE**: CNTLR size must be ≤ PLSL size).See Application Section.*

CNTLR	Width of Central Region
0	10 samples wide
1	12 samples wide

CI_l[5] — *ACC1RES. DPLL Accumulator 1 reset. See Application Section.*

ACC1RES	Accumulator1 Reset
0	ACC1 NOT reset.
1	Reset ACC1.

CI_l[7:6] — *WSL. Sets the width of the "Detection Window". CI_l[6] is LSB, CI_l[7] is MSB. See Application Section.*

WSL	Width of Detection Window
0	4 samples wide
1	6 samples wide
2	8 samples wide
3	10 samples wide

CI_h[0] — *M/SB. Set the SS1101C to be a Master (HI) or Slave (LO). Note: must be set to LO in half-duplex data mode.*

CI_h[3:1] — *T. Number of errors allowed in the UW. CI_h[1]is LSB, CI_h[3] is MSB.*

T	Allowable UW Errors
0	0 bit
1	1 bit
2	2 bits
3	3 bits
4-7	4 bits

CI_h[4] — *LockSMon. Enables the Locking State Machine when set to HI (see Figure 3. for Locking State Machine state diagram).*

CI_h[5] — *Selects Data or Voice Modes: HI (1) selects Data; LO (0) selects Voice*

CI_h[6] — *Selects operation mode: For Voice: HI (1) is 64 Kbps, LO (0) is 32 Kbps. For Data HI (1) is Half-Duplex, LO (0) is Full-Duplex*

CI_h[7] — *RTS_N Bit Value: LO (0) enables RTS, HI (1) disables RTS*

FIFO — *Receive (RXFIFO) and transmit (TXFIFO) registers. One address is used to access both registers. The WRN and RDN signals are used to access the required register. The read/write operations are described in Section 4.1. "Read and Write Operations".*

IE — *Interrupt Enable. Enables interrupts for RXSW, S/N, TXFIFO, and RXFIFO. If more than one interrupt is enabled and interrupts are generated, the IRQ_N pin goes low. All interrupts are ORed to the IRQ_N pin. To service the interrupts the IS register should be read. All interrupts, but RXSW, can be enabled during the transmission, without resetting the SS1101C.*

IS — *Indicates the source of an interrupt or interrupts if the interrupts are enabled in the IE register. The interrupts do not have priorities. It is up to the user's software to define the sequence for servicing the interrupts.*

5.2. Reset

The SS1101C contains one external reset control signal RST1_N. The RST1_N is used to reset the SS1101C and to disable the clocks. The RST1_N reset signal does not affect the values stored in the control registers.

An internal source of reset is the CI_H[7] bit (RTS_N) of the CI_h control register. When the RTS_N bit status is changed the SS1101C is reset.

5.3. RF/IF Analog Interface

The SS1101C interfaces with the RF/IF analog radio through the following pins: DI, MODOUT, PLLSW, TXEN and RFPWR.

DI is a CMOS-level input fed by the analog receiver. MODOUT is a tri-state output to the analog transmitter. It is in high-impedance state when the SS1101C is in the receive mode (TXEN is LO). PLLSW and RFPWR are used respectively to switch the PLL of the analog radio and to power on/off the transmitter power amplifiers. The timings for the RFPWR and PLLSW are shown in Figure 12. and Figure 13. respectively.

The RFPWR switch timing is designed to avoid damage to the sensitive analog receiver. When switching from receive to transmit, RFPWR is delayed relative to TXEN (which can be used for switching the antenna between transmit and receive chain) to ensure that the receiver has been turned off before the transmitter is turned on. Similarly, when switching from transmit to receive, RFPWR is turned off first, before TXEN, to allow extra time for the transmitter to turn off prior to turning on the receiver circuits. Note that the RFPWR timing is valid for both full-duplex and half-duplex modes.

The BURST_CLK shown in Figure 12. is the burst rate clock which is 2.667 times the data rate in full-duplex operation and is equaled to the data rate in half-duplex operation. For example, for a master oscillator of 16.384 MHz, the full-duplex burst rate is 85.333 KHz. Thus, the RFPWR signal will be asserted one burst clock cycle or 11.72 µsec after TXEN assertion and will be de-asserted one burst clock cycle or 11.72 µsec prior to TXEN de-assertion.

The PLLSW timing shown is for the full-duplex mode; for half-duplex operation, PLLSW timing follows that of the RFPWR. The PLLSW signal is designed to switch the RF PLL when different frequencies are used for transmit and receive operation. In this instance, PLLSW is turned on right at the end of receive operation and prior to TXEN assertion to allow the RF PLL to stabilize. Similarly, the PLLSW changes to a LO as soon as transmission is finished and before receiving commences.

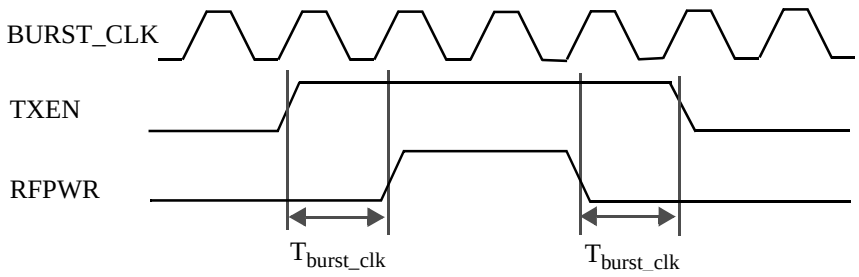


Figure 12. *RFPWR Timing*

The PLLSW is asserted 28 burst clock cycles (duration of G2) prior to TXEN assertion and is de-asserted 1 burst clock cycle before TXEN is de-asserted in the full-duplex mode. Thus, for a master oscillator of 16.384 MHz (corresponding to a burst rate of 85.333 KHz or a burst period of 11.719 µsec), the PLLSW signal will be asserted 328 µsec (28*11.72=328) prior to TXEN assertion.

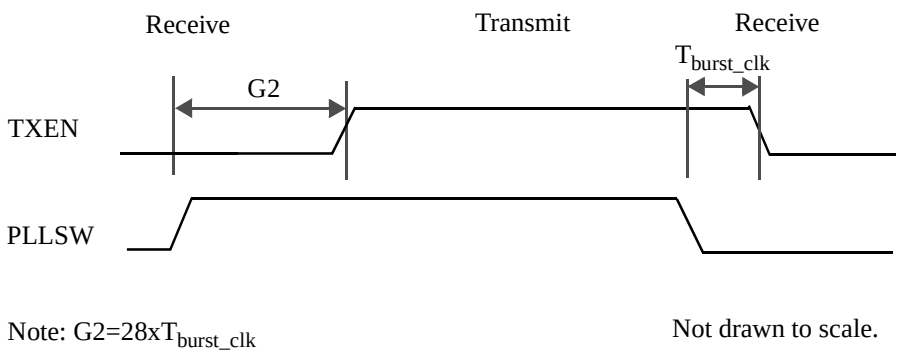


Figure 13. *PLLSW Timing (Full-Duplex Mode)*

6. I/O Description

VDD — **Input**

$3.0 \pm 0.25/3.3 \pm 0.25/5.0 \pm 0.25$ Volts DC. Note, the SS1101C can operate with either a 3.0-Volt, a 3.3-Volt or a 5.0-Volt DC power supply. However, the SS1101C will not operate reliably in a mixed voltage environment.

VSS — **Input.**

Ground.

OSCI16 — **Input.**

To be used for an operating frequency between 10MHz and 24MHz. Input to the on-chip crystal oscillator. When a crystal is used, it is expected to be connected across OSCI16 and OSCO16 pins. If a crystal clock oscillator or an external clock source is used, then OSCI16 should be connected to the clock source and OSCO16 left opened. Any external clock source (or crystal clock oscillator) should have 50 ± 0.25 % duty cycle and ± 50 ppm accuracy.

OSCO16 — **Output.**

10MHz - 24MHz oscillator output. Output of the on-chip crystal oscillator. Should be connected to one side of a crystal or left opened if an external clock source or crystal clock oscillator is used.

OSCI32 — **Input.**

To be used for an operating frequency between 20MHz and 60MHz. Input to the on-chip crystal oscillator. When a crystal is used, it is expected to be connected across OSCI32 and OSCO32 pins. If a crystal clock oscillator or an external clock source is used, then OSCI32 should be connected to the clock source and OSCO32 left opened. Any external clock source (or crystal clock oscillator) should have 50 ± 0.25 % duty cycle and ± 50 ppm accuracy.

OSCO32 — **Output.**

20MHz - 60MHz oscillator output. Output of the on-chip crystal oscillator. Should be connected to one side of a crystal or left opened if an external clock source or crystal clock oscillator is used.

CLKSEL — **Input.**

Oscillator 16 or oscillator 32 enable. When low enables a crystal connected to OSCI16-OSCO16. When high enables a crystal connected to OSCI32-OSCO32. The unused set of input pins should be grounded (OSCI32 and OSCO32 should be grounded when using OSCI16-OSCO16 and vice versa.

CLKEN **Input.**
Oscillators enable. Enables the on-chip crystal oscillators when asserted, otherwise, the on-chip crystal oscillators are disabled.

OSCUP **Output.**
Microprocessor clock. This is a clock signal generated internally from the master oscillator. It is a divide-by-4 version of the master oscillator. For example, when using a 16.384 MHz master oscillator, the OSCUP pin delivers a 4.096 MHz clock. Its main purpose is to reduce the required number of clock signals for the system.

TX **Input.**
TX pin accepts the ADPCM/PCM sample input from a codec.

RX **Output.**
The SS1101C delivers the received ADPCM/PCM samples to a codec.

MHZ2_ST **Output.**
The MHZ2_ST pin delivers the 2.048 MHz bit rate clock signal to the ADPCM or PCM codec. Note, the SS1101C latches TX data on the falling edge of MHZ2_ST.

FCLK_RT **Output.**
The FCLK_RT pin delivers the 8 KHz framing clock to the ADPCM/PCM codec.

BSYNC_OUT **Output.**
Burst sync output. Burst synchronization pulse. Can be used in a wireless PBX environment, where several radios are co-located, to synchronize the burst timing, thereby reducing “far-near” interference.

BSYNC_IN **Input.**
Burst sync input. To be externally looped back to BSYNC_OUT or to an external burst timing source.

RFPWR **Output**
RF power switch. Designed to switch the transmitter on when asserted and off when de-asserted. Discussed in more detail in the Operational Section.

PLLSW **Output**
Phase-lock loop switch. Designed to switch the transceiver synthesizer between TX and RX frequencies. It is asserted for TX and de-asserted for RX. See Operational Section for more detail.

TXEN	**Output** Transmitter enable. When asserted, connects the antenna to the transmitter. When LO, connects the antenna to the receiver.
MODOUT	**Output** Modulation output. Spread spectrum modulated chip output.
DI	**Input.** Received data input. CMOS compatible input from the analog receiver.
RST1_N	**Input.** Reset. When LO resets the storage elements in the SS1101C and freezes all clocks except the master oscillator.
CHIPSEL_N	**Input.** Chip select. When LO validates the address on the address bus. When HI, the SS1101C ignores all activity on the address bus.
ADDR[3:0]	**Inputs.** PBI address bus. MSB is bit 3, LSB is bit 0. Used to select the address of the Control registers or FIFOs for reading or writing data.
IRQ_N	**Output.** Indicates that there is an interrupt. To identify the source of the interrupt the content of the IS register should be read.
D[7:0]	**Bi directional.** PBI data bus. MSB is bit 7, LSB is bit 0. Used for reading or writing of external data.
RDN	**Input.** PBI external data read strobe
WRN	**Input.** PBI external data write strobe

7. I/O Buffer Information

In this section, the DC characteristics of the I/O buffers are presented.

I/O Type	I/O Characteristics
OSCO OUTPUT	VOL_{min} = VSS, VOL_{max} = 0.4 V VOH_{min} = 2.4 V, VOH_{max} = VDD 0 mA < IOL <6.0 mA -5.5 mA < IOH < -0 mA
OUTPUT	VOL_{min} = VSS, VOL_{max} = 0.4 V VOH_{min} = 2.4 V, VOH_{max} = VDD IOL = 2 mA, IOH = -2 mA (VDD = 5.0) IOL = 1 mA, IOH = -1 mA (VDD = 3.0)
INPUT	VIL_{min} = VSS, VIL_{max} = 0.3*VDD VIH_{min} =.7*VDD, VIH_{max} = VDD IIL_{min} = -1 µA, IIH_{max} = 1 µA
BI-DIREC-TIONAL	TBD

TABLE 2. *I/O Buffer DC Characteristics*

Note: TBD - To Be Defined

8. Timing Information

Information regarding selected waveforms is presented in this section.

General Timing

These are valid for all pins unless specified otherwise.

Parameter	Symbol	Min.	Nom.	Max.	Unit
Setup Time	T_{setup}	0	1.17	2.54	nS
Hold Time	T_{hold}	0	0.50	1.18	nS
Pulse Width	T_{width}	1.25			nS

TABLE 3. *General AC Timing Information*

9. Absolute Maximum Rating

Parameter	Symbol	Value	Unit
DC Supply Voltage	$V_{dd} - V_{ss}$	-0.3 to 7.0	V
Voltage, Any Pin to V_{ss}	V_{in}	-0.3 to V_{dd} + 0.3	V
DC Current, Any Pin (except V_{dd} and V_{SS})	I	±10	mA
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	-55 to 150	°C

TABLE 4. *Absolute Maximum Rating*

10. Recommended Operating Conditions

Parameter	Symbol	Min.	Nom.	Max.	Unit
DC Supply Voltage	V_{dd}	2.7	3.0/3.3/5.0	5.5	V
Power Dissipation at 5V	P_{dis}	15	90	130	mW
Master Oscillator	f_{osc}		5-40	60*	MHz

TABLE 5. *Recommended Operating Conditions*

Note: * denotes estimated value.

11. System Performance

A significant number of the system performance parameters depend heavily on the RF/ Analog circuits. The information presented here therefore represents only an estimate of these parameters.

Parameter	Estimated Performance
Oscillator Stability	Depends primarily on the analog circuitry but < 15 ppm over temperature range and aging (for 1 dB sensitivity degradation) should be achievable.
Acquisition Time	< 100 bits average < 200 bits for 99.9% probability of acquisition at S/N of 2 dB (applies for first burst only).
Interference Immunity In channel (±1.365 MHz)	-6 dB J/S worst case CW Jammer to Signal power ratio
Sensitivity in White Noise (half-duplex mode)	19.0 dB E_b/N_0 for BER = 10^{-5}. 17.5 dB E_b/N_0 for BER = 10^{-4}. 16.5 dB E_b/N_0 for BER = 10^{-3}.
Estimated Power Dissipation (5 Volt operation)	50.7 mW average in TDD mode at 32 Kbps full-duplex 76.8 mW average in TDD mode at 64 Kbps full-duplex
Estimated Power Dissipation (3 Volt operation)	15.0 mW average in TDD mode at 32 Kbps full-duplex

TABLE 6. *System Performance*

12. Pin Assignment

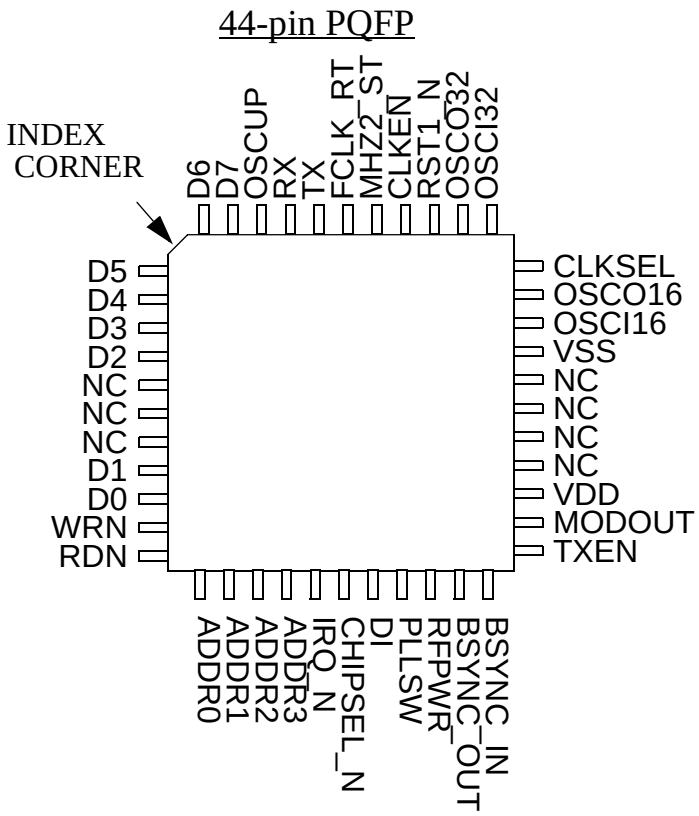


Figure 14. *Pin Assignment*

13. Application Information

In this section, several application issues concerning the use of the SS1101C are discussed.

13.1. Notes on half-duplex Operation

The receiver will not be locked until the initial acquisition process has been completed. This process typically takes from 60-110 bits depending on the condition of the radio link. It is imperative, therefore, for the packet to carry framing information so that the beginning and end of the packet can be detected (for example, a high-speed synchronous data link protocol such as HDLC provides its own framing structure in the packets it transmits).

In addition, sufficient preamble bits must be transmitted prior to actual data transmission so that the receiver will be locked and ready to deliver data when actual data arrives. The chip will generate RXFIFO interrupts after the lock is achieved. The interrupt can be generated even if there is no data sent by the transmitting side. A transmitting chip with no data to send continuously sends all “0”s, this will lock a receiving chip and continuously generate the RXFIFO interrupt on the receiving side.

The TXFIFO interrupt should be disabled in a receiving chip, while the RXFIFO interrupt should be disabled in the transmitting chip. This should be done to avoid the need to service any non-useful interrupts.

13.2. Selecting the Master Oscillator Frequency

A complete clock generator has been included in the SS1101C as to reduce the system clocking requirement. Nominally, only a single crystal or clock oscillator is required for powering the entire SS1101C. The required crystal or clock oscillator frequency is dependent on the data rate and in general can be calculated from the following equations:

$$\begin{aligned} f_{osc} &= 192 \times 2.6667 x f_{codec} = \quad \text{for full-duplex voice} \\ f_{osc} &= 512 \times f_{data} \quad \text{for full-duplex data} \\ f_{osc} &= 192 \times f_{data} \quad \text{for half-duplex data} \end{aligned} \qquad \textbf{(EQ 5)}$$

where f_{osc} is the master oscillator frequency, f_{codec} is the bit-rate clock of the codec, and f_{data} is the data rate. For example, for a 32 Kbps ADPCM voice, f_{codec}= 32KHz, and the required f_{osc} is 16.384 MHz. For 64 Kbps full-duplex data, f_{data} = 64 Kbps and the required master oscillator frequency is 32.768 MHz. For 170 Kbps half-duplex data, f_{data} = 170 Kbps and the required master oscillator frequency is 30.72 MHz.

13.3. Programming the SS1101C

In the following, a brief discussion on programming the SS1101C for the various modes of operation is presented. First, the loading of the PN sequences A, B, C, D and UW is required for operation in all modes.

The programming of the PLSL, CNTLR, ACC1RES, and WSL depend on several environmental and system related factors. For example, the sizing of PLSL and CNTLR windows involves trade-off considerations in the PLL’s dynamic performance. In general, if smaller window size is used, the PLL will behave as if it has a smaller loop bandwidth with higher noise filtering but at the expense of slower dynamic response. If larger window size is used, the PLL will respond quicker dynamically but its performance will be degraded because more noise is allowed to enter the system. ***Please note that the width of the Central Zone must be smaller than or equal to the size of the ESD window*** (this means that the ESD window size should NOT be set to 8, it was included on the chip for testing purpose only).

Similarly, the width of the detection window, WSL, should be large enough to take advantage of multipath combining but should not be so large that excessive noise is allowed into the receiver causing receiver sensitivity degradation. In general, these

parameters can be experimentally optimized for a particular environment. Otherwise, it is recommended that these parameters be programmed to values in the middle of the programmable range (for example, set PLSL to 12 samples wide, CNTLR to 10 samples wide, and WSL to 8 samples wide).

In the full-duplex or TDD mode, ACC1RES should normally be set to “0” for no ACC1 reset during each “freeze PLL” period. The only instance where ACC1RES should be set “1” to reset ACC1 is if the frequency offset between the transmitter and receiver is known to be very small. In this case, the performance of the PLL will be slightly enhanced if ACC1 is reset during each “freeze PLL” period. In half-duplex operation. ACC1RES should be set to “1” to always reset ACC1.

CI_h[0] is used to set the SS1101C to be either a master or a slave. Typically, in a cordless phone application, the unit (either the handset or the base station) that initiates the signalling process should be programmed to become the master. Thus, when dialing into the PSTN (Public Switched Telephone Network), the handset unit is configured to be the master and when receiving an incoming phone call, the base station is configured as the master.

NOTE, for half-duplex operation, CI_h[0] MUST be set to LO (e.g., as a slave). There is no concept of master or slave in the half-duplex operation. Instead, the SS1101C is keyed by the RTS_N bit enable to go into transmit mode. The SS1101C stays in the receive mode otherwise.

The number of allowable errors in UW depends on the application. For example, applications that can tolerate a larger BER can usually allow more UW errors while still maintaining a reasonable communication link as in the case of voice applications.

Finally, CI_h[4] enables or disables the Locking State Machine. The locking state machine when used in conjunction with the programmable allowable UW errors gives the system designer the flexibility to tailor the SS1101C for a particular operating environment. Typically, by enabling the Locking State Machine and by allowing more UW errors, the SS1101C will continue to operate normally even in a marginal communication link channel without repeatedly loosing lock and going into acquisition. The disadvantage is the corresponding increase in the data errors; for some critical applications, this might not be tolerable. In this case, the number of allowable UW errors can be reduced and the locking state machine turned off.

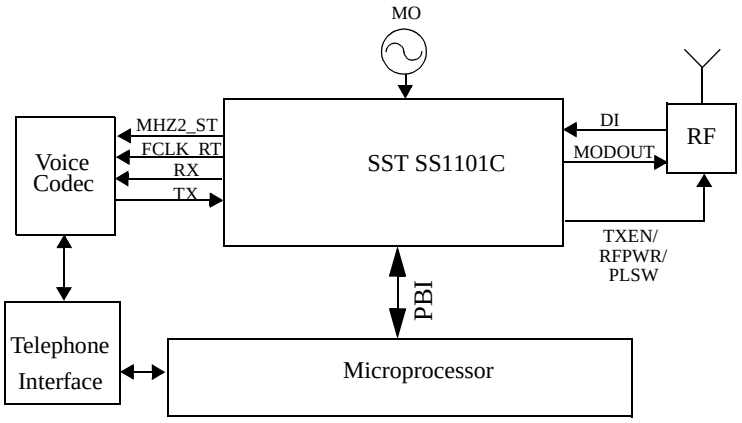


Figure 15. *Sample Block Diagram for a Cordless Phone System*

In Figure 15., a simple cordless phone system block diagram is shown. Note that the setup in the base station will be slightly different than that for the handset. For simplicity, only a generic block diagram is shown.

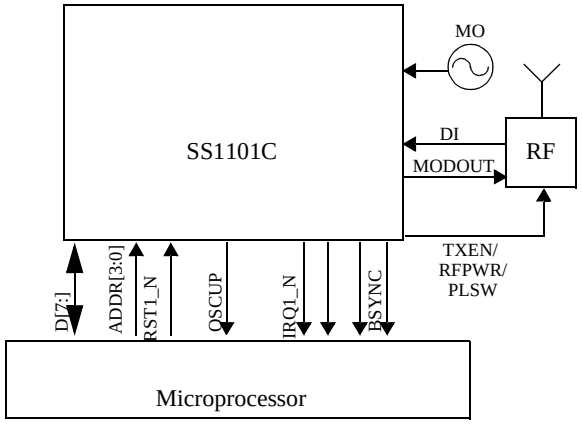


Figure 16. *Sample Block Diagram for a Data Modem*

In FIGURE 16, a sample block diagram for use as a data modem is shown.

13.4. PN Sequence and UW Selection

Four 32-bit PN sequences and one 22-bit Unique Word (UW) are required for each spread spectrum communication device. Together, they can constitute a “security code” or “identification code” which can be use to distinguish different users as well as to provide privacy. In addition, the PN sequences and UW participate in the signal acquisition and burst synchronization processes. In order to ensure good system performance, the PN sequences and UW must be selected with some care. In the following, guidelines for choosing the PN sequences and UW are presented.

13.4.1 PN Sequence Selection

The four PN sequences are used to represent a di-bit symbol in the SS1101C. In order to correctly decode the transmitted symbol at the receiver, the following principles should be followed when choosing the four PN sequences.

1. The four PN sequences should be orthogonal to each other. Two PN sequences A and B are orthogonal to each other if,

$$\sum_{i=0}^{31} a_i \cdot b_i = 0 \qquad \textbf{(EQ 6)}$$

   where PN sequence $A = [A_{31}, A_{30}, A_{29},\ldots, A_1, A_0]$, $a_i = -1$ for $A_i = 0$, and $a_i = 1$ for $A_i = 1$; similarly for B.
2. The PN sequences should be even, i.e., each sequence should have the same number of zeros and ones.
3. The PN sequences should not have more than four consecutive identical bits.

With these three criteria outlined above, it is possible to generate a large set of valid PN sequences. Two additional and optional criteria can be used to further identify PN sequences for reduced self- and cross-interference.

1. The auto-correlation side lobes of the PN sequences should be less than the auto-correlation of the main lobe by at least 4.
2. The cross-correlation of PN sequences between sets (one set being the four orthogonal PN sequences for one spread spectrum chip) should also be less than the auto-correlation of the main lobe by at least 4.

13.4.2 UW Selection

The UW is used in the receiver in full-duplex mode to establish synchronization. To avoid interference, the UW must be chosen such that it has good auto-correlation and cross-correlation properties. The auto-correlation of a sequence A denoted as S_N is defined as,

$$S_N = \sum_{i=0}^{L} a_i \cdot a_{i-N} \qquad \textbf{(EQ 7)}$$

where L is the length of the sequence A, $-L < N < L$, $N \neq 0$, $a_i = -1$ for $i < 0$, and $a_i = a_{i-22}$ for $i \geq L$. A “window” version of S_N can also be defined as per (EQ 7) with the exception that $0 < N < W$, where W is the window size. The desired auto-correlation

property is that the maximum value of the auto-correlation S_N (with or without the window where the window size is the size of the detection window, WSL) is less than $L - 2 \times T$, where T is the allowable number of UW errors programmed into the SS1101C.

The cross-correlation of two sequences A and B, denoted by R_N is defined as,

$$R_N = \sum_{i=0}^{L} a_i \cdot b_{i-N} \quad \textbf{(EQ 8)}$$

where L is the length of the sequence, $0 \le N < L$, and $b_i = b_{i+22}$ for $i < 0$. As before, the desirable cross-correlation property is that the maximum value of the cross-correlation R_N is less than $L - 2 \times T$, where L and T are as defined previously.

Requirements for choosing good UWs can be thus summarized by the following equations.

$$\begin{aligned} S_N &< L - 2 \times T \\ R_N &< L - 2 \times T \end{aligned} \quad \textbf{(EQ 9)}$$

For example, when T is programmed to be 4, then S_N and R_N should be less than 14 since L is 22.

13.5. Generating the PN and UW sequences

There are many ways of generating the PN and UW sequences, including brute force search of the complete code space. A more efficient but probably not optimal way of generating the PN and UW sequences is to

1. Generate the M and Gold sequences of order N where

$$N = \log_2 L \quad \textbf{(EQ 10)}$$

   and where L is the length of the PN or UW sequence.
2. Because M and Gold sequences are only $2^N - 1$ bits long, it is necessary to append an additional bit to these sequences so that they are 2^N bits long. The additional bit should be chosen such that the modified M or Gold sequence is even.
3. Apply the criteria outlined in the previous sections to pick out the good set of PN and UW sequences.

13.6. Using Burst Synchronization Feature

The SS1101C contains a burst synchronization feature that allows multiple chips to transmit and receive signals synchronously. By synchronizing their bursts, the interference amongst these units is greatly reduced. In order for the burst synchronization feature to work correctly, the SS1101Cs must be setup appropriately. First, a Master must be chosen so that the other devices derive their timing from it. For the Master, the BURST_OUT signal is connected to its own BURST_IN signal as well

as to the BURST_IN signals of the other devices. This establishes burst-level synchronization by forcing the burst cycle of each device to follow that of the Master.

13.7. Example of RF Front-End Block Diagram

In the following page an example of RF block diagram for the SS1101C chip is presented.

This block diagram is an example of RF front-end architecture; it uses minimum-frequency shift modulation (MSK / FSK). Other architectures are also possible using the SS1101C chip.

The chip rate depends on the data rate and the mode (duplex or half-duplex) of the application:

Mode	Application	Bit-Rate	Chip Rate	MSK Bandwidth
Full-Duplex	Voice or Data	32 Kbps	1.365 Mbps	2.048 Mhz
Full-Duplex	Data	50 Kbps	2.133 Mbps	3.200 Mhz
Full-Duplex	Voice or Data	64 Kbps	2.731 Mbps	4.096 Mhz
half-duplex	Data	32 Kbps	512 Kbps	768 Khz
half-duplex	Data	50 Kbps	800 Kbps	1.200 Mhz
half-duplex	Data	64 Kbps	1.024 Mbps	1.536 Mhz

Other data rates are possible up to the half-duplex maximum of 400 Kbps for the SS1101C.

The filters as shown in the block diagram should be specified as follows:

The antenna Band-Pass filter should cover the complete frequency range, for instance, 902 - 928 Mhz.

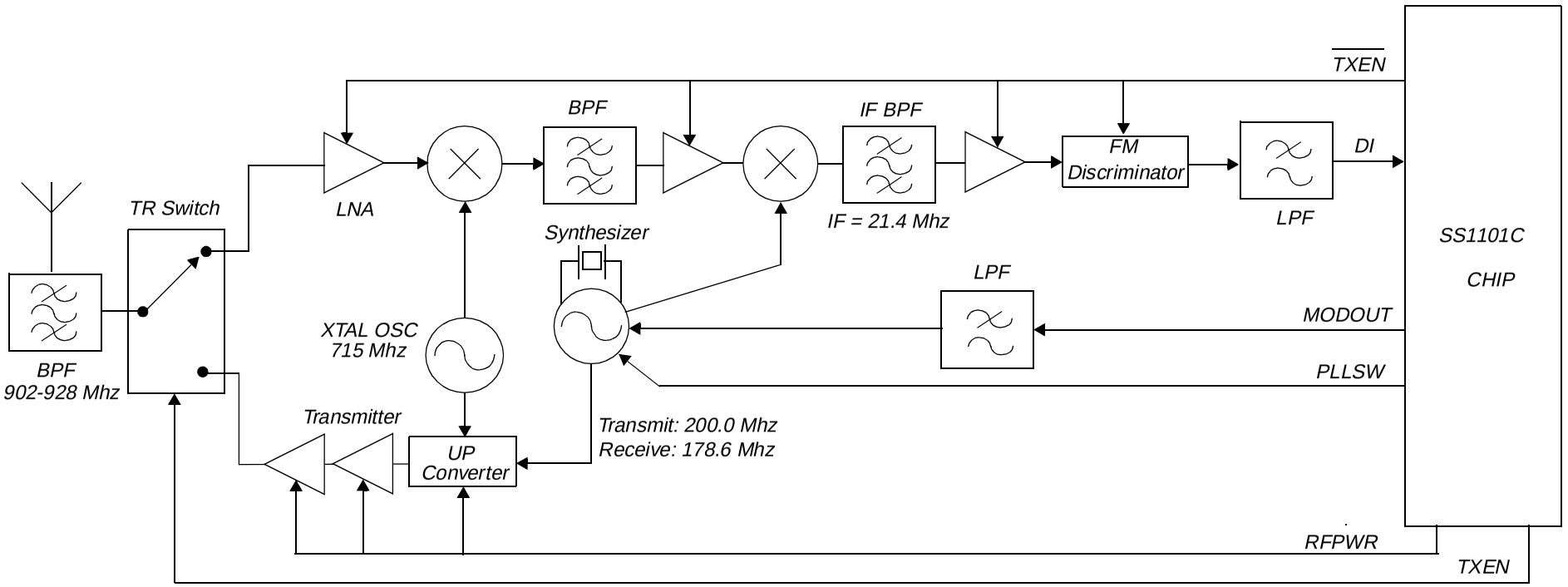
The receiver IF BPF should be 20% wider than twice the chip rate. By making it somewhat wider, you can avoid excessive group delay distortion at the band edges.

The LPF following the discriminator should have a 3 dB cutoff frequency around the chip rate.

The LPF preceding the synthesizer should also have its 3 dB cutoff frequency around the chip rate.

The bandwidth of the phase-lock loop of the synthesizer should not be wider than 0.75% of the chip rate. That way it will not suppress modulation at 3% of the chip rate and above.

Frequency Stability: within 50 Khz for the total chain: transmit and receive units. This should be easy to achieve.



Example of MSK Radio RF Front-End