

**SSD1300**

***Advance Information***

**104 x 48 Dot Matrix  
OLED/PLED Segment/Common Driver with Controller**

This document contains information on a new product. Specifications and information herein are subject to change without notice.

## 1 GENERAL INFORMATION

SSD1300 is a single-chip CMOS OLED/PLED driver with controller for organic/polymer light emitting diode dot-matrix graphic display system. SSD1300 consists of 104 segments, 48 commons that can support a maximum display resolution of 104x48. Besides, there are 4 colour selections to support monochrome or area colour OLED/PLED. This IC is designed for Common Cathode type OLED panel.

SSD1300 embeds with contrast control, display RAM and oscillator, which reduces the number of external components and power consumption. SSD1300 is suitable for many compact portable applications, such as mobile phone sub-display, calculator and MP3 player, etc.

## 2 FEATURES

- Support maximum 104 x 48 dot matrix panel
- Area colour support with 4 Colour Selection and 64 steps per colour
- Logic voltage supply: VDD=2.4V - 3.5V
- High voltage supply: VCC=7.0V - 16.0V
- Segment output current: 320uA
- Maximum common sink current: 45mA
- Embedded 104x48 bit SRAM display buffer
- 256-step contrast control on monochrome passive OLED panel
- On-Chip Oscillator
- Programmable Frame Frequency and Multiplexing Ratio
- 8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface, Serial Peripheral Interface
- Row re-mapping and Column re-mapping
- Vertical scrolling
- Automatic horizontal scrolling function
- Low power consumption
- Wide range of operating temperatures: -40 to 85 °C

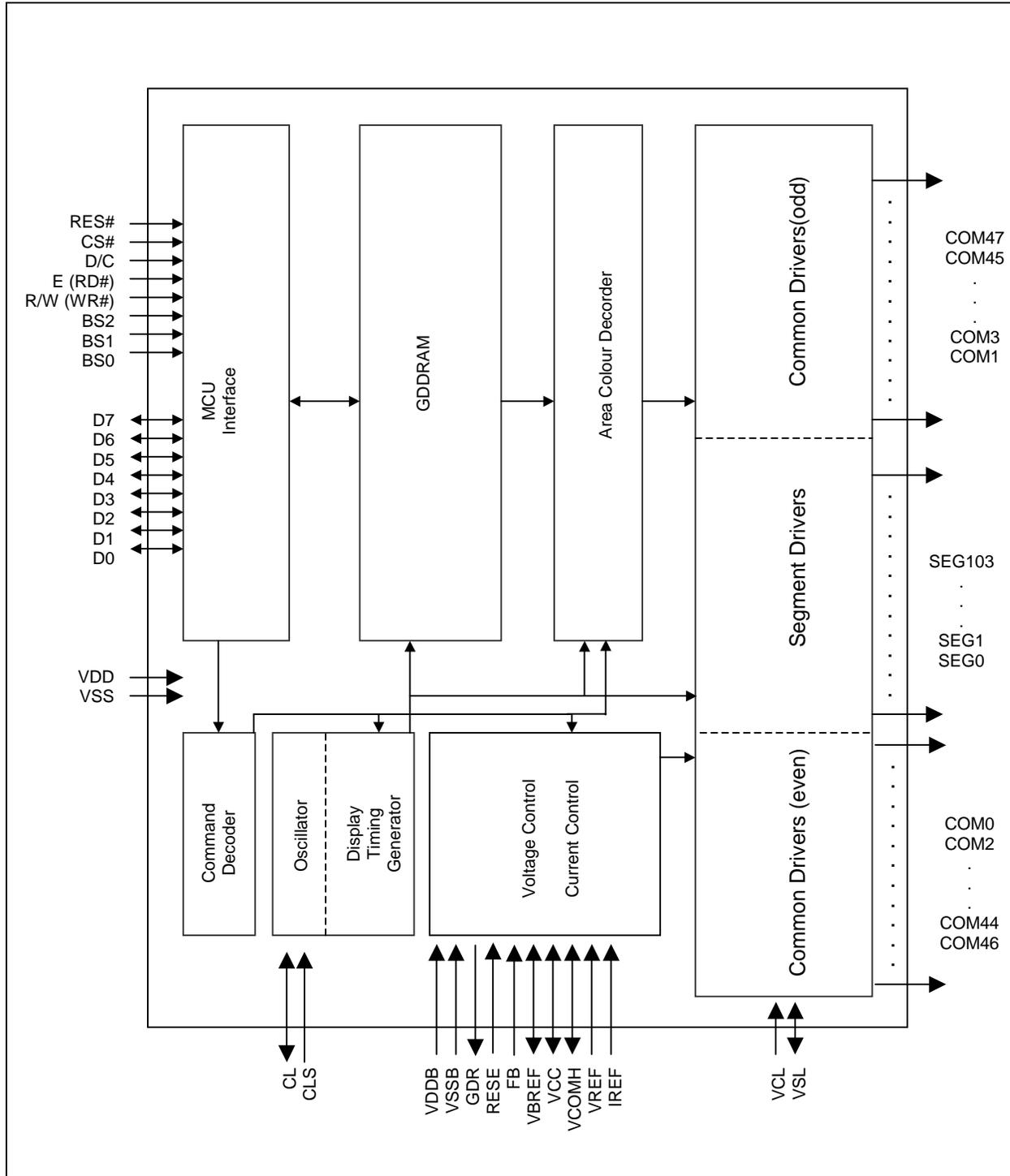
## 3 ORDERING INFORMATION

Table 1 - Ordering Information

Ordering Part Number	SEG	COM	Package Form	Reference	Remark
SSD1300Z	104	48	Gold Bump Die	Page 6	Die size: 7.29mm x 1.56mm Pad pitch: COM 51.8µm SEG 52.2µm
SSD1300TR1	104	48	TAB	Page 41	<ul style="list-style-type: none"><li>• 35mm film</li><li>• 4 sprocket hole</li><li>• Folding TAB</li><li>• 80 / 68 / SPI interface</li><li>• Output lead pitch 0.0998mm</li></ul>
SSD1300T3R1	96	48	TAB	Page 35	<ul style="list-style-type: none"><li>• 35mm film</li><li>• 4 sprocket hole</li><li>• Folding TAB</li><li>• 80 / 68 / SPI interface</li><li>• Output lead pitch 0.12974mm</li></ul>

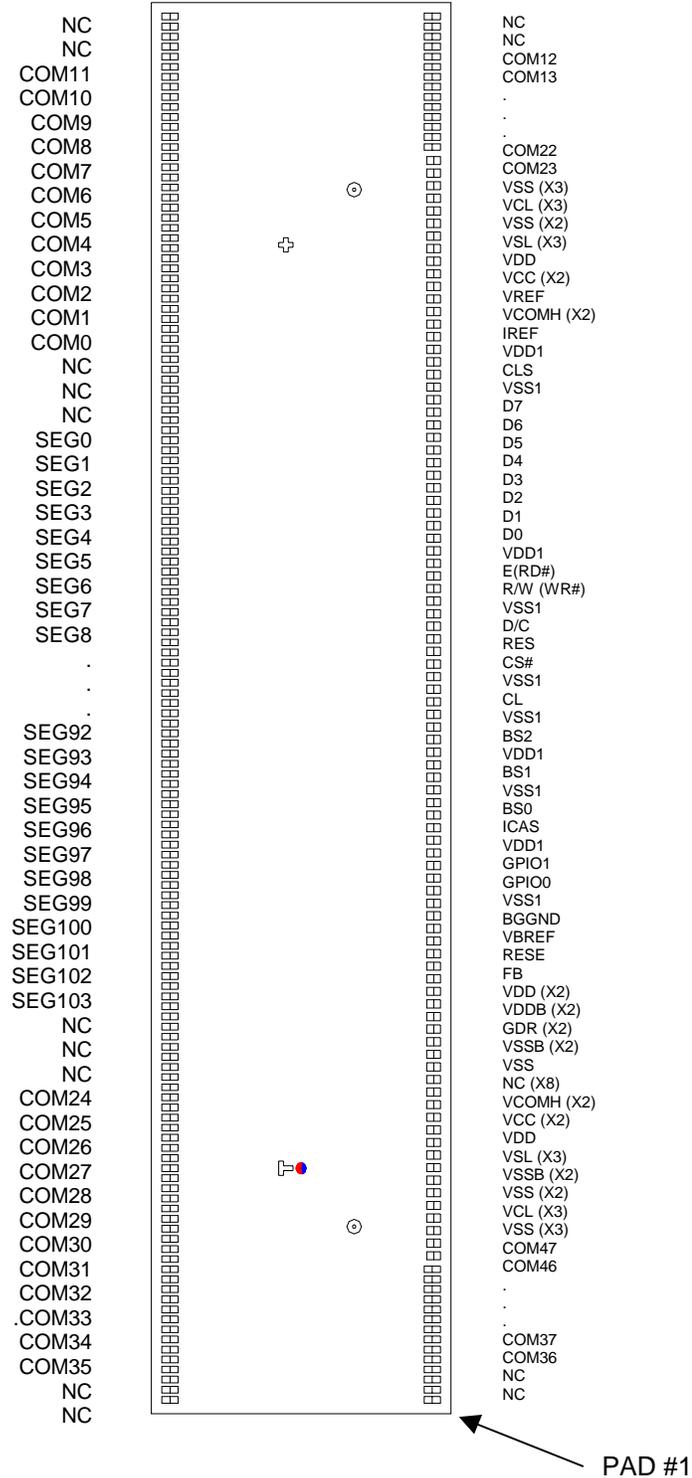
## 4 BLOCK DIAGRAM

Figure 1 - Block Diagram



## 5 SSD1300 GOLD-BUMP DIE PAD ASSIGNMENT

Figure 2 - SSD1300Z Pin Assignment

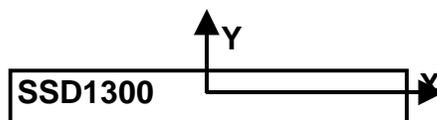


**Table 2 - SSD1300Z Die Pad Coordinates**

Pad no.	Signal	X-pos	Y-pos	Pad no.	Signal	X-pos	Y-pos	Pad no.	Signal	X-pos	Y-pos
1	NC	-3571.3	-679.6	61	BS1	162.5	-686.6	121	COM9	3363.3	679.6
2	NC	-3519.1	-679.6	62	VDD1	227.5	-686.6	122	COM8	3311.5	679.6
3	COM36	-3466.9	-679.6	63	BS2	292.5	-686.6	123	COM7	3259.7	679.6
4	COM37	-3415.1	-679.6	64	VSS1	357.5	-686.6	124	COM6	3207.9	679.6
5	COM38	-3363.3	-679.6	65	CL	422.5	-686.6	125	COM5	3156.1	679.6
6	COM39	-3311.5	-679.6	66	VSS1	487.5	-686.6	126	COM4	3104.3	679.6
7	COM40	-3259.7	-679.6	67	CSB	552.5	-686.6	127	COM3	3052.5	679.6
8	COM41	-3207.9	-679.6	68	RES	617.5	-686.6	128	COM2	3000.7	679.6
9	COM42	-3156.1	-679.6	69	D/C	682.5	-686.6	129	COM1	2948.9	679.6
10	COM43	-3104.3	-679.6	70	VSS1	747.5	-686.6	130	COM0	2897.1	679.6
11	COM44	-3052.5	-679.6	71	R/W (WR#)	812.5	-686.6	131	NC	2844.9	679.6
12	COM45	-3000.7	-679.6	72	E(RD#)	877.5	-686.6	132	NC	2792.7	679.6
13	COM46	-2948.9	-679.6	73	VDD1	942.5	-686.6	133	NC	2740.5	679.6
14	COM47	-2897.1	-679.6	74	D0	1007.5	-686.6	134	SEG0	2688.3	679.6
15	VSS	-2827.5	-686.6	75	D1	1072.5	-686.6	135	SEG1	2636.1	679.6
16	VSS	-2762.5	-686.6	76	D2	1137.5	-686.6	136	SEG2	2583.9	679.6
17	VSS	-2697.5	-686.6	77	D3	1202.5	-686.6	137	SEG3	2531.7	679.6
18	VCL	-2632.5	-686.6	78	D4	1267.5	-686.6	138	SEG4	2479.5	679.6
19	VCL	-2567.5	-686.6	79	D5	1332.5	-686.6	139	SEG5	2427.3	679.6
20	VCL	-2502.5	-686.6	80	D6	1397.5	-686.6	140	SEG6	2375.1	679.6
21	VSS	-2437.5	-686.6	81	D7	1462.5	-686.6	141	SEG7	2322.9	679.6
22	VSS	-2372.5	-686.6	82	VSS1	1527.5	-686.6	142	SEG8	2270.7	679.6
23	VSSBUF	-2307.5	-686.6	83	CLS	1592.5	-686.6	143	SEG9	2218.5	679.6
24	VSSBUF	-2242.5	-686.6	84	VDD1	1657.5	-686.6	144	SEG10	2166.3	679.6
25	VSL	-2177.5	-686.6	85	IREF	1722.5	-686.6	145	SEG11	2114.1	679.6
26	VSL	-2112.5	-686.6	86	VCOMH	1787.5	-686.6	146	SEG12	2061.9	679.6
27	VSL	-2047.5	-686.6	87	VCOMH	1852.5	-686.6	147	SEG13	2009.7	679.6
28	VDD	-1982.5	-686.6	88	VREF	1917.5	-686.6	148	SEG14	1957.5	679.6
29	VCC	-1917.5	-686.6	89	VCC	1982.5	-686.6	149	SEG15	1905.3	679.6
30	VCC	-1852.5	-686.6	90	VCC	2047.5	-686.6	150	SEG16	1853.1	679.6
31	VCOMH	-1787.5	-686.6	91	VDD	2112.5	-686.6	151	SEG17	1800.9	679.6
32	VCOMH	-1722.5	-686.6	92	VSL	2177.5	-686.6	152	SEG18	1748.7	679.6
33	NC	-1657.5	-686.6	93	VSL	2242.5	-686.6	153	SEG19	1696.5	679.6
34	NC	-1592.5	-686.6	94	VSL	2307.5	-686.6	154	SEG20	1644.3	679.6
35	NC	-1527.5	-686.6	95	VSS	2372.5	-686.6	155	SEG21	1592.1	679.6
36	NC	-1462.5	-686.6	96	VSS	2437.5	-686.6	156	SEG22	1539.9	679.6
37	NC	-1397.5	-686.6	97	VCL	2502.5	-686.6	157	SEG23	1487.7	679.6
38	NC	-1332.5	-686.6	98	VCL	2567.5	-686.6	158	SEG24	1435.5	679.6
39	NC	-1267.5	-686.6	99	VCL	2632.5	-686.6	159	SEG25	1383.3	679.6
40	NC	-1202.5	-686.6	100	VSS	2697.5	-686.6	160	SEG26	1331.1	679.6
41	VSS	-1137.5	-686.6	101	VSS	2762.5	-686.6	161	SEG27	1278.9	679.6
42	VSSBUF	-1072.5	-686.6	102	VSS	2827.5	-686.6	162	SEG28	1226.7	679.6
43	VSSBUF	-1007.5	-686.6	103	COM23	2892.5	-679.6	163	SEG29	1174.5	679.6
44	GDR	-942.5	-686.6	104	COM22	2948.9	-679.6	164	SEG30	1122.3	679.6
45	GDR	-877.5	-686.6	105	COM21	3000.7	-679.6	165	SEG31	1070.1	679.6
46	VDDBUF	-812.5	-686.6	106	COM20	3052.5	-679.6	166	SEG32	1017.9	679.6
47	VDDBUF	-747.5	-686.6	107	COM19	3104.3	-679.6	167	SEG33	965.7	679.6
48	VDD	-682.5	-686.6	108	COM18	3156.1	-679.6	168	SEG34	913.5	679.6
49	VDD	-617.5	-686.6	109	COM17	3207.9	-679.6	169	SEG35	861.3	679.6
50	FB	-552.5	-686.6	110	COM16	3259.7	-679.6	170	SEG36	809.1	679.6
51	RESE	-487.5	-686.6	111	COM15	3311.5	-679.6	171	SEG37	756.9	679.6
52	VBREF	-422.5	-686.6	112	COM14	3363.3	-679.6	172	SEG38	704.7	679.6
53	BGGND	-357.5	-686.6	113	COM13	3415.1	-679.6	173	SEG39	652.5	679.6
54	VSS1	-292.5	-686.6	114	COM12	3466.9	-679.6	174	SEG40	600.3	679.6
55	GPIO0	-227.5	-686.6	115	NC	3519.1	-679.6	175	SEG41	548.1	679.6
56	GPIO1	-162.5	-686.6	116	NC	3571.3	-679.6	176	SEG42	495.9	679.6
57	VDD1	-97.5	-686.6	117	NC	3571.3	679.6	177	SEG43	443.7	679.6
58	ICAS	-32.5	-686.6	118	NC	3519.1	679.6	178	SEG44	391.5	679.6
59	BS0	32.5	-686.6	119	COM11	3466.9	679.6	179	SEG45	339.3	679.6
60	VSS1	97.5	-686.6	120	COM10	3415.1	679.6	180	SEG46	287.1	679.6

Pad no.	Signal	X-pos	Y-pos
181	SEG47	234.9	679.6
182	SEG48	182.7	679.6
183	SEG49	130.5	679.6
184	SEG50	78.3	679.6
185	SEG51	26.1	679.6
186	SEG52	-26.1	679.6
187	SEG53	-78.3	679.6
188	SEG54	-130.5	679.6
189	SEG55	-182.7	679.6
190	SEG56	-234.9	679.6
191	SEG57	-287.1	679.6
192	SEG58	-339.3	679.6
193	SEG59	-391.5	679.6
194	SEG60	-443.7	679.6
195	SEG61	-495.9	679.6
196	SEG62	-548.1	679.6
197	SEG63	-600.3	679.6
198	SEG64	-652.5	679.6
199	SEG65	-704.7	679.6
200	SEG66	-756.9	679.6
201	SEG67	-809.1	679.6
202	SEG68	-861.3	679.6
203	SEG69	-913.5	679.6
204	SEG70	-965.7	679.6
205	SEG71	-1017.9	679.6
206	SEG72	-1070.1	679.6
207	SEG73	-1122.3	679.6
208	SEG74	-1174.5	679.6
209	SEG75	-1226.7	679.6
210	SEG76	-1278.9	679.6
211	SEG77	-1331.1	679.6
212	SEG78	-1383.3	679.6
213	SEG79	-1435.5	679.6
214	SEG80	-1487.7	679.6
215	SEG81	-1539.9	679.6
216	SEG82	-1592.1	679.6
217	SEG83	-1644.3	679.6
218	SEG84	-1696.5	679.6
219	SEG85	-1748.7	679.6
220	SEG86	-1800.9	679.6
221	SEG87	-1853.1	679.6
222	SEG88	-1905.3	679.6
223	SEG89	-1957.5	679.6
224	SEG90	-2009.7	679.6
225	SEG91	-2061.9	679.6
226	SEG92	-2114.1	679.6
227	SEG93	-2166.3	679.6
228	SEG94	-2218.5	679.6
229	SEG95	-2270.7	679.6
230	SEG96	-2322.9	679.6
231	SEG97	-2375.1	679.6
232	SEG98	-2427.3	679.6
233	SEG99	-2479.5	679.6
234	SEG100	-2531.7	679.6
235	SEG101	-2583.9	679.6
236	SEG102	-2636.1	679.6
237	SEG103	-2688.3	679.6
238	NC	-2740.5	679.6
239	NC	-2792.7	679.6
240	NC	-2844.9	679.6

Pad no.	Signal	X-pos	Y-pos
241	COM24	-2897.1	679.6
242	COM25	-2948.9	679.6
243	COM26	-3000.7	679.6
244	COM27	-3052.5	679.6
245	COM28	-3104.3	679.6
246	COM29	-3156.1	679.6
247	COM30	-3207.9	679.6
248	COM31	-3259.7	679.6
249	COM32	-3311.5	679.6
250	COM33	-3363.3	679.6
251	COM34	-3415.1	679.6
252	COM35	-3466.9	679.6
253	NC	-3519.1	679.6
254	NC	-3571.3	679.6



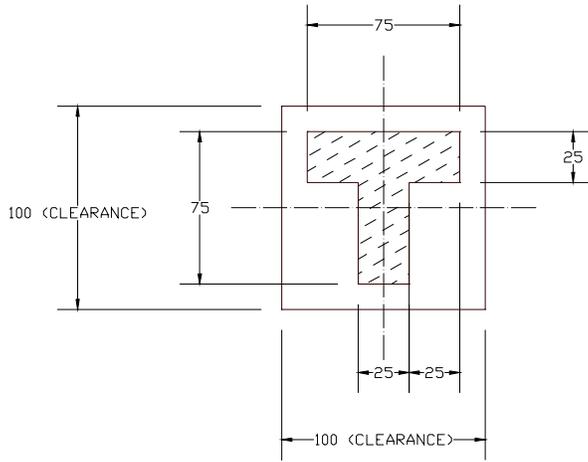
↑  
**Pad 1,2,3,? >116**  
 Gold Bumps face up

Die size	7.29mm x 1.56mm
Die height	457 +/- 25um

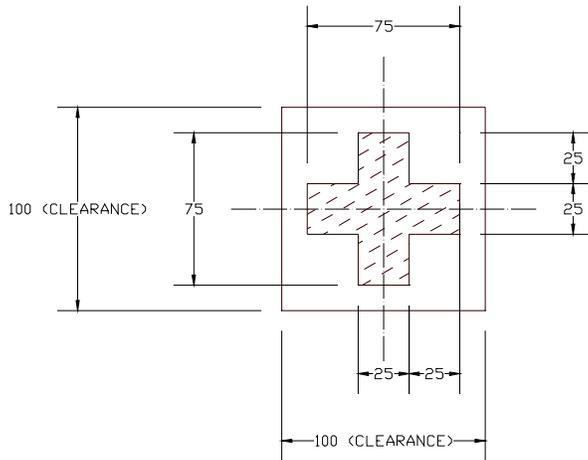
Bump height	Nominal 18um
Bump size	
Pad 1-14, 103-254	34um x 84um
Pad 15-102	42um x 70um

Alignment mark		
T shape	(-2392.0, 79.5)	75um x 75um
+ shape	(2392.0, 79.5)	75um x 76um
Circle	(-2677.0, -274.6)	R37.5um, inner 18um
Circle	(2677.0, -274.6)	R37.5um, inner 18um

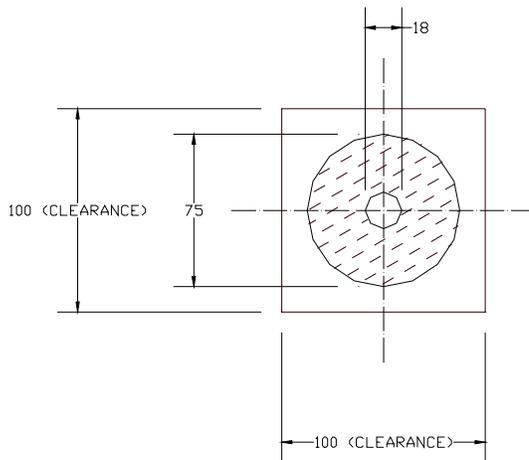
**Figure 3 - SSD1300Z Alignment mark dimensions**



T shape



+ shape



Circle

Unit in um

## 6 PIN DESCRIPTION

### CL

This pin is the system clock input. When internal clock is enabled, this pin should be left open. The internal clock is output from this pin. When internal oscillator is disabled, this pin receives display clock signal from external clock source.

### CLS

This is the internal clock enable pin. When it is pulled HIGH, internal clock is enabled. When it is pulled LOW, the internal clock is disabled, an external clock source must be connected to the CL pin for normal operation.

### BS0, BS1, BS2

These pins are MCU interface selection input. See the following table:

	6800-parallel interface	8080-parallel interface	Serial interface
BS0	0	0	0
BS1	0	1	0
BS2	1	1	0

### CS#

This pin is the chip select input. The chip is enabled for MCU communication only when CS# had been pulled low.

### RES#

This is a reset signal input pin. When it is pulled LOW, initialization of the chip is executed.

### D/C

This is the Data/Command control pin. When it is pulled HIGH, the input at D<sub>7</sub>-D<sub>0</sub> is treated as display data. When it is pulled LOW, the input at D<sub>7</sub>-D<sub>0</sub> is transferred to the command registers. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.

### R/W (WR#)

This is a MCU interface input pin. When 6800-series Parallel Interface mode is selected, this pin is used as Read/Write (R/W) selection input. Pull this pin to HIGH for read mode and pull it to LOW for write mode.

When 8080-series Parallel Interface mode is selected, this pin is used as Write (WR#) selection input. Pull this pin to LOW for write mode. Data write operation is initiated when this pin is pulled LOW and the CS# is pulled LOW.

### E (RD#)

This is a MCU interface input pin. When 6800-series Parallel Interface is selected, this pin is used as Enable (E) signal. Read/Write operation is initiated when this pin is pulled HIGH and the CS# pin is pulled LOW. When 8080-series Parallel Interface is selected, this pin is used to receive the Read Data (RD#) signal. Data read operation is initiated when this pin is pulled LOW and CS# pin is pulled LOW.

### D<sub>7</sub>-D<sub>0</sub>

These are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial interface mode is selected, D<sub>1</sub> will be the serial data input, SDIN, and D<sub>0</sub> will be the serial clock input, SCLK.

**VDD**

This is a voltage supply pin. It must be connected to external source.

**VSS**

This is a ground pin. It also acts as a reference for the logic pins and the OLED driving voltages. It must be connected to external ground.

**BGGND**

This is a ground pin for analog circuits. It must be connected to external ground

**VCC**

This is the most positive voltage supply pin of the chip. It should be supplied externally.

**VREF**

This is a voltage reference pin for pre-charge voltage in driving OLED device. Voltage should be set to match with the OLED driving voltage in current drive phase. It can either be supplied externally or by connecting to VCC.

**IREF**

This is a segment current reference pin. A resistor should be connected between this pin and  $V_{SS}$ . Set the current at 10uA.

**VCOMH**

This is an input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and VSS.

**Vddb**

This is a power supply pin for the internal buffer of the DC-DC voltage converter. It must be connected to  $V_{DD}$  when the converter is used.

**VSSB**

This is a ground pin for the internal buffer of the DC-DC voltage converter. It must be connected to  $V_{SS}$  when the converter is used.

**GDR**

This is an output pin drives the gate of the external NMOS of the booster circuit.

**RESE**

This is a source current pin of the external NMOS of the booster circuit.

**VB<sub>REF</sub>**

This is an internal voltage reference pin for booster circuit. A stabilization capacitor, typ. 1uF, should be connected to Vss.

**FB**

This is a feedback resistor input pin for the booster circuit. It is used to adjust the booster output voltage level,  $V_{cc}$ .

**COM0-COM47**

These pins provide the Common switch signals to the OLED panel. These pins are in high impedance state when display is OFF.

**SEG0-SEG103**

These pins provide the OLED segment driving signals. These pins are in high impedance stage when display is off.

**GPIO0, GPIO1, ICAS and M**

These are reserved pins. No connection should be made for these pins and left float individually.

**VSL**

This is a segment voltage reference pin. This pin should be connected to VSS externally.

**VCL**

This is a common voltage reference pin. This pin should be connected to VSS externally.

**VDD1**

VDD1 is internally connected to VDD. They are for pull high purpose for the neighbouring pins if necessary.

Main power supply should connect to VDD pins.

**VSS1**

VSS1 is internally connected to VSS. They are for pull low purpose for the neighbouring pins if necessary.

Main power supply should connect to VSS pin.

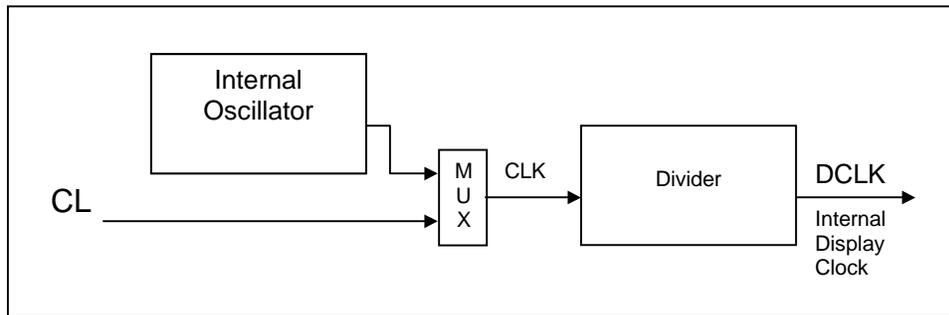
**NC**

These are reserved pins and should not be connected. Do not group or short NC pins.

## 7 FUNCTIONAL BLOCK DESCRIPTIONS

### Oscillator Circuit and Display Time Generator

Figure 4 - Oscillator Circuit



This module is an On-Chip low power RC oscillator circuitry (Figure 4). The oscillator generates the clock for the Display Timing Generator.

### Reset Circuit

When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 104x48 Display Mode
3. Normal segment and display data column address and row address mapping (SEG0 mapped to column address 00H and COM0 mapped to row address 00H)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 80H
9. Internal DC/DC booster is enable

### Command Decoder and Command Interface

This module determines whether the input data is interpreted as data or command. When the D/C# pin is pulled HIGH, the inputs at D<sub>7</sub>-D<sub>0</sub> are interpreted as data and will be written to Graphic Display Data RAM (GDDRAM). When it is pulled LOW, the inputs at D<sub>7</sub>-D<sub>0</sub> are interpreted as command, they will be decoded and be written to the corresponding command registers.

### MPU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D<sub>7</sub>-D<sub>0</sub>), R/W (WR#), E (RD#), D/C, CS#. When the R/W (WR#) pin is pulled HIGH, Read operation from the Graphic Display Data RAM (GDDRAM) or the status register occurs. When the R/W (WR#) pin is pulled LOW, Write operation to Display Data RAM or Internal Command Registers occurs, depending on the status of D/C input. The E (RD#) input serves as data latch signal (clock) when HIGH provided that CS# is LOW. Refer to Parallel Interface Timing Diagram of 6800-series microprocessors.

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed, which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 5 below.

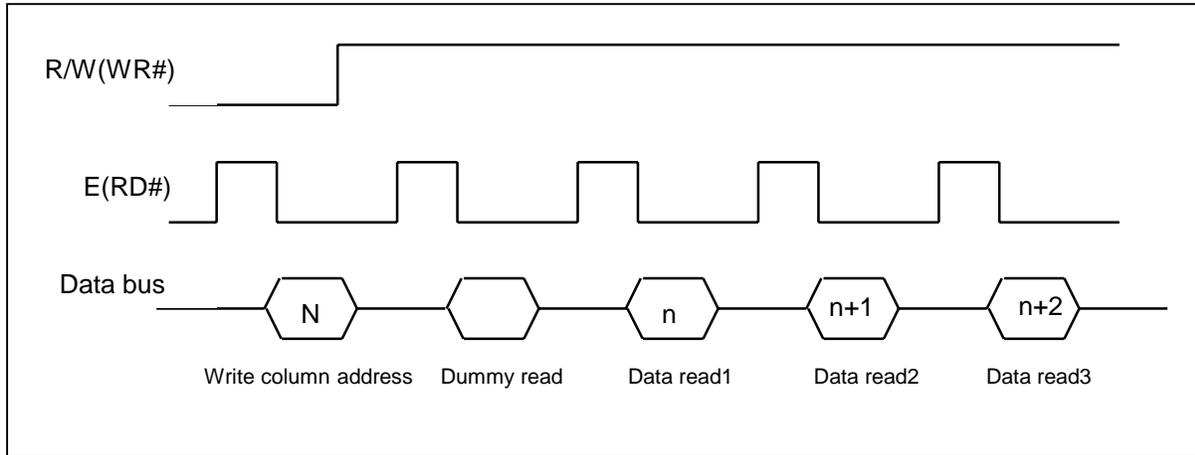


Figure 5 - Display data read back procedure - insertion of dummy read

### MPU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins (D<sub>7</sub>-D<sub>0</sub>), E (RD#), R/W(WR#), D/C, CS#. The E (RD#) input serves as data read latch signal (clock) when it is low, and provided that CS# is low. Display data or status register read is controlled by D/C.

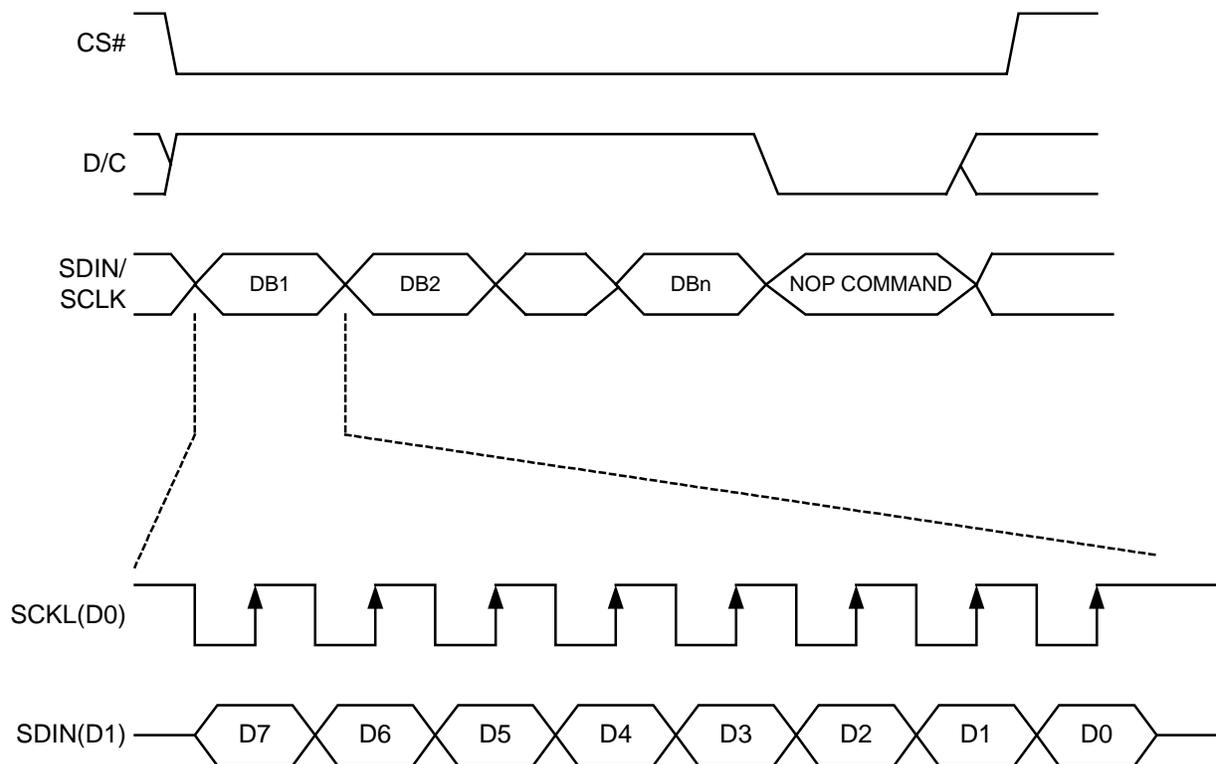
R/W (WR#) input serves as data write latch signal (clock) when it is high and provided that CS# is low. Display data or command register write is controlled by D/C. Refer to Parallel Interface Timing Diagram of 8080-series microprocessor. Similar to 6800-series interface, a dummy read is also required before the first actual display data read.

## MPU Serial Interface

The serial interface consists of serial clock SCLK, serial data SDIN, D/C, CS#. SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D<sub>7</sub>, D<sub>6</sub>, ... D<sub>0</sub>. D/C is sampled on every eighth clock and the data byte in the shift register is written to the Display Data RAM or command register in the same clock.

During data writing, an additional NOP command should be inserted before the CS# goes high (Refer to Figure 6).

**Figure 6 – Display data write procedure in SPI mode**



## Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 104x48 bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.

For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display.

## Current Control and Voltage Control

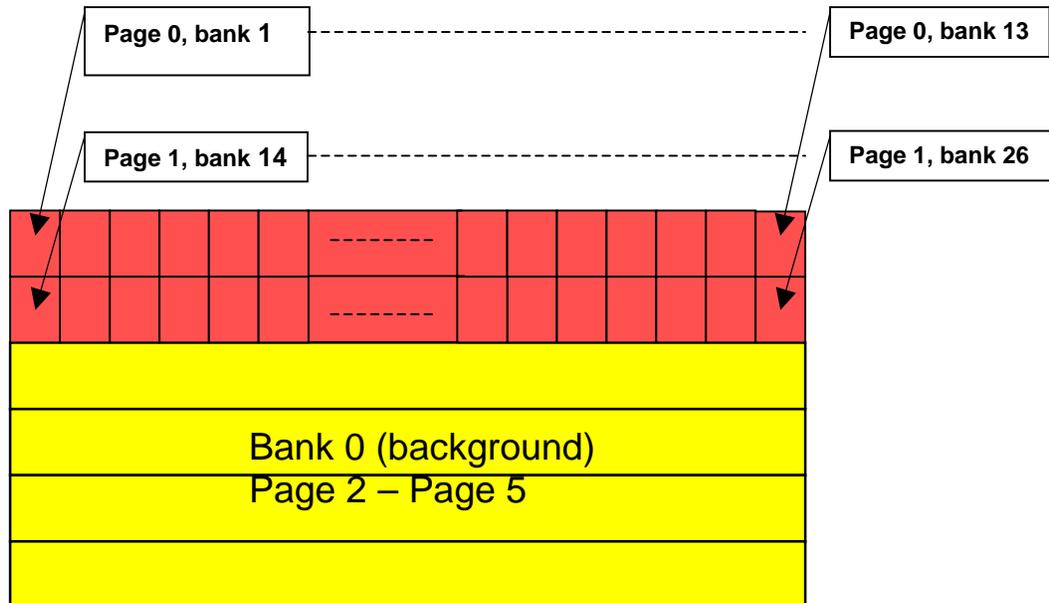
This block is used to derive the incoming power sources into the different levels of internal use voltage and current. V<sub>CC</sub> and V<sub>DD</sub> are external power supplies. V<sub>REF</sub> is reference voltage, which is used to derive driving voltage for segments and commons. I<sub>REF</sub> is a reference current source for segment current drivers.

### Segment Drivers/Common Drivers

Segment drivers deliver 104 current sources to drive OLED panel. The driving current can be adjusted from 0 to 320uA with 256 steps. Common drivers generate voltage scanning pulses.

### Area Colour Decoder

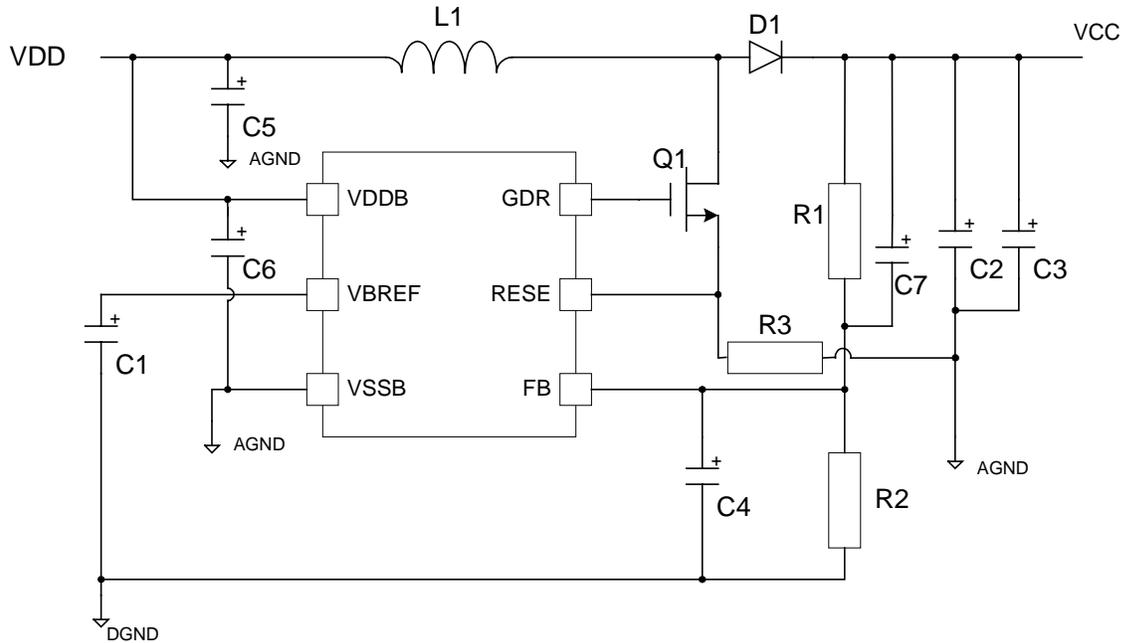
Page 0 and Page 1 of the display are divided into 26 banks. Each bank comprises of a display area of 8x8 pixels. Each bank can be matrices of 8x8 pixels. Each bank can be programmed to any one of the 4 colours (colour A, B, C, D). Detailed operation can be referred to the Command Table.



## DC-DC Voltage Converter

It is a switching voltage generator circuit, designed for handheld applications. In SSD1300, internal DC-DC voltage converter accompanying with an external application circuit (shown in below figure) can generate a high voltage supply  $V_{CC}$  from a low voltage supply input  $V_{DD}$ .  $V_{CC}$  is the voltage supply to the OLED driver block. Below application circuit is an example for the input voltage of 3V  $V_{DD}$  to generate  $V_{CC}$  of 12V @0mA ~ 20mA application.

Figure 7 - DC-DC voltage converter circuit



Remark:

1.  $V_{SSB}$  is tied to  $V_{SS}$  on SSD1300T3 package.
2.  $L1$ ,  $D1$ ,  $Q1$ ,  $C5$  should be grouped closed together on PCB layout.
3.  $R1$ ,  $R2$ ,  $C1$ ,  $C4$  should be grouped closed together on PCB layout.
4. The  $V_{CC}$  output voltage level can be adjusted by  $R1$  and  $R2$ , the reference formula is:  
$$V_{CC} = 1.2 \times (R1 + R2) / R2$$
  
The value of  $(R1 + R2)$  should be between 500k to 1M Ohm.

**Table 3 - Passive component selection:**

Components	Typical Value	Remark
L1	Inductor, 10 $\mu$ H	1A
D1	Schottky diode	1A, 25V e.g. 1N5822, BAT54 [Philips Semiconductors]
Q1	MOSFET	N-FET with low $R_{DS(on)}$ and low $V_{th}$ voltage. e.g. MGSF1N02LT1 [ON SEMI]
R1, R2	Resistor	1%, 1/10W
R3	Resistor, 1.2 $\Omega$	1%, 1/2W
C1	Capacitor, 1 $\mu$ F	16V
C2	Capacitor, 6.8 $\mu$ F	Low ESR, 25V
C3	Capacitor, 1 $\mu$ F	16V
C4	Capacitor, 10nF	16V
C5	Capacitor, 1 ~ 10 $\mu$ F	16V
C6	Capacitor, 0.1 ~ 1 $\mu$ F	16V
C7	Capacitor, 15nF	16V

## 8 COMMAND TABLE

**Table 4 - Command table**

(D/C =0, R/W(WR#)=0, E(RD#)=1)

Note: commands marked with "\*\*\*" are compatible to SSD1301

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	00-0F	0	0	0	0	X <sub>3</sub>	X <sub>2</sub>	X <sub>1</sub>	X <sub>0</sub>	Set Lower Column Address **	Set the lower nibble of the column address register using X <sub>3</sub> X <sub>2</sub> X <sub>1</sub> X <sub>0</sub> as data bits. The initial display line register is reset to 0000b after POR.
0	10-1F	0	0	0	1	X <sub>3</sub>	X <sub>2</sub>	X <sub>1</sub>	X <sub>0</sub>	Set Higher Column Address **	Set the higher nibble of the column address register using X <sub>3</sub> X <sub>2</sub> X <sub>1</sub> X <sub>0</sub> as data bits. The initial display line register is reset to 0000b after POR.
0	2F	0	0	1	0	1	1	1	1	Activate horizontal scroll	Start horizontal scrolling
0	2E	0	0	1	0	1	1	1	0	Deactivate horizontal scroll	Stop horizontal scrolling
0 0 0 0 0	26 A[3:0] B[2:0] C[1:0] D[2:0]	0 * * * *	0 * * * *	1 * * * *	0 * * * *	0 A <sub>3</sub> * * *	1 A <sub>2</sub> * * *	1 A <sub>1</sub> B <sub>2</sub> * *	0 A <sub>0</sub> B <sub>1</sub> C <sub>1</sub> D <sub>2</sub>	Horizontal scroll setup	A[3:0] Set the number of column scroll per step Valid value: 0001b to 1000b B[2:0] Define start page address C[1:0] Set time interval between each scroll step in terms of frame frequency 00b – 12 frames 01b – 64 frames 10b – 128 frames 11b – 256 frames D[2:0] Define end page address Set the value of D[2:0] larger or equal to B[2:0]
0	40-6F	0	1	X <sub>5</sub>	0	X <sub>3</sub>	X <sub>2</sub>	X <sub>1</sub>	X <sub>0</sub>	Set Display Start Line	Set display RAM display start line register from 0-47 using X <sub>5</sub> X <sub>3</sub> X <sub>2</sub> X <sub>1</sub> X <sub>0</sub> .  Display start line register is reset to 000000 during POR.
0 0	81 A[7:0]	1 A <sub>7</sub>	0 A <sub>6</sub>	0 A <sub>5</sub>	0 A <sub>4</sub>	0 A <sub>3</sub>	0 A <sub>2</sub>	0 A <sub>1</sub>	1 A <sub>0</sub>	Set Contrast Control Register **	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (POR = 80h)
0 0 0 0 0	91 X[5:0] A[5:0] B[5:0] C[5:0]	1 * * * *	0 * * * *	0 X <sub>5</sub> A <sub>5</sub> * *	1 X <sub>4</sub> A <sub>4</sub> B <sub>5</sub> *	0 X <sub>3</sub> A <sub>3</sub> B <sub>4</sub> C <sub>5</sub>	0 X <sub>2</sub> A <sub>2</sub> B <sub>3</sub> C <sub>4</sub>	0 X <sub>1</sub> A <sub>1</sub> B <sub>2</sub> C <sub>3</sub>	1 X <sub>0</sub> A <sub>0</sub> B <sub>1</sub> C <sub>2</sub>	Set Look Up Table (LUT) for area colour	Set current drive pulse width of Bank 0, Colour A, B and C.  Bank 0: X[5:0] = 0... 47; for pulse width set to 1 ~ 64 clk  Colour A: A[5:0] same as above Colour B: B[5:0] same as above Colour C: C[5:0] same as above Note: colour D pulse width is fixed at 64 clks pulse.

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0 0 0 0	92 A[7:0] B[7:0] C[7:0] D[1:0]	1 A <sub>7</sub> B <sub>7</sub> C <sub>7</sub> *	0 A <sub>6</sub> B <sub>6</sub> C <sub>6</sub> *	0 A <sub>5</sub> B <sub>5</sub> C <sub>5</sub> *	1 A <sub>4</sub> B <sub>4</sub> C <sub>4</sub> *	0 A <sub>3</sub> B <sub>3</sub> C <sub>3</sub> *	0 A <sub>2</sub> B <sub>2</sub> C <sub>2</sub> *	1 A <sub>1</sub> B <sub>1</sub> C <sub>1</sub> *	0 A <sub>0</sub> B <sub>0</sub> C <sub>0</sub> D <sub>1</sub>	Set bank colour of for bank 1-13 (Page 0)	A[1:0] : 00, 01, 10, or 11 for Colour = A, B, C or D of bank 1 A[3:2] : 00, 01, 10, or 11 for Colour = A, B, C or D of bank 2 : : D[1:0]: 00, 01, 10, or 11 for Colour = A, B, C or D of bank 13
0 0 0 0 0	93 A[7:0] B[7:0] C[7:0] D[1:0]	1 A <sub>7</sub> B <sub>7</sub> C <sub>7</sub> *	0 A <sub>6</sub> B <sub>6</sub> C <sub>6</sub> *	0 A <sub>5</sub> B <sub>5</sub> C <sub>5</sub> *	1 A <sub>4</sub> B <sub>4</sub> C <sub>4</sub> *	0 A <sub>3</sub> B <sub>3</sub> C <sub>3</sub> *	0 A <sub>2</sub> B <sub>2</sub> C <sub>2</sub> *	1 A <sub>1</sub> B <sub>1</sub> C <sub>1</sub> *	1 A <sub>0</sub> B <sub>0</sub> C <sub>0</sub> D <sub>1</sub>	Set bank colour of for bank 14-26 (Page 1)	A[1:0] : 00, 01, 10, or 11 for Colour = A, B, C or D of bank 14 A[3:2] : 00, 01, 10, or 11 for Colour = A, B, C or D of bank 15 : : D[1:0]: 00, 01, 10, or 11 for Colour = A, B, C or D of bank 26
0	A0~ A1	1	0	1	0	0	0	0	X <sub>0</sub>	Set Segment Re-map **	X <sub>0</sub> =0:column address 0 is mapped to SEG0 (POR)  X <sub>0</sub> =1:column address 103 is mapped to SEG0
0	A4~A5	1	0	1	0	0	1	0	X <sub>0</sub>	Set Entire Display On/Off **	X <sub>0</sub> =0:normal display (POR) X <sub>0</sub> =1:entire display on
0	A6~A7	1	0	1	0	0	1	1	X <sub>0</sub>	Set Normal/Inverse Display **	X <sub>0</sub> =0:normal display (POR) X <sub>0</sub> =1:inverse display
0 0	A8 A[5:0]	1 *	0 *	1 A <sub>5</sub>	0 A <sub>4</sub>	1 A <sub>3</sub>	0 A <sub>2</sub>	0 A <sub>1</sub>	0 A <sub>0</sub>	Set Multiplex Ratio **	The next command, A[5:0] determines multiplex ratio N from 16MUX-48MUX, POR= 48MUX
0	AA	1	0	1	0	1	0	1	0	NOP	Reserved, do not use
0	AB	1	0	1	0	1	0	1	1	NOP	Reserved, do not use
0 0	AD A[2:0]	1 1	0 0	1 0	0 0	1 1	1 0	0 X <sub>1</sub>	1 X <sub>0</sub>	Set DC-DC on/off	X <sub>0</sub> : 1 DC-DC will be turned on when display on (POR) 0 DC-DC is disable X <sub>1</sub> =0, Select external VCOMH voltage supply at Display ON X <sub>1</sub> =1, Select internal VCOMH regulator at Display ON (POR)
0	AE~AF	1	0	1	0	1	1	1	X <sub>0</sub>	Set Display On/Off **	X <sub>0</sub> =0:turns off OLED panel (POR) X <sub>0</sub> =1:turns on OLED panel
0	B0~BF	1	0	1	1	X <sub>3</sub>	X <sub>2</sub>	X <sub>1</sub>	X <sub>0</sub>	Set Page Address **	Set GDDRAM Page Address (0~5) for read/write using X <sub>3</sub> X <sub>2</sub> X <sub>1</sub> X <sub>0</sub>
0	C0/C8	1	1	0	0	X <sub>3</sub>	*	*	*	Set COM Output Scan Direction **	X <sub>3</sub> =0:normal mode (POR) Scan from COM 0 to COM [N-1]  X <sub>3</sub> =1:remapped mode. Scan from COM [N-1] to COM0 Where N is the Multiplex ratio.

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	D0-D1	1	1	0	1	0	0	0	X <sub>0</sub>	Reserved	Reserved, do not use
0 0	D3 A[5:0]	1 *	1 *	0 A <sub>5</sub>	1 A <sub>4</sub>	0 A <sub>3</sub>	0 A <sub>2</sub>	1 A <sub>1</sub>	1 A <sub>0</sub>	Set Display Offset **	Set vertical scroll by COM from 0-47. The value is reset to 00H after POR.
0	D5 A[3:0] A[7:4]	1 * A <sub>7</sub>	1 * A <sub>6</sub>	0 * A <sub>5</sub>	1 * A <sub>4</sub>	0 A <sub>3</sub> *	1 A <sub>2</sub> *	0 A <sub>1</sub> *	1 A <sub>0</sub> *	Set Display Clock Divide Ratio/Oscillator Frequency	The lower nibble of the next command sets the divide ratio of the display clocks (dclk). The ratio is the value of A[3:0] +1  Divide ratio= 1-16, POR value is 0000b (divide by 1). The higher nibble of the next command sets the Oscillator  Frequency. Oscillator Frequency increases with the value of A[7:4] and vice versa.
0 0	D8	1 0	1 0	0 X <sub>5</sub>	1 X <sub>4</sub>	1 0	0 X <sub>2</sub>	0 0	0 X <sub>0</sub>	Set area colour mode on/off & low power display mode	X <sub>5</sub> X <sub>4</sub> = 00 (POR) : mono mode X <sub>5</sub> X <sub>4</sub> = 11" Area Colour enable X <sub>2</sub> =0 and X <sub>0</sub> =0: Normal (POR) power mode X <sub>2</sub> =1 and X <sub>0</sub> =1: Set low power save mode
0 0	D9 A[7:0]	1 A <sub>7</sub>	1 A <sub>6</sub>	0 A <sub>5</sub>	1 A <sub>4</sub>	1 A <sub>3</sub>	0 A <sub>2</sub>	0 A <sub>1</sub>	1 A <sub>0</sub>	Set Pre-charge period	A[3:0] Phase 1 period of up to 15 dclk clocks [POR=2h]  A[7:4] Phase 2 period of up to 15 dclk clocks [POR=2h]
0 0	DA 02/22	1 0	1 0	0 0	1 X <sub>4</sub>	1 0	0 0	1 1	0 0	Set COM pins hardware configuration	X <sub>4</sub> =0, Sequential COM pin configuration (i.e. COM23, 22, ...,2, 0 ; SEG0-103; COM24,25....46,47)  X <sub>4</sub> =1(POR), Alternative COM pin configuration (i.e. COM46,44,...,2, 0; SEG0 -103; COM1,3,5....,45,47)
0 0	DB A[6:0]	1 *	1 A <sub>6</sub>	0 A <sub>5</sub>	1 A <sub>4</sub>	1 A <sub>3</sub>	0 A <sub>2</sub>	1 A <sub>1</sub>	1 A <sub>0</sub>	Set VCOMH	A[6:0] 0000000 0.43*Vref 0111111 0.83*Vref (POR) 1111111 1.0*Vref
0	E2	1	1	1	0	0	0	1	0	Reserved	Reserved
0	E3	1	1	1	0	0	0	1	1	NOP **	Command for No Operation

Note: Remark "\*\*\*" stands for "Don't Care"

**Table 5 - Read command table**

(D/C=0, R/W(WR#)=1, E(RD#)=1 for 6800 or E(RD#)=0 for 8080)

Bit Pattern	Command	Description
D <sub>7</sub> D <sub>6</sub> D <sub>5</sub> D <sub>4</sub> D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub>	Status Register Read *	D <sub>7</sub> : "1" for Command lock D <sub>6</sub> : "1" for display OFF / "0" for display ON D <sub>5</sub> : Reserve D <sub>4</sub> : Reserve D <sub>3</sub> : Reserve D <sub>2</sub> : Reserve D <sub>1</sub> : Reserve D <sub>0</sub> : Reserve

Note: Patterns other than that given in Command Table are prohibited to enter to the chip as a command; otherwise, unexpected result will occur.

### Data Read / Write

To read data from the GDDRAM, input High to R/W(WR#) pin and D/C# pin for 6800-series parallel mode, Low to E(RD#) pin and High to D/C pin for 8080-series parallel mode. No data read is provided for serial mode.

In normal data read mode, GDDRAM column address pointer will be increased by one automatically after each data read. However, no automatic increase will be performed in read-modify-write mode. Also, a dummy read is required before the first data read. See Figure 5 in Functional Block Description.

To write data to the GDDRAM, input Low to R/W#(WR#) pin and High to D/C# pin for 6800-series parallel mode AND 8080-series parallel mode. For serial interface mode, it is always in write mode. GDDRAM column address pointer will be increased by one automatically after each data write.

**Table 6 - Address increment table (Automatic)**

D/C#	R/W(WR#)	Comment	Address Increment
0	0	Write Command	No
0	1	Read Status	No
1	0	Write Data	Yes
1	1	Read Data	Yes*1

\*1. If read-data command is issued in read-modify-write mode, address increase is not applied.

## 9 COMMAND DESCRIPTIONS

### Set Lower Column Address

This command specifies the lower nibble of the 8-bit column address of the display data RAM. The column address will be incremented by each data access after it is pre-set by the MCU.

### Set Higher Column Address

This command specifies the higher nibble of the 8-bit column address of the display data RAM. The column address will be incremented by each data access after it is pre-set by the MCU.

### Activate Horizontal Scroll

Start motion of horizontal scrolling. This command should only be issued after Horizontal scroll setup parameters are defined.

The following actions are prohibited after the horizontal scroll is activated

1. RAM access (Data write or read)
2. Changing horizontal scroll setup parameters

The SSD1300 horizontal scroll is designed for 96 columns scrolling only. The 8 remaining columns are reserved for computation during scrolling and should be left open.

**Figure 8 - Horizontal scroll direction**

Remap Setting	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	...	...	SEG92	SEG93	SEG94	SEG95	SEG96	SEG97	SEG98	SEG99	SEG100	SEG101	SEG102	SEG103
A0	A	B	C	D	E	F	G	H	I	J	K	L	→	→	W	X	Y	Z	Invalid data							
A1	Invalid data								Z	Y	X	W	←	←	L	K	J	I	H	G	F	E	D	C	B	A

Scroll direction

### Deactivate Horizontal Scroll

Stop motion of horizontal scrolling.

### Horizontal Scroll Setup

This command consists of 5 consecutive bytes to set up the horizontal scroll parameters. It determines scroll direction, scrolling start page, end page and scrolling speed.

Before issuing this command, the horizontal scroll must be deactivated (2Fh). Otherwise, ram content may be corrupted.

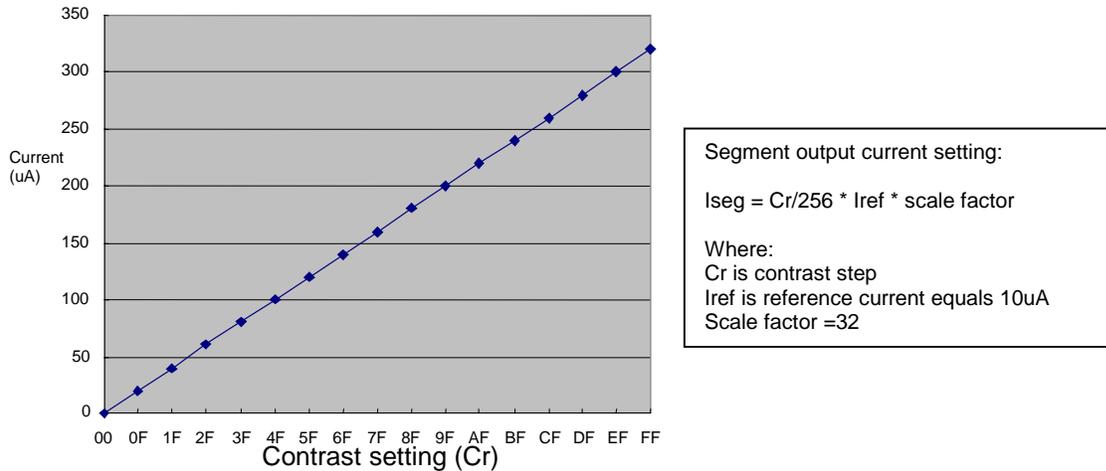
### Set Display Start Line

This command is to set Display Start Line register to determine starting address of display RAM to be displayed by selecting a value from 0 to 47. With value equals to 0, D<sub>0</sub> of Page 0 is mapped to COM0. With value equals to 1, D<sub>1</sub> of Page0 is mapped to COM0. The display start line values of 0 to 47 are assigned to Page 0 to 7.

### Set Contrast Control Register

This command is to set Contrast Setting of the display. The chip has 256 contrast steps from 00 to FF. The segment output current increases as the contrast step value increases. See Figure 6 below.

Figure 9 - Segment current vs Contrast setting  
Segment current vs Contrast setting



### Set Look Up Table (LUT) for area colour

SSD1300 provides 4 colour (pulse width) settings - Colour A, B, C and D. The colour intensity (or grey scale) is defined by the current drive pulse width. The pulse width of colour A, B, C can be programmable from 1 to 64 DCLK\* duration. The colour D is fixed at 64 DCLK pulse width. This colour setting has to be stored in the Look Up Table (LUT).

For the background colour, the colour intensity is defined by a variable X[5:0].

Set LUT command:     10010001  
                           X[5:0]  
                           A[5:0]  
                           B[5:0]  
                           C[5:0]

	Description	Number of DCLKs
Bank 0	Set background colour	X[5:0]
Colour A	Set Pulse Width A	A[5:0]
Colour B	Set Pulse Width B	B[5:0]
Colour C	Set Pulse Width C	C[5:0]
Colour D	Pulse width D is fixed to 64 DCLK	64 (fixed)

DCLK: Internal Display Clock

Set bank colour of bank 1-13 (Page 0) and bank colour of bank 14-26 (Page 1)

Next step is to define the colour of each display area. The 104x48 display matrix is divided into 8 pages of 8 commons per pages. The first two pages, page 0 and page 1, are divided into 32 banks: Each bank comprise of a display area of 8x8 pixels. Each bank can be programmable to any 1 of the 4 colour (A, B, C, D). User can use 92h and 93h command for the bank colour setting. Note: Only applicable in colour mode.

#### **Set Segment Re-map**

This command changes the mapping between the display data column address and segment driver. It allows flexibility in OLED module design. Refer to Command Table.

#### **Set Entire Display On/Off**

This command forces the entire display to be "ON" regardless of the contents of the display data RAM. This command has priority over normal/reverse display. This command will be used with "Set Display ON/OFF" command to form a compound command for entering power save mode.

#### **Set Normal/Inverse Display**

This command sets the display to be either normal/inverse. In normal display, a RAM data of 1 indicates an "ON" pixel while in inverse display; a RAM data of 0 indicates an "ON" pixel.

#### **Set Multiplex Ratio**

This command switches default 47 multiplex mode to any multiplex ratio from 2 to 47. The output pads COM0-COM47 will be switched to corresponding COM signal.

#### **Set Display On/Off**

This command turns the display on or off. When the display is off, the segment and common output are in high impedance state.

#### **Set Page Address**

This command positions the page address from 0 to 5 in GDDRAM. Refer to Command Table.

#### **Set COM Output Scan Direction**

This command sets the scan direction of the COM output allowing layout flexibility in OLED module design. In addition, the display will have immediate effect once this command is issued. That is, if this command is sent during normal display, the graphic display will be vertically flipped.

## Set Display Offset

This is a double byte command. The next command specifies the mapping of display start line (it is assumed that COM0 is the display start line, display start line register equals to 0) to one of COM0-47.

For example, to move the COM16 towards the COM0 direction for 16 lines, the 6-bit data in the second byte should be given by 010000. To move in the opposite direction by 16 lines, the 6-bit data should be given by (48 – 16) and so the second byte should be 100000.

Hardware pin name	Output												Set MUX ratio(A8) COM Normal / Remapped (C0 / C8) Display offset (D3) Display start line (40 - 7F)	
	48		48		48		40		40		40			32
	Remap		Remap		Remap		Remap		Remap		Remap			Remap
	0	8	8	8	0	0	8	8	0	0	8	8		16
COM0	Row47	Ram47	Row7	Ram7	Row47	Ram7	-	-	Row7	Ram7	-	-	Row7	Ram23
COM1	Row46	Ram46	Row6	Ram6	Row46	Ram6	-	-	Row6	Ram6	-	-	Row6	Ram22
COM2	Row45	Ram45	Row5	Ram5	Row45	Ram5	-	-	Row5	Ram5	-	-	Row5	Ram21
COM3	Row44	Ram44	Row4	Ram4	Row44	Ram4	-	-	Row4	Ram4	-	-	Row4	Ram20
COM4	Row43	Ram43	Row3	Ram3	Row43	Ram3	-	-	Row3	Ram3	-	-	Row3	Ram19
COM5	Row42	Ram42	Row2	Ram2	Row42	Ram2	-	-	Row2	Ram2	-	-	Row2	Ram18
COM6	Row41	Ram41	Row1	Ram1	Row41	Ram1	-	-	Row1	Ram1	-	-	Row1	Ram17
COM7	Row40	Ram40	Row0	Ram0	Row40	Ram0	-	-	Row0	Ram0	-	-	Row0	Ram16
COM8	Row39	Ram39	Row47	Ram47	Row39	Ram47	Row39	RAM39	-	-	Row39	RAM47	-	-
COM9	Row38	Ram38	Row46	Ram46	Row38	Ram46	Row38	RAM38	-	-	Row38	RAM46	-	-
COM10	Row37	Ram37	Row45	Ram45	Row37	Ram45	Row37	RAM37	-	-	Row37	RAM45	-	-
COM11	Row36	Ram36	Row44	Ram44	Row36	Ram44	Row36	RAM36	-	-	Row36	RAM44	-	-
COM12	Row35	Ram35	Row43	Ram43	Row35	Ram43	Row35	RAM35	-	-	Row35	RAM43	-	-
COM13	Row34	Ram34	Row42	Ram42	Row34	Ram42	Row34	RAM34	-	-	Row34	RAM42	-	-
COM14	Row33	Ram33	Row41	Ram41	Row33	Ram41	Row33	RAM33	-	-	Row33	RAM41	-	-
COM15	Row32	Ram32	Row40	Ram40	Row32	Ram40	Row32	RAM32	-	-	Row32	RAM40	-	-
COM16	Row31	Ram31	Row39	Ram39	Row31	Ram39	Row31	RAM31	Row39	RAM39	Row31	RAM39	-	-
COM17	Row30	Ram30	Row38	Ram38	Row30	Ram38	Row30	RAM30	Row38	RAM38	Row30	RAM38	-	-
COM18	Row29	Ram29	Row37	Ram37	Row29	Ram37	Row29	RAM29	Row37	RAM37	Row29	RAM37	-	-
COM19	Row28	Ram28	Row36	Ram36	Row28	Ram36	Row28	RAM28	Row36	RAM36	Row28	RAM36	-	-
COM20	Row27	Ram27	Row35	Ram35	Row27	Ram35	Row27	RAM27	Row35	RAM35	Row27	RAM35	-	-
COM21	Row26	Ram26	Row34	Ram34	Row26	Ram34	Row26	RAM26	Row34	RAM34	Row26	RAM34	-	-
COM22	Row25	Ram25	Row33	Ram33	Row25	Ram33	Row25	RAM25	Row33	RAM33	Row25	RAM33	-	-
COM23	Row24	Ram24	Row32	Ram32	Row24	Ram32	Row24	RAM24	Row32	RAM32	Row24	RAM32	-	-
COM24	Row23	Ram23	Row31	Ram31	Row23	Ram31	Row23	RAM23	Row31	RAM31	Row23	RAM31	Row31	RAM47
COM25	Row22	Ram22	Row30	Ram30	Row22	Ram30	Row22	RAM22	Row30	RAM30	Row22	RAM30	Row30	RAM46
COM26	Row21	Ram21	Row29	Ram29	Row21	Ram29	Row21	RAM21	Row29	RAM29	Row21	RAM29	Row29	RAM45
COM27	Row20	Ram20	Row28	Ram28	Row20	Ram28	Row20	RAM20	Row28	RAM28	Row20	RAM28	Row28	RAM44
COM28	Row19	Ram19	Row27	Ram27	Row19	Ram27	Row19	RAM19	Row27	RAM27	Row19	RAM27	Row27	RAM43
COM29	Row18	Ram18	Row26	Ram26	Row18	Ram26	Row18	RAM18	Row26	RAM26	Row18	RAM26	Row26	RAM42
COM30	Row17	Ram17	Row25	Ram25	Row17	Ram25	Row17	RAM17	Row25	RAM25	Row17	RAM25	Row25	RAM41
COM31	Row16	Ram16	Row24	Ram24	Row16	Ram24	Row16	RAM16	Row24	RAM24	Row16	RAM24	Row24	RAM40
COM32	Row15	Ram15	Row23	Ram23	Row15	Ram23	Row15	RAM15	Row23	RAM23	Row15	RAM23	Row23	RAM39
COM33	Row14	Ram14	Row22	Ram22	Row14	Ram22	Row14	RAM14	Row22	RAM22	Row14	RAM22	Row22	RAM38
COM34	Row13	Ram13	Row21	Ram21	Row13	Ram21	Row13	RAM13	Row21	RAM21	Row13	RAM21	Row21	RAM37
COM35	Row12	Ram12	Row20	Ram20	Row12	Ram20	Row12	RAM12	Row20	RAM20	Row12	RAM20	Row20	RAM36
COM36	Row11	Ram11	Row19	Ram19	Row11	Ram19	Row11	RAM11	Row19	RAM19	Row11	RAM19	Row19	RAM35
COM37	Row10	Ram10	Row18	Ram18	Row10	Ram18	Row10	RAM10	Row18	RAM18	Row10	RAM18	Row18	RAM34
COM38	Row9	Ram9	Row17	Ram17	Row9	Ram17	Row9	RAM9	Row17	RAM17	Row9	RAM17	Row17	RAM33
COM39	Row8	Ram8	Row16	Ram16	Row8	Ram16	Row8	RAM8	Row16	RAM16	Row8	RAM16	Row16	RAM32
COM40	Row7	Ram7	Row15	Ram15	Row7	Ram15	Row7	RAM7	Row15	RAM15	Row7	RAM15	Row15	RAM31
COM41	Row6	Ram6	Row14	Ram14	Row6	Ram14	Row6	RAM6	Row14	RAM14	Row6	RAM14	Row14	RAM30
COM42	Row5	Ram5	Row13	Ram13	Row5	Ram13	Row5	RAM5	Row13	RAM13	Row5	RAM13	Row13	RAM29
COM43	Row4	Ram4	Row12	Ram12	Row4	Ram12	Row4	RAM4	Row12	RAM12	Row4	RAM12	Row12	RAM28
COM44	Row3	Ram3	Row11	Ram11	Row3	Ram11	Row3	RAM3	Row11	RAM11	Row3	RAM11	Row11	RAM27
COM45	Row2	Ram2	Row10	Ram10	Row2	Ram10	Row2	RAM2	Row10	RAM10	Row2	RAM10	Row10	RAM26
COM46	Row1	Ram1	Row9	Ram9	Row1	Ram9	Row1	RAM1	Row9	RAM9	Row1	RAM9	Row9	RAM25
COM47	Row0	Ram0	Row8	Ram8	Row0	Ram8	Row0	RAM0	Row8	RAM8	Row0	RAM8	Row8	RAM24

Hardware pin name	Output												Set MUX ratio(A8) COM Normal / Remapped (C0 / C8) Display offset (D3) Display start line (40 - 7F)
	48		48		48		40		40		40		
	Normal		Normal		Normal		Normal		Normal		Normal		
	0		8		8		0		8		8		
COM0	Row0	RAM0	Row8	RAM8	Row0	RAM8	Row0	RAM0	Row8	RAM8	Row0	RAM8	
COM1	Row1	RAM1	Row9	RAM9	Row1	RAM9	Row1	RAM1	Row9	RAM9	Row1	RAM9	
COM2	Row2	RAM2	Row10	RAM10	Row2	RAM10	Row2	RAM2	Row10	RAM10	Row2	RAM10	
COM3	Row3	RAM3	Row11	RAM11	Row3	RAM11	Row3	RAM3	Row11	RAM11	Row3	RAM11	
COM4	Row4	RAM4	Row12	RAM12	Row4	RAM12	Row4	RAM4	Row12	RAM12	Row4	RAM12	
COM5	Row5	RAM5	Row13	RAM13	Row5	RAM13	Row5	RAM5	Row13	RAM13	Row5	RAM13	
COM6	Row6	RAM6	Row14	RAM14	Row6	RAM14	Row6	RAM6	Row14	RAM14	Row6	RAM14	
COM7	Row7	RAM7	Row15	RAM15	Row7	RAM15	Row7	RAM7	Row15	RAM15	Row7	RAM15	
COM8	Row8	RAM8	Row16	RAM16	Row8	RAM16	Row8	RAM8	Row16	RAM16	Row8	RAM16	
COM9	Row9	RAM9	Row17	RAM17	Row9	RAM17	Row9	RAM9	Row17	RAM17	Row9	RAM17	
COM10	Row10	RAM10	Row18	RAM18	Row10	RAM18	Row10	RAM10	Row18	RAM18	Row10	RAM18	
COM11	Row11	RAM11	Row19	RAM19	Row11	RAM19	Row11	RAM11	Row19	RAM19	Row11	RAM19	
COM12	Row12	RAM12	Row20	RAM20	Row12	RAM20	Row12	RAM12	Row20	RAM20	Row12	RAM20	
COM13	Row13	RAM13	Row21	RAM21	Row13	RAM21	Row13	RAM13	Row21	RAM21	Row13	RAM21	
COM14	Row14	RAM14	Row22	RAM22	Row14	RAM22	Row14	RAM14	Row22	RAM22	Row14	RAM22	
COM15	Row15	RAM15	Row23	RAM23	Row15	RAM23	Row15	RAM15	Row23	RAM23	Row15	RAM23	
COM16	Row16	RAM16	Row24	RAM24	Row16	RAM24	Row16	RAM16	Row24	RAM24	Row16	RAM24	
COM17	Row17	RAM17	Row25	RAM25	Row17	RAM25	Row17	RAM17	Row25	RAM25	Row17	RAM25	
COM18	Row18	RAM18	Row26	RAM26	Row18	RAM26	Row18	RAM18	Row26	RAM26	Row18	RAM26	
COM19	Row19	RAM19	Row27	RAM27	Row19	RAM27	Row19	RAM19	Row27	RAM27	Row19	RAM27	
COM20	Row20	RAM20	Row28	RAM28	Row20	RAM28	Row20	RAM20	Row28	RAM28	Row20	RAM28	
COM21	Row21	RAM21	Row29	RAM29	Row21	RAM29	Row21	RAM21	Row29	RAM29	Row21	RAM29	
COM22	Row22	RAM22	Row30	RAM30	Row22	RAM30	Row22	RAM22	Row30	RAM30	Row22	RAM30	
COM23	Row23	RAM23	Row31	RAM31	Row23	RAM31	Row23	RAM23	Row31	RAM31	Row23	RAM31	
COM24	Row24	RAM24	Row32	RAM32	Row24	RAM32	Row24	RAM24	Row32	RAM32	Row24	RAM32	
COM25	Row25	RAM25	Row33	RAM33	Row25	RAM33	Row25	RAM25	Row33	RAM33	Row25	RAM33	
COM26	Row26	RAM26	Row34	RAM34	Row26	RAM34	Row26	RAM26	Row34	RAM34	Row26	RAM34	
COM27	Row27	RAM27	Row35	RAM35	Row27	RAM35	Row27	RAM27	Row35	RAM35	Row27	RAM35	
COM28	Row28	RAM28	Row36	RAM36	Row28	RAM36	Row28	RAM28	Row36	RAM36	Row28	RAM36	
COM29	Row29	RAM29	Row37	RAM37	Row29	RAM37	Row29	RAM29	Row37	RAM37	Row29	RAM37	
COM30	Row30	RAM30	Row38	RAM38	Row30	RAM38	Row30	RAM30	Row38	RAM38	Row30	RAM38	
COM31	Row31	RAM31	Row39	RAM39	Row31	RAM39	Row31	RAM31	Row39	RAM39	Row31	RAM39	
COM32	Row32	RAM32	Row40	RAM40	Row32	RAM40	Row32	RAM32	-	-	Row32	RAM40	
COM33	Row33	RAM33	Row41	RAM41	Row33	RAM41	Row33	RAM33	-	-	Row33	RAM41	
COM34	Row34	RAM34	Row42	RAM42	Row34	RAM42	Row34	RAM34	-	-	Row34	RAM42	
COM35	Row35	RAM35	Row43	RAM43	Row35	RAM43	Row35	RAM35	-	-	Row35	RAM43	
COM36	Row36	RAM36	Row44	RAM44	Row36	RAM44	Row36	RAM36	-	-	Row36	RAM44	
COM37	Row37	RAM37	Row45	RAM45	Row37	RAM45	Row37	RAM37	-	-	Row37	RAM45	
COM38	Row38	RAM38	Row46	RAM46	Row38	RAM46	Row38	RAM38	-	-	Row38	RAM46	
COM39	Row39	RAM39	Row47	RAM47	Row39	RAM47	Row39	RAM39	-	-	Row39	RAM47	
COM40	Row40	RAM40	Row0	RAM0	Row40	RAM48	-	-	Row0	RAM0	-	-	
COM41	Row41	RAM41	Row1	RAM1	Row41	RAM49	-	-	Row1	RAM1	-	-	
COM42	Row42	RAM42	Row2	RAM2	Row42	RAM50	-	-	Row2	RAM2	-	-	
COM43	Row43	RAM43	Row3	RAM3	Row43	RAM51	-	-	Row3	RAM3	-	-	
COM44	Row44	RAM44	Row4	RAM4	Row44	RAM52	-	-	Row4	RAM4	-	-	
COM45	Row45	RAM45	Row5	RAM5	Row45	RAM53	-	-	Row5	RAM5	-	-	
COM46	Row46	RAM46	Row6	RAM6	Row46	RAM54	-	-	Row6	RAM6	-	-	
COM47	Row47	RAM47	Row7	RAM7	Row47	RAM55	-	-	Row7	RAM7	-	-	

### Set Display Clock Divide Ratio/ Oscillator Frequency

This command is used to set the frequency of the internal display clocks, DCLKs. It is defined as the divide ratio (Value from 1 to 16) used to divide the oscillator frequency. POR is 0000b which means the divide ratio is 1. Frame frequency is determined by divide ratio, number of display clocks per row, MUX ratio and oscillator frequency.

### Set Area Colour Mode on/off

This command is used to enable area colour mode. POR is mono mode.

### Set Low Power Display Mode

This is a double byte command. This command is set to reduce power consumption during IC operation.

### Set Pre-charge period

This command is used to set the duration of the pre-charge period. The interval is counted in number of DCLK. POR is 2 DCLK.

### Set COM pins hardware configuration

This command is to set the COM signals pin configuration (sequential or alternative) to match the OLED panel hardware layout

Alternative COM pin configuration (POR):

COM46, 44, 42...0	SEG0, 1, 2... 103	COM1, 3, 5...47
-------------------	-------------------	-----------------

Sequential COM pin configuration:

COM23, 22, 21...0	SEG0, 1, 2... 103	COM24, 25, 26...47
-------------------	-------------------	--------------------

### NOP

No Operation Command

### Status register Read

This command is issued by setting D/C# Low during a data read (refer to Figure 8 and Figure 9 parallel interface waveform). It allows the MCU to monitor the internal status of the chip. No status read is provided for serial mode.

### Set DC-DC on/off

This command is to control the DC-DC voltage converter. The converter will be turned on by issuing this command then DISPLAY ON command. The panel display must be off while issuing this command. POR the DC-DC will be turned on.

### Set $V_{COMH}$ Voltage

This command sets the high voltage level of common pins,  $V_{COMH}$ , when it is selected to generate internally by command ADh. The level of  $V_{COMH}$  is programmed with reference to  $V_{REF}$ .

## 10 MAXIMUM RATINGS

**Table 7 - Maximum Ratings**

(Voltage Reference to  $V_{SS}$ )

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply Voltage	-0.3 to +4.0	V
$V_{CC}$		0.0 to 18.0	V
$V_{REF}$		0.0 to 18.0	V
$V_{COMH}$	Supply Voltage/Output voltage	0.0 to 18.0	V
-	SEG/COM output voltage	0.0 to 18.0	V
$V_{in}$	Input voltage	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
$T_A$	Operating Temperature	-30 to +85	°C
$T_{stg}$	Storage Temperature Range	-65 to +150	°C

Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description.

## 11 DC CHARACTERISTICS

**Table 8 - DC Characteristics**

(Unless otherwise specified, Voltage Referenced to  $V_{SS}$ ,  $V_{DD} = 2.4$  to  $3.5V$ ,  $T_A = 25^\circ C$ )

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
$V_{CC}$	Operating Voltage	-	7	12	16	V
$V_{DD}$	Logic Supply Voltage	-	2.4	-	3.5	V
$V_{DD}$	Logic Supply Voltage (internal DC/DC enable)	-	3.0	-	3.5	V
$V_{OH}$	High Logic Output Level	$I_{OUT} = 100\mu A, 3.3MHz$	$0.9 \cdot V_{DD}$	-	$V_{DD}$	V
$V_{OL}$	Low Logic Output Level	$I_{OUT} = 100\mu A, 3.3MHz$	0	-	$0.1 \cdot V_{DD}$	V
$V_{IH}$	High Logic Input Level	$I_{OUT} = 100\mu A, 3.3MHz$	$0.8 \cdot V_{DD}$	-	$V_{DD}$	V
$V_{IL}$	Low Logic Input Level	$I_{OUT} = 100\mu A, 3.3MHz$	0	-	$0.2 \cdot V_{DD}$	V
$I_{CC, SLEEP}$	Sleep mode Current	$V_{DD}=2.7V$ , display OFF, No panel attached	-15	-	+15	$\mu A$
$I_{DD, SLEEP}$	Sleep mode Current	$V_{DD}=2.7V$ , display OFF, No panel attached	-15	-	+15	$\mu A$
$I_{CC}$	$V_{CC}$ Supply Current	Contrast = FF	-	550	-	$\mu A$
$I_{DD}$	$V_{DD}$ Supply Current	Contrast = FF	-	190	-	$\mu A$
$I_{SEG}$	Segment Output Current  $V_{DD}=2.7V$ , $V_{CC}=12V$ , $I_{REF}=10\mu A$ , Display on, Segment pin under test is connected with a 20K resistive load to VSS	Contrast=FF	285	320	355	$\mu A$
		Contrast=AF	-	220	-	
		Contrast=5F	-	120	-	
		Contrast=0F	-	20	-	
Dev	Segment output current uniformity	$Dev = (I_{SEG} - I_{MID})/I_{MID}$ $I_{MID} = (I_{MAX} + I_{MIN})/2$ $I_{SEG}[0:103] =$ Segment current at contrast = FF	-	-	$\pm 3$	%
Adj. Dev	Adjacent pin output current uniformity (contrast = FF)	$Adj\ Dev = (I[n]-I[n+1]) / (I[n]+I[n+1])$	-	$\pm 2.0$	--	%
$V_{CC}$	DC-DC converter output voltage	$V_{DD}$ input=3V, L=10 $\mu H$ ; R1=450Kohm; R2=50Kohm; Icc = 20mA (loading)	11.0	12.0	13.0	V
		-	7	-	16	
Pwr	DC-DC Converter output power	$V_{DD}$ input=3V, L=10 $\mu H$ ; $V_{CC} = 12V$	-	-	400	mW

## 12 AC CHARACTERISTICS

**Table 9 - AC Characteristics**

(Unless otherwise specified, Voltage Referenced to  $V_{SS}$ ,  $V_{DD} = 2.4$  to  $3.5V$ ,  $T_A = 25^\circ C$ .)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
$F_{OSC}$	Oscillation Frequency of Display Timing Generator	$V_{DD} = 2.7V$	260	280	310	kHz
$F_{FRM}$	Frame Frequency for 48 MUX Mode	104x48 Graphic Display Mode, Display ON, Internal Oscillator Enabled	-	$F_{OSC} \times 1/(D \times K \times 48)$	-	Hz

D: divide ratio (default value = 1)

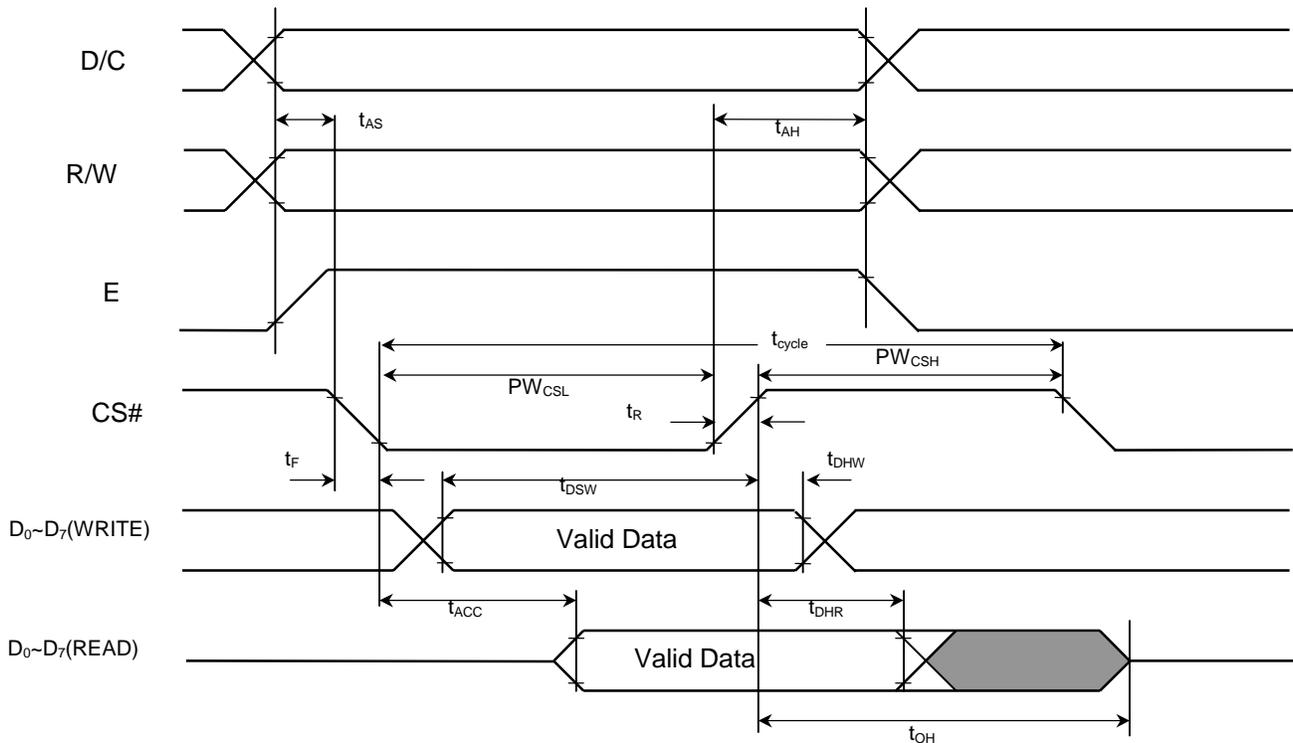
K: number of display clocks (default value = 54)

Refer to command table for detail description

**Table 10 - 6800-Series MPU Parallel Interface Timing Characteristics**

( $V_{DD} - V_{SS} = 2.4$  to  $3.5V$ ,  $T_A = 25^\circ C$ )

Symbol	Parameter	Min	Typ	Max	Unit
$t_{cycle}$	Clock Cycle Time	300	-	-	ns
$t_{AS}$	Address Setup Time	0	-	-	ns
$t_{AH}$	Address Hold Time	0	-	-	ns
$t_{DSW}$	Write Data Setup Time	40	-	-	ns
$t_{DHW}$	Write Data Hold Time	7	-	-	ns
$t_{DHR}$	Read Data Hold Time	20	-	-	ns
$t_{OH}$	Output Disable Time	-	-	70	ns
$t_{ACC}$	Access Time	-	-	140	ns
$PW_{CSL}$	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
$PW_{CSH}$	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
$t_R$	Rise Time	-	-	15	ns
$t_F$	Fall Time	-	-	15	ns

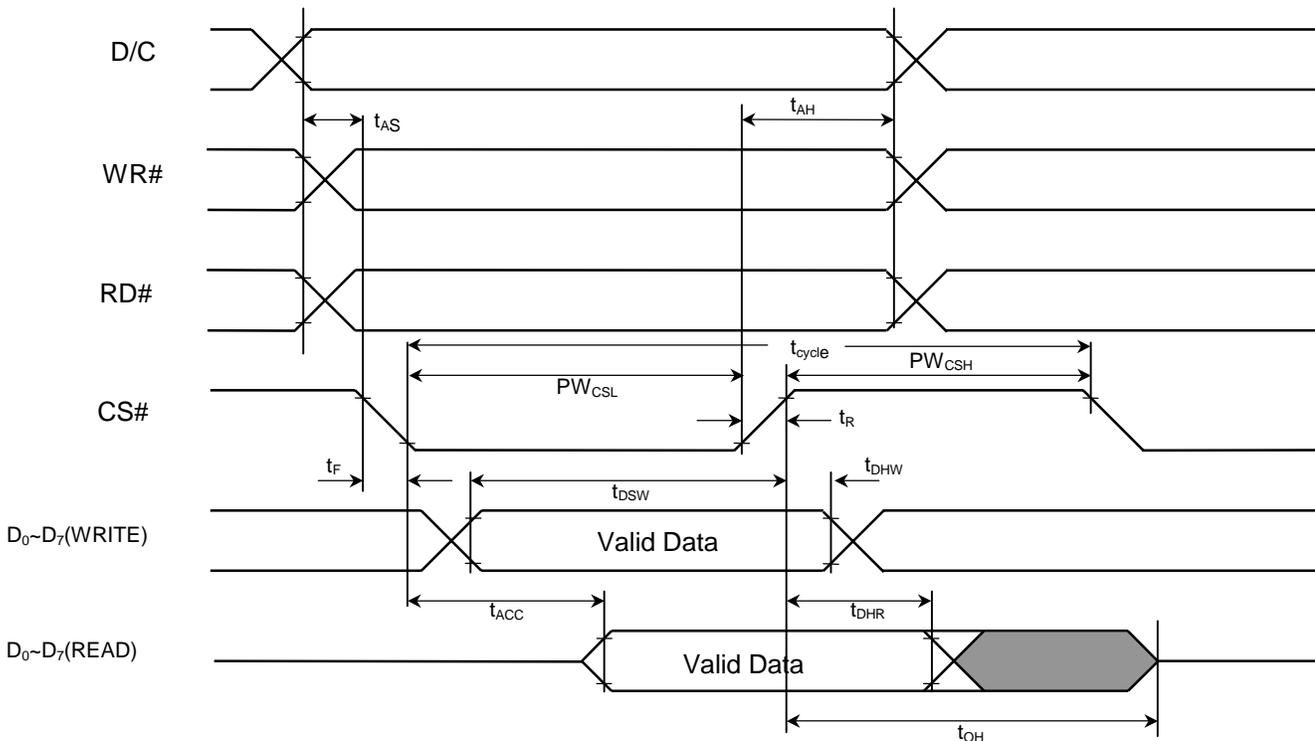


**Figure 10 - 6800-series MPU parallel interface characteristics**

**Table 11 - 8080-Series MPU Parallel Interface Timing Characteristics**

( $V_{DD} - V_{SS} = 2.4$  to  $3.5V$ ,  $T_A = 25^\circ C$ )

Symbol	Parameter	Min	Typ	Max	Unit
$t_{cycle}$	Clock Cycle Time	300	-	-	ns
$t_{AS}$	Address Setup Time	0	-	-	ns
$t_{AH}$	Address Hold Time	0	-	-	ns
$t_{DSW}$	Write Data Setup Time	40	-	-	ns
$t_{DHW}$	Write Data Hold Time	7	-	-	ns
$t_{DHR}$	Read Data Hold Time	20	-	-	ns
$t_{OH}$	Output Disable Time	-	-	70	ns
$t_{ACC}$	Access Time	-	-	140	ns
$PW_{CSL}$	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
$PW_{CSH}$	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
$t_R$	Rise Time	-	-	15	ns
$t_F$	Fall Time	-	-	15	ns

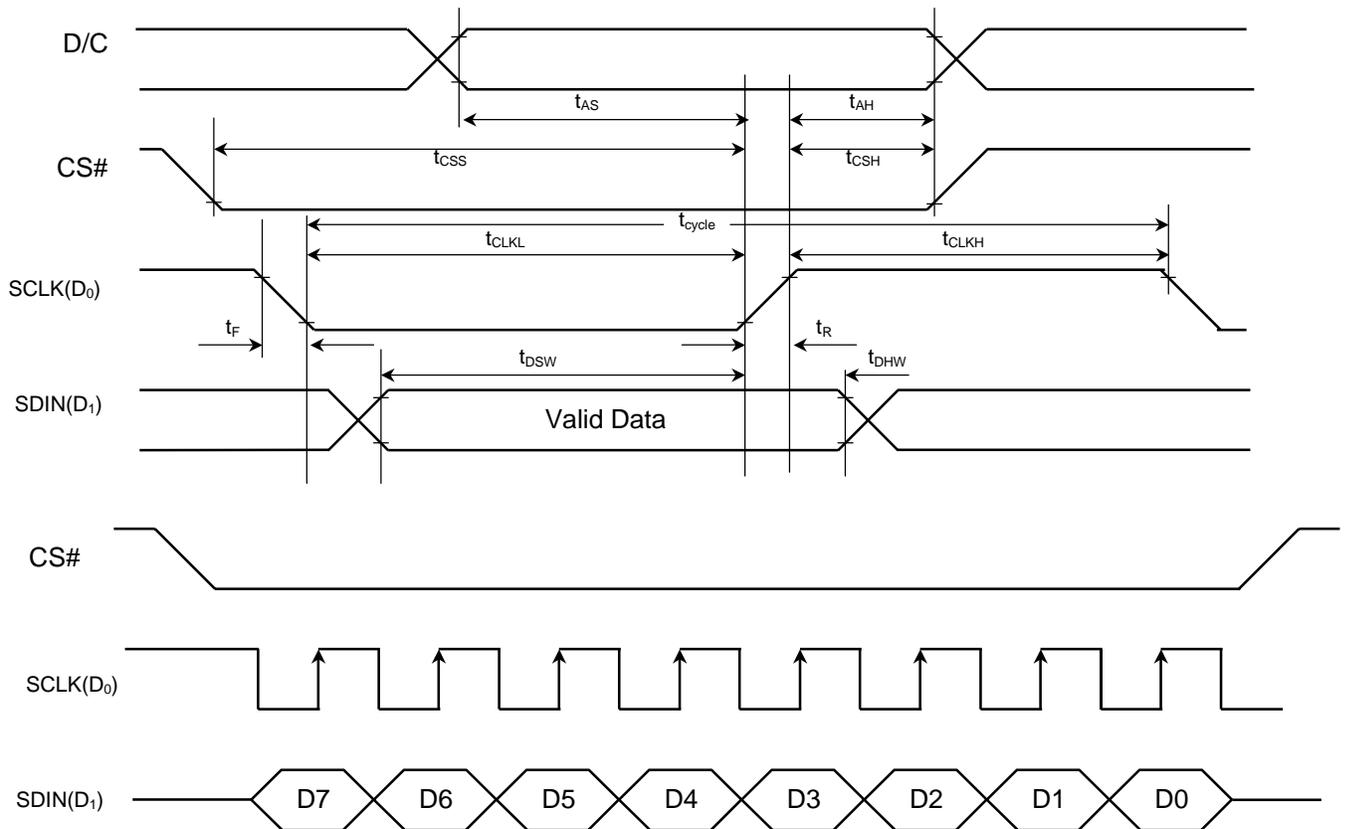


**Figure 11 - 8080-series MPU parallel interface characteristics**

**Table 12 - Serial Interface Timing Characteristics**

( $V_{DD} - V_{SS} = 2.4$  to  $3.5V$ ,  $T_A = 25^\circ C$ )

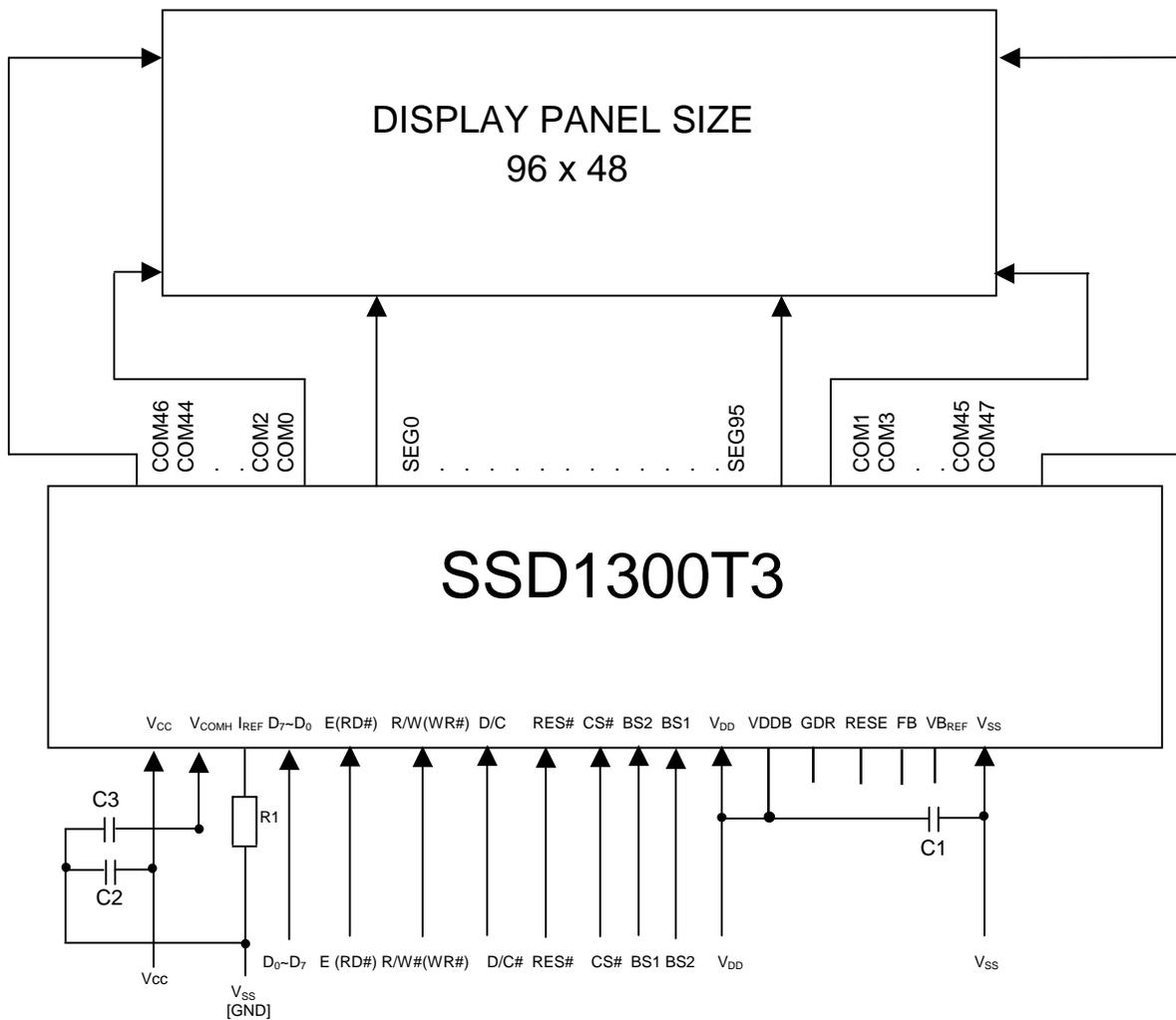
Symbol	Parameter	Min	Typ	Max	Unit
$t_{cycle}$	Clock Cycle Time	250	-	-	ns
$t_{AS}$	Address Setup Time	150	-	-	ns
$t_{AH}$	Address Hold Time	150	-	-	ns
$t_{CSS}$	Chip Select Setup Time	120	-	-	ns
$t_{CSH}$	Chip Select Hold Time	60	-	-	ns
$t_{DSW}$	Write Data Setup Time	100	-	-	ns
$t_{DHW}$	Write Data Hold Time	100	-	-	ns
$t_{CLKL}$	Clock Low Time	100	-	-	ns
$t_{CLKH}$	Clock High Time	100	-	-	ns
$t_R$	Rise Time	-	-	15	ns
$t_F$	Fall Time	-	-	15	ns



**Figure 12 - Serial interface characteristics**

### 13 APPLICATION EXAMPLE

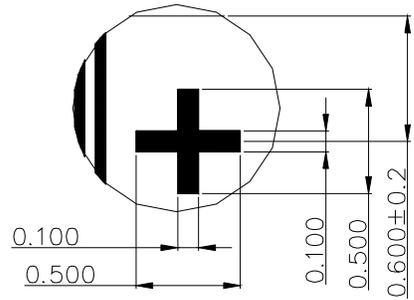
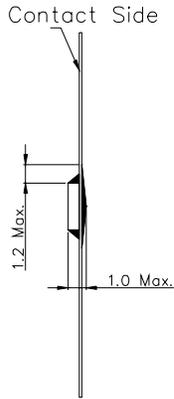
The configuration for 6800-parallel interface mode, externally  $V_{CC}$  is shown in the following diagram:  
 ( $V_{DD}=2.7V$ ,  $V_{CC}=V_{REF}=12V$ ,  $I_{REF}=10\mu A$ )



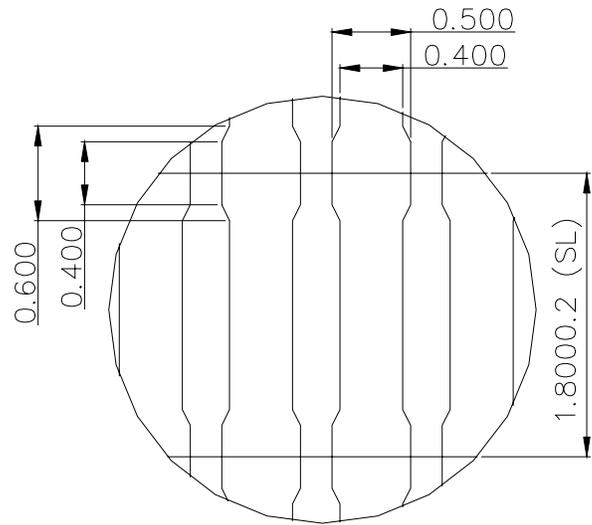
Pin connected to MCU interface: D0~D7, E, R/W#, D/C, CS#, RES#  
 Pin externally connected to VSS: BS0, VSSB  
 Pin internally connected to VCC: VREF  
 GDR, RESE,  $V_{BREF}$ , FB should be left open individually;  
 SSD1300T3R1 uses internal clock as CLS is connected to VDD inside the TAB

C1~ C3: 4.7uF  
 R1: 910kΩ,  $R1=(\text{Voltage at IREF pin}-V_{SS})/I_{REF}$   
 Voltage at IREF pin =  $V_{CC}-3V$



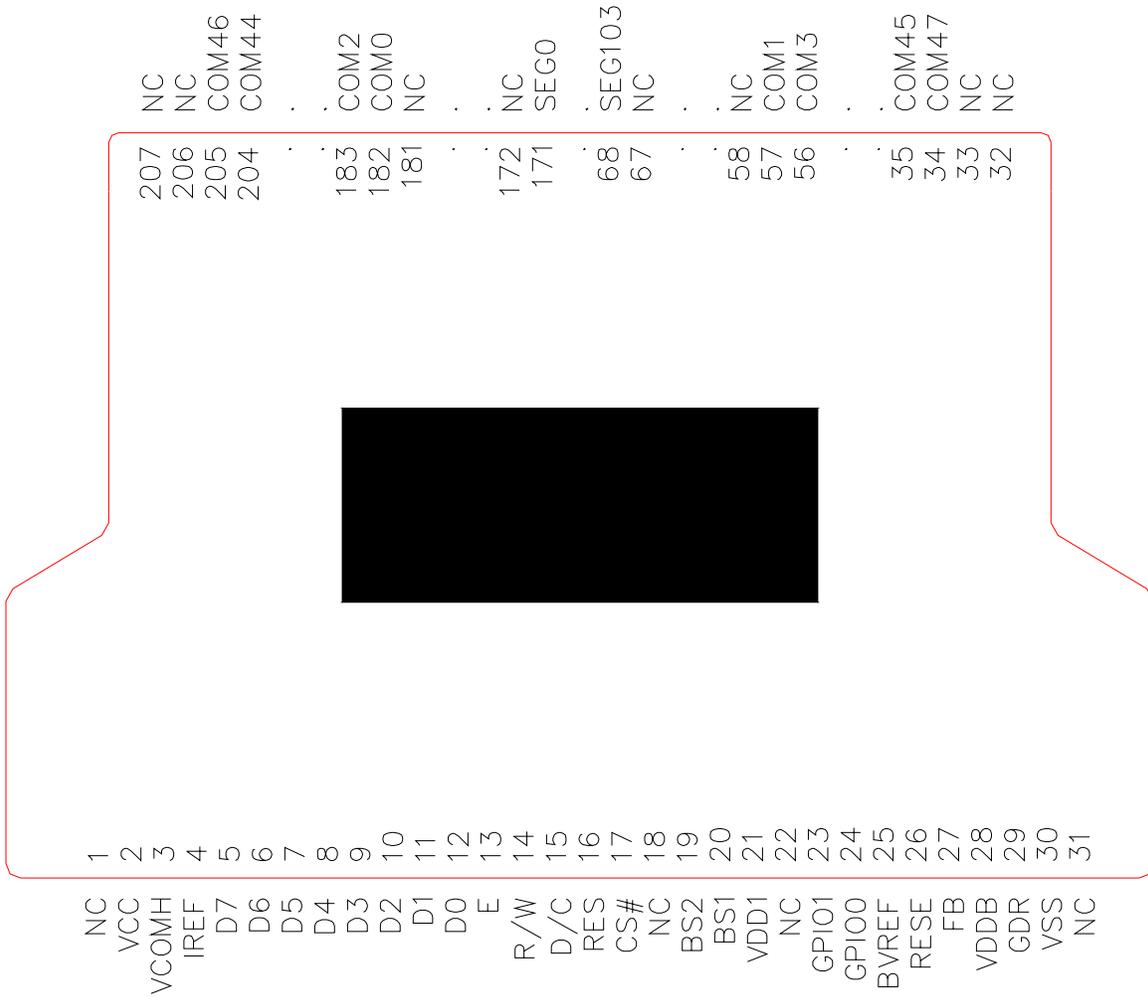


Detail A Scale 5:1  
Tolerance: 0.02mm



Detail B Scale 4:1

**Figure 14 - SSD1300TR1 pin assignment**



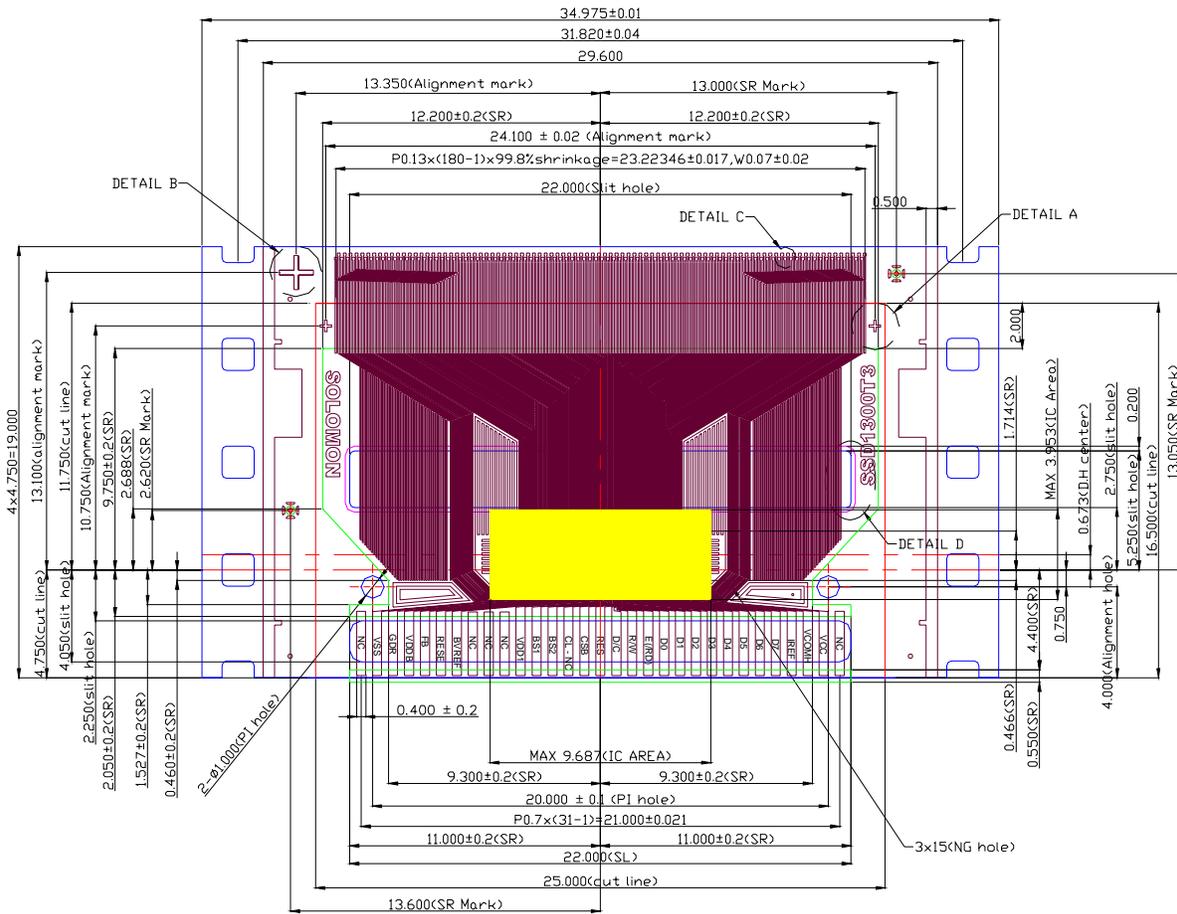
**Table 13 - SSD1300T pin assignment**

Pin no.	Pin Name	Pin no.	Pin Name	Pin no.	Pin Name
1	NC	81	SEG90	161	SEG10
2	VCC	82	SEG89	162	SEG9
3	VCOMH	83	SEG88	163	SEG8
4	IREF	84	SEG87	164	SEG7
5	D7	85	SEG86	165	SEG6
6	D6	86	SEG85	166	SEG5
7	D5	87	SEG84	167	SEG4
8	D4	88	SEG83	168	SEG3
9	D3	89	SEG82	169	SEG2
10	D2	90	SEG81	170	SEG1
11	D1	91	SEG80	171	SEG0
12	D0	92	SEG79	172	NC
13	E	93	SEG78	173	NC
14	R/W	94	SEG77	174	NC
15	D/C	95	SEG76	175	NC
16	RES#	96	SEG75	176	NC
17	CS#	97	SEG74	177	NC
18	NC	98	SEG73	178	NC
19	BS2	99	SEG72	179	NC
20	BS1	100	SEG71	180	NC
21	VDD1	101	SEG70	181	NC
22	NC	102	SEG69	182	COM0
23	GPIO1	103	SEG68	183	COM2
24	GPIO0	104	SEG67	184	COM4
25	VBREF	105	SEG66	185	COM6
26	RESE	106	SEG65	186	COM8
27	FB	107	SEG64	187	COM10
28	VDDB	108	SEG63	188	COM12
29	GDR	109	SEG62	189	COM14
30	VSS	110	SEG61	190	COM16
31	NC	111	SEG60	191	COM18
32	NC	112	SEG59	192	COM20
33	NC	113	SEG58	193	COM22
34	COM47	114	SEG57	194	COM24
35	COM45	115	SEG56	195	COM26
36	COM43	116	SEG55	196	COM28
37	COM41	117	SEG54	197	COM30
38	COM39	118	SEG53	198	COM32
39	COM37	119	SEG52	199	COM34
40	COM35	120	SEG51	200	COM36
41	COM33	121	SEG50	201	COM38
42	COM31	122	SEG49	202	COM40
43	COM29	123	SEG48	203	COM42
44	COM27	124	SEG47	204	COM44
45	COM25	125	SEG46	205	COM46
46	COM23	126	SEG45	206	NC
47	COM21	127	SEG44	207	NC
48	COM19	128	SEG43		
49	COM17	129	SEG42		
50	COM15	130	SEG41		
51	COM13	131	SEG40		
52	COM11	132	SEG39		
53	COM9	133	SEG38		
54	COM7	134	SEG37		
55	COM5	135	SEG36		
56	COM3	136	SEG35		
57	COM1	137	SEG34		
58	NC	138	SEG33		
59	NC	139	SEG32		
60	NC	140	SEG31		
61	NC	141	SEG30		
62	NC	142	SEG29		
63	NC	143	SEG28		
64	NC	144	SEG27		
65	NC	145	SEG26		
66	NC	146	SEG25		
67	NC	147	SEG24		
68	SEG103	148	SEG23		
69	SEG102	149	SEG22		
70	SEG101	150	SEG21		
71	SEG100	151	SEG20		
72	SEG99	152	SEG19		
73	SEG98	153	SEG18		
74	SEG97	154	SEG17		
75	SEG96	155	SEG16		
76	SEG95	156	SEG15		
77	SEG94	157	SEG14		
78	SEG93	158	SEG13		
79	SEG92	159	SEG12		
80	SEG91	160	SEG11		

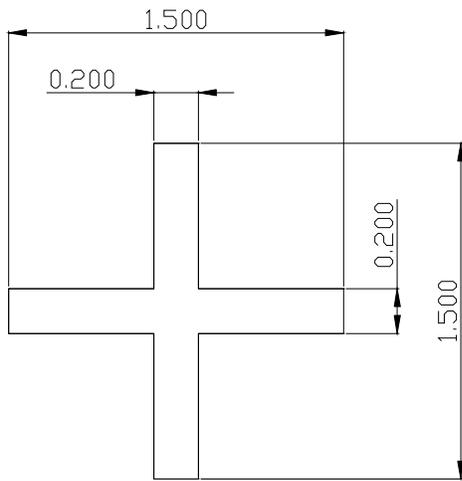
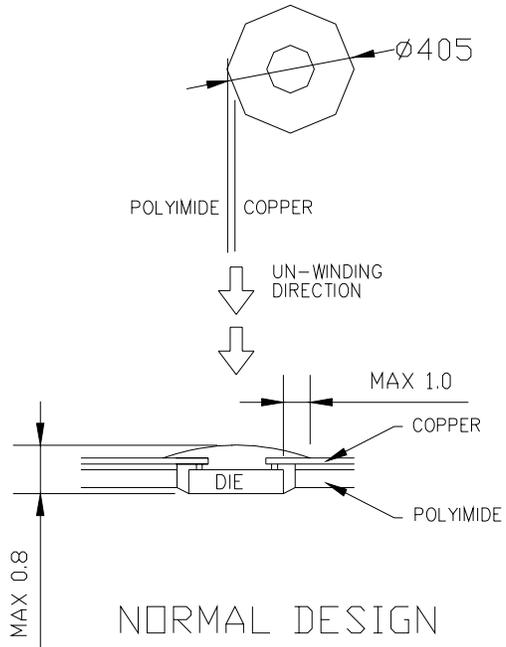
# 15 SSD1300T3R1 TAB PACKAGE

Figure 15- SSD1300TR1 detail dimensions

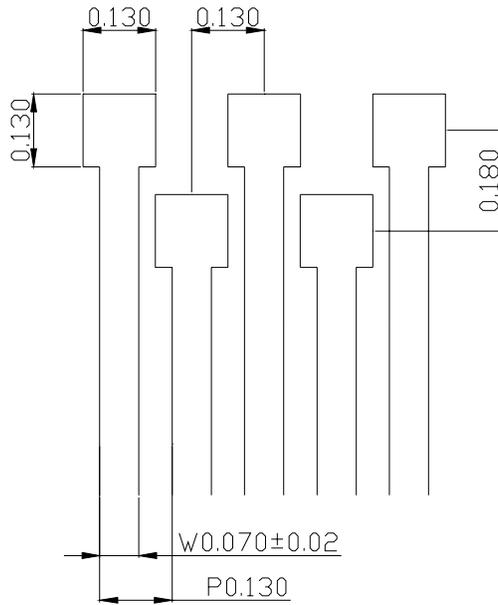
↑  
TAPE  
UN-WINDING  
DIRECTION



- NOTE:
1. GENERAL TOLERANCE:  $\pm 0.05\text{MM}$
  2. MATERIAL
    - PI: UPILEX-S  $75\pm 6\mu\text{m}$
    - ADHESIVE:  $12\pm 2\mu\text{m}$
    - CU:  $18\mu\text{m}$
    - SR:  $26\pm 14\mu\text{m}$
    - TOLERANCE  $\pm 0.200$
    - FLEX COATING:  $\text{Min}10\mu\text{m}$
  3. SN PLATING:  $0.200\pm 0.05\mu\text{m}$
  4. TAPESITE: 4 SPH,  $19\text{mm}$

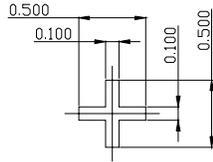


DETAIL B  
SCALE 2:1

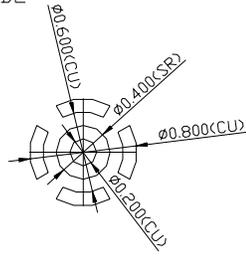


DETAIL C  
SCALE 5:1

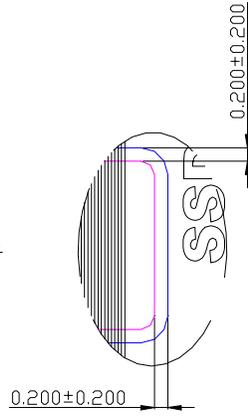
\* OPTIONAL FEATURE FOR SOLOMON SYSTECH  
 INTERNAL USE ONLY WHICH MAY BE  
 REPLACED BY PUNCHING HERE



DETAIL A\*  
 SCALE 2:1

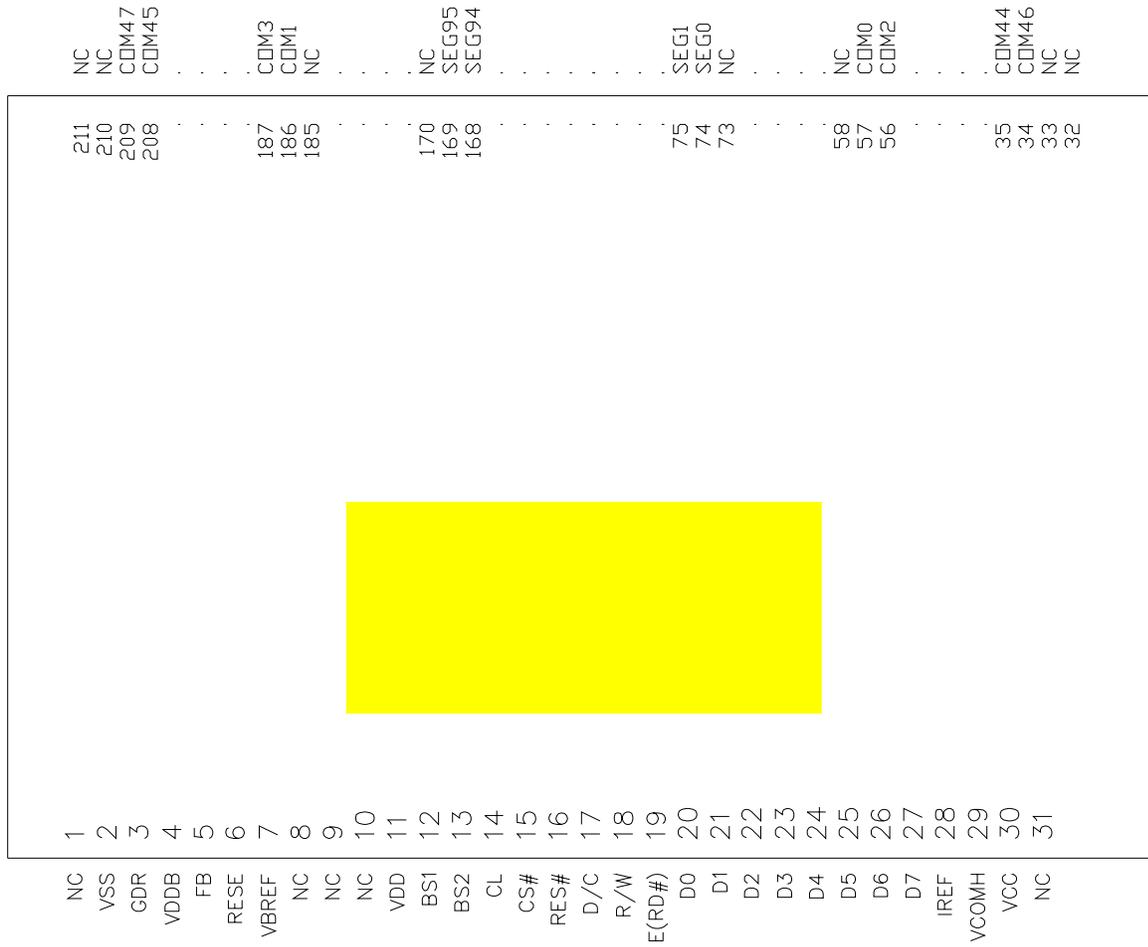


SR Mark  
 SCALE 2:1



DETAIL D  
 SCALE 1:1

**Figure 16 - SSD1300T3 pin assignment (Copper view)**



**Table 14 - SSD1300T3R1 pin assignment**

Pin no.	Pin name
1	NC
2	VSS
3	GDR
4	VDDB
5	FB
6	RESE
7	VBREF
8	NC
9	NC
10	NC
11	VDD1
12	BS1
13	BS2
14	CL
15	CS#
16	RES#
17	D/C
18	R/W
19	E/RD
20	D0
21	D1
22	D2
23	D3
24	D4
25	D5
26	D6
27	D7
28	IREF
29	VCOMH
30	VCC
31	NC
32	NC
33	NC
34	COM46
35	COM44
36	COM42
37	COM40
38	COM38
39	COM36
40	COM34
41	COM32
42	COM30
43	COM28
44	COM26
45	COM24
46	COM22
47	COM20
48	COM18
49	COM16
50	COM14
51	COM12
52	COM10
53	COM8
54	COM6
55	COM4
56	COM2
57	COM0
58	NC
59	NC
60	NC
61	NC
62	NC
63	NC
64	NC
65	NC
66	NC
67	NC
68	NC
69	NC
70	NC
71	NC
72	NC
73	NC
74	SEG0
75	SEG1
76	SEG2
77	SEG3
78	SEG4
79	SEG5
80	SEG6

Pin no.	Pin name
81	SEG7
82	SEG8
83	SEG9
84	SEG10
85	SEG11
86	SEG12
87	SEG13
88	SEG14
89	SEG15
90	SEG16
91	SEG17
92	SEG18
93	SEG19
94	SEG20
95	SEG21
96	SEG22
97	SEG23
98	SEG24
99	SEG25
100	SEG26
101	SEG27
102	SEG28
103	SEG29
104	SEG30
105	SEG31
106	SEG32
107	SEG33
108	SEG34
109	SEG35
110	SEG36
111	SEG37
112	SEG38
113	SEG39
114	SEG40
115	SEG41
116	SEG42
117	SEG43
118	SEG44
119	SEG45
120	SEG46
121	SEG47
122	SEG48
123	SEG49
124	SEG50
125	SEG51
126	SEG52
127	SEG53
128	SEG54
129	SEG55
130	SEG56
131	SEG57
132	SEG58
133	SEG59
134	SEG60
135	SEG61
136	SEG62
137	SEG63
138	SEG64
139	SEG65
140	SEG66
141	SEG67
142	SEG68
143	SEG69
144	SEG70
145	SEG71
146	SEG72
147	SEG73
148	SEG74
149	SEG75
150	SEG76
151	SEG77
152	SEG78
153	SEG79
154	SEG80
155	SEG81
156	SEG82
157	SEG83
158	SEG84
159	SEG85
160	SEG86

Pin no.	Pin name
161	SEG87
162	SEG88
163	SEG89
164	SEG90
165	SEG91
166	SEG92
167	SEG93
168	SEG94
169	SEG95
170	NC
171	NC
172	NC
173	NC
174	NC
175	NC
176	NC
177	NC
178	NC
179	NC
180	NC
181	NC
182	NC
183	NC
184	NC
185	NC
186	COM1
187	COM3
188	COM5
189	COM7
190	COM9
191	COM11
192	COM13
193	COM15
194	COM17
195	COM19
196	COM21
197	COM23
198	COM25
199	COM27
200	COM29
201	COM31
202	COM33
203	COM35
204	COM37
205	COM39
206	COM41
207	COM43
208	COM45
209	COM47
210	NC
211	NC

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