SSD1702

Advance Information

240 Outputs
Common / Segment Driver

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1. General Description

SSD1702 is a 240-outputs LCD driver capable of both COMMON or SEGMENT driving, selected by hardware pin setting. It is designed for high resolution dot matrix type LCD panel for the use on PDA or terminal.

SSD1702 can be used in cascade mode to support display system with more than 240 rows or columns. In segment mode, 4-bit or 8-bit parallel input modes are available through pin selection.

2. FEATURES

BOTH SEGMENT AND COMMON MODE
Supply voltage for LC driver: +15.0 to +30.0 V
Supply voltage for logic system: +2.4 to +3.6 V
240 outputs for either common or segment driving
Pin selectable between common and segment mode
Low output impedance
Low power consumption

SEGMENT MODE
Maximum XCK clock frequency: 20 MHz (VDD = +3.0 to +3.6V)
15 MHz (VDD = +2.4 to +3.0V)
Pin selectable 4-bit or 8-bit input modes
Automatic transfer function of enable signal
Automatically stop the internal clock after counting 240 bits of input data in chip select mode
Line latch circuit reset function when DISPOFF# active

COMMON MODE
Maximum LP clock frequency: 1 MHz (VDD = +2.4 to 3.6V)
Built-in 240 bits bi-directional shift register
Single (240 bits shift register) or Dual mode (two 120 bits shift register) operations
Shift register circuit reset function when DISPOFF# active

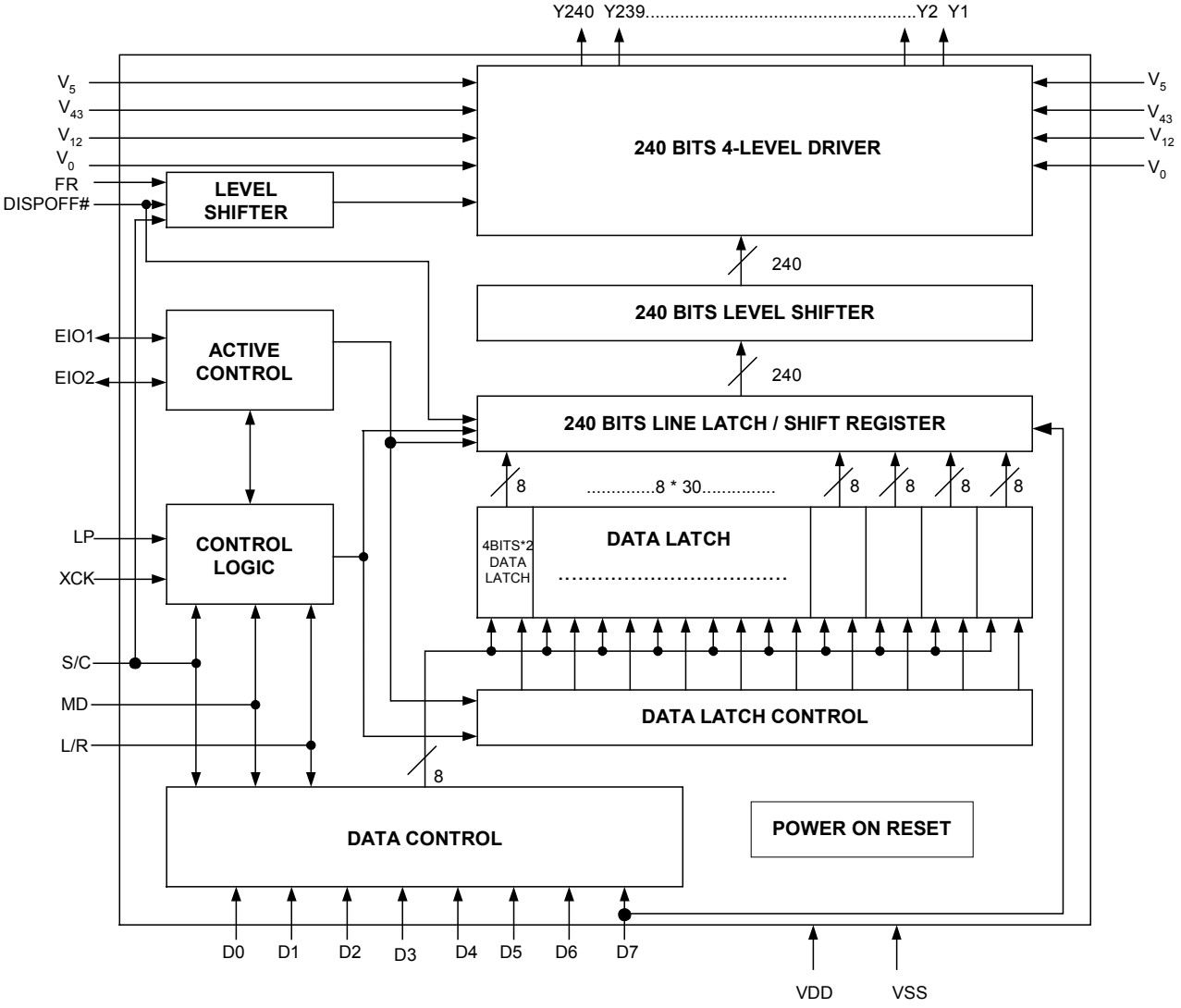
3. ORDERING INFORMATION

Table 1 - Ordering Information

Ordering Part Number	Outerlead pitch (mm)	Package Form	Reference	Remark
SSD1702Z	N/A	Gold Bump Die	Figure 2 on page 7	-
SSD1702T1R1	0.21	TAB	Figure 20 on page 39	-
SSD1702T2R1	0.20	TAB	Figure 21 on page 41	-
SSD1702T3R1	0.055	TAB	Figure 22 on page 43	-

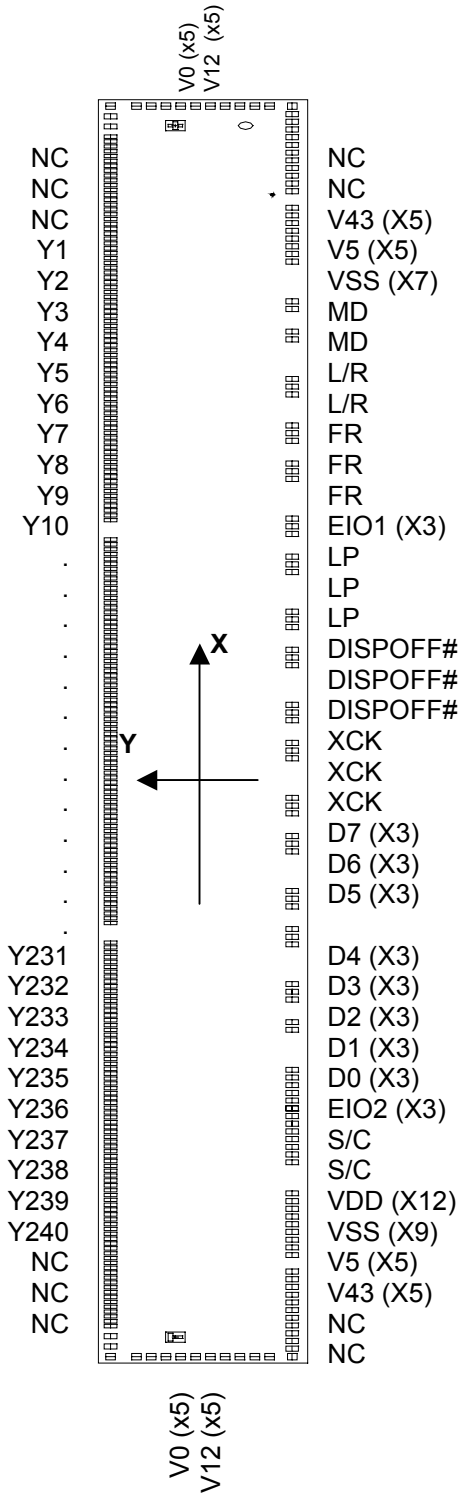
4. BLOCK DIAGRAM

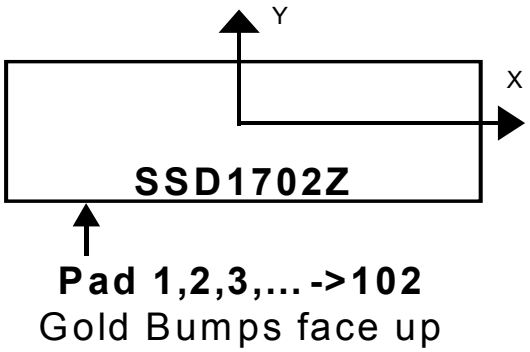
Figure 1 - Block Diagram of SSD1702



5. DIE PAD COORDINATES

Figure 2 - SSD1702Z die pad assignment





Die Size:	12.65mm x 1.25 mm
Die Height:	533um

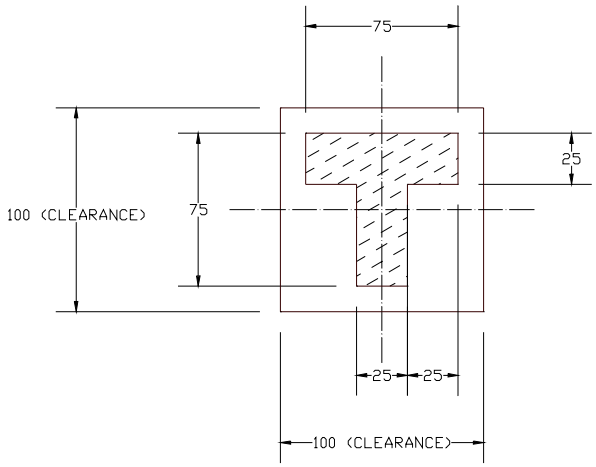
Bump Size:

Pad 1, 102, 113, 358	65um x 50um
Pad 2-101	49um x 105um
Pad 103-112, 359-368	65um x 49um
Pad 114, 115, 356, 357	50um x 95um
Pad 116-355	33um x 95um

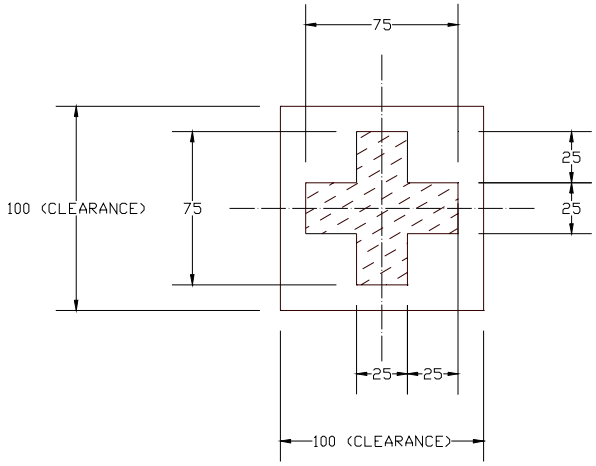
Alignment Mark:

Type	Size	Coordinate
T shape	75um x 75um	-5989.0, 147.3
+ shape	75um x 75um	5989.0, 147.3
Circle	R-37.5um	-5989.0,-215.0
Circle	R-37.5um	5989.0,-215.0

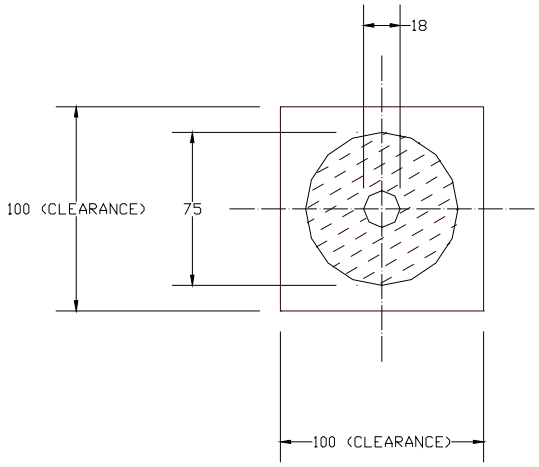
Figure 3 - Alignment mark detail dimensions



T shape



+ shape



Circle

Unit in μm

Table 2 - SSD1702Z die pad coordinates

Pad no.	Pad name	X	Y
1	NC	-6181.5	-473.9
2	NC	-6102.7	-473.9
3	V43	-6026.5	-473.9
4	V43	-5950.3	-473.9
5	V43	-5874.1	-473.9
6	V43	-5797.9	-473.9
7	V43	-5721.7	-473.9
8	V5	-5645.5	-473.9
9	V5	-5569.3	-473.9
10	V5	-5493.1	-473.9
11	V5	-5416.9	-473.9
12	V5	-5340.7	-473.9
13	VSS	-5177.3	-473.9
14	VSS	-5101.1	-473.9
15	VSS	-5024.9	-473.9
16	VSS	-4948.7	-473.9
17	VSS	-4872.5	-473.9
18	VSS	-4796.3	-473.9
19	VSS	-4720.1	-473.9
20	VSS	-4643.9	-473.9
21	VSS	-4567.7	-473.9
22	VDD	-4259.9	-473.9
23	VDD	-4183.7	-473.9
24	VDD	-4107.5	-473.9
25	VDD	-4031.3	-473.9
26	VDD	-3955.1	-473.9
27	VDD	-3878.9	-473.9
28	VDD	-3802.7	-473.9
29	VDD	-3726.5	-473.9
30	VDD	-3650.3	-473.9
31	VDD	-3574.1	-473.9
32	VDD	-3497.9	-473.9
33	VDD	-3421.7	-473.9
34	VDD	-3345.5	-473.9
35	S/C	-2950.9	-473.9
36	S/C	-2874.7	-473.9
37	EIO2	-2650.7	-473.9
38	EIO2	-2574.5	-473.9
39	EIO2	-2498.3	-473.9
40	D0	-2106.7	-473.9
41	D0	-2030.5	-473.9
42	D0	-1954.3	-473.9
43	D1	-1730.3	-473.9
44	D1	-1654.1	-473.9
45	D1	-1577.9	-473.9
46	D2	-1186.3	-473.9
47	D2	-1110.1	-473.9
48	D2	-1033.9	-473.9
49	D3	-809.9	-473.9
50	D3	-733.7	-473.9
51	D3	-657.5	-473.9
52	D4	-265.9	-473.9
53	D4	-189.7	-473.9
54	D4	-113.5	-473.9
55	D5	110.5	-473.9
56	D5	186.7	-473.9
57	D5	262.9	-473.9
58	D6	654.5	-473.9
59	D6	730.7	-473.9
60	D6	806.9	-473.9
61	D7	1030.9	-473.9
62	D7	1107.1	-473.9
63	D7	1183.3	-473.9
64	XCK	1574.9	-473.9
65	XCK	1651.1	-473.9
66	XCK	1727.3	-473.9
67	DISPOFF#	1951.3	-473.9
68	DISPOFF#	2027.5	-473.9
69	DISPOFF#	2103.7	-473.9
70	LP	2495.3	-473.9
71	LP	2571.5	-473.9
72	LP	2647.7	-473.9
73	EIO1	2871.7	-473.9
74	EIO1	2947.9	-473.9
75	EIO1	3024.1	-473.9
76	FR	3331.9	-473.9
77	FR	3408.1	-473.9
78	FR	3484.3	-473.9
79	L/R	3875.9	-473.9
80	L/R	3952.1	-473.9
81	MD	4176.1	-473.9
82	MD	4252.3	-473.9
83	VSS	4643.9	-473.9
84	VSS	4720.1	-473.9
85	VSS	4796.3	-473.9
86	VSS	4872.5	-473.9
87	VSS	4948.7	-473.9
88	VSS	5024.9	-473.9
89	VSS	5101.1	-473.9
90	VSS	5177.3	-473.9
91	V5	5340.7	-473.9
92	V5	5416.9	-473.9
93	V5	5493.1	-473.9
94	V5	5569.3	-473.9
95	V5	5645.5	-473.9
96	V43	5721.7	-473.9
97	V43	5797.9	-473.9
98	V43	5874.1	-473.9
99	V43	5950.3	-473.9
100	V43	6026.5	-473.9
101	NC	6102.7	-473.9
102	NC	6181.5	-473.9
103	V12	6181.5	-337.9
104	V12	6181.5	-261.7
105	V12	6181.5	-185.5
106	V12	6181.5	-109.3
107	V12	6181.5	-33.1
108	V0	6181.5	43.1
109	V0	6181.5	119.3
110	V0	6181.5	195.5
111	V0	6181.5	271.7
112	V0	6181.5	347.9
113	NC	6181.5	495.9
114	NC	6081.0	495.9
115	NC	5980.5	495.9
116	Y1	5880.0	495.9
117	Y2	5832.0	495.9
118	Y3	5784.0	495.9
119	Y4	5736.0	495.9
120	Y5	5688.0	495.9
121	Y6	5640.0	495.9
122	Y7	5592.0	495.9
123	Y8	5544.0	495.9
124	Y9	5496.0	495.9
125	Y10	5448.0	495.9
126	Y11	5400.0	495.9
127	Y12	5352.0	495.9
128	Y13	5304.0	495.9
129	Y14	5256.0	495.9
130	Y15	5208.0	495.9
131	Y16	5160.0	495.9
132	Y17	5112.0	495.9
133	Y18	5064.0	495.9
134	Y19	5016.0	495.9
135	Y20	4968.0	495.9
136	Y21	4920.0	495.9
137	Y22	4872.0	495.9
138	Y23	4824.0	495.9
139	Y24	4776.0	495.9
140	Y25	4728.0	495.9
141	Y26	4680.0	495.9
142	Y27	4632.0	495.9
143	Y28	4584.0	495.9
144	Y29	4536.0	495.9
145	Y30	4488.0	495.9
146	Y31	4440.0	495.9
147	Y32	4392.0	495.9
148	Y33	4344.0	495.9
149	Y34	4296.0	495.9
150	Y35	4248.0	495.9
151	Y36	4200.0	495.9
152	Y37	4152.0	495.9
153	Y38	4104.0	495.9
154	Y39	4056.0	495.9
155	Y40	4008.0	495.9
156	Y41	3960.0	495.9
157	Y42	3912.0	495.9
158	Y43	3864.0	495.9
159	Y44	3816.0	495.9
160	Y45	3768.0	495.9
161	Y46	3720.0	495.9
162	Y47	3672.0	495.9
163	Y48	3624.0	495.9
164	Y49	3576.0	495.9
165	Y50	3528.0	495.9
166	Y51	3480.0	495.9
167	Y52	3432.0	495.9
168	Y53	3384.0	495.9
169	Y54	3336.0	495.9
170	Y55	3288.0	495.9
171	Y56	3240.0	495.9
172	Y57	3192.0	495.9
173	Y58	3144.0	495.9
174	Y59	3096.0	495.9
175	Y60	3048.0	495.9
176	Y61	3000.0	495.9
177	Y62	2952.0	495.9
178	Y63	2904.0	495.9
179	Y64	2856.0	495.9
180	Y65	2808.0	495.9

Pad no.	Pad name	X	Y
181	Y66	2760.0	495.9
182	Y67	2712.0	495.9
183	Y68	2664.0	495.9
184	Y69	2616.0	495.9
185	Y70	2568.0	495.9
186	Y71	2520.0	495.9
187	Y72	2472.0	495.9
188	Y73	2424.0	495.9
189	Y74	2376.0	495.9
190	Y75	2328.0	495.9
191	Y76	2280.0	495.9
192	Y77	2232.0	495.9
193	Y78	2184.0	495.9
194	Y79	2136.0	495.9
195	Y80	2088.0	495.9
196	Y81	1896.0	495.9
197	Y82	1848.0	495.9
198	Y83	1800.0	495.9
199	Y84	1752.0	495.9
200	Y85	1704.0	495.9
201	Y86	1656.0	495.9
202	Y87	1608.0	495.9
203	Y88	1560.0	495.9
204	Y89	1512.0	495.9
205	Y90	1464.0	495.9
206	Y91	1416.0	495.9
207	Y92	1368.0	495.9
208	Y93	1320.0	495.9
209	Y94	1272.0	495.9
210	Y95	1224.0	495.9
211	Y96	1176.0	495.9
212	Y97	1128.0	495.9
213	Y98	1080.0	495.9
214	Y99	1032.0	495.9
215	Y100	984.0	495.9
216	Y101	936.0	495.9
217	Y102	888.0	495.9
218	Y103	840.0	495.9
219	Y104	792.0	495.9
220	Y105	744.0	495.9
221	Y106	696.0	495.9
222	Y107	648.0	495.9
223	Y108	600.0	495.9
224	Y109	552.0	495.9
225	Y110	504.0	495.9
226	Y111	456.0	495.9
227	Y112	408.0	495.9
228	Y113	360.0	495.9
229	Y114	312.0	495.9
230	Y115	264.0	495.9
231	Y116	216.0	495.9
232	Y117	168.0	495.9
233	Y118	120.0	495.9
234	Y119	72.0	495.9
235	Y120	24.0	495.9
236	Y121	-24.0	495.9
237	Y122	-72.0	495.9
238	Y123	-120.0	495.9
239	Y124	-168.0	495.9
240	Y125	-216.0	495.9

Pad no.	Pad name	X	Y
241	Y126	-264.0	495.9
242	Y127	-312.0	495.9
243	Y128	-360.0	495.9
244	Y129	-408.0	495.9
245	Y130	-456.0	495.9
246	Y131	-504.0	495.9
247	Y132	-552.0	495.9
248	Y133	-600.0	495.9
249	Y134	-648.0	495.9
250	Y135	-696.0	495.9
251	Y136	-744.0	495.9
252	Y137	-792.0	495.9
253	Y138	-840.0	495.9
254	Y139	-888.0	495.9
255	Y140	-936.0	495.9
256	Y141	-984.0	495.9
257	Y142	-1032.0	495.9
258	Y143	-1080.0	495.9
259	Y144	-1128.0	495.9
260	Y145	-1176.0	495.9
261	Y146	-1224.0	495.9
262	Y147	-1272.0	495.9
263	Y148	-1320.0	495.9
264	Y149	-1368.0	495.9
265	Y150	-1416.0	495.9
266	Y151	-1464.0	495.9
267	Y152	-1512.0	495.9
268	Y153	-1560.0	495.9
269	Y154	-1608.0	495.9
270	Y155	-1656.0	495.9
271	Y156	-1704.0	495.9
272	Y157	-1752.0	495.9
273	Y158	-1800.0	495.9
274	Y159	-1848.0	495.9
275	Y160	-1896.0	495.9
276	Y161	-2088.0	495.9
277	Y162	-2136.0	495.9
278	Y163	-2184.0	495.9
279	Y164	-2232.0	495.9
280	Y165	-2280.0	495.9
281	Y166	-2328.0	495.9
282	Y167	-2376.0	495.9
283	Y168	-2424.0	495.9
284	Y169	-2472.0	495.9
285	Y170	-2520.0	495.9
286	Y171	-2568.0	495.9
287	Y172	-2616.0	495.9
288	Y173	-2664.0	495.9
289	Y174	-2712.0	495.9
290	Y175	-2760.0	495.9
291	Y176	-2808.0	495.9
292	Y177	-2856.0	495.9
293	Y178	-2904.0	495.9
294	Y179	-2952.0	495.9
295	Y180	-3000.0	495.9
296	Y181	-3048.0	495.9
297	Y182	-3096.0	495.9
298	Y183	-3144.0	495.9
299	Y184	-3192.0	495.9
300	Y185	-3240.0	495.9

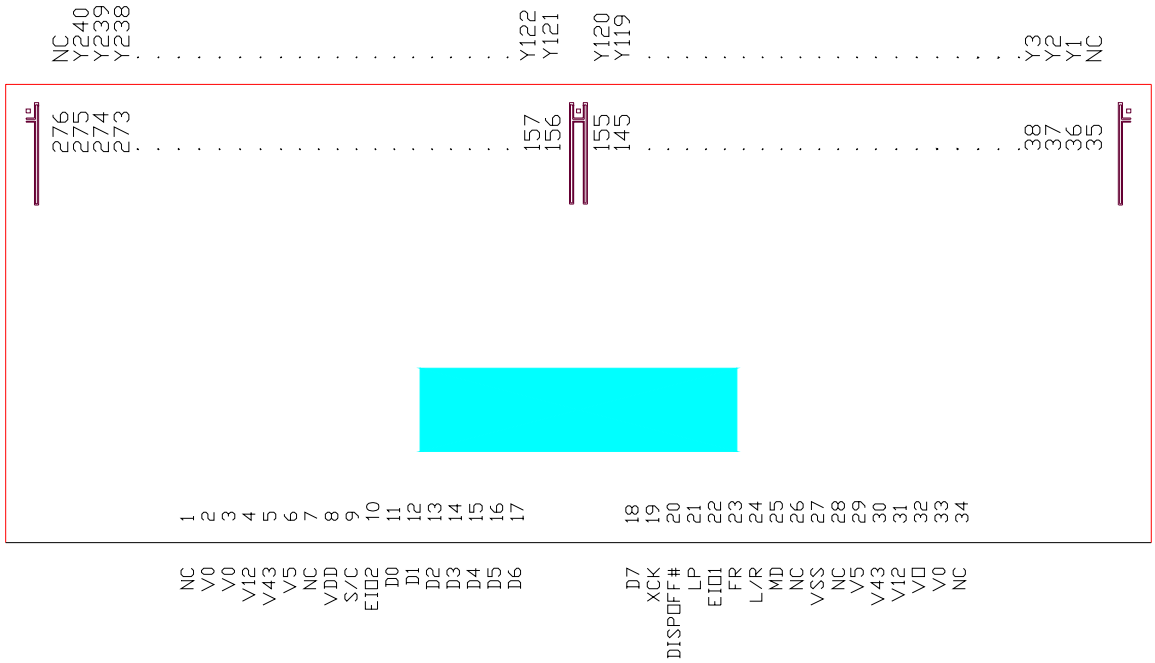
Pad no.	Pad name	X	Y
301	Y186	-3288.0	495.9
302	Y187	-3336.0	495.9
303	Y188	-3384.0	495.9
304	Y189	-3432.0	495.9
305	Y190	-3480.0	495.9
306	Y191	-3528.0	495.9
307	Y192	-3576.0	495.9
308	Y193	-3624.0	495.9
309	Y194	-3672.0	495.9
310	Y195	-3720.0	495.9
311	Y196	-3768.0	495.9
312	Y197	-3816.0	495.9
313	Y198	-3864.0	495.9
314	Y199	-3912.0	495.9
315	Y200	-3960.0	495.9
316	Y201	-4008.0	495.9
317	Y202	-4056.0	495.9
318	Y203	-4104.0	495.9
319	Y204	-4152.0	495.9
320	Y205	-4200.0	495.9
321	Y206	-4248.0	495.9
322	Y207	-4296.0	495.9
323	Y208	-4344.0	495.9
324	Y209	-4392.0	495.9
325	Y210	-4440.0	495.9
326	Y211	-4488.0	495.9
327	Y212	-4536.0	495.9
328	Y213	-4584.0	495.9
329	Y214	-4632.0	495.9
330	Y215	-4680.0	495.9
331	Y216	-4728.0	495.9
332	Y217	-4776.0	495.9
333	Y218	-4824.0	495.9
334	Y219	-4872.0	495.9
335	Y220	-4920.0	495.9
336	Y221	-4968.0	495.9
337	Y222	-5016.0	495.9
338	Y223	-5064.0	495.9
339	Y224	-5112.0	495.9
340	Y225	-5160.0	495.9
341	Y226	-5208.0	495.9
342	Y227	-5256.0	495.9
343	Y228	-5304.0	495.9
344	Y229	-5352.0	495.9
345	Y230	-5400.0	495.9
346	Y231	-5448.0	495.9
347	Y232	-5496.0	495.9
348	Y233	-5544.0	495.9
349	Y234	-5592.0	495.9
350	Y235	-5640.0	495.9
351	Y236	-5688.0	495.9
352	Y237	-5736.0	495.9
353	Y238	-5784.0	495.9
354	Y239	-5832.0	495.9
355	Y240	-5880.0	495.9
356	NC	-5980.5	495.9
357	NC	-6081.0	495.9
358	NC	-6181.5	495.9
359	V0	-6181.5	347.9
360	V0	-6181.5	271.7

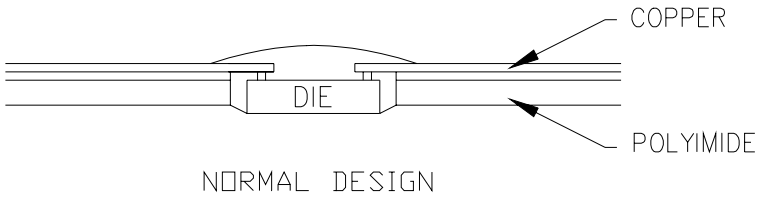
Pad no.	Pad name	X	Y
361	V0	-6181.5	195.5
362	V0	-6181.5	119.3
363	V0	-6181.5	43.1
364	V12	-6181.5	-33.1
365	V12	-6181.5	-109.3
366	V12	-6181.5	-185.5
367	V12	-6181.5	-261.7
368	V12	-6181.5	-337.9

6. TAB package pin assignment

SSD1702T1 TAB

Figure 4 - SSD1702T1 pin assignment (Copper view)





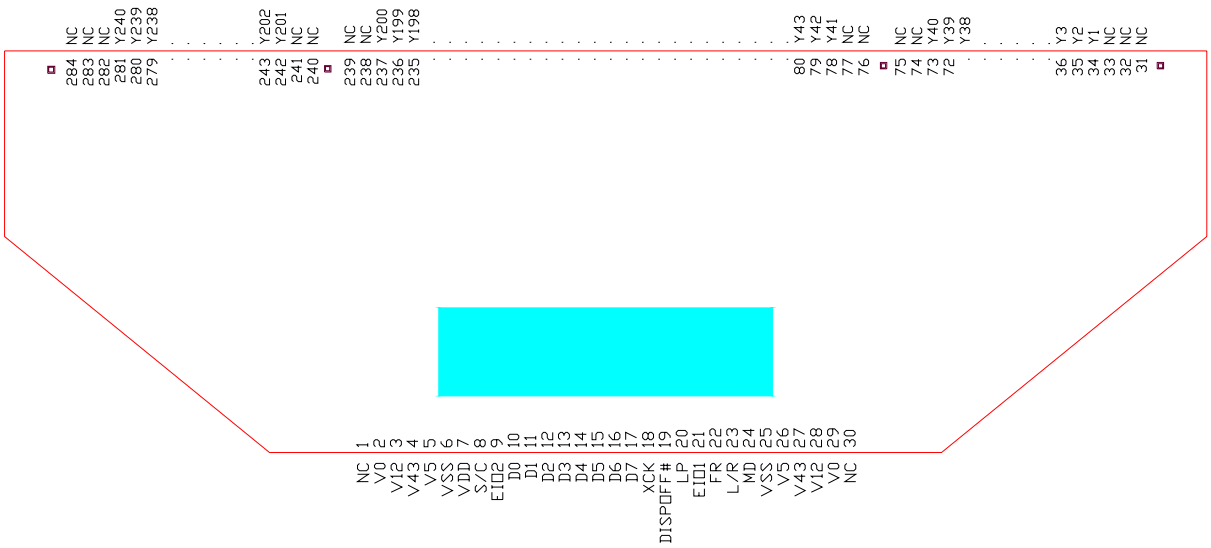
NORMAL DESIGN

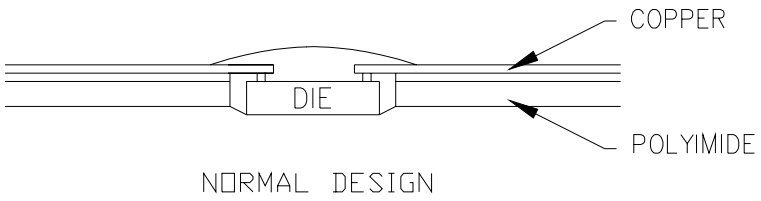
Table 3 - SSD1702T1 pin assignment

Pin no.	Pin Name	Pin no.	Pin Name	Pin no.	Pin Name	Pin no.	Pin Name	Pin no.	Pin Name
1	NC	61	Y26	121	Y86	181	Y146	241	Y206
2	V0	62	Y27	122	Y87	182	Y147	242	Y207
3	V0	63	Y28	123	Y88	183	Y148	243	Y208
4	V12	64	Y29	124	Y89	184	Y149	244	Y209
5	V43	65	Y30	125	Y90	185	Y150	245	Y210
6	V5	66	Y31	126	Y91	186	Y151	246	Y211
7	NC	67	Y32	127	Y92	187	Y152	247	Y212
8	VDD	68	Y33	128	Y93	188	Y153	248	Y213
9	S/C	69	Y34	129	Y94	189	Y154	249	Y214
10	EIO2	70	Y35	130	Y95	190	Y155	250	Y215
11	D0	71	Y36	131	Y96	191	Y156	251	Y216
12	D1	72	Y37	132	Y97	192	Y157	252	Y217
13	D2	73	Y38	133	Y98	193	Y158	253	Y218
14	D3	74	Y39	134	Y99	194	Y159	254	Y219
15	D4	75	Y40	135	Y100	195	Y160	255	Y220
16	D5	76	Y41	136	Y101	196	Y161	256	Y221
17	D6	77	Y42	137	Y102	197	Y162	257	Y222
18	D7	78	Y43	138	Y103	198	Y163	258	Y223
19	XCK	79	Y44	139	Y104	199	Y164	259	Y224
20	DISPOFF#	80	Y45	140	Y105	200	Y165	260	Y225
21	LP	81	Y46	141	Y106	201	Y166	261	Y226
22	EIO1	82	Y47	142	Y107	202	Y167	262	Y227
23	FR	83	Y48	143	Y108	203	Y168	263	Y228
24	L/R	84	Y49	144	Y109	204	Y169	264	Y229
25	MD	85	Y50	145	Y110	205	Y170	265	Y230
26	NC	86	Y51	146	Y111	206	Y171	266	Y231
27	VSS	87	Y52	147	Y112	207	Y172	267	Y232
28	NC	88	Y53	148	Y113	208	Y173	268	Y233
29	V5	89	Y54	149	Y114	209	Y174	269	Y234
30	V43	90	Y55	150	Y115	210	Y175	270	Y235
31	V12	91	Y56	151	Y116	211	Y176	271	Y236
32	V0	92	Y57	152	Y117	212	Y177	272	Y237
33	V0	93	Y58	153	Y118	213	Y178	273	Y238
34	NC	94	Y59	154	Y119	214	Y179	274	Y239
35	NC	95	Y60	155	Y120	215	Y180	275	Y240
36	Y1	96	Y61	156	Y121	216	Y181	276	NC
37	Y2	97	Y62	157	Y122	217	Y182		
38	Y3	98	Y63	158	Y123	218	Y183		
39	Y4	99	Y64	159	Y124	219	Y184		
40	Y5	100	Y65	160	Y125	220	Y185		
41	Y6	101	Y66	161	Y126	221	Y186		
42	Y7	102	Y67	162	Y127	222	Y187		
43	Y8	103	Y68	163	Y128	223	Y188		
44	Y9	104	Y69	164	Y129	224	Y189		
45	Y10	105	Y70	165	Y130	225	Y190		
46	Y11	106	Y71	166	Y131	226	Y191		
47	Y12	107	Y72	167	Y132	227	Y192		
48	Y13	108	Y73	168	Y133	228	Y193		
49	Y14	109	Y74	169	Y134	229	Y194		

SSD1702T2 TAB

Figure 5 - SSD1702T2 pin assignment (Copper view)





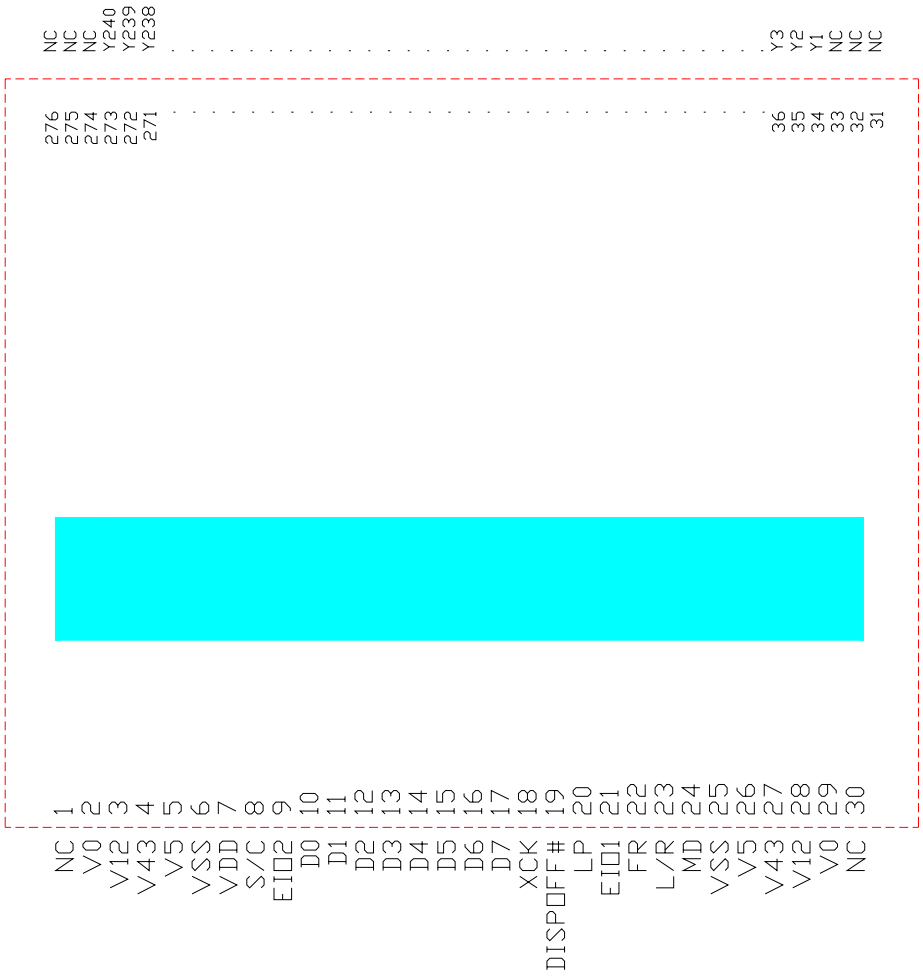
NORMAL DESIGN

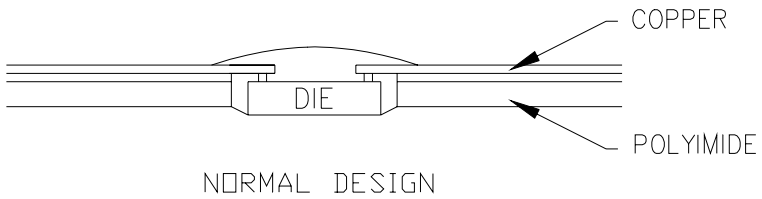
Table 4 - SSD1702T2 pin assignment

Pin no.	Pin Name	Pin no.	Pin Name	Pin no.	Pin Name	Pin no.	Pin Name	Pin no.	Pin Name
1	NC	61	Y28	121	Y84	181	Y144	241	NC
2	V0	62	Y29	122	Y85	182	Y145	242	Y201
3	V12	63	Y30	123	Y86	183	Y146	243	Y202
4	V43	64	Y31	124	Y87	184	Y147	244	Y203
5	V5	65	Y32	125	Y88	185	Y148	245	Y204
6	NC	66	Y33	126	Y89	186	Y149	246	Y205
7	VDD	67	Y34	127	Y90	187	Y150	247	Y206
8	S/C	68	Y35	128	Y91	188	Y151	248	Y207
9	EIO2	69	Y36	129	Y92	189	Y152	249	Y208
10	D0	70	Y37	130	Y93	190	Y153	250	Y209
11	D1	71	Y38	131	Y94	191	Y154	251	Y210
12	D2	72	Y39	132	Y95	192	Y155	252	Y211
13	D3	73	Y40	133	Y96	193	Y156	253	Y212
14	D4	74	NC	134	Y97	194	Y157	254	Y213
15	D5	75	NC	135	Y98	195	Y158	255	Y214
16	D6	76	NC	136	Y99	196	Y159	256	Y215
17	D7	77	NC	137	Y100	197	Y160	257	Y216
18	XCK	78	Y41	138	Y101	198	Y161	258	Y217
19	DISPOFF#	79	Y42	139	Y102	199	Y162	259	Y218
20	LP	80	Y43	140	Y103	200	Y163	260	Y219
21	EIO1	81	Y44	141	Y104	201	Y164	261	Y220
22	FR	82	Y45	142	Y105	202	Y165	262	Y221
23	L/R	83	Y46	143	Y106	203	Y166	263	Y222
24	MD	84	Y47	144	Y107	204	Y167	264	Y223
25	VSS	85	Y48	145	Y108	205	Y168	265	Y224
26	V5	86	Y49	146	Y109	206	Y169	266	Y225
27	V43	87	Y50	147	Y110	207	Y170	267	Y226
28	V12	88	Y51	148	Y111	208	Y171	268	Y227
29	V0	89	Y52	149	Y112	209	Y172	269	Y228
30	NC	90	Y53	150	Y113	210	Y173	270	Y229
31	NC	91	Y54	151	Y114	211	Y174	271	Y230
32	NC	92	Y55	152	Y115	212	Y175	272	Y231
33	NC	93	Y56	153	Y116	213	Y176	273	Y232
34	Y1	94	Y57	154	Y117	214	Y177	274	Y233
35	Y2	95	Y58	155	Y118	215	Y178	275	Y234
36	Y3	96	Y59	156	Y119	216	Y179	276	Y235
37	Y4	97	Y60	157	Y120	217	Y180	277	Y236
38	Y5	98	Y61	158	Y121	218	Y181	278	Y237
39	Y6	99	Y62	159	Y122	219	Y182	279	Y238
40	Y7	100	Y63	160	Y123	220	Y183	280	Y239
41	Y8	101	Y64	161	Y124	221	Y184	281	Y240
42	Y9	102	Y65	162	Y125	222	Y185	282	NC
43	Y10	103	Y66	163	Y126	223	Y186	283	NC
44	Y11	104	Y67	164	Y127	224	Y187	284	NC
45	Y12	105	Y68	165	Y128	225	Y188		
46	Y13	106	Y69	166	Y129	226	Y189		
47	Y14	107	Y70	167	Y130	227	Y190		
48	Y15	108	Y71	168	Y131	228	Y191		
49	Y16	109	Y72	169	Y132	229	Y192		

SSD1702T3 TAB

Figure 6 - SSD1702T3 pin assignment (Copper view)





NORMAL DESIGN

Table 5 - SSD1702T3 pin assignment

Pin no.	Pin Name	Pin no.	Pin Name	Pin no.	Pin Name	Pin no.	Pin Name	Pin no.	Pin Name
1	NC	61	Y28	121	Y88	181	Y148	241	Y208
2	V0	62	Y29	122	Y89	182	Y149	242	Y209
3	V12	63	Y30	123	Y90	183	Y150	243	Y210
4	V43	64	Y31	124	Y91	184	Y151	244	Y211
5	V5	65	Y32	125	Y92	185	Y152	245	Y212
6	NC	66	Y33	126	Y93	186	Y153	246	Y213
7	VDD	67	Y34	127	Y94	187	Y154	247	Y214
8	S/C	68	Y35	128	Y95	188	Y155	248	Y215
9	EIO2	69	Y36	129	Y96	189	Y156	249	Y216
10	D0	70	Y37	130	Y97	190	Y157	250	Y217
11	D1	71	Y38	131	Y98	191	Y158	251	Y218
12	D2	72	Y39	132	Y99	192	Y159	252	Y219
13	D3	73	Y40	133	Y100	193	Y160	253	Y220
14	D4	74	Y41	134	Y101	194	Y161	254	Y221
15	D5	75	Y42	135	Y102	195	Y162	255	Y222
16	D6	76	Y43	136	Y103	196	Y163	256	Y223
17	D7	77	Y44	137	Y104	197	Y164	257	Y224
18	XCK	78	Y45	138	Y105	198	Y165	258	Y225
19	DISPOFF#	79	Y46	139	Y106	199	Y166	259	Y226
20	LP	80	Y47	140	Y107	200	Y167	260	Y227
21	EIO1	81	Y48	141	Y108	201	Y168	261	Y228
22	FR	82	Y49	142	Y109	202	Y169	262	Y229
23	L/R	83	Y50	143	Y110	203	Y170	263	Y230
24	MD	84	Y51	144	Y111	204	Y171	264	Y231
25	VSS	85	Y52	145	Y112	205	Y172	265	Y232
26	V5	86	Y53	146	Y113	206	Y173	266	Y233
27	V43	87	Y54	147	Y114	207	Y174	267	Y234
28	V12	88	Y55	148	Y115	208	Y175	268	Y235
29	V0	89	Y56	149	Y116	209	Y176	269	Y236
30	NC	90	Y57	150	Y117	210	Y177	270	Y237
31	NC	91	Y58	151	Y118	211	Y178	271	Y238
32	NC	92	Y59	152	Y119	212	Y179	272	Y239
33	NC	93	Y60	153	Y120	213	Y180	273	Y240
34	Y1	94	Y61	154	Y121	214	Y181	274	NC
35	Y2	95	Y62	155	Y122	215	Y182	275	NC
36	Y3	96	Y63	156	Y123	216	Y183	276	NC
37	Y4	97	Y64	157	Y124	217	Y184		
38	Y5	98	Y65	158	Y125	218	Y185		
39	Y6	99	Y66	159	Y126	219	Y186		
40	Y7	100	Y67	160	Y127	220	Y187		
41	Y8	101	Y68	161	Y128	221	Y188		
42	Y9	102	Y69	162	Y129	222	Y189		
43	Y10	103	Y70	163	Y130	223	Y190		
44	Y11	104	Y71	164	Y131	224	Y191		
45	Y12	105	Y72	165	Y132	225	Y192		
46	Y13	106	Y73	166	Y133	226	Y193		
47	Y14	107	Y74	167	Y134	227	Y194		
48	Y15	108	Y75	168	Y135	228	Y195		
49	Y16	109	Y76	169	Y136	229	Y196		

6. PIN DESCRIPTION

Pin Name	SEGMENT MODE	COMMON MODE
VDD	This is the logic system power supply pin.	
VSS	Ground pin	
V0, V12, V43, V5	These are the power supply pins for LC driving voltage. Normally, the bias voltages used are set by a resistor divider. Voltage level must be set such that $VSS \leq V_5 \leq V_{43} \leq V_{12} \leq V_0$. Refer to Section 8 for more details.	
S/C	This pin switches the driver between Segment and Common mode. It should be set to H when segment mode is used. It should be set to L when common mode is used.	
MD	This is for the selection of input interface. When MD is set to H, 4-bit parallel input mode is selected. When MD is set to L, 8-bit parallel input mode is selected. The relationship between display data and driver output is shown in Table 8 and Table 9.	This is for the selection between Single mode and Dual mode operation. When MD is set to L, Single mode operation is selected. When MD is set to H, Dual mode operation is selected. In Single mode, the internal shift register will work as a 240-bit one. The scan pulse will run between Y1 to Y240. In Dual mode, the internal shift register will be divided into two independent half, each with 120 bits. Two independent scan pulses are allowed running simultaneously. One scan pulse run between Y1 to Y120 and the other run between Y121 to Y240. This makes the chip effectively work like two 120 channels common driver, which and thus allowing split screen application. Application examples can be found in Figure 12 to Figure 15.

Pin Name	SEGMENT MODE	COMMON MODE
L/R	L/R selects the scan direction of display data output. When L/R is set to L, data is read sequentially at the direction of Y240 to Y1. When L/R is set to H, data is read sequentially at the direction of Y1 to Y240. Refer to Table 8 and Table 9 for more illustration.	L/R selects shift direction of shift register. When L/R is set to L, data is shifted from Y240 to Y1. When L/R is set to H, data is shifted from Y1 to Y240. Refer to Table 10 for more illustration.
DISPOFF#	This is the display off control pin. When DISPOFF# is set to H, the input signal is level-shifted from logic voltage level to LCD driving voltage level and controls LCD drive circuit. When it is set to L, the contents stored in the line latch will be reset and Y1-Y240 will output V_5 level. However, data can still be read into data latch regardless of the condition of DISPOFF#. After the DISPOFF# function is cancelled, the driver will output deselected level (V_{12} or V_{43}, depends on the level of FR) until it encounters a falling edge of LP. DISPOFF# removal time must meet the AC characteristics shown in Table 14 and Table 15. Otherwise, the driver may not be able to output the correct data.	This is the display off control pin. When DISPOFF# is set to H, the input signal is level-shifted from logic voltage level to LCD driving voltage level and controls the LCD driving circuit. When it is set to L, the contents stored in the shift register will be reset and Y1-Y240 will output V_5. After the DISPOFF# function is cancelled, the driver will output deselected level (V_{12} or V_{43}, depends on the level of FR) until it encounters a falling edge of LP. DISPOFF# removal time must meet the AC characteristics shown in Table 16. Otherwise, the driver may not be able to output the correct data.
D0 – D7	These are display data input pins. For 4 bits operation, only D0 - D3 are used and D4 - D7 should be connected to either VDD or VSS.	D0 - D6 are not used in common mode. They should be tied to VSS. D7 is used as input pin in dual mode. Data is input starting from the 121st bit according to the data shift register.
XCK	This is the shift clock input pin. Data is read at the falling edge of the clock pulse.	It is not used in common mode. It should be connected to VSS or left open.
LP	This is the latch pulse input pin. Data is latched at the falling edge of the clock pulse.	This is the bi-directional shift register clock pulse input pin. Data is shifted at the falling edge of this clock pulse.

Pin Name	SEGMENT MODE	COMMON MODE
FR	FR is the AC signal input for LC driving waveform. Normally it is the frame inversion signal. The input signal is level-shifted from logic voltage level to LC driving voltage level to control the LC driving circuit. The output voltage of the LC driver output pins are set by the line latch / shift register output signal and the FR signal. Their relationship is shown in Table 6 and Table 7.	
EIO1, EIO2	These are the I/O pins for chip selection. When L/R is set to L, EIO1 will be the output and EIO2 will be the input. When L/R is set to H, EIO1 will be the input and EIO2 will be the output. After an LP signal is input and the EIO(input) is set to L, the chip will be selected. It will be deselected automatically after reading 240 bits of data. EIO(output) is normally H. It will only be pull L for one XCK cycle (from falling edge to falling edge of XCK) when 240 bits of data have been read. Refer to Figure 10 for details timing.	These are the bi-directional shift register shift data I/O pin. When L/R is set to L, EIO1 will be the output and EIO2 will be the input. When L/R is set to H, EIO1 will be the input and EIO2 will be the output. A YD signal (Vertical scanning start pulse) is expected at the EIO(input). A H level at EIO(input) during LP falling edge indicates the start of a vertical frame. Refer to Figure 11 for details timing.
Y1-Y240	These are LC driver output pins. The output level can be referred Table 6 and Table 7.	

Note: Logic H means VDD level
Logic L means VSS level

7. FUNCTIONAL BLOCK DESCRIPTIONS

Active control

In segment mode, this block controls the selection of the chip.

Following an LP signal input, and after the chip select signal is input, a select signal is generated internally until 240 bits of data have been read in.

Once the data input is completed, a selection signal for cascade connection will be output and the chip will be deselected.

In common mode, this block controls the input/output data of bi-directional pins.

Data Control

When the chip is in segment mode with 4-bit parallel mode enable, this block collects one 4-bit data and transfers the data to Data Latch block in 4-bit format.

When the chip is in segment mode with 8-bit parallel mode enable, this block collects one 8-bit data every XCK cycle and transfers the data to Data Latch block in 8-bit format.

This block has no function in common mode.

Data Latch

This block is only active in segment mode. It latches the data on the data bus which used to determine the output level of each output pins. The latched state of each LC driver output pin is controlled by the Data latch control.

Data Latch Control

This block is only active in segment mode.

There are 30 data latch unit in the chip. Each can store two 4-bit data. Data latch control determines which of the data latch unit should receive the data from Data Control block.

The shift direction is controlled by the Control Logic block. After reading every 4 or 8 bits of data (depending on 4-bit or 8-bit parallel mode), the selection signal will shift one bit to next data latch based on the state of the control circuit logic.

Line Latch/Shift Register

In segment mode, it simultaneously latches all 240 bits of data into data latch at the falling edge of the LP signal and output to the level shift block.

In common mode, it shifts data from the data input pin by one bit at the falling edge of the LP signal.

Level Shifter

The logic voltage signal is level-shifted to the LCD driving voltage level and outputs to the driver block.

4-level Driver

This block is used to output appropriate LCD driving voltage level (V_0, V_{12}, V_{43}, V_5) based on the combinations of S/C, FR and DISPOFF# signals and the data from the line latch or shift register.

Control Logic

This block controls the operation of other blocks. In segment mode, when a LP pulse has been input, it controls the Line latch to latches 240 bits data simultaneously and then resets the Data latch control block.

In common mode, this block controls the direction of data shift.

Power on reset

Reset all blocks during power on. All outputs (Y1 – Y240) will be set to deselect level.

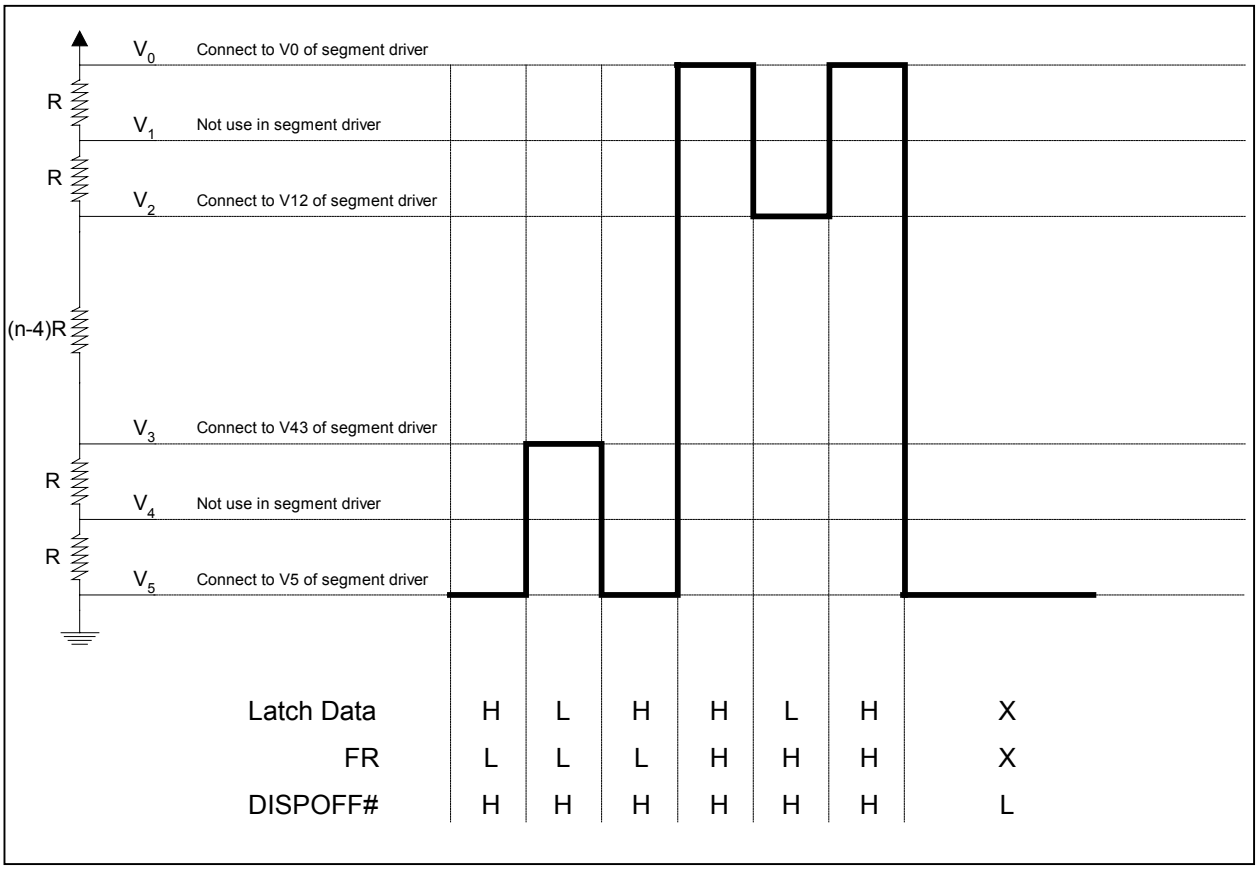
8. FUNCTIONAL OPERATIONS

Output voltage level mapping

Table 6 - Output level truth table for segment mode

FR	Latch Data	DISPOFF#	Driver output voltage level
L	L	H	V_{43}
L	H	H	V_5
H	L	H	V_{12}
H	H	H	V_0
X	X	L	V_5

Figure 7 - Illustration of output voltages in segment mode



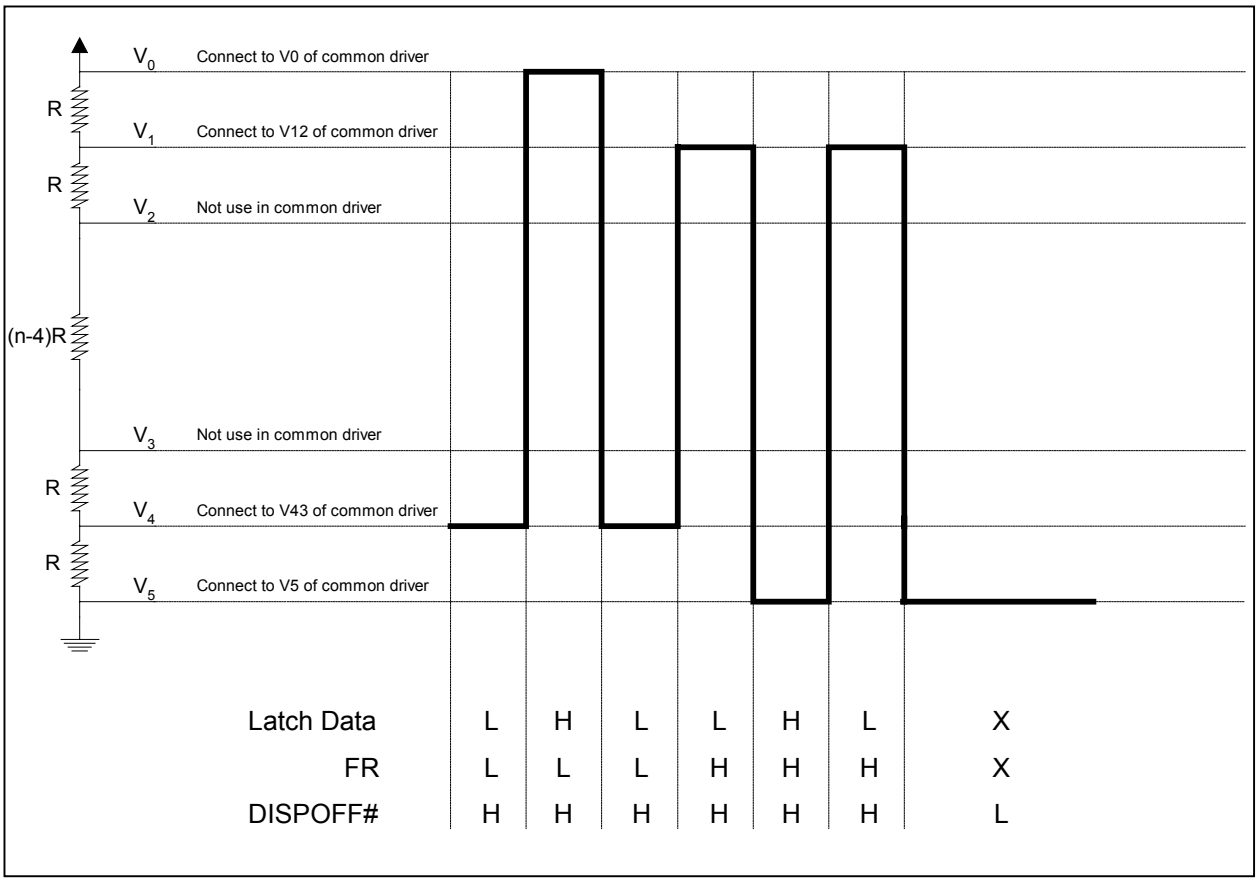
Remark:

- In segment mode, the voltage levels V_1 and V_4 are not used. V_{12} pin should be connected to voltage level V_2 and V_{43} pin should be connected to voltage level V_3.
- 1/n bias is assumed
- $VSS \le V_5 \le V_4 \le V_3 \le V_2 \le V_1 \le V_0$
- H: VDD; L: VSS; X: Don't care. These pins should be tied to either H or L and avoided from floating.

Table 7 - Output level truth table for common mode

FR	Latch Data	DISPOFF#	Driver output voltage level
L	L	H	V_{43}
L	H	H	V_0
H	L	H	V_{12}
H	H	H	V_5
X	X	L	V_5

Figure 8 - Illustration of output voltages in common mode



Remark:

- In segment mode, the voltage levels V_2 and V_3 are not used. V_{12} pin should be connected to voltage level V_1 and V_{43} pin should be connected to voltage level V_4.
- 1/n bias is assumed
- $VSS \le V_5 \le V_4 \le V_3 \le V_2 \le V_1 \le V_0$
- H: VDD; L: VSS; X: Don't care. These pins should be tied to either H or L and avoided from floating.

9. DISPLAY DATA AND DRIVER OUTPUT PINS MAPPING

Table 8 – 4-bit parallel, Segment Mode

MD	L/R	EIO1	EIO2	Data Input	Number of clock						
					1st	2nd	3rd	…	58th	59th	60th
H	L	Output	Input	D0	Y237	Y233	Y229	…	Y9	Y5	Y1
				D1	Y238	Y234	Y230	…	Y10	Y6	Y2
				D2	Y239	Y235	Y231	…	Y11	Y7	Y3
				D3	Y240	Y236	Y232	…	Y12	Y8	Y4
H	H	Input	Output	D0	Y4	Y8	Y12	…	Y232	Y236	Y240
				D1	Y3	Y7	Y11	…	Y231	Y235	Y239
				D2	Y2	Y6	Y10	…	Y230	Y234	Y238
				D3	Y1	Y5	Y9	…	Y229	Y233	Y237

Table 9 – 8-bit parallel, Segment Mode

MD	L/R	EIO1	EIO2	Data Input	Number of clock						
					1st	2nd	3rd	…	28th	29th	30th
L	L	Output	Input	D0	Y233	Y225	Y217	…	Y17	Y9	Y1
				D1	Y234	Y226	Y218	…	Y18	Y10	Y2
				D2	Y235	Y227	Y219	…	Y19	Y11	Y3
				D3	Y236	Y228	Y220	…	Y20	Y12	Y4
				D4	Y237	Y229	Y221	…	Y21	Y13	Y5
				D5	Y238	Y230	Y222	…	Y22	Y14	Y6
				D6	Y239	Y231	Y223	…	Y23	Y15	Y7
				D7	Y240	Y232	Y224	…	Y24	Y16	Y8
L	H	Input	Output	D0	Y8	Y16	Y24	…	Y224	Y232	Y240
				D1	Y7	Y15	Y23	…	Y223	Y231	Y239
				D2	Y6	Y14	Y22	…	Y222	Y230	Y238
				D3	Y5	Y13	Y21	…	Y221	Y229	Y237
				D4	Y4	Y12	Y20	…	Y220	Y228	Y236
				D5	Y3	Y11	Y19	…	Y219	Y227	Y235
				D6	Y2	Y10	Y18	…	Y218	Y226	Y234
				D7	Y1	Y9	Y17	…	Y217	Y225	Y233

Table 10 – Common Mode

MD	L/R	Data transfer direction	EIO1	EIO2	D7
L	L	Y240 → Y1	Output	Input	X
	H	Y1 → Y240	Input	Output	X
H	L	Y240 → Y121 Y120 → Y1	Output	Input	Input
	H	Y1 → Y120 Y121 → Y240	Input	Output	Input

Where H: VDD
L: VSS
X: Don't care. The pin should be tied to either H or L and avoided from floating.

10. PRECAUTION

This IC is a high voltage LC driver. If voltage is supplied to the LC driver power supply while the power supply of the logic system is floating, there may have high current flow inside the IC and permanently damaged the system.

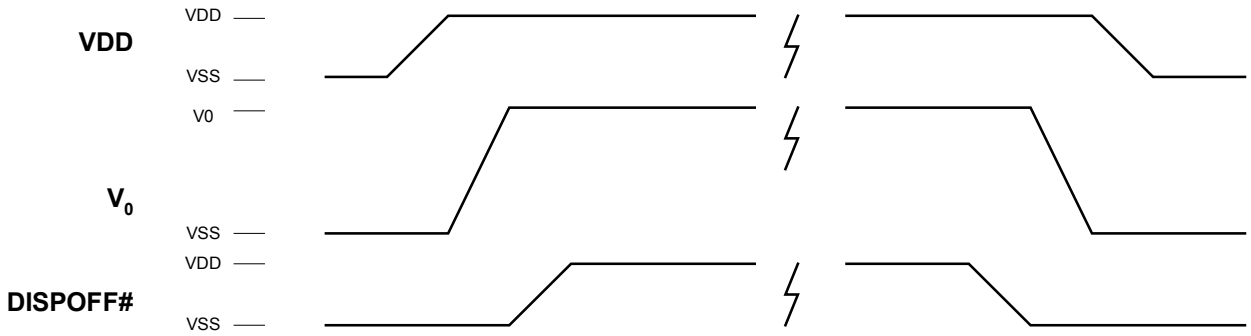
Besides, the logic condition inside IC is undefined when the logic power is just applied, therefore a DISPOFF# signal is suggested for resetting the IC.

The recommend power up and down sequence is as follow:

Power up:
- Provide power to the logic system (VDD, VSS)
- Pull DISPOFF# to L
- Provide the LCD driving power (V0, V12, V43, V5)
- DISPOFF# can then be pulled H for normal operation

Power down:
- Pull DISPOFF# to L
- Disconnect LCD driving power supply
- Disconnect Logic system power supply

Figure 9 – Recommended power up and down sequence



11. MAXIMUM RATINGS

Table 11 - Maximum Ratings (Voltage Referenced to VSS)

Symbol	Parameter	Value	Unit
VDD	Logic supply voltage	-0.3 to +4.0	V
V_0	LC driving voltage supply	-0.3 to +32.0	V
V_{12}		-0.3 to + V_0+0.3	V
V_{43}		-0.3 to + V_0+0.3	V
V_5		-0.3 to + V_0+0.3	V
V_I	Input voltage	-0.3 to VDD+0.3	V
T_A	Operating Temperature	-30 to +85	°C
T_{STG}	Storage Temperature	-65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, it is recommended that V_{IN} and V_{OUT} be constrained to the range VSS ≤ (V_{IN} or V_{OUT}) ≤ VDD. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (e.g. either VSS or VDD). Unused outputs must be left open. All dummy and NC pins should be left open and unconnected. Do not group dummy or NC pins together. This device may be light sensitive. Caution should be taken to avoid exposed of this device to any light source during normal operation. This device is not radiation protected.

12. DC CHARACTERISTICS

SEGMENT MODE

Table 12 - DC Characteristics (Unless otherwise specified, voltage referenced to VSS, VDD = 2.4 to 3.6V, V_0=+15.0 to +30.0V, T_A = -30 to 85°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VDD	VDD operation voltage	-	2.4	-	3.6	V
V0	V0 operation voltage	-	15.0	-	30.0	V
I_{STB}	Stand-by current at VDD pin	VDD = +3.6V, V_0 = +30V, V1 = VSS, all input static	-	-	5	μA
I_{DD1}	Consumed current at VDD (Chip is in deselected stage, i.e. non data-taking)	VDD = +3.6V, V_0 = +30V, f_{XCK} = 20MHz, f_{LP} = 333kHz, f_{FR}=1389Hz, No-load, EIO(input)=VDD, 4-bit mode, D0-D4 switch at every XCK cycle	-	450	900	μA
I_{DD2}	Consumed current at VDD (Chip is in selected stage, i.e. data-taking)	VDD = +3.6V, V_0 = +30V, f_{XCK} = 20MHz, f_{LP} = 333kHz, f_{FR}=1389Hz, No-load, EIO(input)=VSS, 4-bit mode, D0-D4 switch at every XCK cycle	-	750	1500	μA
I_O	Consumed current at V0	VDD = +3.6V, V_0 = +30V, f_{XCK} = 20MHz, f_{LP} = 333kHz, f_{FR}=1389Hz, No-load, EIO(input)=VSS, 4-bit mode, D0-D4 switch at every XCK cycle	-	-	2.5	mA
V_{IH}	Input voltage at D0-D7, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2, DISPOFF#		0.8xVDD	-	-	V
V_{IL}			-	-	0.2xVDD	V
V_{OH}	Output voltage at EIO1, EIO2	I_{OH} = -0.4mA	0.9xVDD	-	-	V
V_{OL}		I_{OL} = +0.4mA	-	-	0.1xVDD	V
IL_{IH}	Input leakage current at D0-D7, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2, DISPOFF#	V_I = VDD	-	-	5	μA
IL_{IL}		V_I = VSS	-	-	5	μA
R_{ON}	Output resistance	$\|\Delta V_{ON}\|$ = 0.5V, V_0 = +30V	-	1.1	1.5	kΩ
		$\|\Delta V_{ON}\|$ = 0.5V, V_0 = +20V	-	1.1	2.0	kΩ

COMMON MODE

Table 13 - DC Characteristics (Unless otherwise specified, voltage referenced to VSS, VDD = 2.4 to 3.6V, V_0=+15.0 to +30.0V, T_A = -30 to 85°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VDD	VDD operation voltage	-	2.4	-	3.6	V
V0	V0 operation voltage	-	15.0	-	30.0	V
I_{STB}	Stand-by current at VDD pin	VDD = +3.6V, V_0 = +30V, V_I = VSS, all input static	-	-	5.0	μA
I_{DD1}	Consumed current at VDD pin	VDD = +3.6V, V_0 = +30V, f_{LP} = 333kHz, f_{FR}=1389Hz, 1/240 duty operation, No-load	-	15	100	μA
I_O	Consumed current at V0 pin	VDD = +3.6V, V0 = +30V, f_{LP} = 333kHz, f_{FR}=1389Hz, 1/240 duty operation, No-load	-	-	500	μA
V_{IH}	Input voltage at D0-D7, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2, DISPOFF#		0.8xVDD	-	-	V
V_{IL}			-	-	0.2xVDD	V
V_{OH}	Output voltage at EIO1, EIO2	I_{OH} = -0.4mA	0.9xVDD	-	-	V
V_{OL}		I_{OL} = +0.4mA	-	-	0.1xVDD	V
IL_{IH}	Input leakage current at D0-D7, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2, DISPOFF#	V_I = VDD	-	-	5	μA
IL_{IL}		V_I = VSS	-	-	5	μA
R_{ON}	Output resistance at Y1-Y240	ΔV_{ON} = 0.5V, V_0 = +30V	-	1.1	1.5	kΩ
		ΔV_{ON} = 0.5V, V_0 = +20V	-	1.1	2.0	kΩ

13. AC CHARACTERISTICS

SEGMENT MODE

Table 14 - Interface Timing Characteristics (Unless otherwise specified, voltage referenced to VSS, VDD = +3.0 to +3.6V, V_0=+15.0 to +30.0V, T_A = -30 to 85°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
T_{WCK}	Shift clock period (1)	T_R, $T_F \leq$ 10ns	50	-	-	ns
T_{WCKH}	Shift clock H pulse width	-	15	-	-	ns
T_{WCKL}	Shift clock L pulse width	-	15	-	-	ns
T_{DS}	Data setup time	-	10	-	-	ns
T_{DH}	Data hold time	-	12	-	-	ns
T_{WLPH}	Latch pulse H pulse width	-	15	-	-	ns
T_{LD}	Shift clock rise to Latch pulse rise time	-	0	-	-	ns
T_{SL}	Shift clock fall to Latch pulse fall time	-	25	-	-	ns
T_{LS}	Latch pulse rise to Shift clock rise time	-	25	-	-	ns
T_{LH}	Latch pulse fall to Shift pulse fall time	-	25	-	-	ns
T_R	Input signal rise time (2)	-	-	-	50	ns
T_F	Input signal fall time (2)	-	-	-	50	ns
T_S	Enable setup time	-	10	-	-	ns
T_{SD}	DISPOFF# removal time	-	100	-	-	ns
T_{WDL}	DISPOFF# L pulse width	-	1.2	-	-	µs
T_D	Output delay time1	CL = 15pF	-	-	30	ns
T_{PD1}, T_{PD2}	Output delay time 2	CL = 15pF	-		400	ns
T_{PD3}	Output delay time 3	CL = 15pF	-	-	400	ns

Note:

(1) Take the cascade connection into consideration
(2) $(T_{CK}-T_{WCKH}-T_{WCKL})/2$ is maximum in the case of high speed operation.

SEGMENT MODE

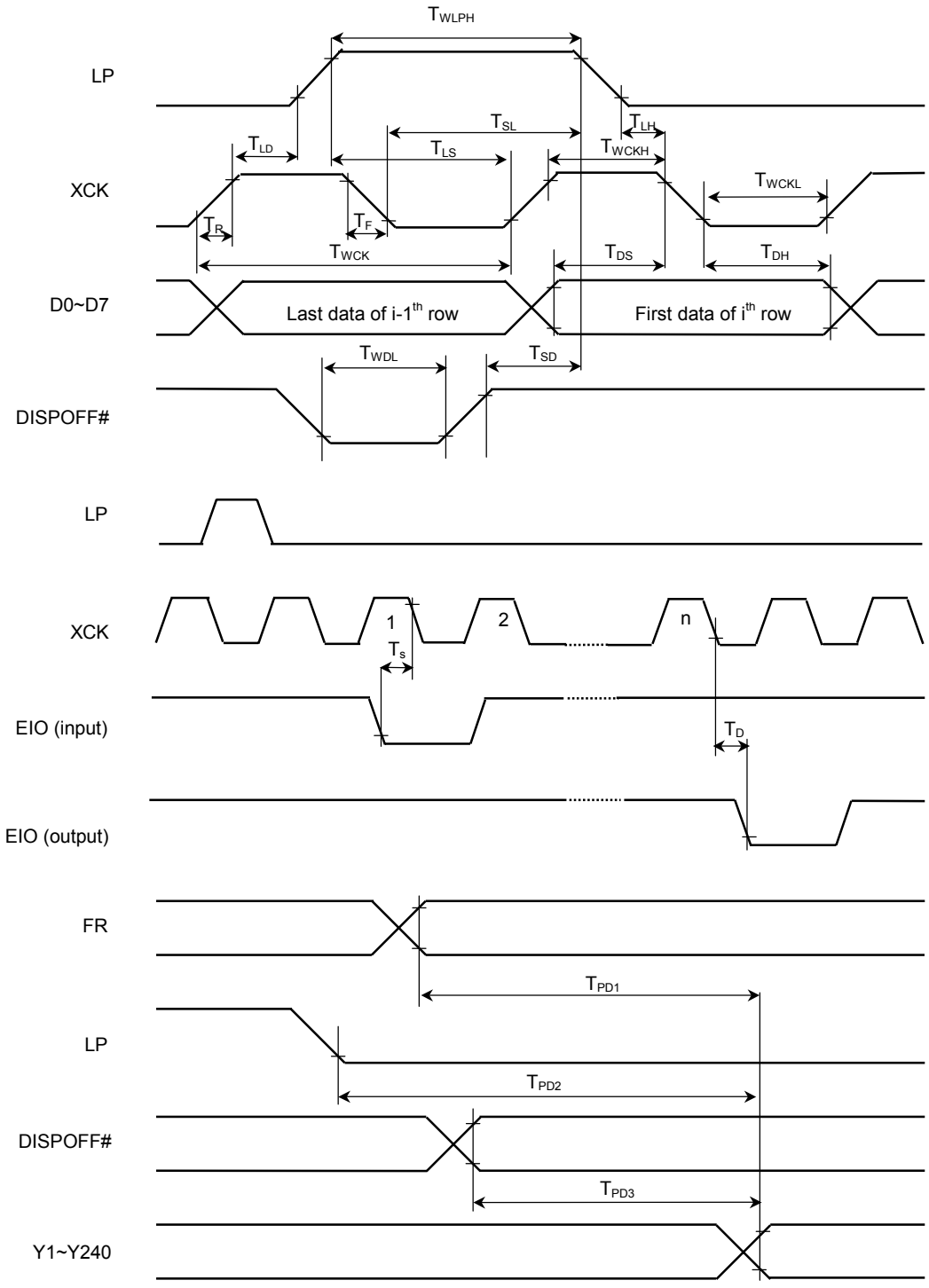
Table 15 - Interface Timing Characteristics (VDD – VSS = +2.4 to +3.0V, V0=+15.0 to +30.0V, T_A = -35 to 85°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
T_{WCK}	Shift clock period (1)	T_R, $T_F \leq$ 10ns	66	-	-	ns
T_{WCKH}	Shift clock H pulse width	-	23	-	-	ns
T_{WCKL}	Shift clock L pulse width	-	23	-	-	ns
T_{DS}	Data setup time	-	15	-	-	ns
T_{DH}	Data hold time	-	23	-	-	ns
T_{WLPH}	Latch pulse H pulse width	-	30	-	-	ns
T_{LD}	Shift clock rise to Latch pulse rise time	-	0	-	-	ns
T_{SL}	Shift clock fall to Latch pulse fall time	-	50	-	-	ns
T_{LS}	Latch pulse rise to Shift clock rise time	-	30	-	-	ns
T_{LH}	Latch pulse fall to Shift pulse fall time	-	30	-	-	ns
T_R	Input signal rise time (2)	-	-	-	50	ns
T_F	Input signal fall time (2)	-	-	-	50	ns
T_S	Enable setup time	-	15	-	-	ns
T_{SD}	DISPOFF# removal time	-	100	-	-	ns
T_{WDL}	DISPOFF# L pulse width	-	1.2	-	-	µs
T_D	Output delay time1	CL = 15pF	-	-	41	ns
T_{PD1}, T_{PD2}	Output delay time 2	CL = 15pF	-	-	400	µs
T_{PD3}	Output delay time 3	CL = 15pF	-	-	400	µs

Note:

(1) Take the cascade connection into consideration
(2) $(T_{CK}-T_{WCKH}-T_{WCKL})/2$ is maximum in the case of high speed operation.

Figure 10 – Timing characteristics of SSD1702 in Segment mode



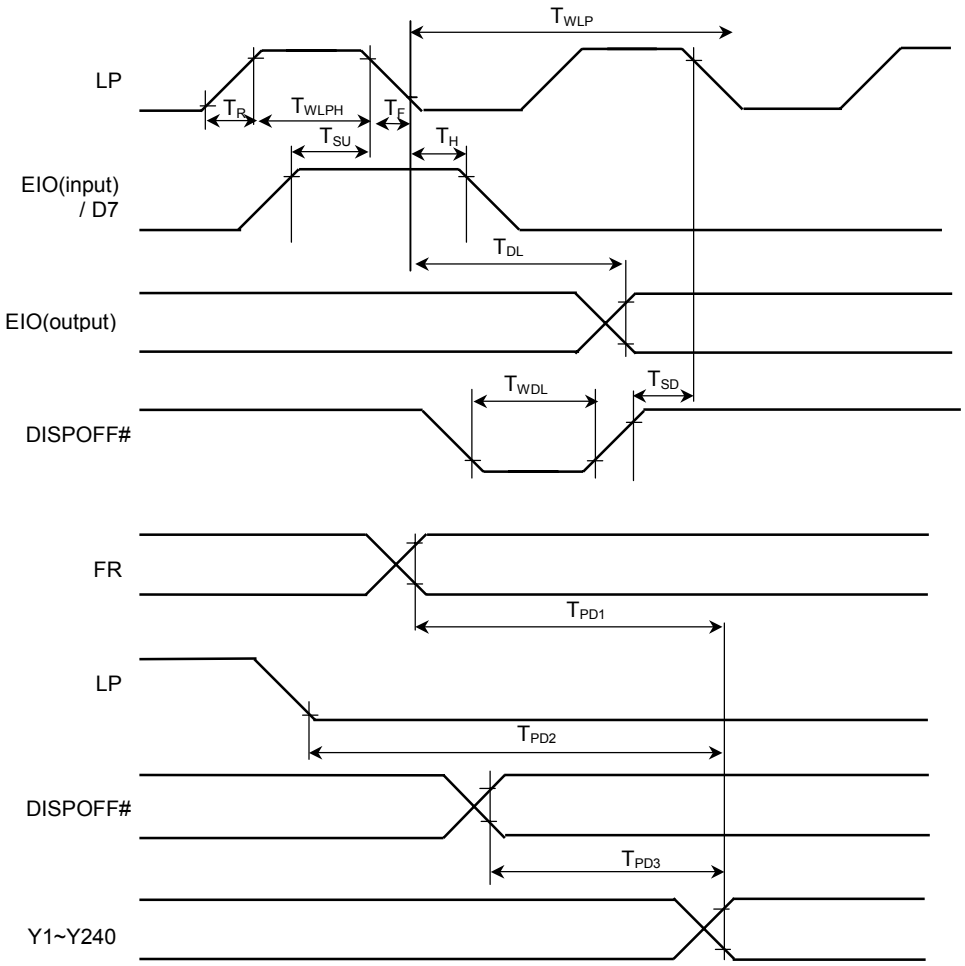
In 4-bit mode, n = 240/4 = 60
In 8-bit mode, n = 240/8 = 30

COMMON MODE

Table 16 - Interface Timing Characteristics (VDD - VSS = +2.4 to +3.6V, V_0=+15.0 to +30.0V, T_A = -35 to 85°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
T_{WLP}	Shift clock period	T_R, $T_F \leq$ 20ns	250	-	-	ns
T_{WLPH}	Shift clock H pulse width	VDD = +3.0 to 3.6V	15	-	-	ns
		VDD = +2.4 to 3.0V	30	-	-	ns
T_{SU}	Data setup time	-	30	-	-	ns
T_H	Data hold time	-	50	-	-	ns
T_R	Input signal rise time	-	-	-	50	ns
T_F	Input signal fall time	-	-	-	50	ns
T_{SD}	DISPOFF# removal time	-	100	-	-	ns
T_{WDL}	DISPOFF# L pulse width	-	1.2	-	-	µs
T_{DL}	Output delay time (1)	C_L=15 pF	-	-	200	ns
T_{PD1},T_{PD2}	Output delay time (2)	C_L=15 pF	-	-	1.2	µs
T_{PD3}	Output delay time (3)	C_L=15 pF	-	-	1.2	µs

Figure 11 – Timing characteristics of SSD1702 in Common mode



14. APPLICATION EXAMPLES OF COMMON DRIVERS

Figure 12 – Application example of Single mode (L/R = L)

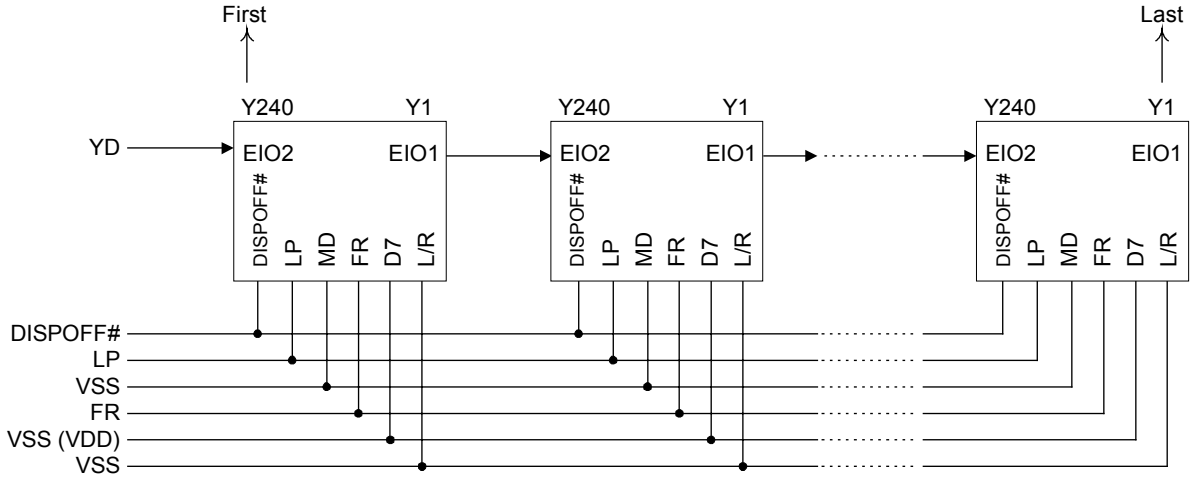


Figure 13 – Application example of Single mode (L/R = H)

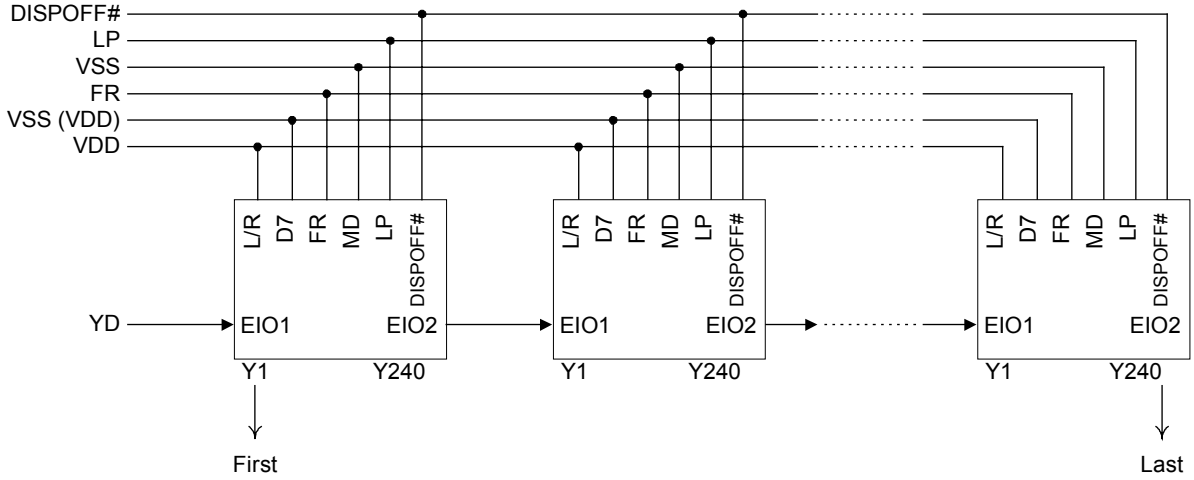


Figure 14 – Application example of Dual mode (L/R = L)

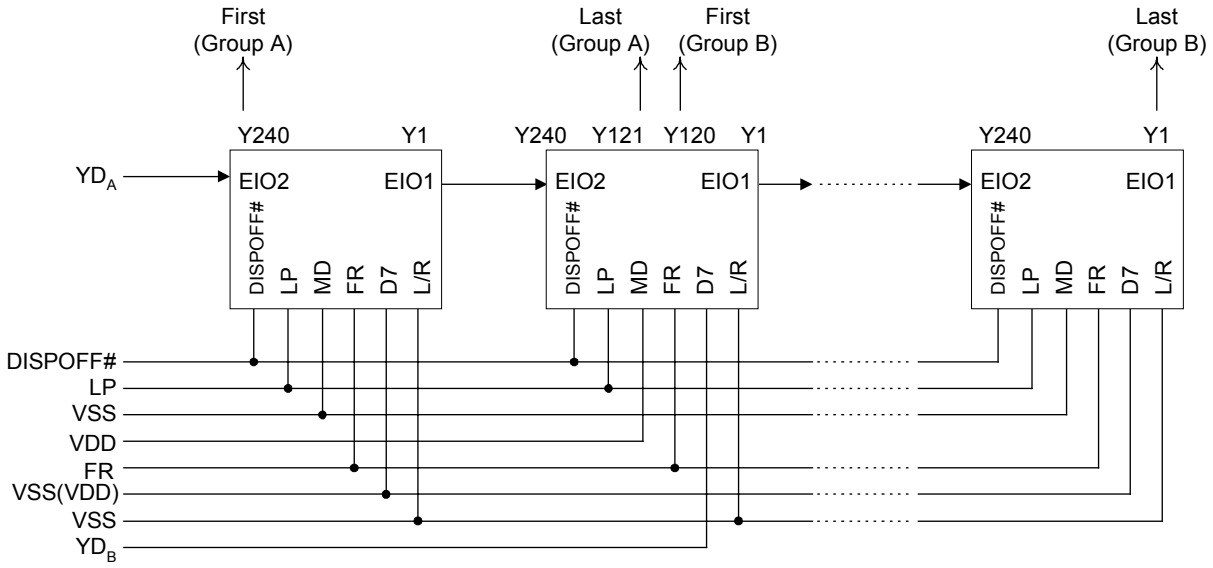
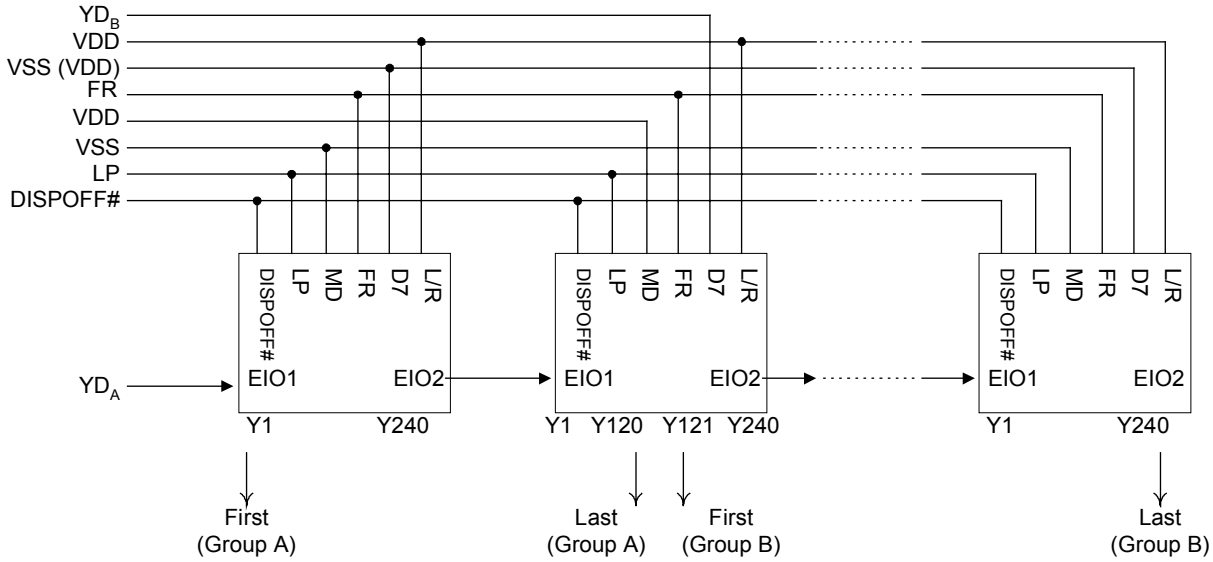


Figure 15 – Application example of Dual mode (L/R = H)



15. APPLICATION EXAMPLES OF SEGMENT DRIVERS

Figure 16 – Application example of Segment mode (L/R = L)

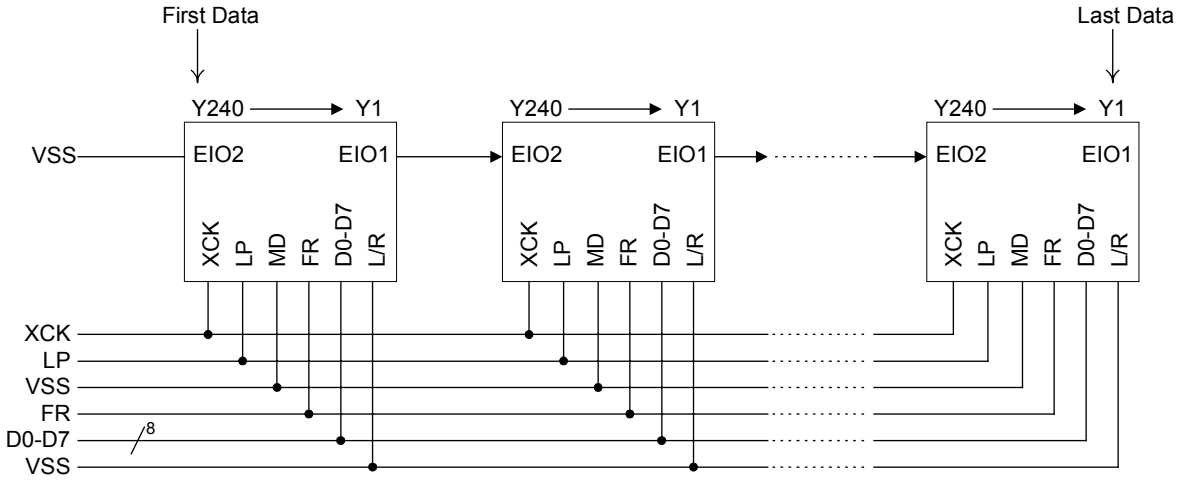
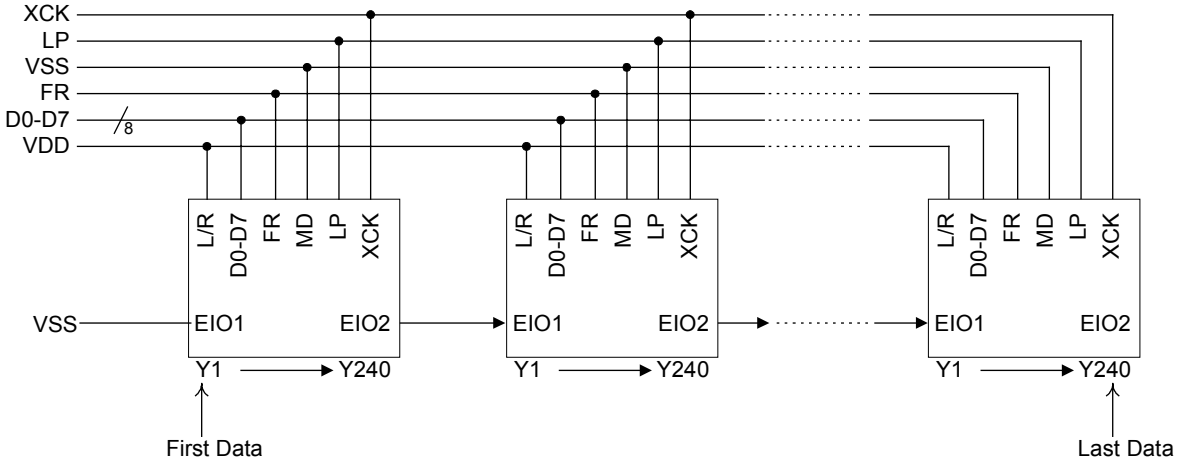
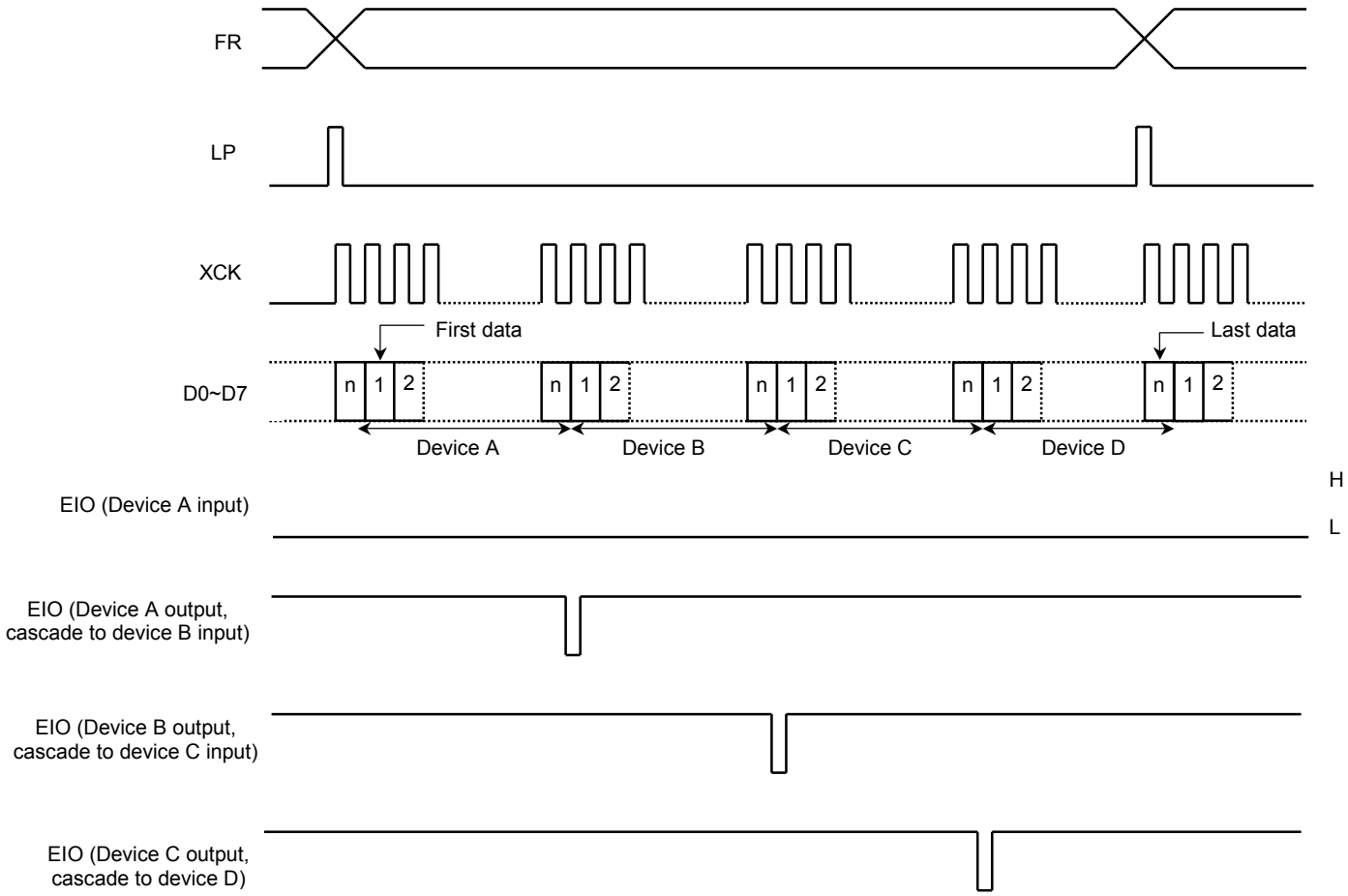


Figure 17 – Application example of Segment mode (L/R = H)



16. TIMING CHART OF CASCADE CONNECTION OF SEGMENT DRIVERS

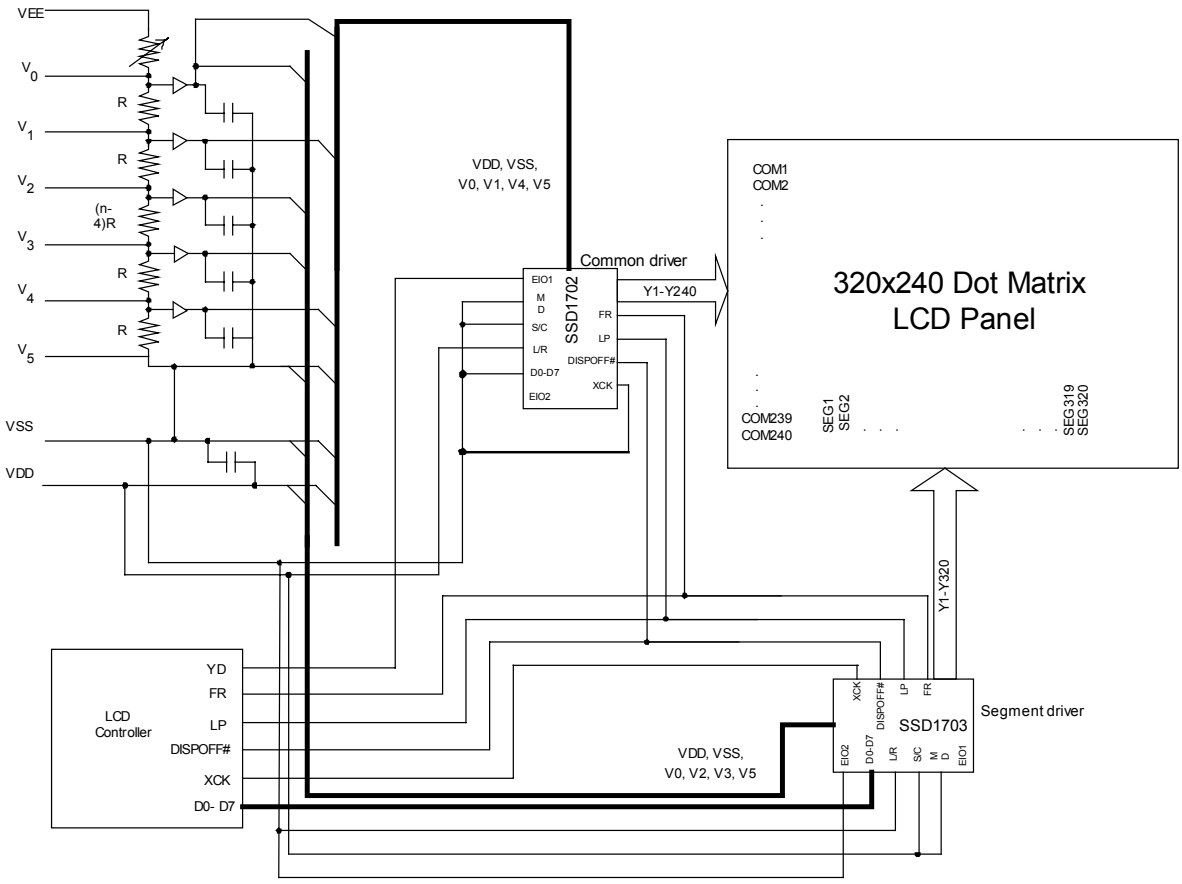
Figure 18 – Timing chart of cascade connection of segment drivers



In 4-bit mode, n = 240/4 = 60
In 8-bit mode, n = 240/8 = 30

17. APPLICATION EXAMPLES

Figure 19 – Typical configuration for 320x240 application



Remark:

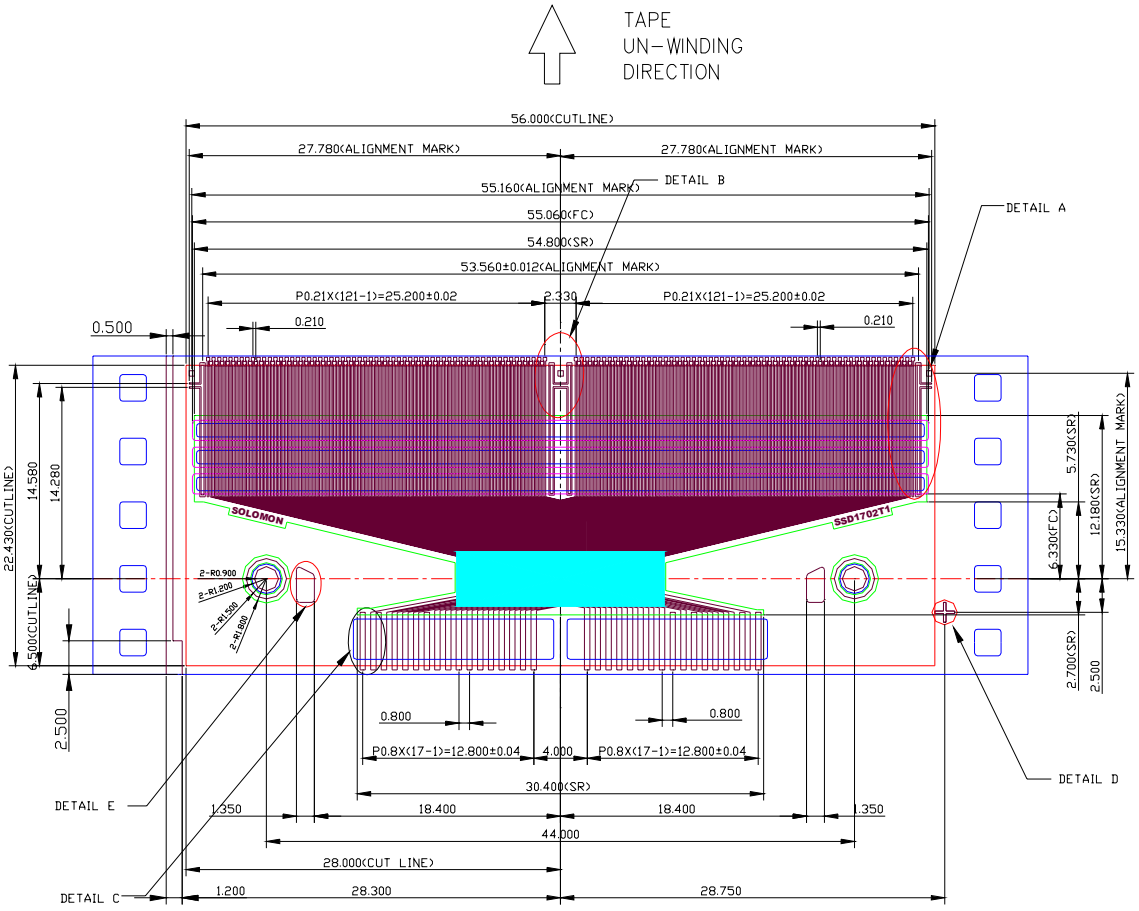
- The circuit is in 1/n bias

- $VSS \le V_5 \le V_4 \le V_3 \le V_2 \le V_1 \le V_0 \le V_{EE}$
- VEE is the maximum driving voltage allowed, which is equal to or above V_0.
- For common driver
    - V_0 should be connected to pin V_0
    - V_1 should be connected to pin V_{12}
    - V_4 should be connected to pin V_{43}
    - V_5 should be connected to pin V_5
- For segment driver
    - V_0 should be connected to pin V_0
    - V_2 should be connected to pin V_{12}
    - V_3 should be connected to pin V_{43}
    - V_5 should be connected to pin V_5

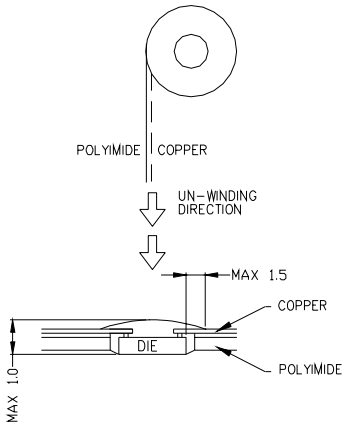
18. TAB PACKAGE DETAIL DIMENSIONS

SSD1702T1 TAB

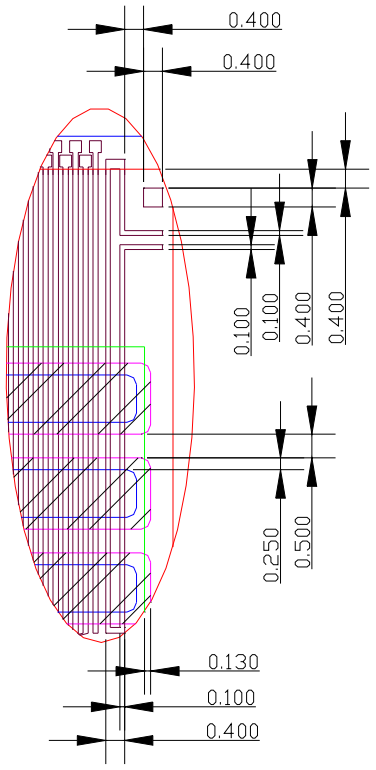
Figure 20 – SSD1702T1 TAB detail dimensions



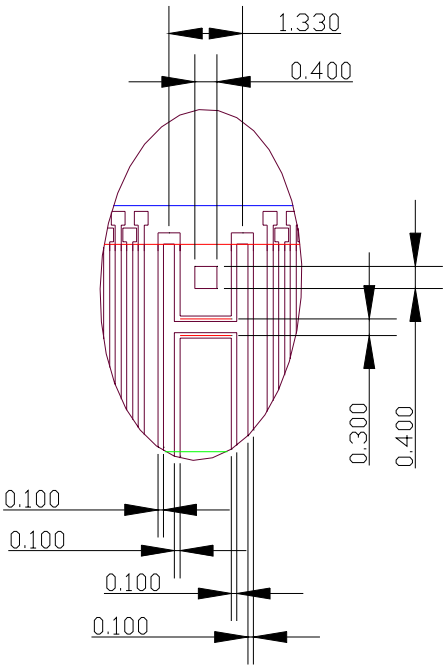
NOTE:
1. GENERAL TOLERANCE: ±0.05MM
2. MATERIAL
   PI: 75±6U
   CU: 18±5UM
   SR: 26±14UM
3. SN PLATING: 0.250±0.05UM
   (PURE TIN 0.18±0.05UM)
4. TAP SIZE: 5 SPH, 23.75MM



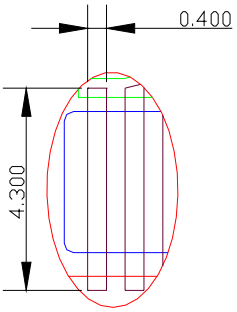
NORMAL DESIGN



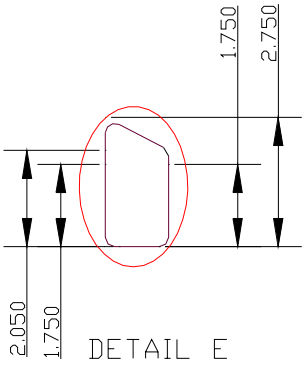
DETAIL A



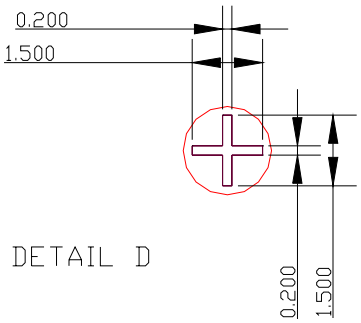
DETAIL B



DETAIL C



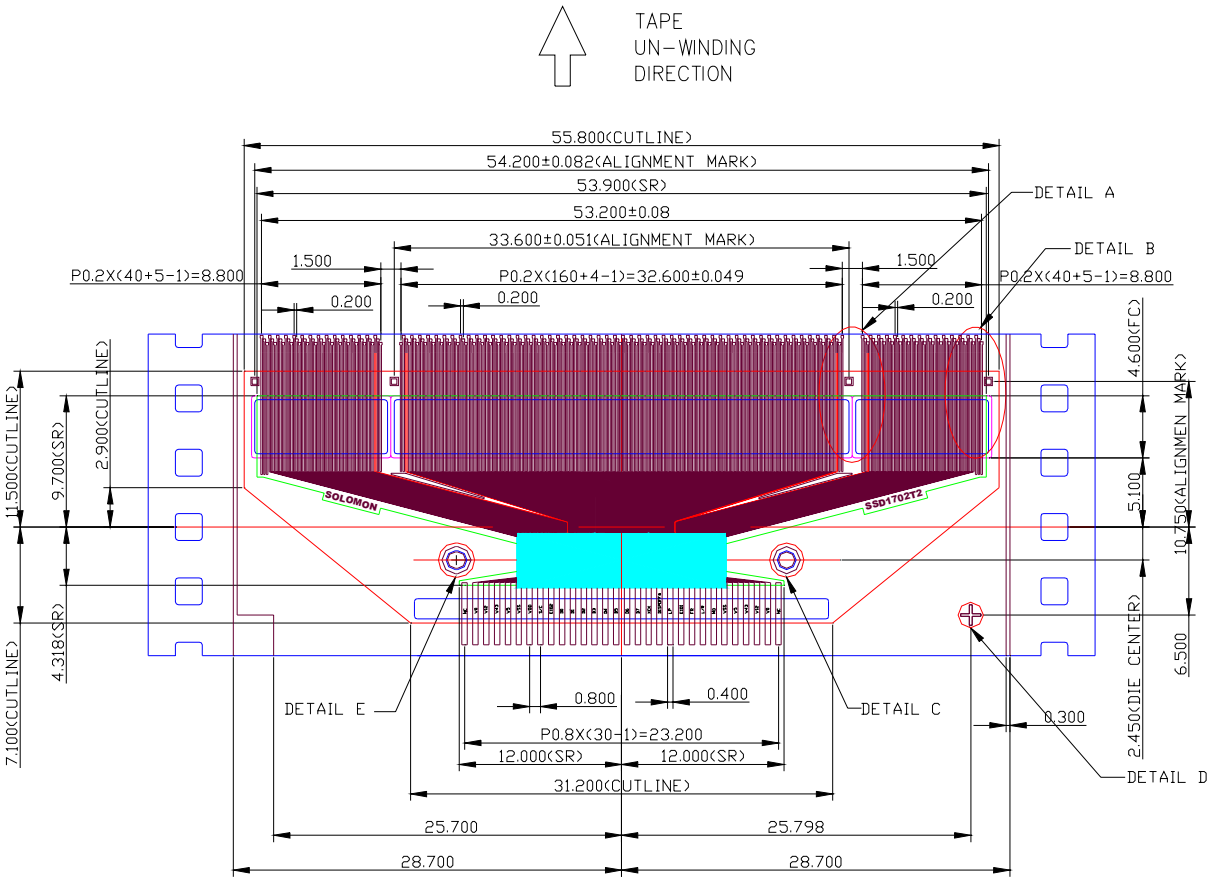
DETAIL E

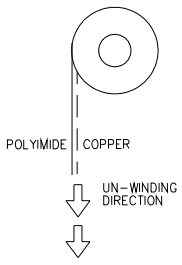


DETAIL D

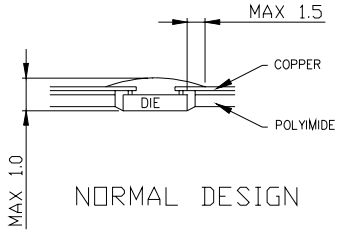
SSD1702T2 TAB

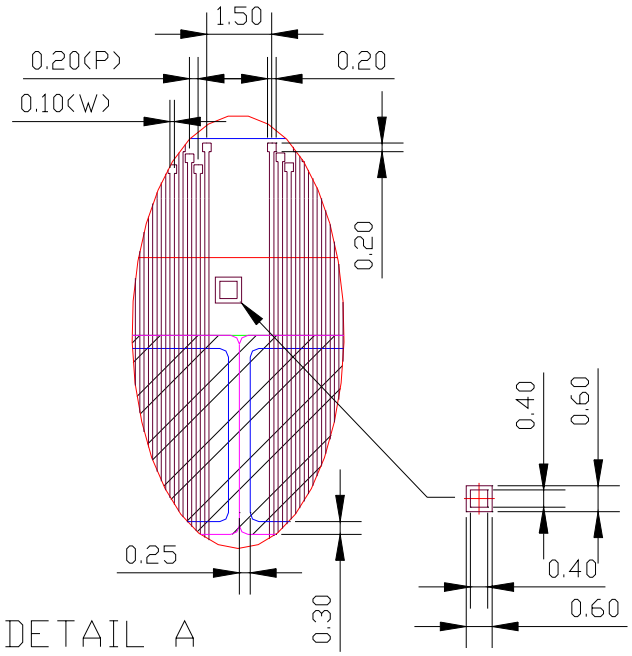
Figure 21 – SSD1702T2 TAB detail dimensions



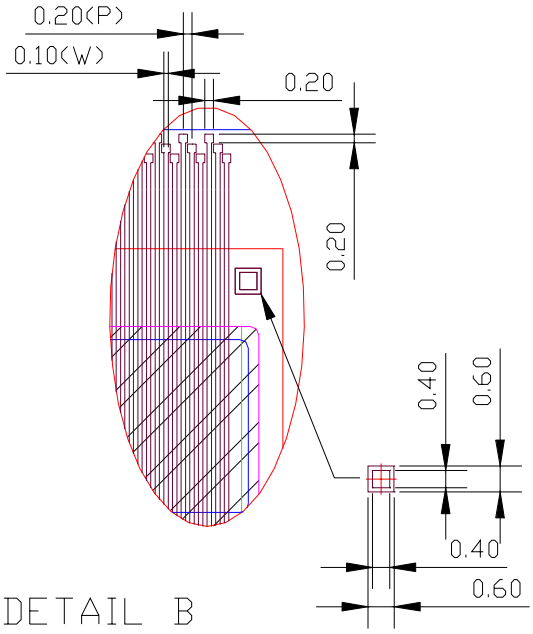


NOTE:
1. GENERAL TOLERANCE: ±0.05mm
2. MATERIAL
   PI: 38±4um
   CU: 12±2um
   SR: 15±10um
3. SN PLATING: PURE SN 0.18±0.05um
4. TAPSITE: 5 SPH, 23.75 mm

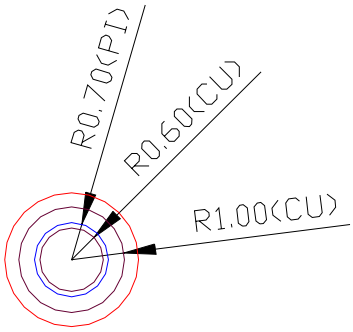




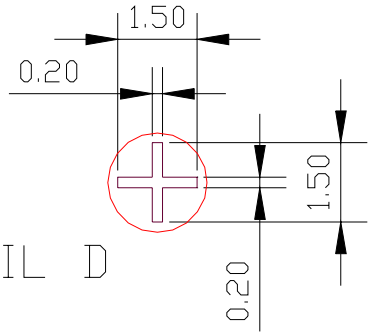
DETAIL A



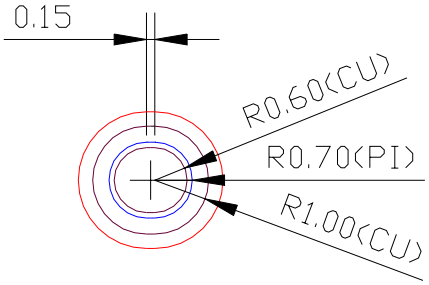
DETAIL B



DETAIL C



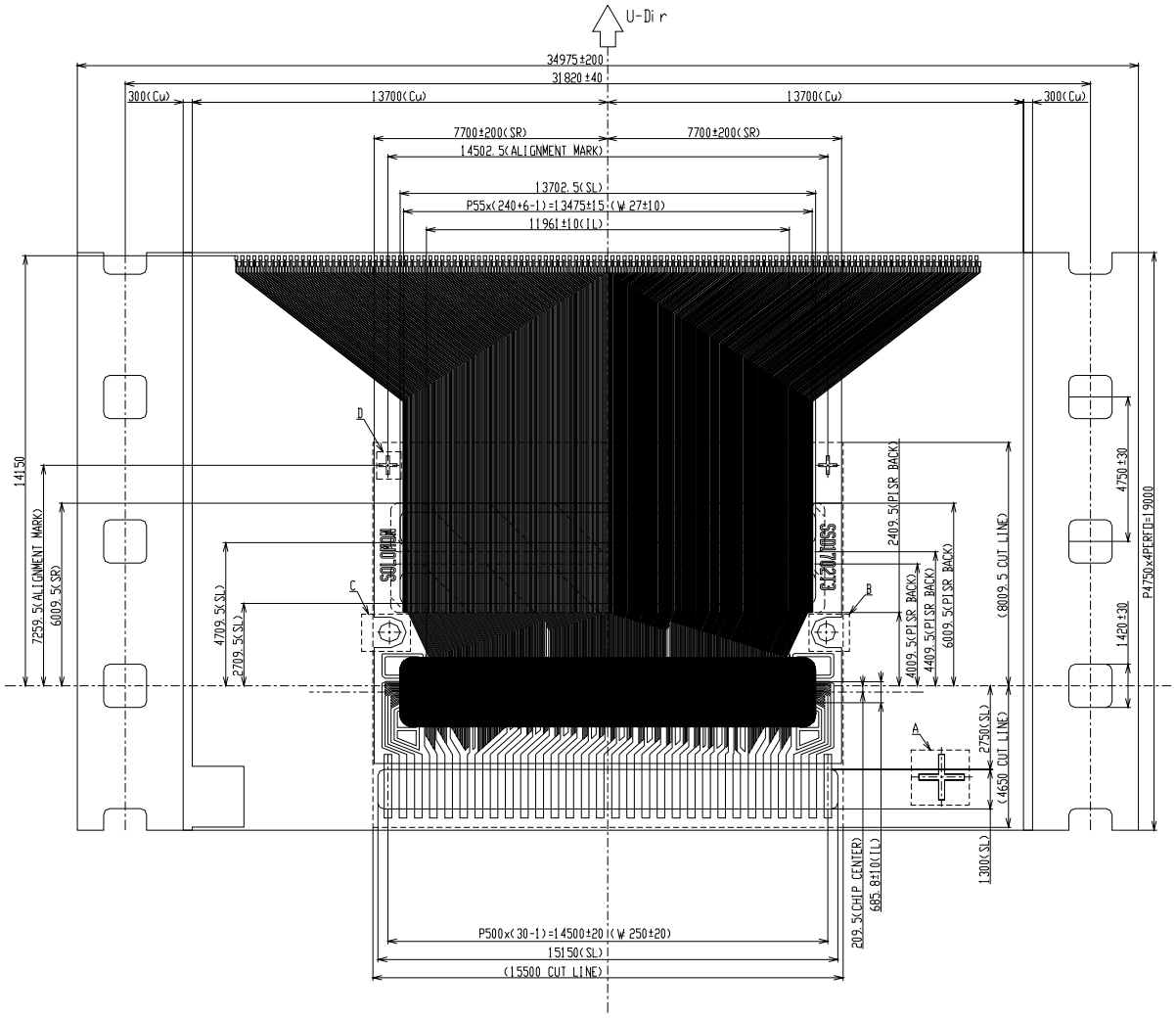
DETAIL D

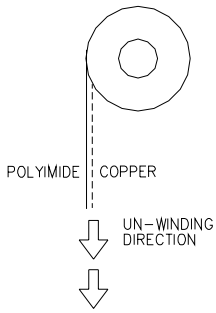


DETAIL E

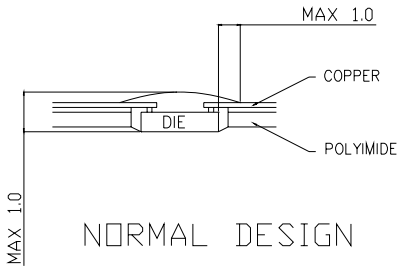
SSD1702T3 TAB

Figure 22 – SSD1702T3 TAB detail dimensions



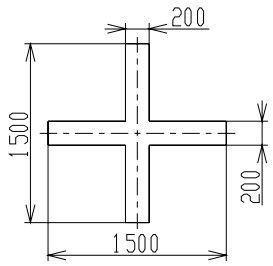


NOTE:
1. GENERAL TOLERANCE: ±0.05mm
2. MATERIAL
   PI: 38±4um
   CU: 12±2um
   SR: 15±10um
3. SN PLATING: PURE SN 0.18±0.05um
4. TAPSITE: 5 SPH, 23.75 mm

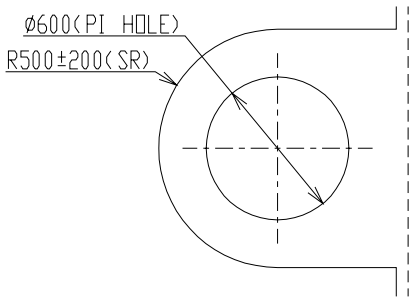


NORMAL DESIGN

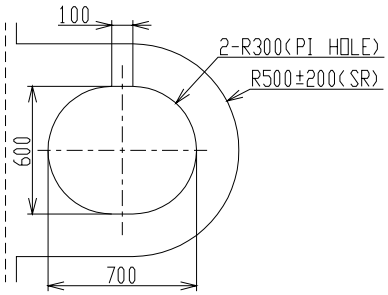
DETAIL A(20/1)



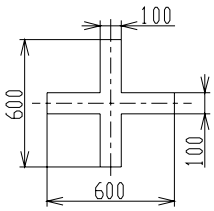
DETAIL B(40/1)



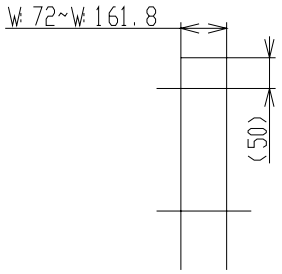
DETAIL C(40/1)



DETAIL D(40/1)



DETAIL E(100/1)



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