GOOD-ARK SEMICONDUCTOR

SSF3415

20V P-Channel MOSFET

Main Product Characteristics

$V_{(BR)DSS}$	-20V
$R_{DS(ON)}$MAX	50mΩ@-4.5V
	60mΩ@-2.5V
	73mΩ@-1.8V
I_D	-4 A

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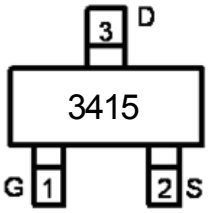
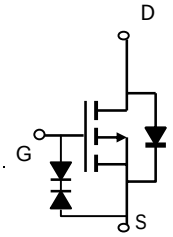


Marking and Pin Assignment



Schematic Diagram

Features and Benefits

- Advanced MOSFET process technology
- Ideal for DC-DC converter, power management in portable battery, computer, printer, cellular and general purpose applications
- Low on-resistance with low gate charge
- Fast switching and reverse body recovery

Description

The SSF3415 utilizes the latest techniques to achieve high cell density and low on-resistance. These features make this device extremely efficient and reliable for use in high efficiency switch mode power supply and a wide variety of other applications.

Absolute Maximum Ratings (T_A=25°C unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	±8	
Continuous Drain Current (t≤10S)	I_D	-4.0	A
Maximum Power Dissipation (t≤10S)	P_D	0.35	W
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	357	°C/W
Operating Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics (T_A=25°C unless otherwise specified)

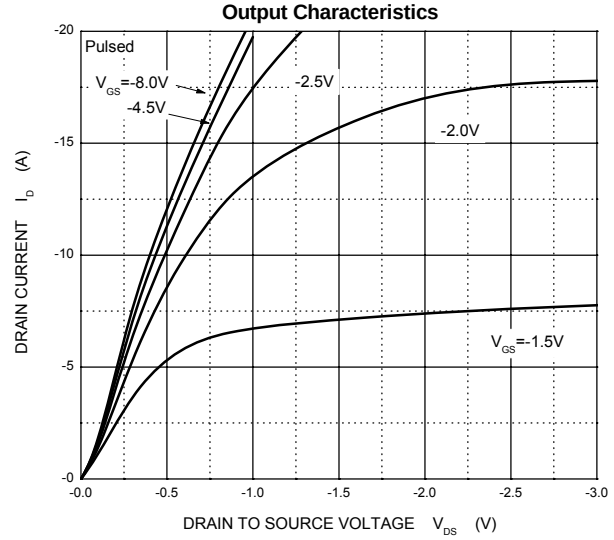
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static Parameters						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D =-250μA	-20			V
Gate threshold voltage	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =-250μA	-0.3	-0.56	-1	
Gate-body leakage current	I_{GSS}	V_{DS} =0V, V_{GS} =±8V			±10	μA
		V_{DS} =0V, V_{GS} =±4.5V			±1	
Zero gate voltage drain current	I_{DSS}	V_{DS} =-16V, V_{GS} =0V			-1	
Drain-source on-state resistance(note1)	$R_{DS(ON)}$	V_{GS} =-4.5V, I_D =-4A		0.037	0.050	Ω
		V_{GS} =-2.5V, I_D =-4A		0.045	0.060	
		V_{GS} =-1.8V, I_D =-2A		0.056	0.073	
Forward transconductance(note2)	g_{FS}	V_{DS} =-5V, I_D =-4A	8			S
Body diode voltage(note2)	V_{SD}	I_S=-1A,V_{GS} =0V			-1	V
Dynamic Parameters						
Input capacitance	C_{iss}	V_{DS} =-10V,V_{GS} =0V,f =1MHz		1450		pF
Output capacitance	C_{oss}			205		
Reverse transfer capacitance	C_{rss}			160		
Gate resistance	R_g	V_{DS} =0V,V_{GS} =0V,f =1MHz		6.5		Ω
Switching Parameters						
Total gate charge	Q_g	V_{DS} =-10V,V_{GS} =-4.5V,I_D =-4A		17.2		nC
Gate-Source charge	Q_{gs}			1.3		
Gate-drain charge	Q_{gd}			4.5		
Turn-on delay time (note3)	$t_{d(on)}$	V_{DS}=-10V, V_{GS}=-4.5V R_{GEN} =3Ω, R_L=2.5Ω,		9.5		nS
Turn-on rise time(note3)	t_r			17		
Turn-off delay time(note3)	$t_{d(off)}$			94		
Turn-off fall time(note3)	t_f			35		

Notes:

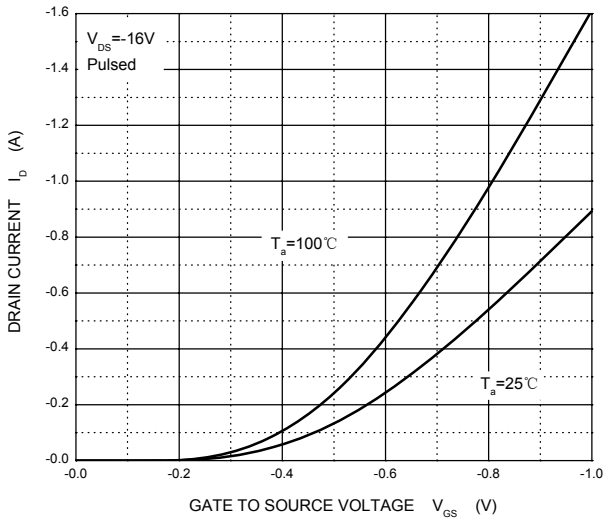
1. Repetitive rating,pulse width limited by junction temperature.
2. Pulse Test : Pulse width≦300μS, duty cycle≦2%.

Typical Electrical and Thermal Characteristics

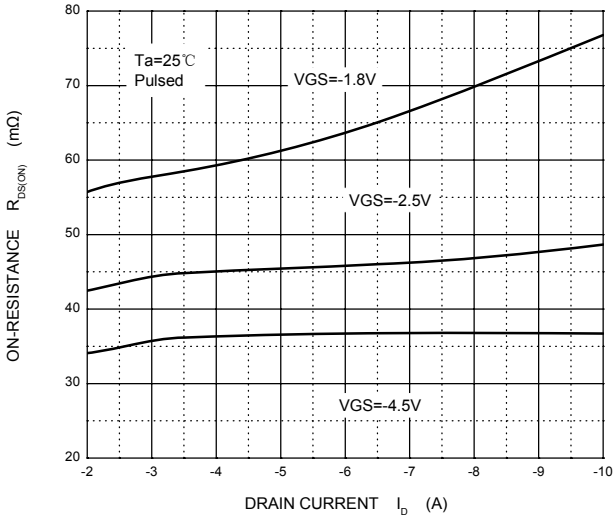
Output Characteristics



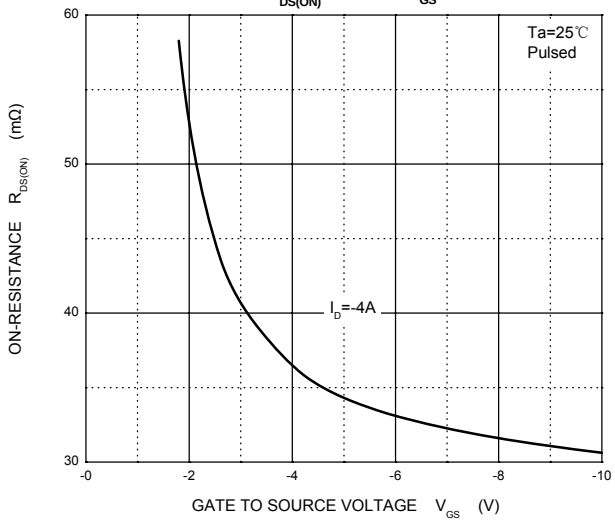
Transfer Characteristics



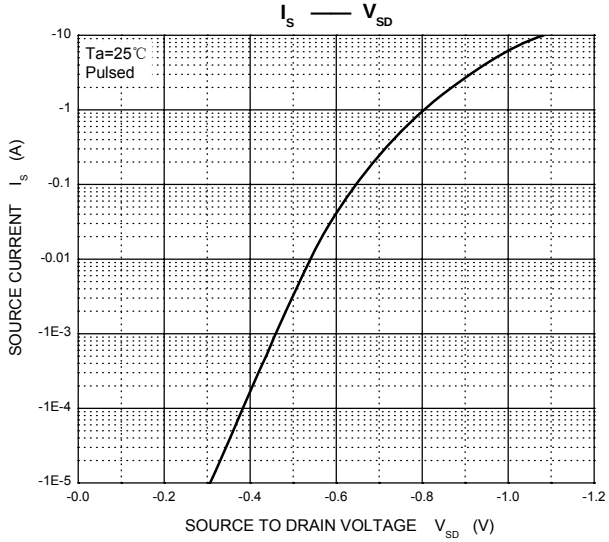
RDS(ON) — ID



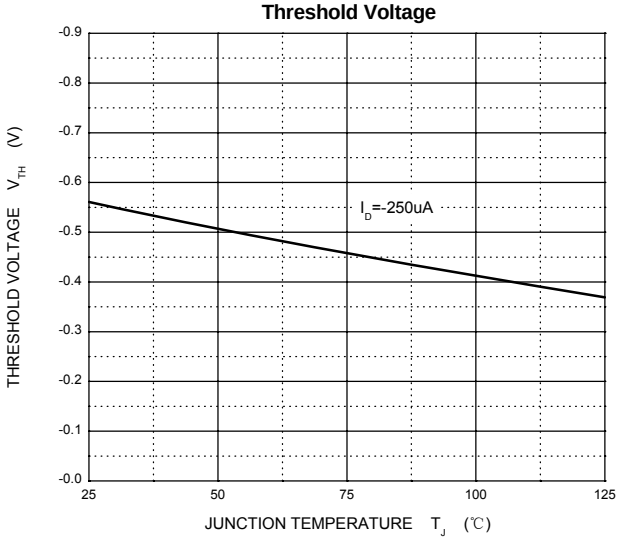
RDS(ON) — VGS



IS — VSD



Threshold Voltage



Package Outline Dimensions

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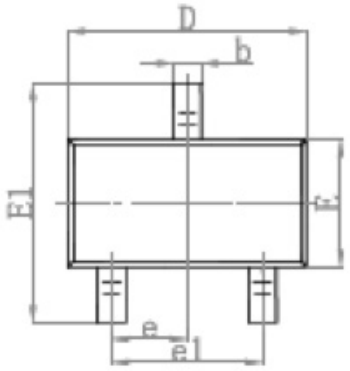
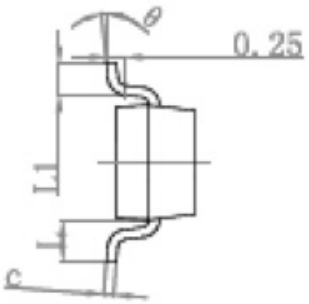
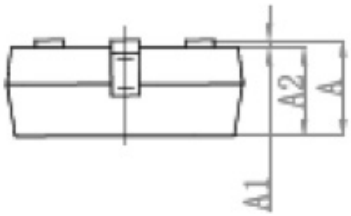
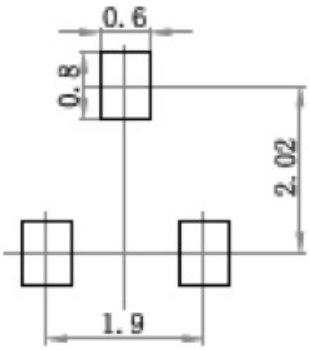






Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.550 REF		0.022 REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.