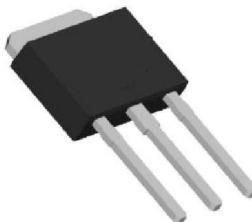
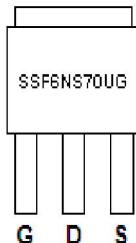


Main Product Characteristics

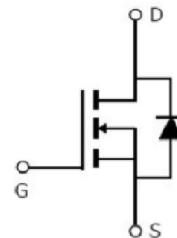
V_{DSS}	700V
$R_{DS(on)}$	0.95Ω (typ.)
I_D	6A ①



TO-251 (IPAK)



Marking and Pin Assignment



Schematic Diagram

Features and Benefits:

- High dv/dt and avalanche capabilities
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance
- Lead free product



Description:

The SSF6NS70UG series MOSFET is a new technology, which combines an innovative super junction technology and advance process. This new technology achieves low $R_{DS(on)}$, energy saving, high reliability and uniformity, superior power density and space saving.

Absolute Max Rating

Symbol	Parameter	Max.	Units
I_D @ $T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	6 ①	A
I_D @ $T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	3.7①	
I_{DM}	Pulsed Drain Current ②	18	
P_D @ $T_C = 25^\circ C$	Power Dissipation ③	33	W
	Linear Derating Factor	0.264	W/ $^\circ C$
V_{DS}	Drain-Source Voltage	700	V
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy @ $L=100mH$	72	mJ
I_{AS}	Avalanche Current @ $L=100mH$	1.2	A
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	$^\circ C$



Thermal Resistance

Symbol	Characteristics	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case ③	—	3.8	°C/W
$R_{\theta JA}$	Junction-to-ambient ($t \leq 10s$) ④	—	62	°C/W

Electrical Characteristics @ $T_A=25^\circ C$ unless otherwise specified

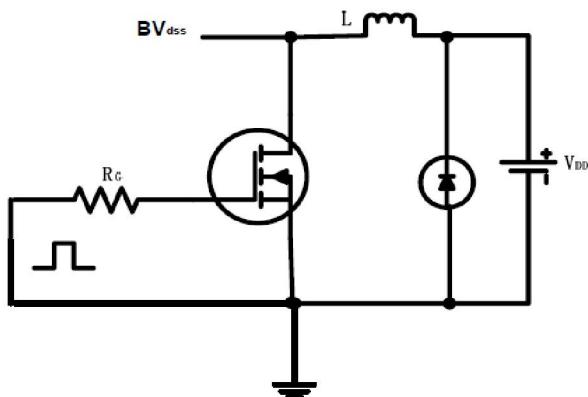
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	700	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	0.95	1.15	Ω	$V_{GS}=10V, I_D = 1A$
		—	2.0	—		$T_J = 125^\circ C$
		—	1.15	1.3	Ω	$V_{GS}=10V, I_D = 2.8A$
		—	2.1	—		$T_J = 125^\circ C$
$V_{GS(th)}$	Gate threshold voltage	2	—	4	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
		—	2.1	—		$T_J = 125^\circ C$
I_{DSS}	Drain-to-Source leakage current	—	—	1	μA	$V_{DS} = 700V, V_{GS} = 0V$
		—	—	50		$T_J = 125^\circ C$
I_{GSS}	Gate-to-Source forward leakage	—	—	100	nA	$V_{GS} = 30V$
		—	—	-100		$V_{GS} = -30V$
Q_g	Total gate charge	—	10.5	—	nC	$I_D = 5A,$ $V_{DS}=200V,$ $V_{GS} = 10V$
Q_{gs}	Gate-to-Source charge	—	2.8	—		
Q_{gd}	Gate-to-Drain("Miller") charge	—	4.5	—		
$t_{d(on)}$	Turn-on delay time	—	8.7	—		
t_r	Rise time	—	5.8	—	ns	$V_{GS}=10V, V_{DS} = 400V,$ $R_{GEN}=10.2\Omega, I_D = 1.5A$
$t_{d(off)}$	Turn-Off delay time	—	24	—		
t_f	Fall time	—	14	—		
C_{iss}	Input capacitance	—	338	—	pF	$V_{GS} = 0V$ $V_{DS} = 100V$ $f = 1MHz$
C_{oss}	Output capacitance	—	17	—		
C_{rss}	Reverse transfer capacitance	—	2.7	—		

Source-Drain Ratings and Characteristics

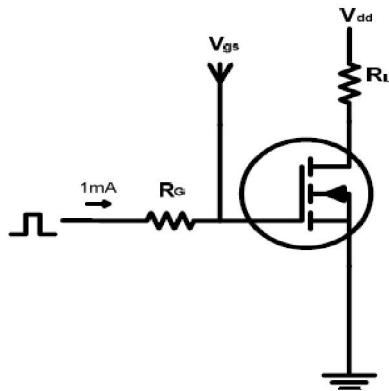
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	6 ①	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode)	—	—	18	A	
V_{SD}	Diode Forward Voltage	—	0.79	1.2	V	$I_S=2.8A, V_{GS}=0V$
t_{rr}	Reverse Recovery Time	—	102	—	nS	$T_J = 25^\circ C, I_F = 1.5A,$ $di/dt = 100A/\mu s$
Q_{rr}	Reverse Recovery Charge	—	421	—	nC	

Test Circuits and Waveforms

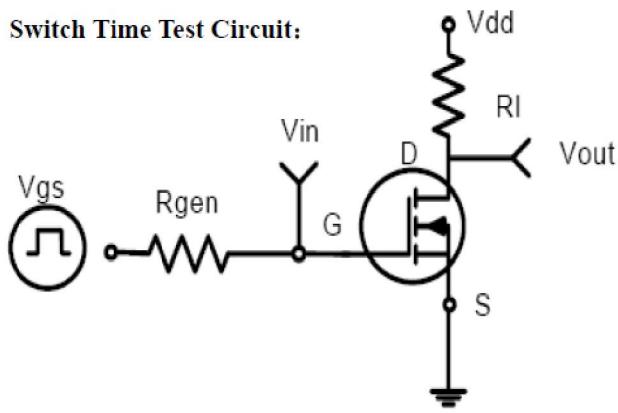
EAS test circuits:



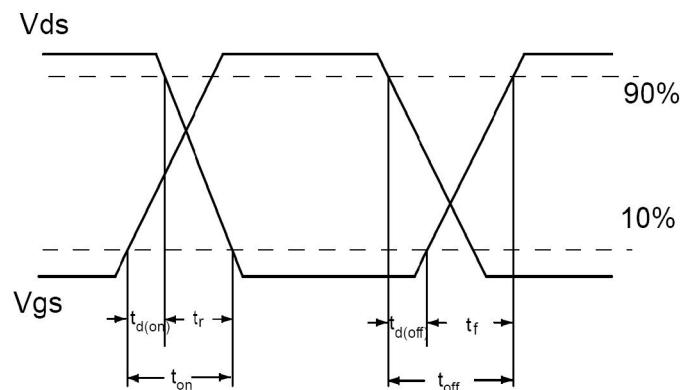
Gate charge test circuit:



Switch Time Test Circuit:



Waveforms:



Notes:

- ① Calculated continuous current based on maximum allowable junction temperature.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- ④ The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $TA = 25^{\circ}\text{C}$

Typical Electrical and Thermal Characteristics

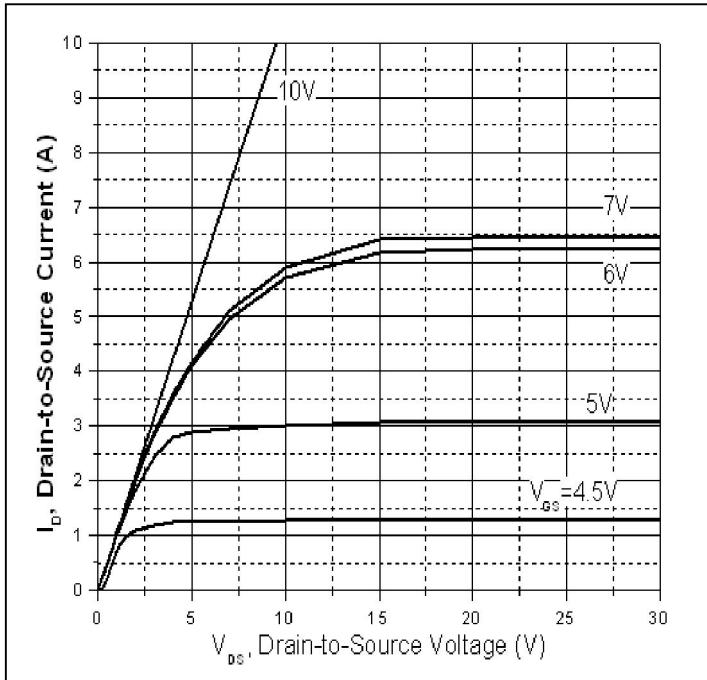


Figure 1: Typical Output Characteristics

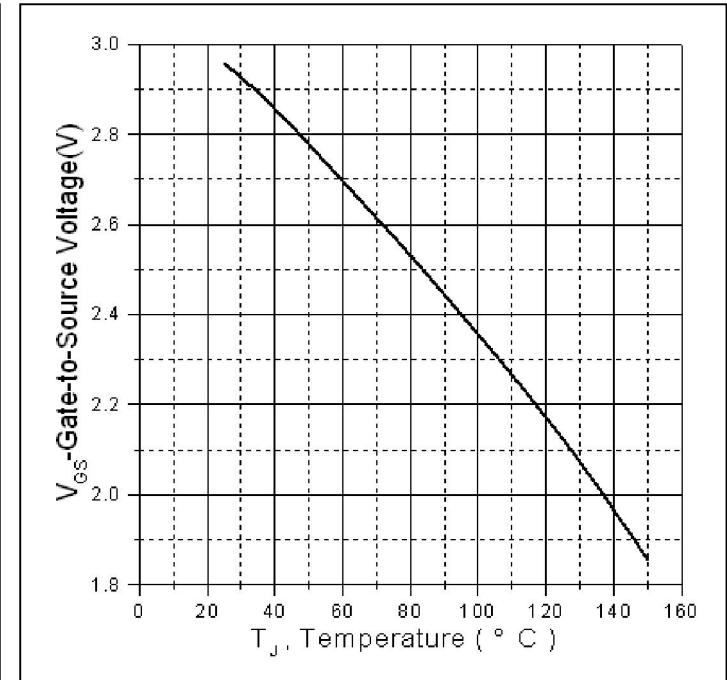


Figure 2. Gate to source cut-off voltage

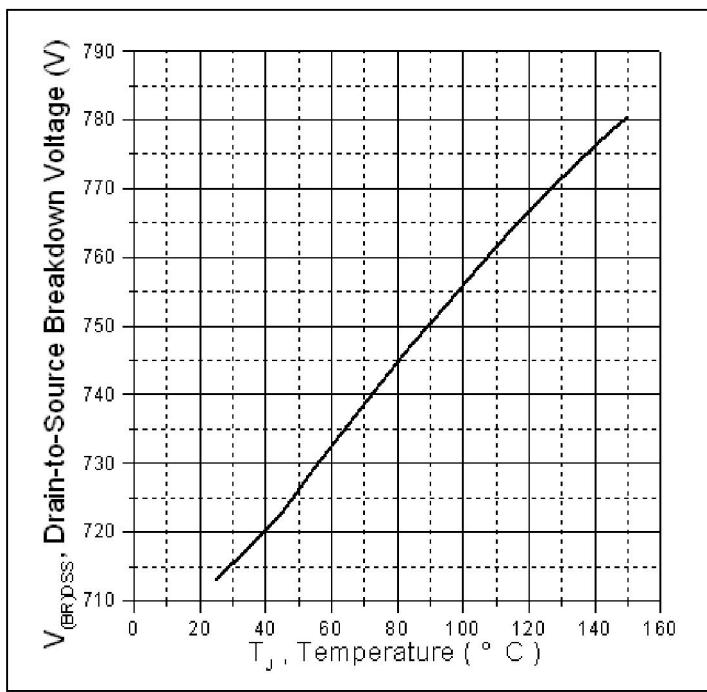


Figure 3. Drain-to-Source Breakdown Voltage Vs.
Case Temperature

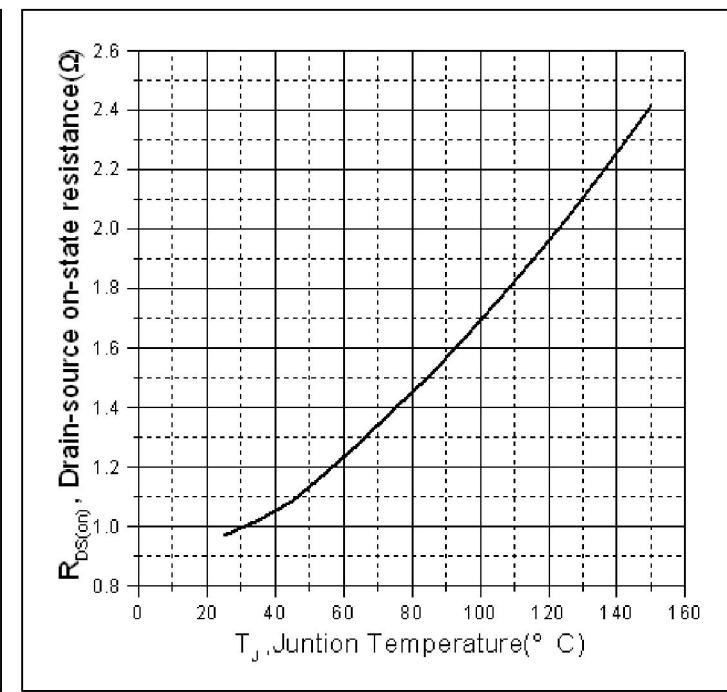


Figure 4: Normalized On-Resistance Vs. Case
Temperature

Typical Electrical and Thermal Characteristics

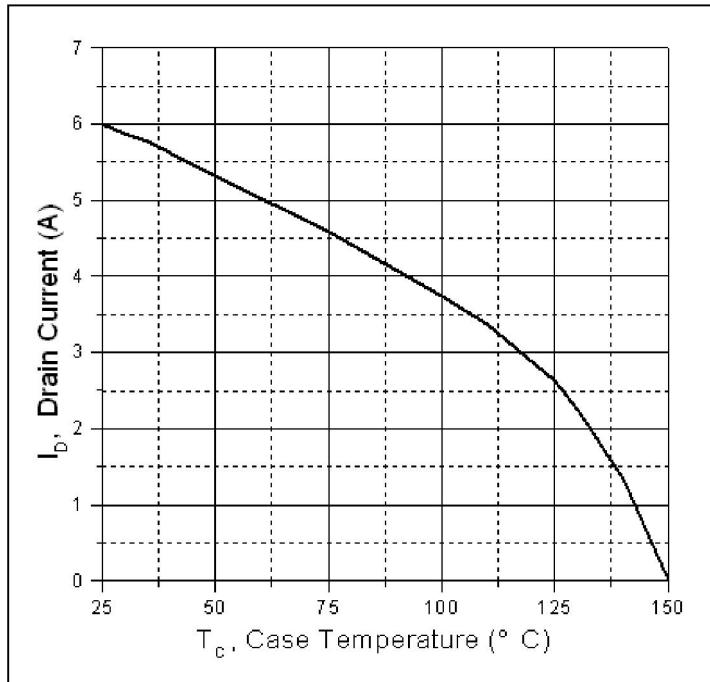


Figure 5. Maximum Drain Current Vs. Case Temperature

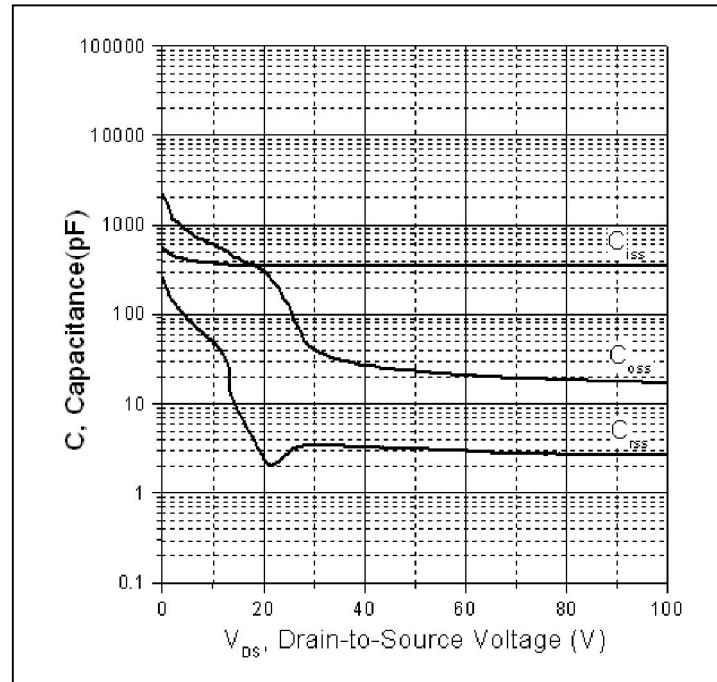


Figure 6. Typical Capacitance Vs. Drain-to-Source Voltage

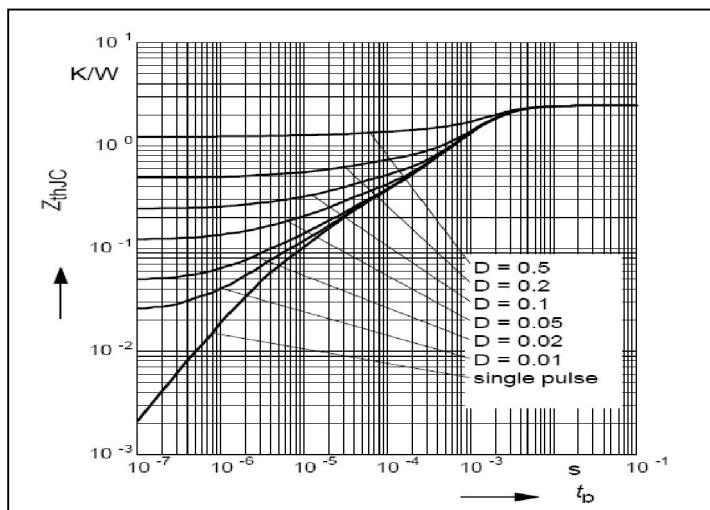
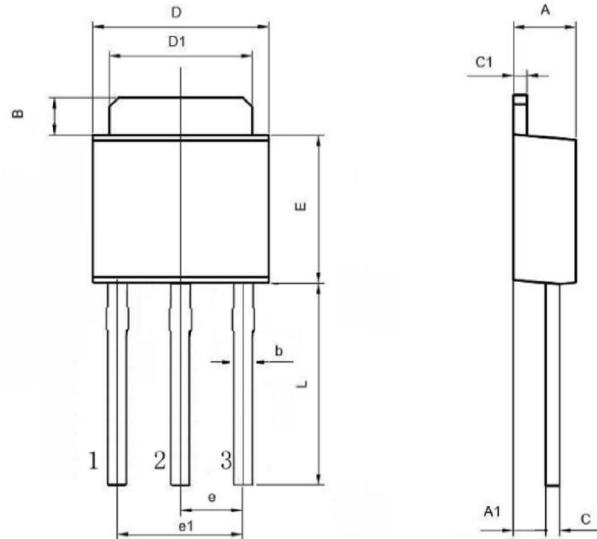


Figure 7. Maximum Effective Transient Thermal Impedance Junction-to-Case

Mechanical Data

TO-251 PACKAGE OUTLINE DIMENSION



Symbol	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	2.200	-	2.400	0.087	-	0.094
A1	0.950	-	1.150	0.037	-	0.045
B	0.950	-	1.250	0.037	-	0.049
b	0.500	-	0.700	0.020	-	0.028
c	0.450	-	0.550	0.018	-	0.022
c1	0.450	-	0.550	0.018	-	0.022
D	6.450	-	6.750	0.254	-	0.266
D1	5.200	-	5.400	0.205	-	0.213
E	5.950	-	6.250	0.234	-	0.246
e	2.240	-	2.340	0.088	-	0.092
e1	4.430	-	4.730	0.174	-	0.186
L	9.000	-	9.400	0.354	-	0.370



SSF6NS70UG
700V N-Channel MOSFET

Ordering and Marking Information

Device Marking: SSF6NS70UG

Package (Available)

TO-251(IPAK)

Operating Temperature Range

C : -55 to 150 °C

Devices per Unit

Package Type	Units/Tube	Tubes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
TO-251	75	60	4500	5	225000

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	$T_j=125^\circ\text{C}$ to 150°C @ 80% of Max $V_{DSS}/V_{CES}/VR$	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	$T_j=150^\circ\text{C}$ @ 100% of Max V_{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices