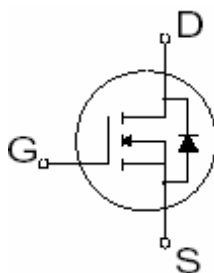


- Extremely high dv/dt capability
- Low Gate Charge Qg results in Simple Drive Requirement
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability



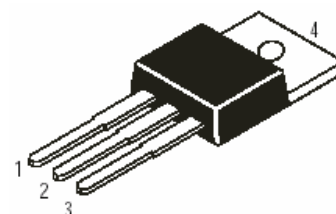
$$V_{DSS} = 650V$$

$$I_{D25} = 2.0A$$

$$R_{DS(ON)} = 4.7 \Omega$$

Description

StarMOS is a new generation of high voltage N-Channel enhancement mode power MOSFETs. This new technology minimises the JFET effect, increases packing density and reduces the on-resistance. StarMOS also achieves faster switching speeds through optimised gate layout with planar stripe DMOS technology.



Pin1-Gate
Pin2-Drain
Pin3-Source

Application

- Switching application

Absolute Maximum Ratings

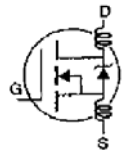
	Parameter	Max.	Units
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS}@10V$	2.0	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS}@10V$	1.35	
I_{DM}	Pulsed Drain Current ①	8	
$P_D@T_C=25^\circ C$	Power Dissipation	54	W
	Linear Derating Factor	0.43	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy ②	120	mJ
I_{AR}	Avalanche Current ①	2.0	A
E_{AR}	Repetitive Avalanche Energy ①	5.4	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	- 55 to +175	°C
	Soldering Temperature, for 10 seconds	300(1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf.in(1.1N.m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case	—	—	2.32	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	50	

Electrical Characteristics @T_J=25 °C(unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	650	—	—	V	V _{GS} =0V, I _D =250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp.Coefficient	—	0.6	—	V/°C	Reference to 25°C, I _D =250μA
R _{DS(on)}	Static Drain-to-Source On-resistance	—	3.6	4.7	Ω	V _{GS} =10V, I _D =1A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} =V _{GS} , I _D =250μA
g _{fs}	Forward Transconductance	—	5.0	—	S	V _{DS} =40V, I _D =1A
I _{DSS}	Drain-to-Source Leakage current	—	—	1	μA	V _{DS} =650V, V _{GS} =0V
		—	—	10		V _{DS} =480V, V _{GS} =0V, T _J =150°C
I _{GSS}	Gate-to-Source Forward leakage	—	—	100	nA	V _{GS} =30V
	Gate-to-Source Reverse leakage	—	—	-100		V _{GS} =-30V
Q _g	Total Gate Charge	—	8.5	12	nC	I _D =2A
Q _{gs}	Gate-to-Source charge	—	1.3	—		V _{DS} =480V
Q _{gd}	Gate-to-Drain("Miller") charge	—	4.1	—		V _{GS} =10V
t _{d(on)}	Turn-on Delay Time	—	9	28	nS	V _{DD} =300V
t _r	Rise Time	—	25	60		I _D =2A
t _{d(off)}	Turn-Off Delay Time	—	24	58		R _G =25Ω
t _f	Fall Time	—	28	66		
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm(0.25in.) from package and center of die contact
L _S	Internal Source Inductance	—	7.5	—		
C _{iss}	Input Capacitance	—	180	235	pF	V _{GS} =0V
C _{oss}	Output Capacitance	—	20	25		V _{DS} =25V
C _{rss}	Reverse Transfer Capacitance	—	4.3	5.6		f=1.0MHz


Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	2	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	8		
V _{SD}	Diode Forward Voltage	—	—	1.4	V	T _J =25°C, I _S =2A, V _{GS} =0V ④
t _{rr}	Reverse Recovery Time	—	230	—	nS	T _J =25°C, I _F =2A
Q _{rr}	Reverse Recovery Charge	—	1.0	—	nC	di/dt=100A/μs ④
t _{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S + L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max.junction temperature(see figure 11)
- ② L = 56mH, I_{AS} = 2 A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C
- ③ I_{SD} ≤ 2A, di/dt ≤ 200A/μS, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 25°C
- ④ Pulse width ≤ 300 μS; duty cycle ≤ 2%