SSG4406F-C

Elektronische Bauelemente

10A, 30V, $R_{DS(ON)}$ 12mΩ
N-Ch Enhancement Mode Power MOSFET

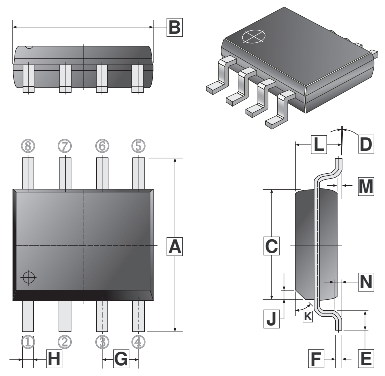
RoHS Compliant Product
A suffix of "-C" specifies halogen free

DESCRIPTION

The SSG4406F-C is the highest performance trench N-ch MOSFETs with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications .

The SSG4406F-C meet the RoHS and Green Product requirement with full function reliability approved.

SOP-8



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	5.79	6.20	H	0.33	0.51
B	4.70	5.11	J	0.375 REF.	
C	3.80	4.00	K	45°REF.	
D	0°	8°	L	1.3	1.752
E	0.40	1.27	M	0	0.25
F	0.10	0.25	N	0.25 REF.	
G	1.27 TYP.				

FEATURES

- Advanced High Cell Density Trench Technology
- Super Low Gate Charge
- Green Device Available

MARKING

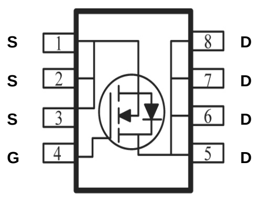
4406F
□□□□ ← □= Date Code

PACKAGE INFORMATION

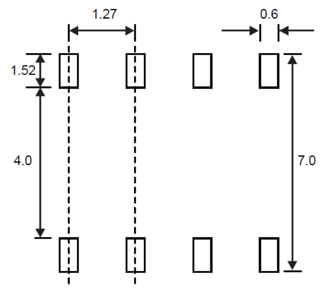
Package	MPQ	Leader Size
SOP-8	4K	13 inch

ORDER INFORMATION

Part Number	Type
SSG4406F-C	Lead (Pb)-free and Halogen-free



Mounting Pad Layout



*Dimensions in millimeters

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [1]	T_A=25℃	I_D	10	A
	T_A=70℃		7	
Pulsed Drain Current [2]		I_{DM}	36	A
Single Pulse Avalanche Energy [3]		E_{AS}	24.2	mJ
Avalanche Current		I_{AS}	22	A
Power Dissipation [4]	T_A=25℃	P_D	1.5	W
Junction & Storage Temperature Range		T_J, T_{STG}	-55~150	℃
Thermal Data				
Thermal Resistance from Junction-Ambient [1]		$R_{\theta JA}$	85	℃/W
Thermal Resistance from Junction-Case [1]		$R_{\theta JC}$	25	

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N-Ch Enhancement Mode Power MOSFET

ELECTRICAL CHARACTERISTICS (T_J=25℃ unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage		BV_{DSS}	30	-	-	V	V_{GS}=0, I_D=250μA
Gate-Threshold Voltage		$V_{GS(th)}$	1.2	-	2.5	V	V_{DS}=V_{GS}, I_D=250μA
Forward Transconductance [1]		g_{fs}	-	24	-	S	V_{DS}=5V, I_D=8A
Drain-Source Leakage Current	T_J=25℃	I_{DSS}	-	-	1	μA	V_{DS}=24V, V_{GS}=0
	T_J=55℃		-	-	5		
Gate-Source Leakage Current		I_{GSS}	-	-	±100	nA	V_{DS}=0, V_{GS}= ±20V
Static Drain-Source On-Resistance [2]		$R_{DS(ON)}$	-	10	12	mΩ	V_{GS}=10V, I_D=8A
			-	15	18		V_{GS}=4.5V, I_D=6A
Gate Resistance		R_g	-	1.8	-	Ω	V_{DS}=0, V_{GS}=0, f=1MHz
Total Gate Charge		Q_g	-	9.63	-	nC	V_{DS}=15V V_{GS}=4.5V I_D=8A
Gate-Source Charge		Q_{gs}	-	3.88	-		
Gate-Drain ("Miller") Change		Q_{gd}	-	3.44	-		
Turn-on Delay Time		$T_{d(on)}$	-	4.2	-	nS	V_{DD}=15V V_{GS}=10V R_G=1.5Ω I_D=8A
Rise Time		T_r	-	8.2	-		
Turn-off Delay Time		$T_{d(off)}$	-	31	-		
Fall Time		T_f	-	4	-		
Input Capacitance		C_{iss}	-	940	-	pF	V_{DS}=15V V_{GS}=0 f=1MHz
Output Capacitance		C_{oss}	-	131	-		
Reverse Transfer Capacitance		C_{rss}	-	109	-		
Source-Drain Diode Characteristics							
Diode Forward Voltage [2]		V_{SD}	-	-	1	V	V_{GS}=0, I_S=10A, T_J=25℃
Continuous Source Current [1,5]		I_S	-	-	10	A	V_G=V_D=0V, Force Current
Pulsed Source Current [2,5]		I_{SM}	-	-	36		
Reverse Recovery Time		t_{rr}	-	8	-	nS	I_F=8A, dI/dt=100A/μs, T_J=25℃
Reverse Recovery Charge		Q_{rr}	-	2.9	-	nC	

Notes:

1. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2oz copper.
2. The data tested by pulsed, pulse width≤300μs, duty cycle≤2%.
3. The E_{AS} data shows Max. rating. The test condition is V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=22A.
4. The power dissipation is limited by 150℃ juncti on temperature.
5. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

CHARACTERISTICS CURVE

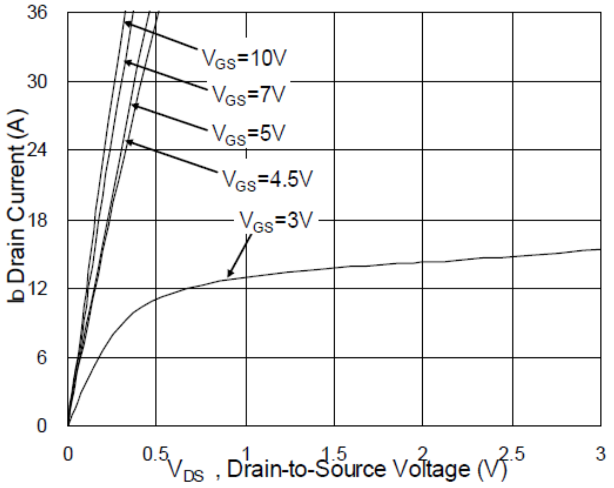

Fig.1 Typical Output Characteristics

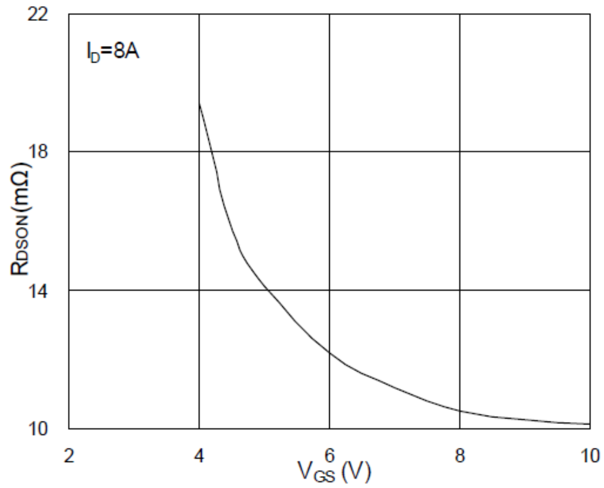

Fig.2 On-Resistance vs. G-S Voltage

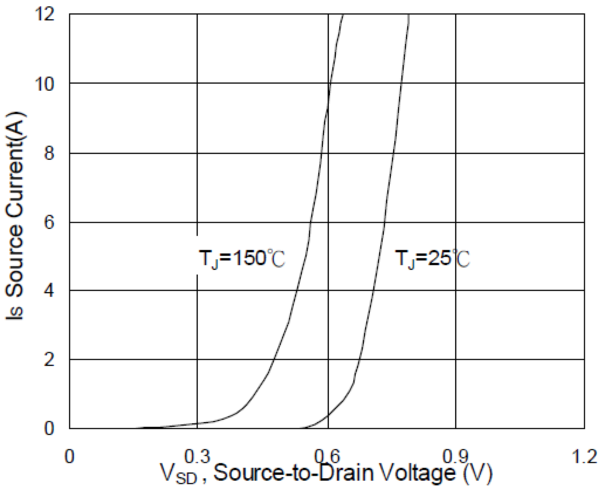

Fig.3 Forward Characteristics of Reverse

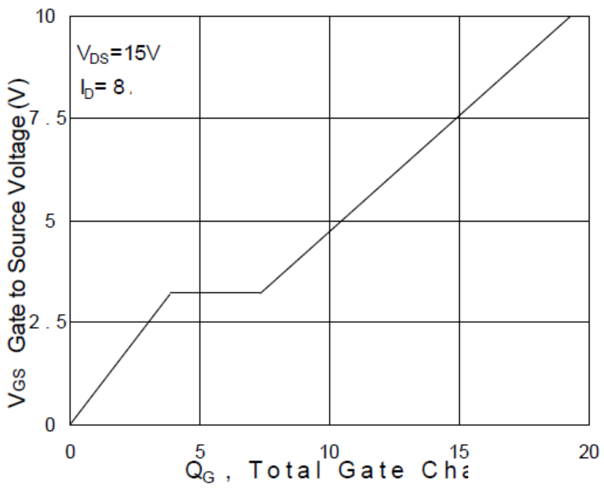

Fig.4 Gate-Charge Characteristics

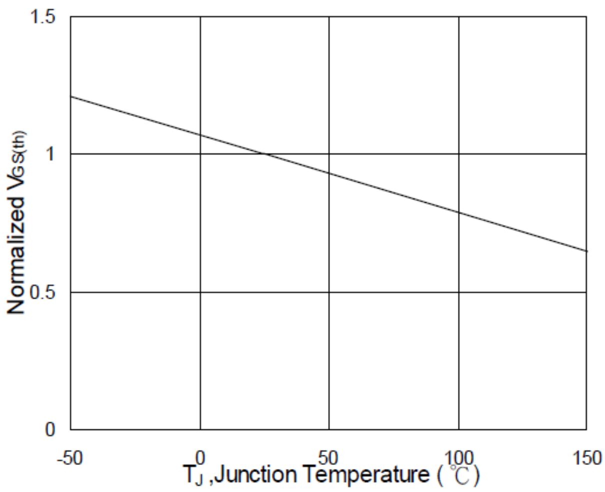

Fig.5 Normalized $V_{GS(th)}$ vs. T_J

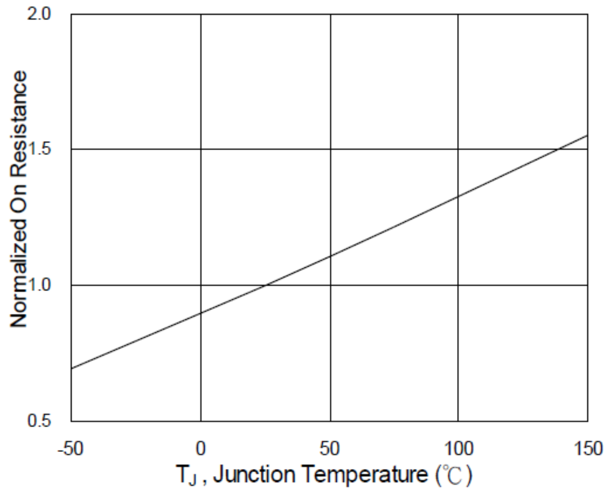

Fig.6 Normalized R_{DSON} vs. T_J

CHARACTERISTICS CURVE

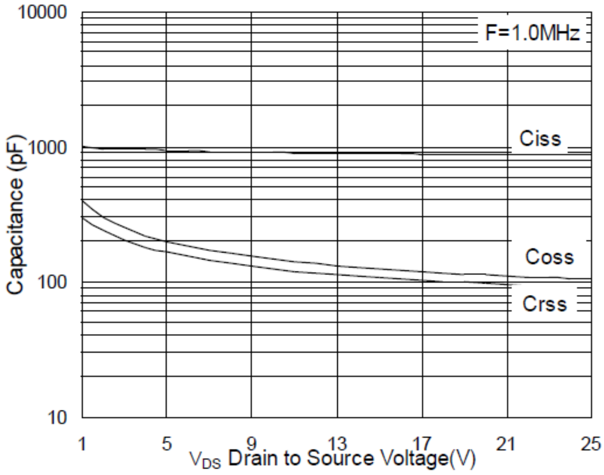

Fig.7 Capacitance

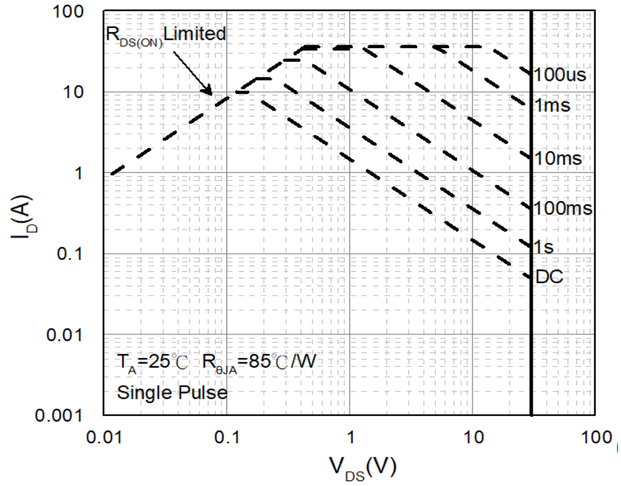

Fig.8 Safe Operating Area

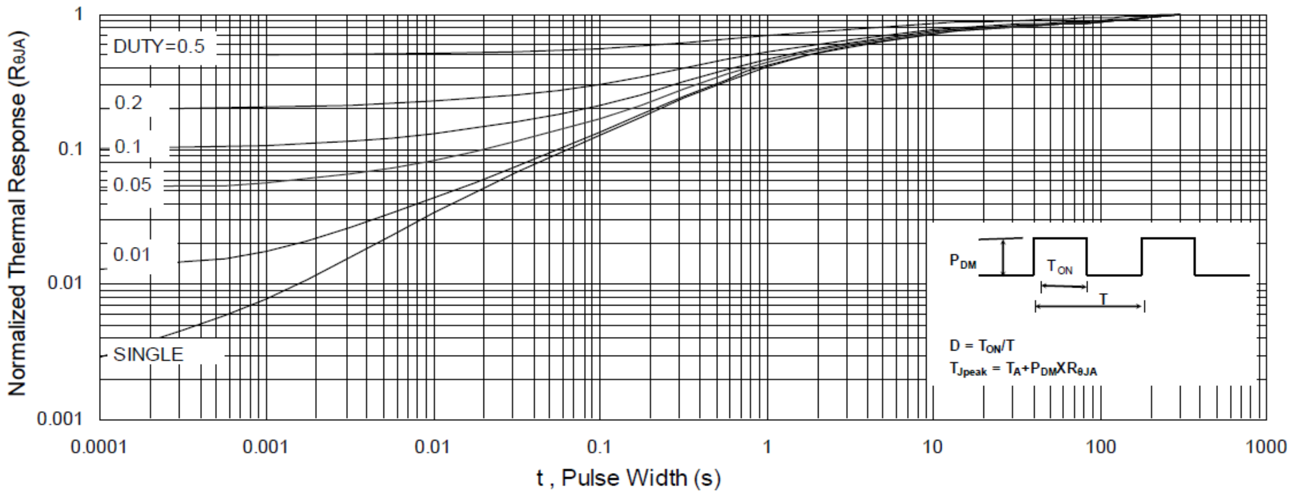

Fig.9 Normalized Maximum Transient Thermal Impedance

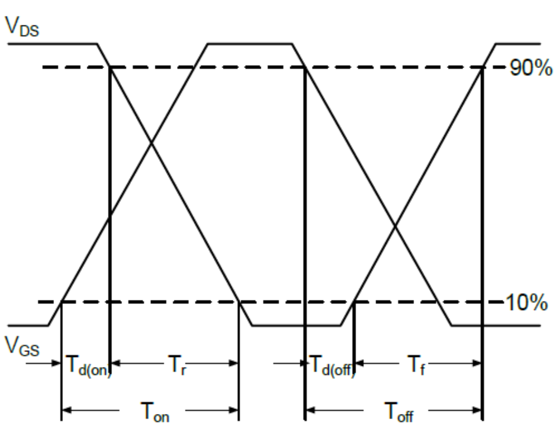

Fig.10 Switching Time Waveform

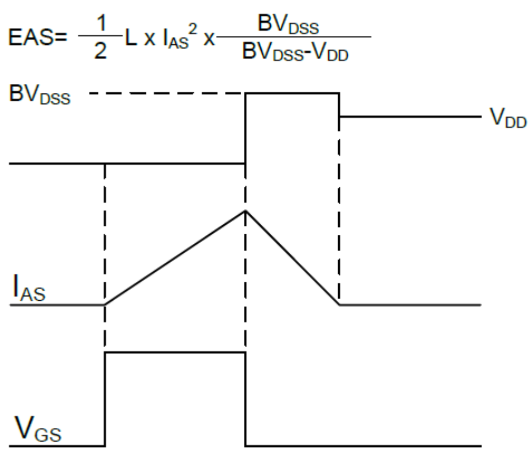

Fig.11 Unclamped Inductive Switching Waveform