SSM1105V

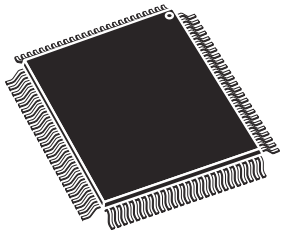
Scalar System Memory (SSM) for Image Processor ICs

NOT FOR NEW DESIGN

FEATURES SUMMARY

- System solution for use with image processing scalar ICs
  - For LCD monitors, projectors, and TVs
  - Compatible with Pixelworks PW11x/PWx64 families (and similar image processors or micro-controllers)
- Single integrated package, including:
  - Dual bank Flash memories
  - DDC, I^2C, and PWM channels
  - General purpose I/O
  - Programmable logic
  - In-System Programming via JTAG
- Dual bank Flash memories
  - Provide concurrent operation
  - 5 Mbit main Flash memory
  - 384 Kbit secondary Flash memory (divided into 10 small sectors)
  - Programmable Decode PLD for flexible address mapping of both memories
- Dual Display Data Channels (DDC)
  - Supports DDC for both analog RGB and digital DVI video input channels
  - DDC1/DDC2B VESA standard compliant
  - 256 byte SRAM buffer for each DDC channel
- Dual independent I^2C channels
  - Each capable of master or slave operation
  - Control A/D converters, video decoders, and future devices (tuner, audio, etc.)
- Four Pulse Width Modulator (PWM) channels
  - 16-bit resolution for period and for duty cycle
  - 16-bit clock prescalers
- Seven I/O ports with 52 I/O pins for Multifunction I/O: GPIO, DDC, I^2C, PWM, PLD I/O, and JTAG
- 3000 gate PLD with 16 macrocells, for creating glue logic, state machines, clock dividers, decoders, chip-selects, inverters; and to prioritize interrupts from DDC, I^2C, PWM

Figure 1. Packages



TQFP100 (U)

- In-System Programming (ISP) with JTAG
  - Program entire chip in 30-40 seconds with no involvement of the processor
  - Program with low-cost FlashLINK
- Content Security: Programmable Security Bit blocks access of device programmers / readers
- Zero-Power Technology: memory and PLD blocks automatically switch to stand-by current between input changes
- Package and Specifications
  - 100-pin TQFP, 14 x 14mm
  - 90 ns memory access time
  - V_{CC} Operating Voltage: 2.7V to 3.6V

This is information on a product still in production but not recommended for new designs.

SUMMARY DESCRIPTION

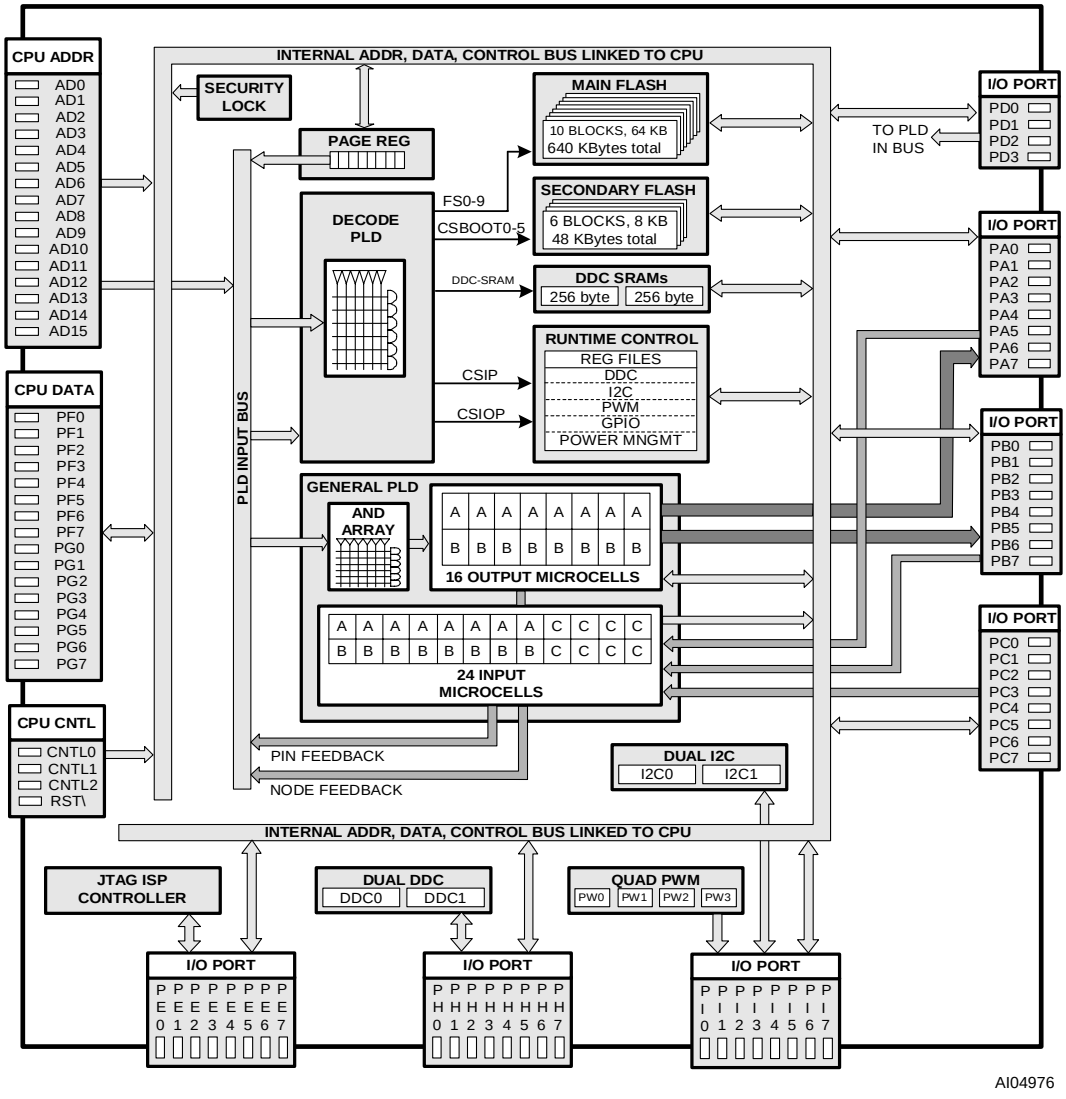
SSM1105V devices bring in-system programmable (ISP) and in-application programmable (IAP) flash memory to LCD monitor, projector and television applications utilizing a scalar IC from either Pixelworks or other similar image processors or micro-controllers (MCU). Figure 3 shows a typical SSM based system with Pixelworks processor.

The SSM1105V devices feature a dual -bank flash architecture, Dual Display Data Channels (DDC), I^2C, PWM channels, general purpose I/O, programmable logic, and in-system programming via either JTAG or I^2C.

The dual-bank Flash memory architecture supports full concurrent operation permitting IAP in the field, which means that firmware can be remotely updated with little interruption of system operation. During run-time, the secondary Flash memory array is ideal for EEPROM emulation, thus eliminating the need for a separate external EEPROM.

An on-chip, decode PLD provides for flexible address mapping for both memories. Dual 256 byte SRAMs provide buffer storage for the DDC channels, thus removing the burden from the processor.

Figure 2. SSM Block Diagram



Note: Additional address lines can be brought in to the device via Port A, B, C or D.

Table 1. Pin Assignments – TQFP100

Pin No.	Pin Assignments	Pin No.	Pin Assignments	Pin No.	Pin Assignments	Pin No.	Pin Assignments
1	PD2	26	PG1	51	PI0	76	PA5
2	PD3	27	PG2	52	PI1	77	PA6
3	GND	28	PG3	53	PI2	78	PA7
4	V_{DD}	29	PG4	54	PI3	79	CNTL0
5	ADIO0	30	PG5	55	PI4	80	CNTL1
6	ADIO1	31	PG6	56	PI5	81	PB0
7	ADIO2	32	PG7	57	PI6	82	PB1
8	ADIO3	33	PF0	58	PI7	83	PB2
9	ADIO4	34	PF1	59	GND	84	PB3
10	ADIO5	35	PF2	60	V_{DD}	85	PB4
11	ADIO6	36	PF3	61	PC0	86	PB5
12	ADIO7	37	PF4	62	PC1	87	PB6
13	ADIO8	38	PF5	63	PC2	88	PB7
14	ADIO9	39	PF6	64	PC3	89	V_{DD}
15	ADIO10	40	PF7	65	PC4	90	GND
16	ADIO11	41	V_{DD}	66	PC5	91	PE0
17	GND	42	GND	67	PC6	92	PE1
18	V_{DD}	43	PH0	68	PC7	93	PE2
19	ADIO12	44	PH1	69	GND	94	PE3
20	ADIO13	45	PH2	70	V_{DD}	95	PE4
21	ADIO14	46	PH3	71	PA0	96	PE5
22	ADIO15	47	PH4	72	PA1	97	PE6
23	$\overline{\text{RESET}}$	48	PH5	73	PA2	98	PE7
24	CNTL2	49	PH6	74	PA3	99	PD0
25	PG0	50	PH7	75	PA4	100	PD1

Figure 3. SSM1105V-Based System Applications

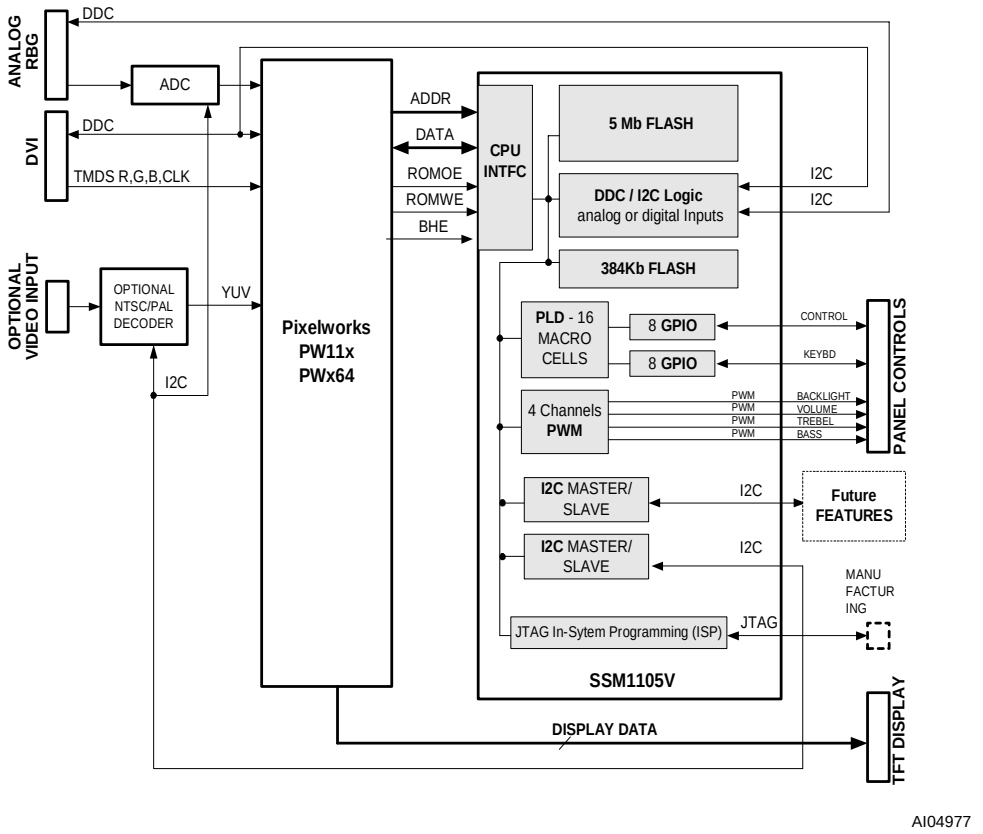


Table 2. Ordering Information Scheme

Example: SSM1105 V – 90 T 1 T

Device Type

SSM1105 = SSM for image processor ICs

Operating Voltage

V = V_{CC} = 2.7 to 3.6V

Speed

90 = 90 ns

Package

T = TQFP100

Temperature Range

1 = 0 to 70 °C (commercial)

Option

T = Tape & Reel Packing