

P-Channel MOSFET

SSM3J135TU

■ Features

- $V_{DS}(V) = -20\text{ V}$

- $I_D = -3.0\text{ A}$

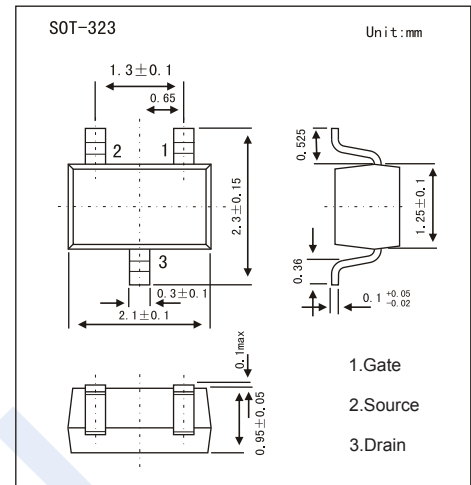
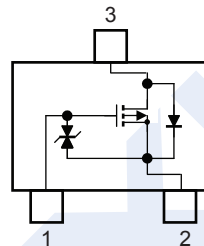
- 1.5 V drive

- Low ON-resistance:

 $R_{DS(ON)} = 260\text{ m}\Omega$ (max) (@ $V_{GS} = -1.5\text{ V}$)

 $R_{DS(ON)} = 180\text{ m}\Omega$ (max) (@ $V_{GS} = -1.8\text{ V}$)

 $R_{DS(ON)} = 132\text{ m}\Omega$ (max) (@ $V_{GS} = -2.5\text{ V}$)

 $R_{DS(ON)} = 103\text{ m}\Omega$ (max) (@ $V_{GS} = -4.5\text{ V}$)
■ Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 8	
Continuous Drain Current	I_D (Note 1)	-3.0	A
Pulsed Drain Current	I_{DP} (Note 1)	-6.0	
Power Dissipation	P_D (Note 2)	500	mW
	P_D ($t < 1\text{ s}$)	1000	
Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55 to 150	

Note 1: The channel temperature should not exceed 150°C during use.

Note 2: Mounted on FR4 board.

(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645 mm²)

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■ Electrical Characteristics (Ta = 25°C)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V _{DSS}	I _D =-1mA, V _{GS} =0V	-20			V
	V _{DSX}	I _D =-1mA, V _{GS} =5V (Note 4)	-15			
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-20V, V _{GS} =0V			-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±8V			±1	
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =-3V, I _D =-1mA	-0.3		-1.0	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =-4.5V, I _D =-1.0A (Note 3)			103	mΩ
		V _{GS} =-2.5V, I _D =-0.6A (Note 3)			132	
		V _{GS} =-1.8V, I _D =-0.4A (Note 3)			180	
		V _{GS} =-1.5V, I _D =-0.2A (Note 3)			260	
Forward Transconductance	g _{FS}	V _{DS} =-3V, I _D =-1.0A (Note 3)	2.2			S
Input Capacitance	C _{iss}	V _{GS} =0V, V _{DS} =-10V, f=1MHz		270		pF
Output Capacitance	C _{oss}			40		
Reverse Transfer Capacitance	C _{rss}			32		
Total Gate Charge	Q _g	V _{GS} =-4.5V, V _{DS} =-10V, I _D =-2.0A		4.6		nC
Gate Source Charge	Q _{gs1}			0.4		
Gate Drain Charge	Q _{gd}			0.9		
Turn-On DelayTime	t _{d(on)}	V _{DS} =-10V, I _D =-1.0A		17		ns
Turn-Off DelayTime	t _{d(off)}	V _{GS} =0 to -2.5V, R _G =4.7Ω		43		
Diode Forward Voltage	V _{SD}	I _S =-3.0A, V _{GS} =0V (Note 3)			-1.2	V

Note 3: Pulse test

Note 4: If a forward bias is applied between gate and source, this device enters V(BR)DSX mode. Note that the drain-source breakdown voltage is lowered in this mode.

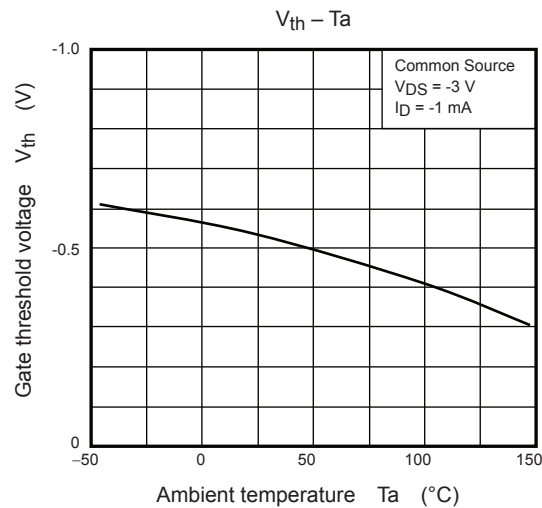
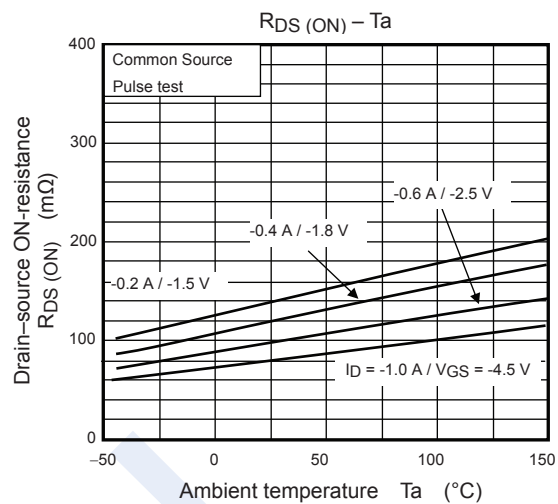
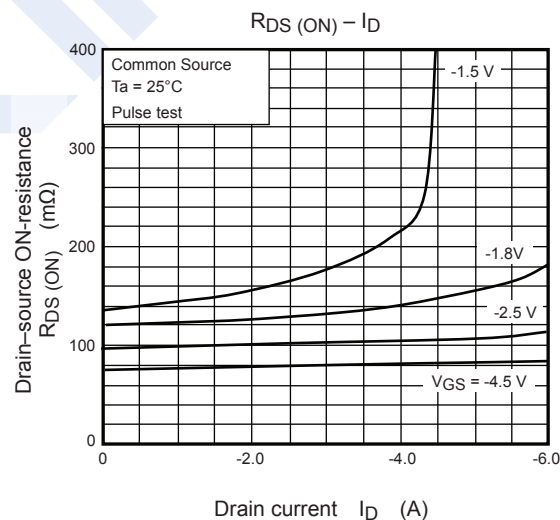
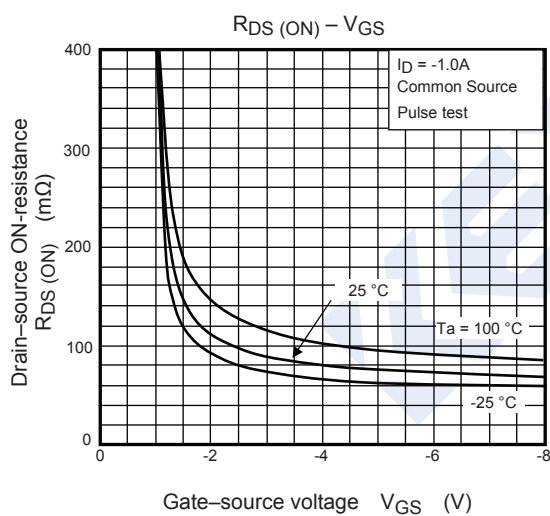
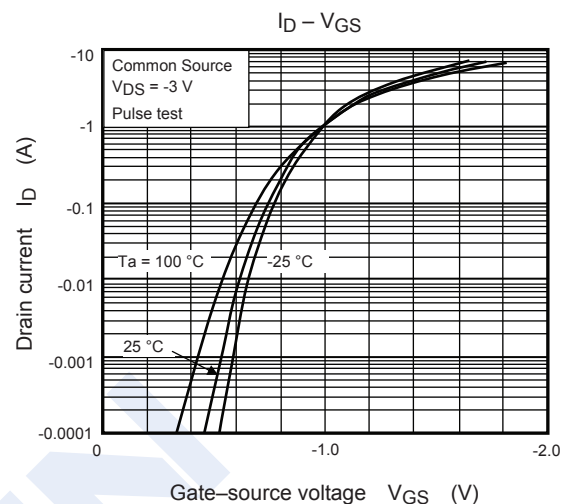
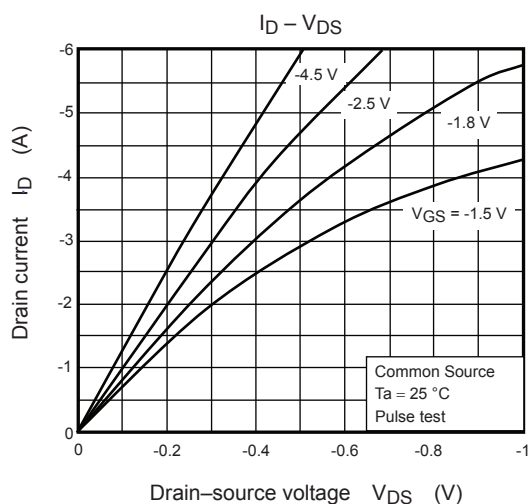
■ Marking

Marking	JJN
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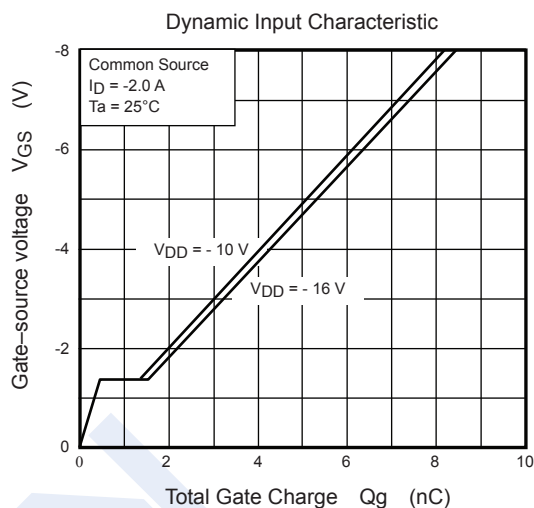
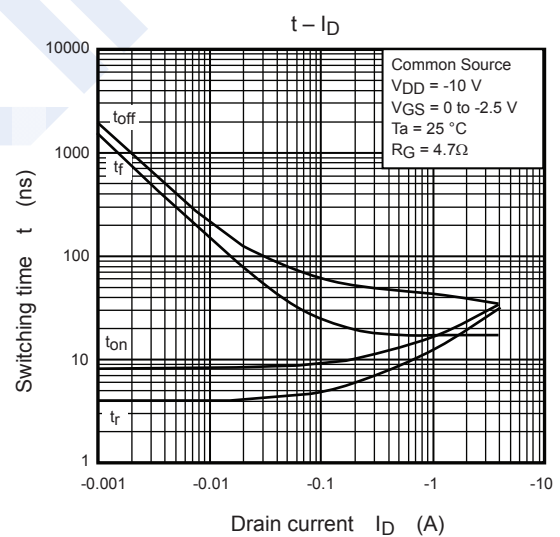
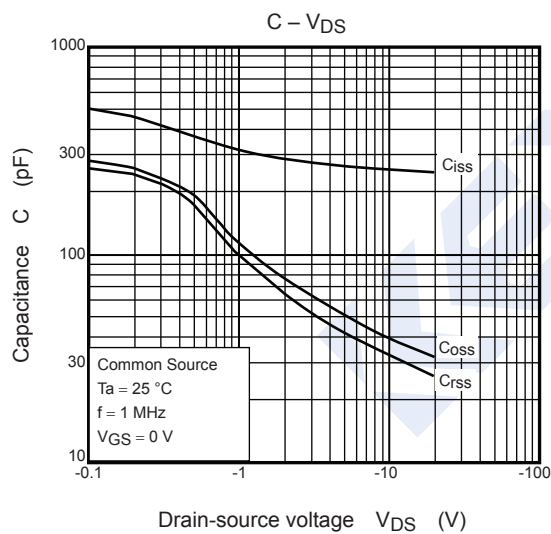
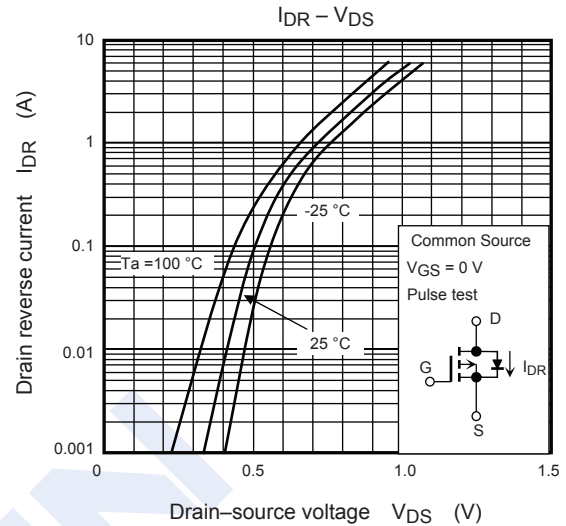
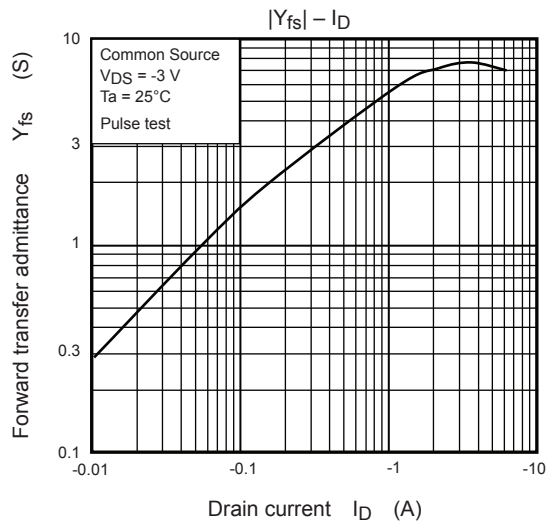
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■ Typical Characteristics



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