

# SSP1N60B/SSS1N60B

## 600V N-Channel MOSFET

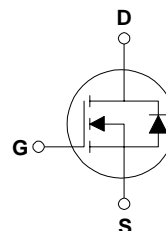
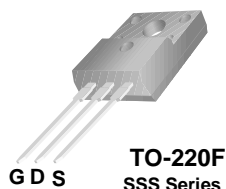
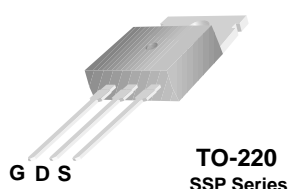
### General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supplies.

### Features

- 1.0A, 600V,  $R_{DS(on)} = 12\Omega @ V_{GS} = 10V$
- Low gate charge ( typical 5.9 nC)
- Low  $C_{rss}$  ( typical 3.6 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	SSP1N60B	SSS1N60B	Units
$V_{DSS}$	Drain-Source Voltage	600		V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ ) - Continuous ( $T_C = 100^\circ\text{C}$ )	1.0	1.0 *	A
		0.6	0.6 *	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	3.0	3.0 *	A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$		V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	50		mJ
$I_{AR}$	Avalanche Current (Note 1)	1.0		A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	3.4		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	5.5		V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ ) - Derate above $25^\circ\text{C}$	34	17	W
		0.27	0.13	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		$^\circ\text{C}$

\* Drain current limited by maximum junction temperature.

### Thermal Characteristics

Symbol	Parameter	SSP1N60B	SSS1N60B	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case Max.	3.67	7.48	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink Typ.	0.5	--	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient Max.	62.5	62.5	$^\circ\text{C}/\text{W}$

**Electrical Characteristics** $T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	600	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.65	--	V/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	--	--	10	$\mu\text{A}$
		$V_{DS} = 480\text{ V}, T_C = 125^\circ\text{C}$	--	--	100	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

**On Characteristics**

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 0.5\text{ A}$	--	9.7	12	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 0.5\text{ A}$ (Note 4)	--	0.97	--	S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	165	215	pF
$C_{oss}$	Output Capacitance		--	18	25	pF
$C_{riss}$	Reverse Transfer Capacitance		--	3.6	4.7	pF

**Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 300\text{ V}, I_D = 1.0\text{ A},$ $R_G = 25\ \Omega$	--	14	40	ns
$t_r$	Turn-On Rise Time		--	45	100	ns
$t_{d(off)}$	Turn-Off Delay Time		--	25	60	ns
$t_f$	Turn-Off Fall Time		(Note 4, 5)	--	35	80
$Q_g$	Total Gate Charge	$V_{DS} = 480\text{ V}, I_D = 1.0\text{ A},$ $V_{GS} = 10\text{ V}$	--	5.9	7.7	nC
$Q_{gs}$	Gate-Source Charge		--	1.0	--	nC
$Q_{gd}$	Gate-Drain Charge		(Note 4, 5)	--	2.7	--

**Drain-Source Diode Characteristics and Maximum Ratings**

$I_S$	Maximum Continuous Drain-Source Diode Forward Current	--	--	1.0	A	
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	--	--	3.0	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1.0\text{ A}$	--	--	1.4	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 1.0\text{ A},$	--	180	--	ns
$Q_{rr}$	Reverse Recovery Charge	$di_F / dt = 100\text{ A}/\mu\text{s}$ (Note 4)	--	0.47	--	$\mu\text{C}$

**Notes:**

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $L = 92\text{ mH}, I_{AS} = 1.0\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 1.0\text{ A}, di/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width  $\leq 300\ \mu\text{s}$ , Duty cycle  $\leq 2\%$
5. Essentially independent of operating temperature

## Typical Characteristics

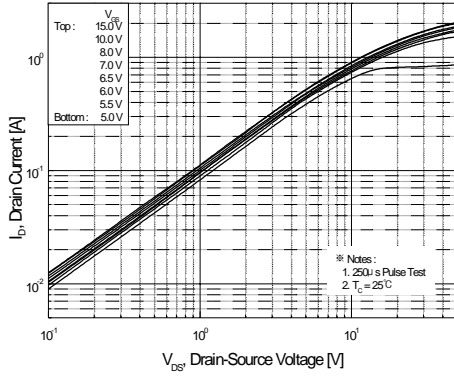


Figure 1. On-Region Characteristics

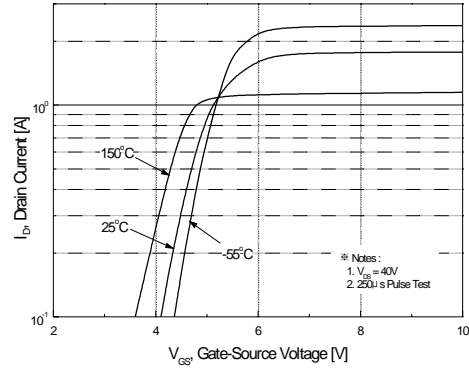


Figure 2. Transfer Characteristics

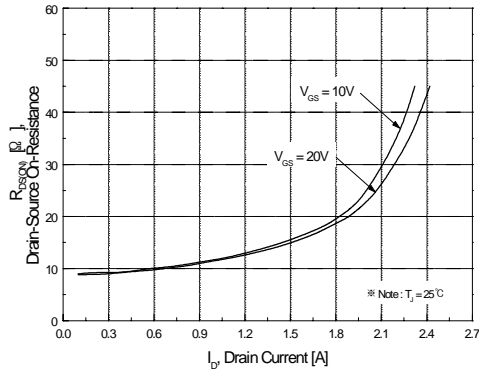


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

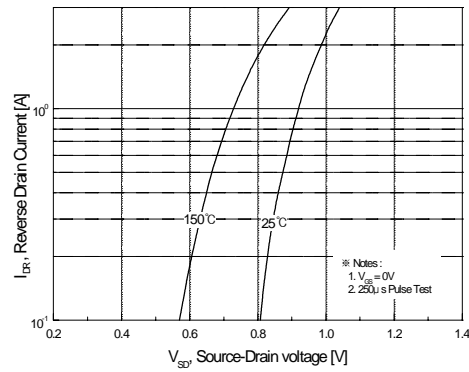


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

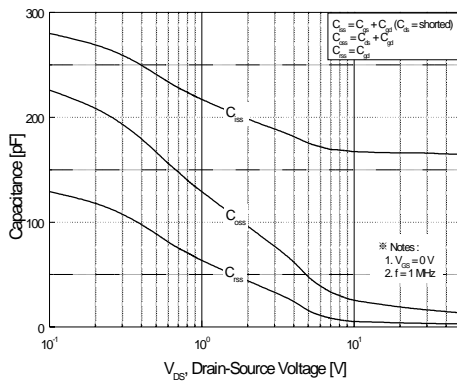


Figure 5. Capacitance Characteristics

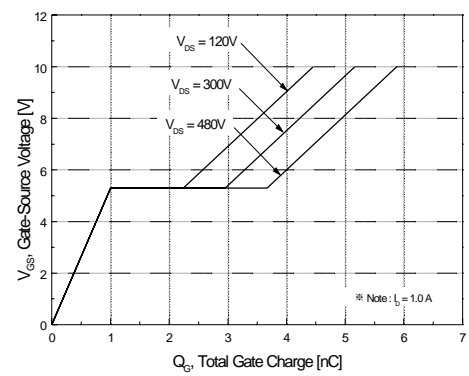


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

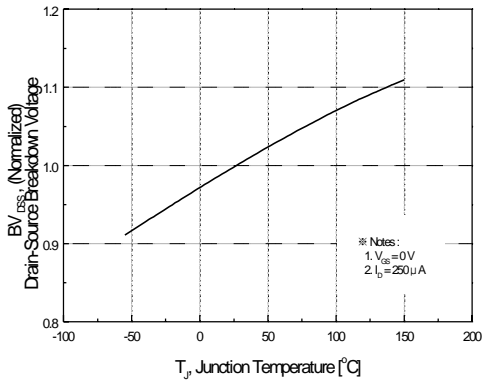


Figure 7. Breakdown Voltage Variation vs Temperature

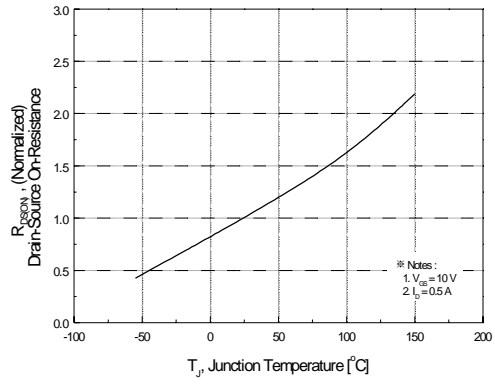


Figure 8. On-Resistance Variation vs Temperature

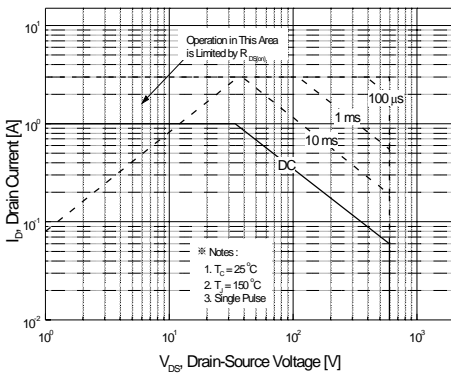


Figure 9-1. Maximum Safe Operating Area for SSP1N60B

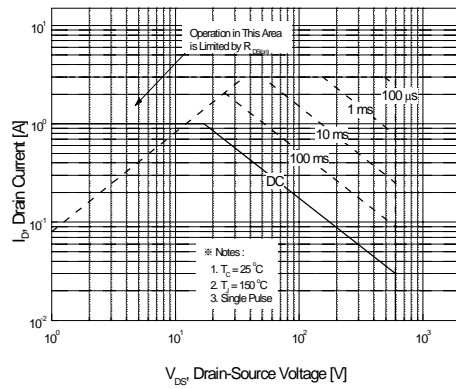


Figure 9-2. Maximum Safe Operating Area for SSS1N60B

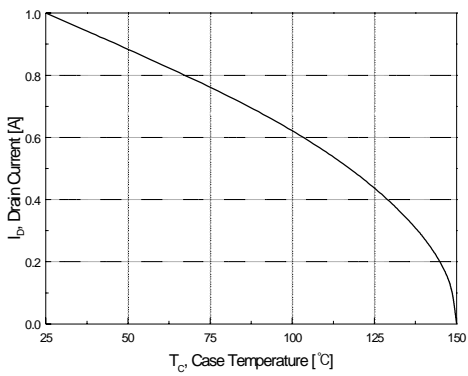


Figure 10. Maximum Drain Current vs Case Temperature

Typical Characteristics (Continued)

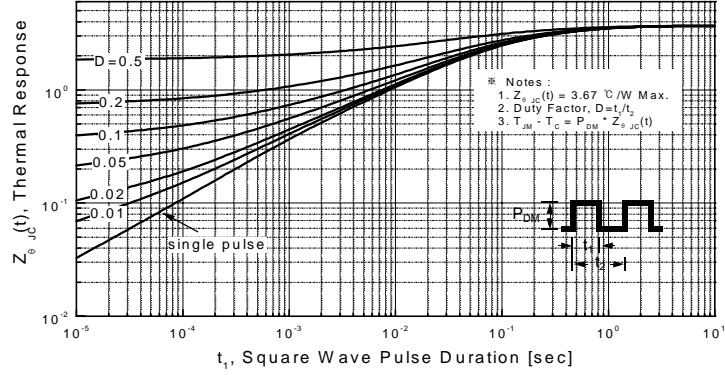


Figure 11-1. Transient Thermal Response Curve for SSP1N60B

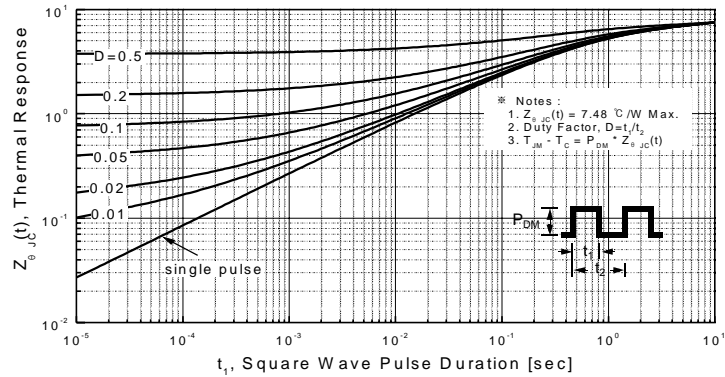


Figure 11-2. Transient Thermal Response Curve for SSS1N60B

Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms



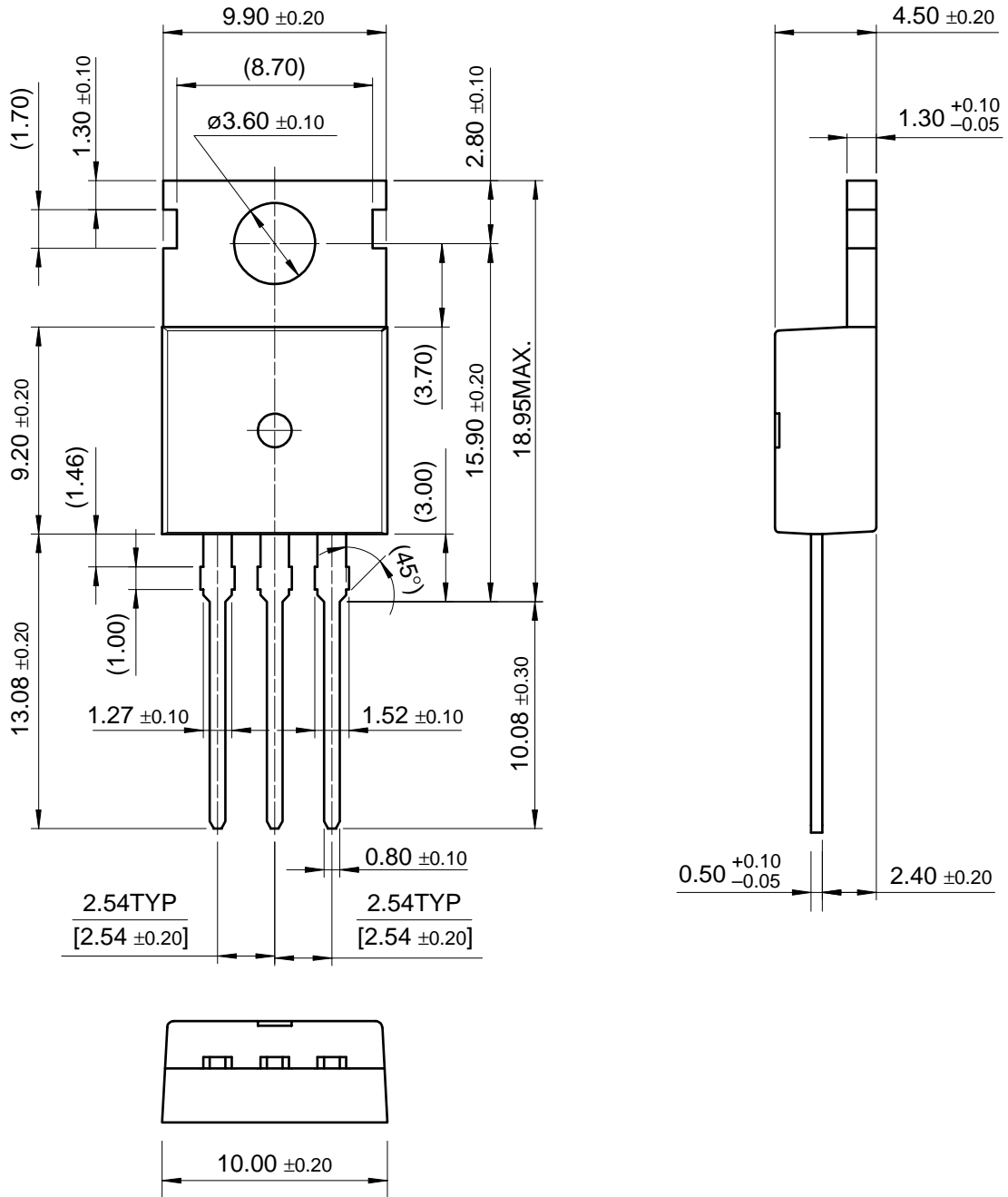
Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimensions

TO-220

SSP1N60B/SSS1N60B

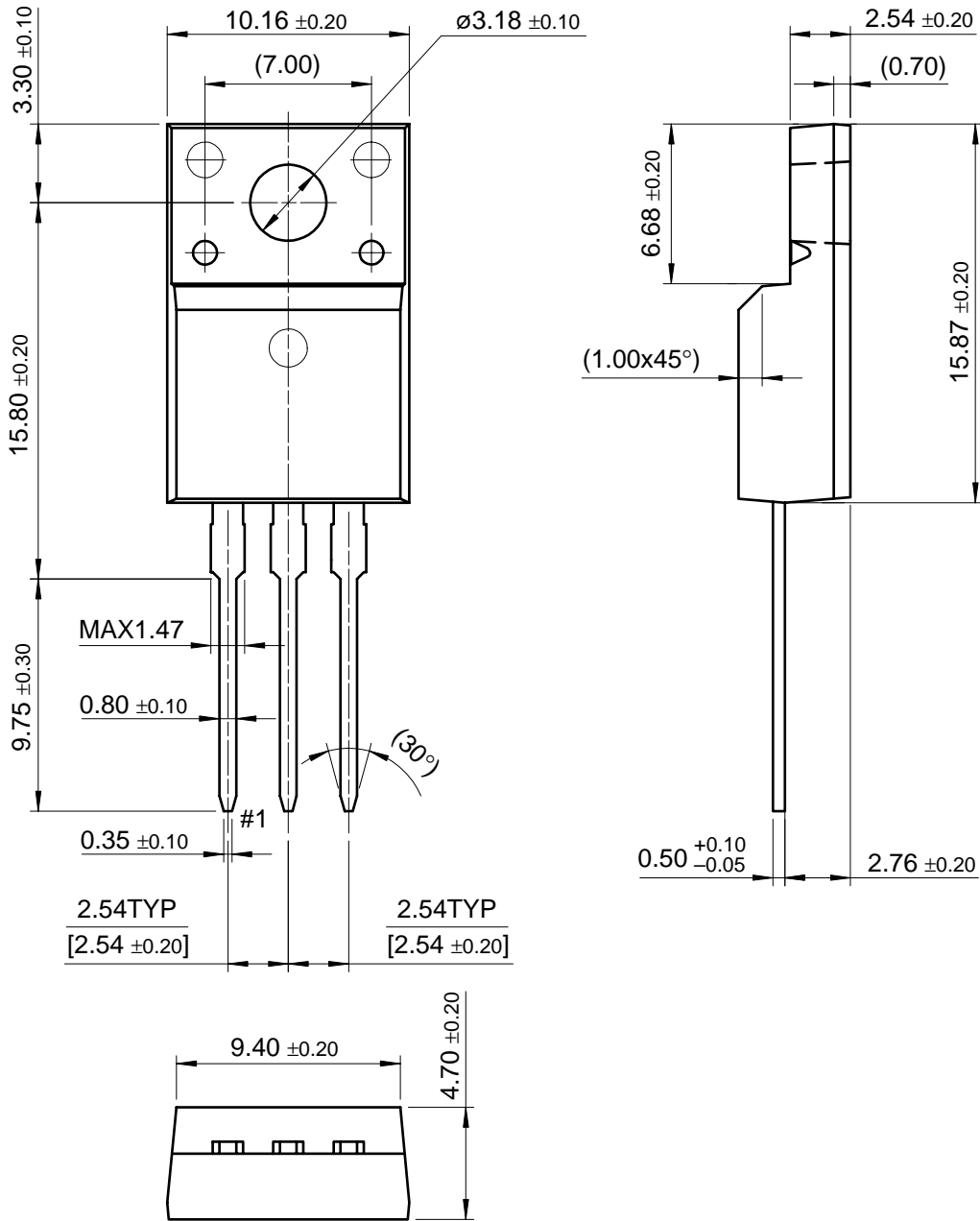


Dimensions in Millimeters



Package Dimensions (Continued)

# TO-220F



SSP1N60B/SSS1N60B

Dimensions in Millimeters

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FACT <sup>TM</sup>	MicroPak <sup>TM</sup>	Quiet Series <sup>TM</sup>	UHC <sup>TM</sup>	
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