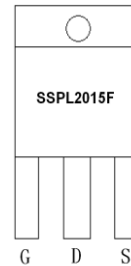


## Main Product Characteristics

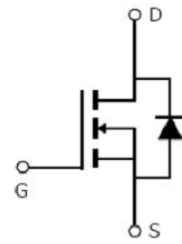
$V_{DS}$	200V
$R_{DS(on)}$	0.13Ω(typ.)
$I_D$	18A <sup>①</sup>



TO-220F



Marking and Pin  
Assignment



Schematic Diagram

## Features and Benefits

- Advanced Process Technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 175°C operating temperature



## Description

These N-Channel enhancement mode power field effect transistors are produced using silikron proprietary MOSFET technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supplies.

## Absolute Max Rating

Symbol	Parameter	Max.	Units
$I_D$ @ TC = 25°C	Continuous Drain Current, $V_{GS}$ @ 10V	18 <sup>①</sup>	A
$I_D$ @ TC = 100°C	Continuous Drain Current, $V_{GS}$ @ 10V	13 <sup>①</sup>	
$I_{DM}$	Pulsed Drain Current <sup>②</sup>	72	
$P_D$ @TC = 25°C	Power Dissipation <sup>③</sup>	75	W
	Linear Derating Factor	0.5	W/°C
$V_{DS}$	Drain-Source Voltage	200	V
$V_{GS}$	Gate-to-Source Voltage	± 30	V
$E_{AS}$	Single Pulse Avalanche Energy @ L=4.2mH	412	mJ
$I_{AS}$	Avalanche Current @ L=4.2mH	14	A
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to +175	°C

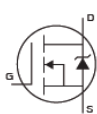
## Thermal Resistance

Symbol	Characteristics	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case ③	—	2.0	°C/W
$R_{\theta JA}$	Junction-to-ambient ( $t \leq 10s$ ) ④	—	62	°C/W
	Junction-to-Ambient (PCB mounted, steady-state) ④	—	40	°C/W

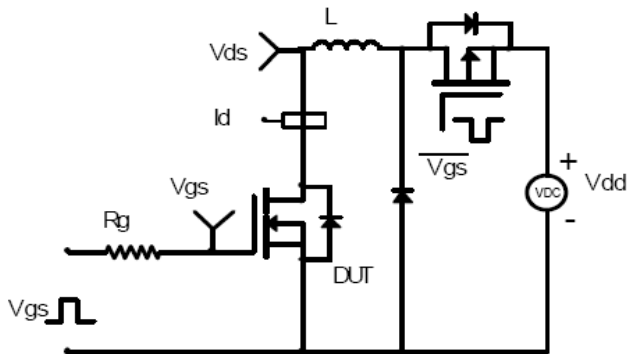
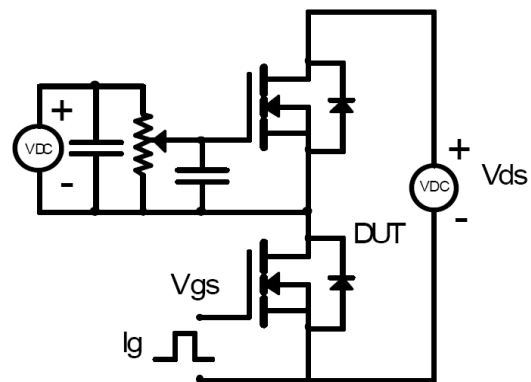
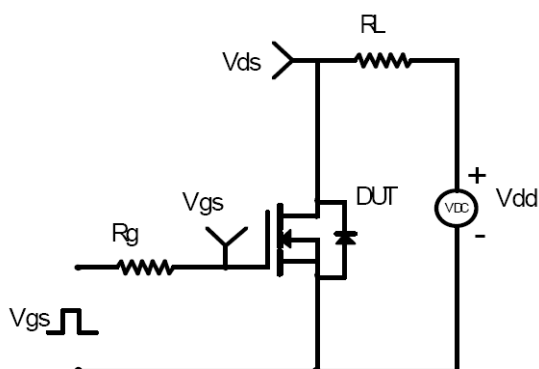
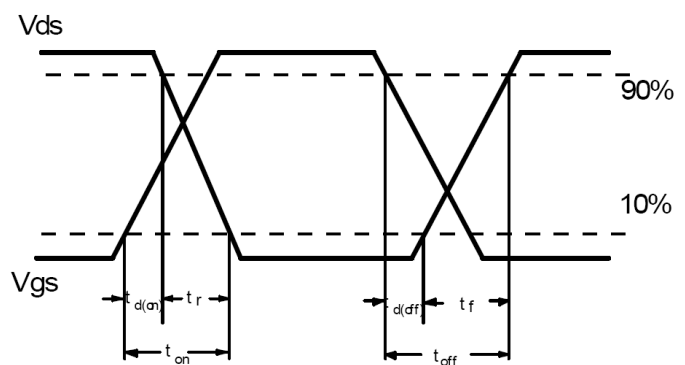
## Electrical Characteristics @ $T_A=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	200	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	0.13	0.15	$\Omega$	$V_{GS}=10V, I_D=11A$
		—	0.27	—		$T_J = 125^\circ\text{C}$
$V_{GS(th)}$	Gate threshold voltage	2	—	4	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
		—	2.26	—		$T_J = 125^\circ\text{C}$
$I_{DSS}$	Drain-to-Source leakage current	—	—	1	$\mu A$	$V_{DS} = 200V, V_{GS} = 0V$
		—	—	50		$T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source forward leakage	—	—	100	nA	$V_{GS} = 20V$
		—	—	-100		$V_{GS} = -20V$
$Q_g$	Total gate charge	—	27	—	nC	$I_D = 11A,$ $V_{DS}=160V,$ $V_{GS} = 10V$
$Q_{gs}$	Gate-to-Source charge	—	5.4	—		
$Q_{gd}$	Gate-to-Drain("Miller") charge	—	11	—		
$t_{d(on)}$	Turn-on delay time	—	11	—	nS	$V_{GS}=10V, V_{DD} = 100V,$ $R_L=9.2\Omega, R_{GEN}=2.55\Omega$ $I_D = 11A$
$t_r$	Rise time	—	23	—		
$t_{d(off)}$	Turn-Off delay time	—	22	—		
$t_f$	Fall time	—	5.2	—		
$C_{iss}$	Input capacitance	—	1010	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output capacitance	—	240	—		$V_{DS} = 25V$
$C_{rss}$	Reverse transfer capacitance	—	57	—		$f = 1\text{MHz}$

## Source-Drain Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	18 ①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode)	—	—	72	A	
$V_{SD}$	Diode Forward Voltage	—	0.87	1.3	V	$I_S=11A, V_{GS}=0V, T_J = 25^\circ\text{C}$
$t_{rr}$	Reverse Recovery Time	—	128	—	nS	$T_J = 25^\circ\text{C}, I_F = 11A,$ $di/dt = 100A/\mu s$
$Q_{rr}$	Reverse Recovery Charge	—	819	—	nC	

## Test circuits and Waveforms

**EAS Test Circuit**

**Gate charge test circuit**

**Switching Time Test Circuit**

**Switching Waveforms**


### Notes:

- ① Calculated continuous current based on maximum allowable junction temperature.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- ④ The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with  $T_A = 25^\circ\text{C}$

## Typical electrical and thermal characteristics

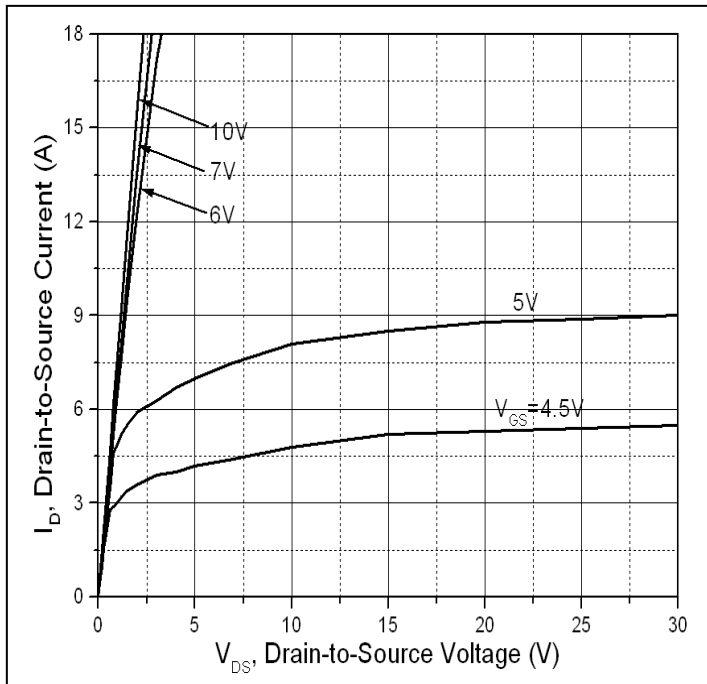


Figure 1: Typical Output Characteristics

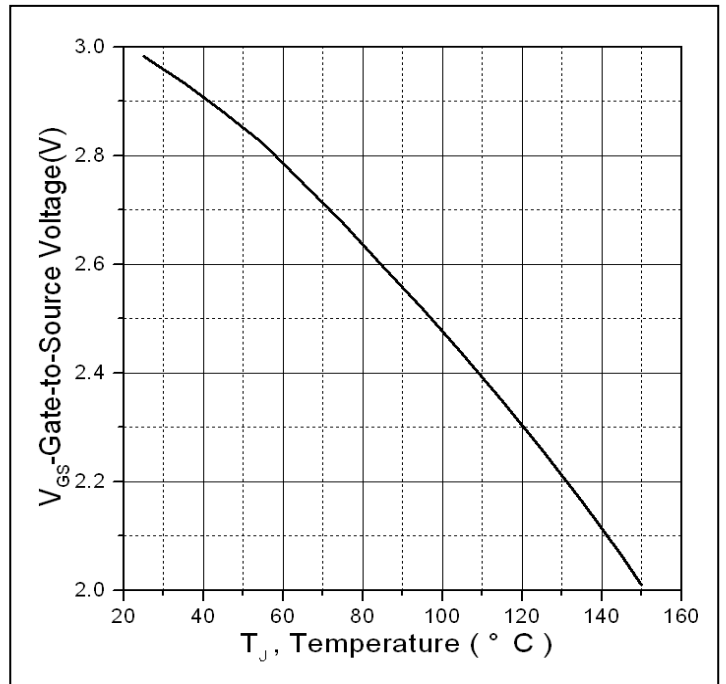


Figure 2. Gate to source cut-off voltage

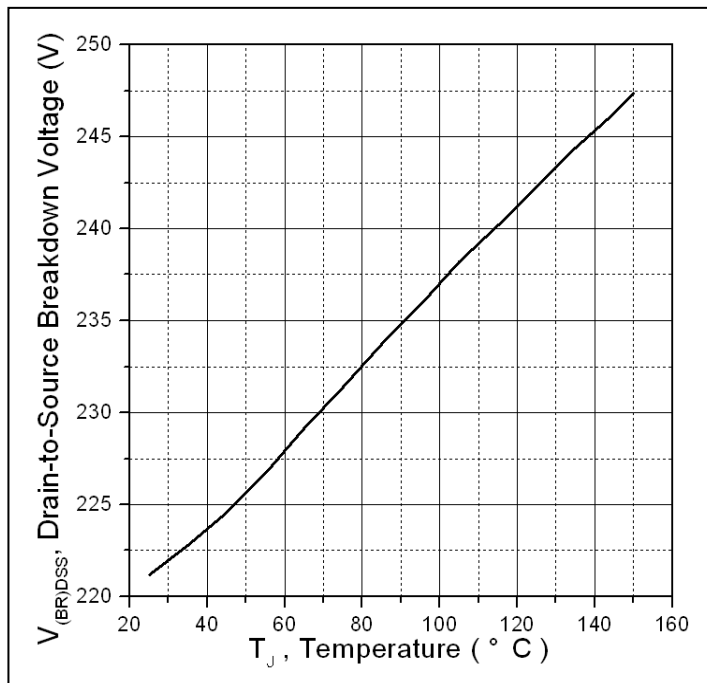


Figure 3. Drain-to-Source Breakdown Voltage vs. Temperature

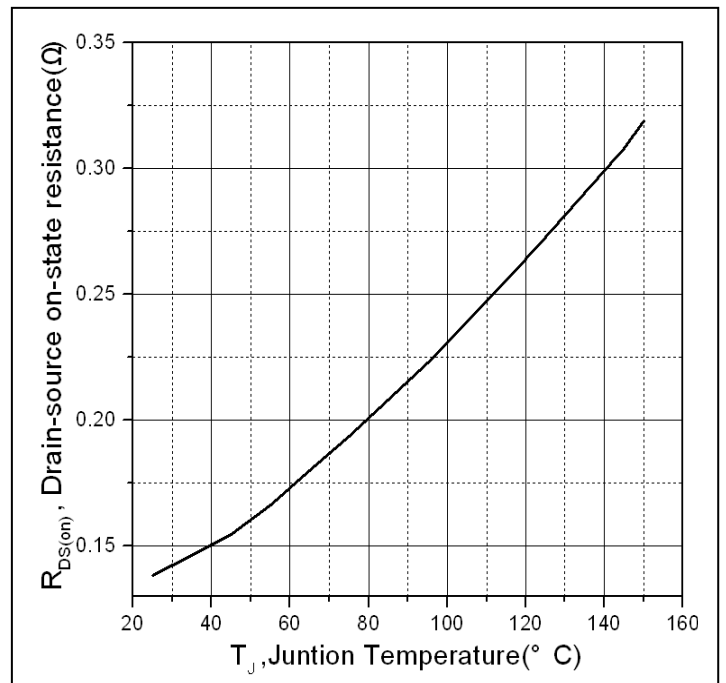


Figure 4: Normalized On-Resistance Vs. Case Temperature

## Typical electrical and thermal characteristics

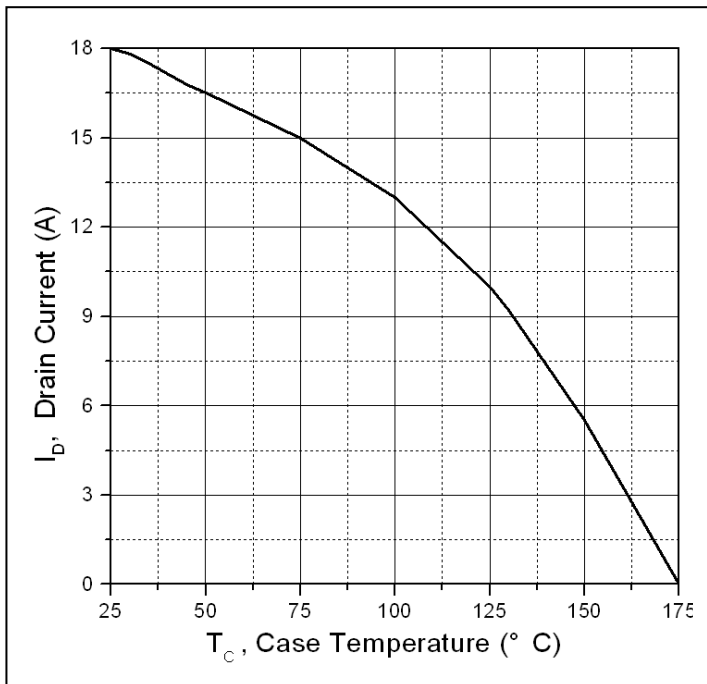


Figure 5. Maximum Drain Current Vs. Case Temperature

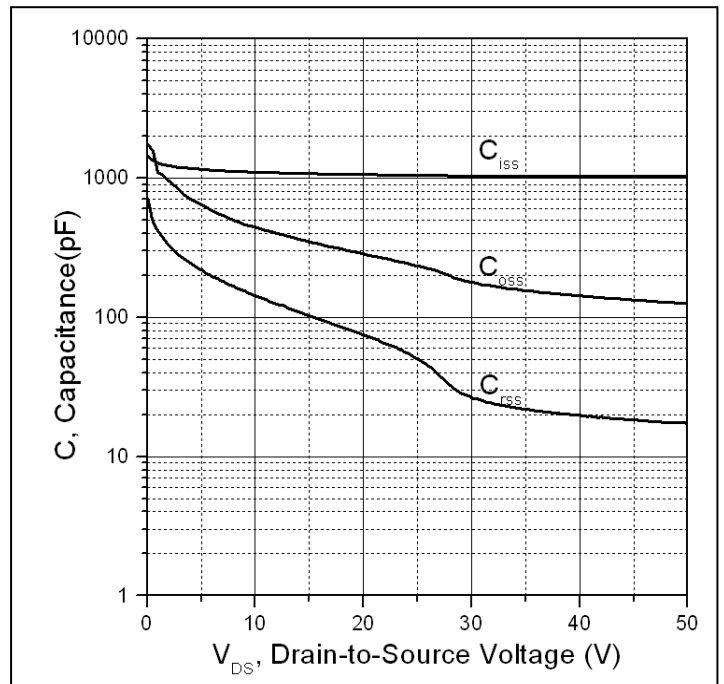


Figure 6. Typical Capacitance Vs. Drain-to-Source Voltage

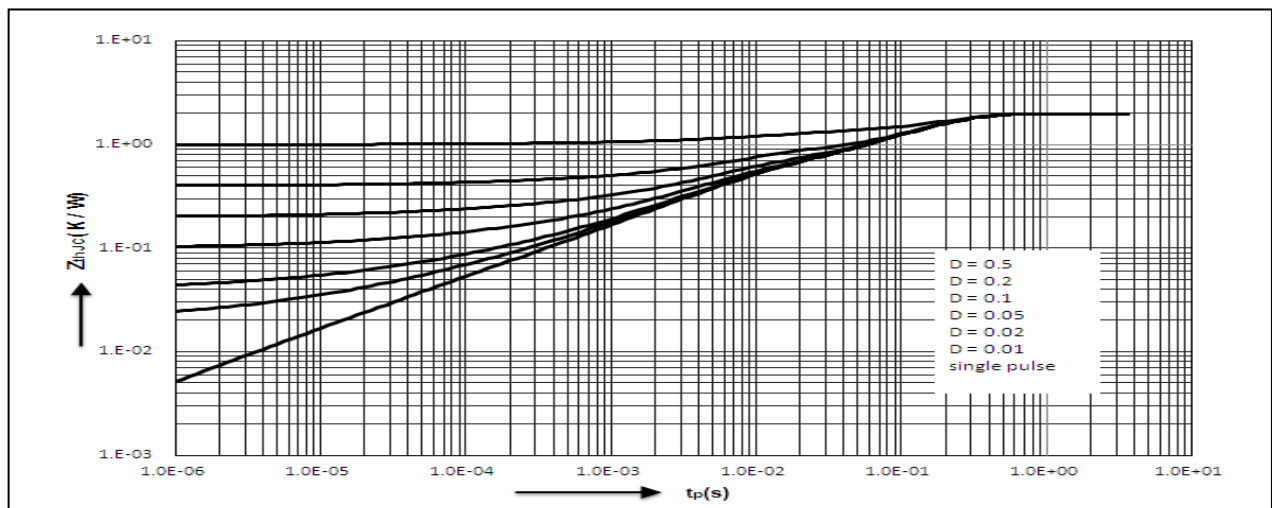
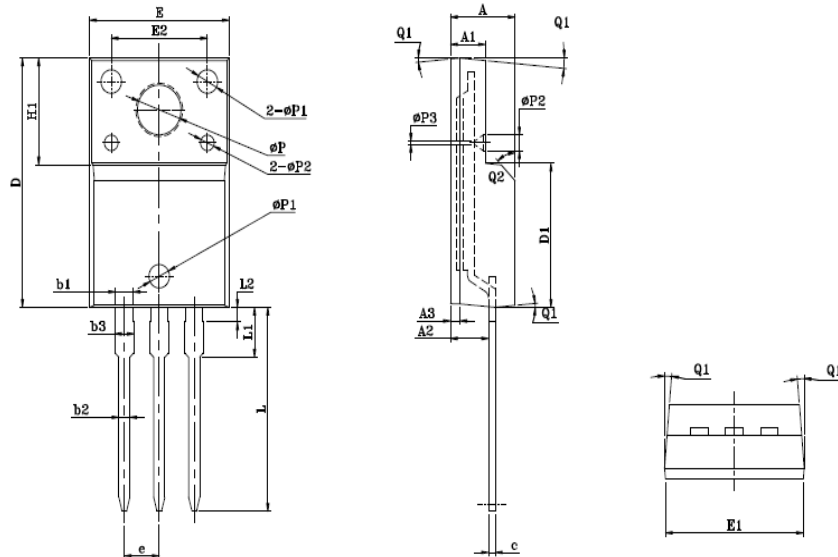


Figure 7. Maximum Effective Transient Thermal Impedance, Junction-to-Case

**Mechanical Data:**
**TO220F PACKAGE OUTLINE DIMENSION\_GN**


Symbol	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
E	9.960	10.160	10.360	0.392	0.400	0.408
E1	9.840	10.040	10.240	0.387	0.395	0.403
E2	6.800	7.000	7.200	0.268	0.276	0.283
A	4.600	4.700	4.800	0.181	0.185	0.189
A1	2.440	2.540	2.640	0.096	0.100	0.104
A2	2.660	2.760	2.860	0.105	0.109	0.113
A3	0.600	0.700	0.800	0.024	0.028	0.031
c	-	0.500	-	-	0.020	-
D	15.780	15.870	15.980	0.621	0.625	0.629
D1	8.970	9.170	9.370	0.353	0.361	0.369
H1	6.500	6.700	6.800	0.256	0.264	0.268
e	2.54BSC			0.10BSC		
φP	3.080	3.180	3.280	0.121	0.125	0.129
φP1	1.400	1.500	1.600	0.055	0.059	0.063
φP2	0.900	1.000	1.100	0.035	0.039	0.043
φP3	0.100	0.200	0.300	0.004	0.008	0.012
L	12.780	12.980	13.180	0.503	0.511	0.519
L1	2.970	3.170	3.370	0.117	0.125	0.133
L2	0.830	0.930	1.030	0.033	0.037	0.041
Q1	3°	5°	7°	3°	5°	7°
Q2	43°	45°	47°	43°	45°	47°
b1	1.180	1.280	1.380	0.046	0.050	0.054
b2	0.760	0.800	0.840	0.030	0.031	0.033
b3	-	-	1.420	-	-	0.056

**Ordering and Marking Information****Device Marking: SSPL2015F**

**Package (Available)**  
**TO-220F**  
**Operating Temperature Range**  
**C : -55 to175 °C**

**Devices per Unit**

<b>Package Type</b>	<b>Units/ Tube</b>	<b>Tubes/Inner Box</b>	<b>Units/Inner Box</b>	<b>Inner Boxes/Carton Box</b>	<b>Units/Carton Box</b>
TO-220F	50	20	1000	6	6000

**Reliability Test Program**

<b>Test Item</b>	<b>Conditions</b>	<b>Duration</b>	<b>Sample Size</b>
<b>High Temperature Reverse Bias(HTRB)</b>	$T_j=125^{\circ}\text{C}$ to $175^{\circ}\text{C}$ @ 80% of Max $V_{DSS}/V_{CES}/V_R$	168 hours 500 hours 1000 hours	3 lots x 77 devices
<b>High Temperature Gate Bias(HTGB)</b>	$T_j=125^{\circ}\text{C}$ or $175^{\circ}\text{C}$ @ 100% of Max $V_{GSS}$	168 hours 500 hours 1000 hours	3 lots x 77 devices

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