

# SST2622

**520mA, 50V, R<sub>DS(ON)</sub> 1.8Ω**
**N-Channel Enhancement Mode Power Mos.FET**

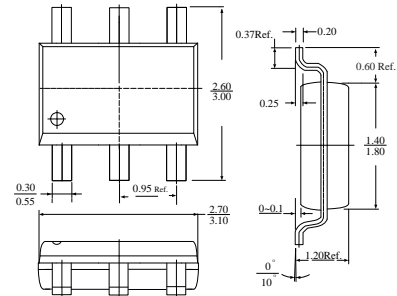
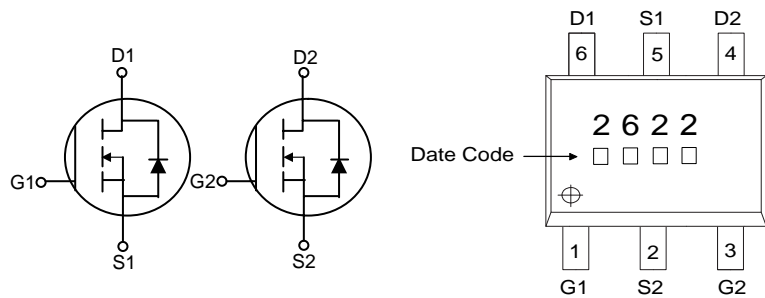
## Description

The SST2622 utilized advance processing techniques to achieve the lowest possible on-resistance, extremely efficient and cost-effectiveness device. The SOT-26 is universally used for all commercial-industrial applications.

## Features

- \* RoHS Compliant
- \* Low Gate Charge
- \* Surface Mount Package

### SOT-26


*Dimensions in millimeters*


## Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V <sub>DS</sub>	50	V
Gate-Source Voltage	V <sub>GS</sub>	±20	V
Continuous Drain Current <sup>3</sup> , V <sub>GS</sub> @10V	I <sub>D</sub> @T <sub>A</sub> =25°C	520	mA
Continuous Drain Current <sup>3</sup> , V <sub>GS</sub> @10V	I <sub>D</sub> @T <sub>A</sub> =70°C	410	mA
Pulsed Drain Current <sup>1</sup>	I <sub>DM</sub>	1.5	A
Total Power Dissipation	P <sub>D</sub> @T <sub>A</sub> =25°C	0.8	W
Linear Derating Factor		0.006	W/°C
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55~+150	°C

## Thermal Data

Parameter	Symbol	Ratings	Unit
Thermal Resistance Junction-ambient <sup>3</sup> (Max)	R <sub>thj-a</sub>	150	°C/W

## Electrical Characteristics( T<sub>j</sub>=25 °C Unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	50	-	-	V	V <sub>GS</sub> =0V, I <sub>D</sub> = 250uA
Breakdown Voltage Temp. Coefficient	ΔBV <sub>DSS</sub> /ΔT <sub>j</sub>	-	0.06	-	V/ °C	Reference to 25°C, I <sub>D</sub> = 1mA
Gate Threshold Voltage	V <sub>GS(th)</sub>	1.0	-	3.0	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA
Gate-Source Leakage Current	I <sub>GSS</sub>	-	-	± 30	uA	V <sub>GS</sub> =±20V
Drain-Source Leakage Current (T <sub>j</sub> =25°C)	I <sub>DSS</sub>	-	-	10	uA	V <sub>DS</sub> =50V, V <sub>GS</sub> =0
Drain-Source Leakage Current (T <sub>j</sub> =70°C)		-	-	100	uA	V <sub>DS</sub> = 40V, V <sub>GS</sub> =0
Static Drain-Source On-Resistance <sup>2</sup>	R <sub>DS(ON)</sub>	-	-	1.8	Ω	V <sub>GS</sub> =10V, I <sub>D</sub> =500mA
		-	-	3.2		V <sub>GS</sub> =4.5V, I <sub>D</sub> =200mA
Total Gate Charge <sup>2</sup>	Q <sub>g</sub>	-	1	1.6	nC	I <sub>D</sub> =500mA V <sub>DS</sub> =40V V <sub>GS</sub> =4.5V
Gate-Source Charge	Q <sub>gs</sub>	-	0.5	-		
Gate-Drain ("Miller") Charge	Q <sub>gd</sub>	-	0.5	-		
Turn-on Delay Time <sup>2</sup>	T <sub>d(ON)</sub>	-	12	-	nS	V <sub>DD</sub> = 25V I <sub>D</sub> = 500mA V <sub>GS</sub> =10V R <sub>G</sub> =3.3Ω R <sub>D</sub> =50Ω
Rise Time	T <sub>r</sub>	-	10	-		
Turn-off Delay Time	T <sub>d(Off)</sub>	-	56	-		
Fall Time	T <sub>f</sub>	-	29	-		
Input Capacitance	C <sub>iss</sub>	-	32	50	pF	V <sub>GS</sub> =0V V <sub>DS</sub> =25V f=1.0MHz
Output Capacitance	C <sub>oss</sub>	-	8	-		
Reverse Transfer Capacitance	C <sub>rss</sub>	-	6	-		
Forward Transconductance	G <sub>fs</sub>	-	600	-	mS	V <sub>DS</sub> =10V, I <sub>D</sub> =500mA

## Source-Drain Diode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Forward On Voltage <sup>2</sup>	V <sub>SD</sub>	-	-	1.3	V	I <sub>S</sub> =600mA, V <sub>GS</sub> =0V.

Notes: 1. Pulse width limited by Max. junction temperature.

2. Pulse width ≤300us, dutycycle ≤2%.

3. Surface mounted on 1 in<sup>2</sup> copper pad of FR4 board; 250°C/W when mounted on min. copper pad.

### Characteristics Curve

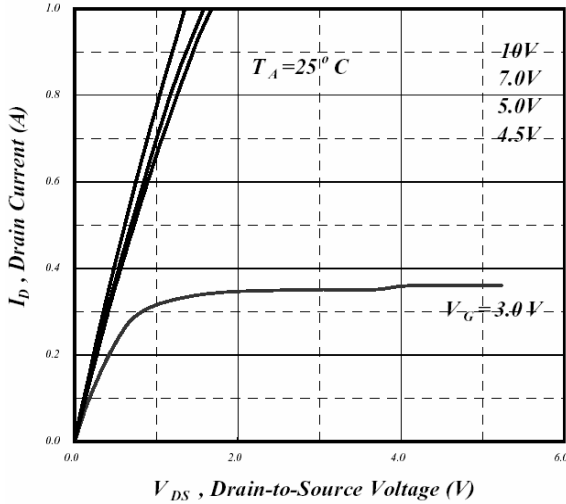


Fig 1. Typical Output Characteristics

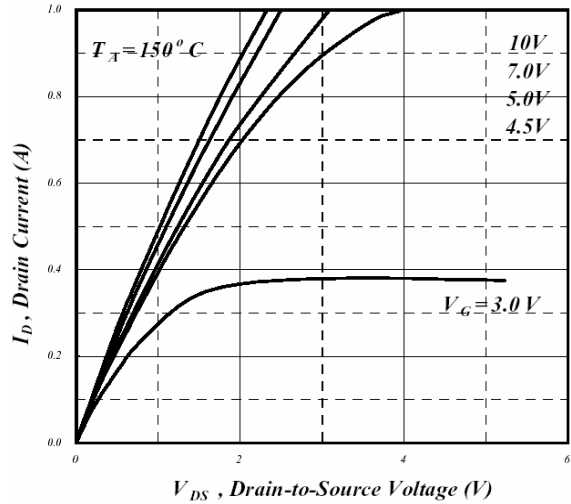


Fig 2. Typical Output Characteristics

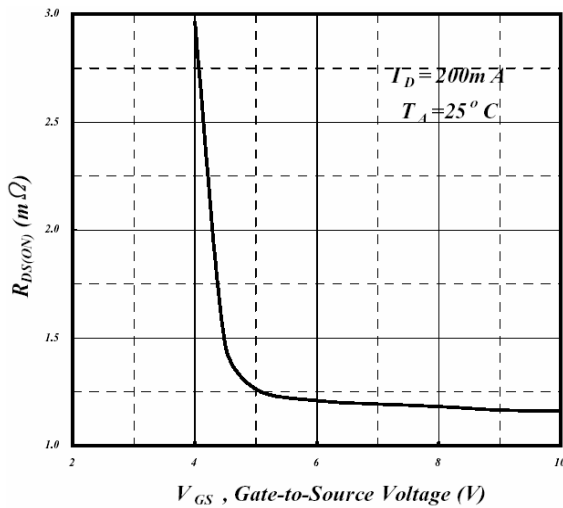


Fig 3. On-Resistance v.s. Gate Voltage

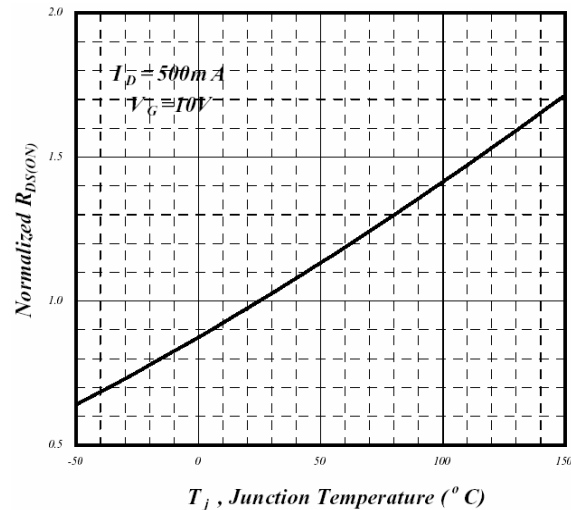


Fig 4. Normalized On-Resistance v.s. Junction Temperature

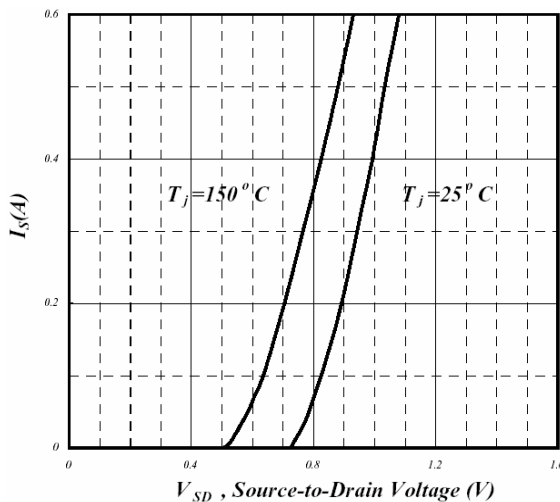


Fig 5. Forward Characteristics of Reverse Diode

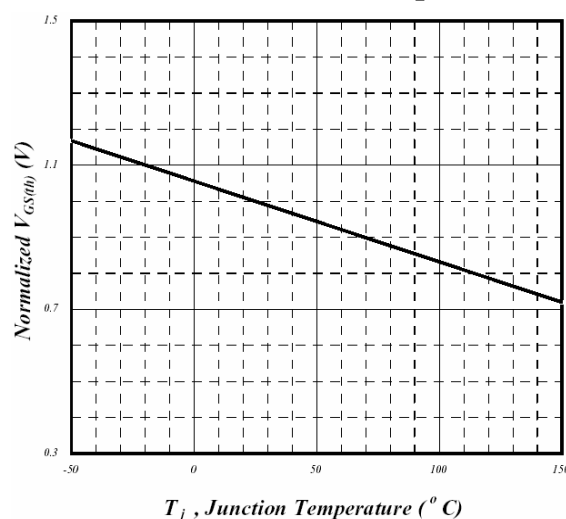


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

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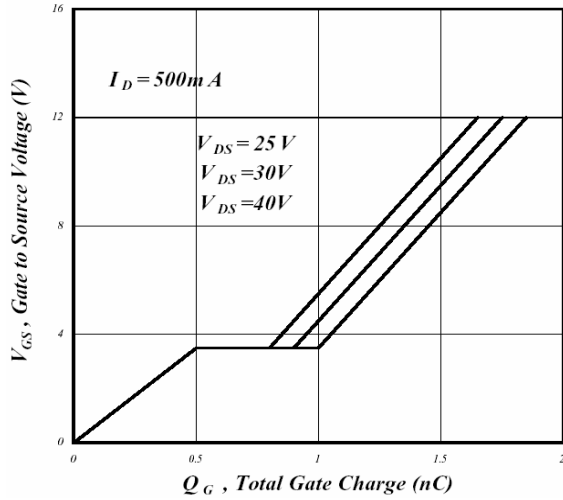


Fig 7. Gate Charge Characteristics

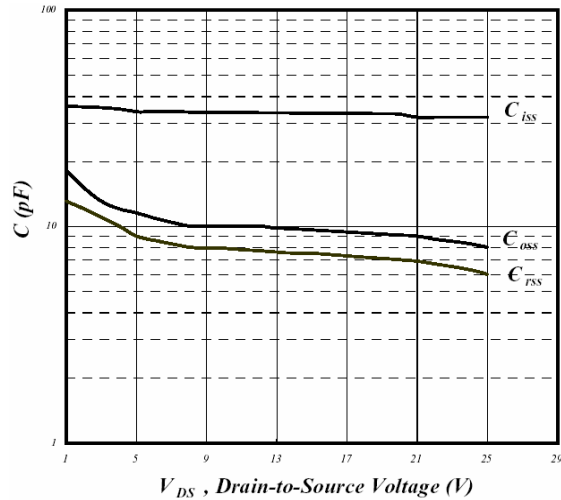


Fig 8. Typical Capacitance Characteristics

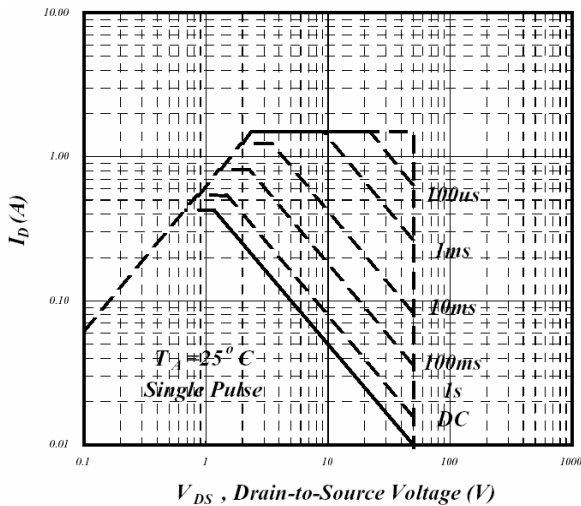


Fig 9. Maximum Safe Operating Area

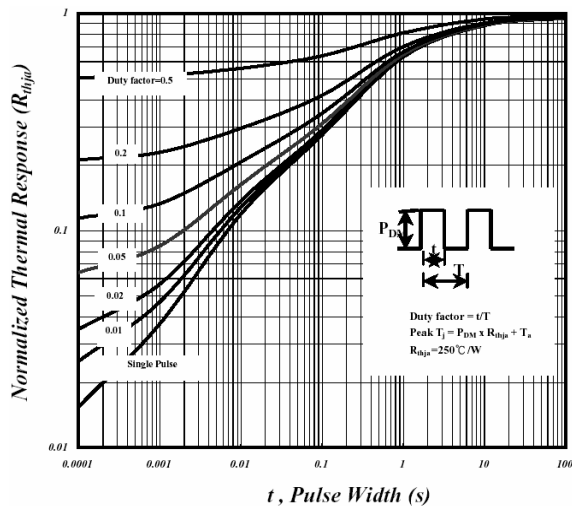


Fig 10. Effective Transient Thermal Impedance

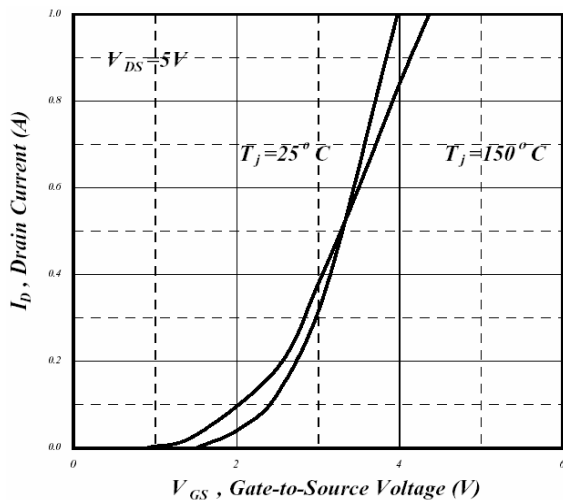


Fig 11. Transfer Characteristics

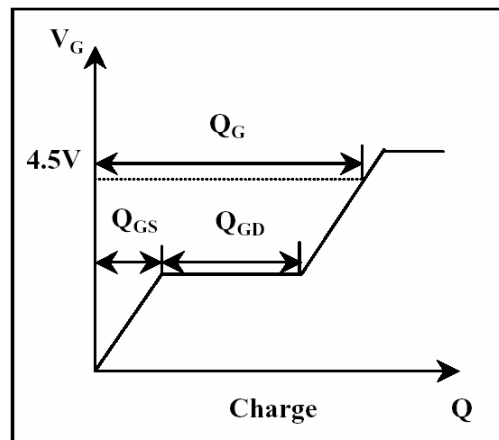


Fig 12. Gate Charge Waveform