4 Mbit Flash + 1 Mbit SRAM ComboMemory

SST31LF041 / SST31LF041A

Preliminary Specifications

FEATURES:

- **Monolithic Flash + SRAM ComboMemory**
  - SST31LF041/041A: 512K x8 Flash + 128K x8 SRAM
- **Single 3.0-3.6V Read and Write Operations**
- **Concurrent Operation**
  - Read from or Write to SRAM while Erase/Program Flash
- **Superior Reliability**
  - Endurance: 100,000 Cycles (typical)
  - Greater than 100 years Data Retention
- **Low Power Consumption:**
  - Active Current: 10 mA (typical) for Flash and 20 mA (typical) for SRAM Read
  - Standby Current: 10 µA (typical)
- **Flash Sector-Erase Capability**
  - Uniform 4 KByte sectors
- **Latched Address and Data for Flash**
- **Fast Read Access Times:**
  - SST31LF041/041A Flash: 70 ns, SRAM: 70 ns
  - SST31LF041A Flash: 300 ns, SRAM: 300 ns
- **Flash Fast Erase and Byte-Program:**
  - Sector-Erase Time: 18 ms (typical)
  - Bank-Erase Time: 70 ms (typical)
  - Byte-Program Time: 14 µs (typical)
  - Bank Rewrite Time: 8 seconds (typical)
- **Flash Automatic Erase and Program Timing**
  - Internal V_{PP} Generation
- **Flash End-of-Write Detection**
  - Toggle Bit
  - Data# Polling
- **CMOS I/O Compatibility**
- **JEDEC Standard Command Set**
- **Packages Available**
  - 32-lead TSOP (8mm x 14mm) SST31LF041A
  - 40-lead TSOP (10mm x 14mm) SST31LF041

PRODUCT DESCRIPTION

The SST31LF041/041A devices are a 512K x8 CMOS flash memory bank combined with a 128K x8 CMOS SRAM memory bank manufactured with SST's proprietary, high performance SuperFlash technology. The SST31LF041/041A devices write (SRAM or flash) with a 3.0-3.6V power supply. The monolithic SST31LF041/041A devices conform to Software Data Protect (SDP) commands for x8 EEPROMs.

Featuring high performance Byte-Program, the flash memory bank provides a maximum Byte-Program time of 20 µsec. The entire flash memory bank can be erased and programmed byte-by-byte in typically 8 seconds, when using interface features such as Toggle Bit or Data# Polling to indicate the completion of Program operation. To protect against inadvertent flash write, the SST31LF041/041A devices have on-chip hardware and Software Data Protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, the SST31LF041/041A devices are offered with a guaranteed endurance of 10,000 cycles. Data retention is rated at greater than 100 years.

The SST31LF041/041A operate as two independent memory banks with respective bank enable signals. The SRAM and flash memory banks are superimposed in the same memory address space. Both memory banks share common address lines, data lines, WE# and OE#. The memory bank selection is done by memory bank enable signals. The SRAM bank enable signal, BES# selects the SRAM bank and the flash memory bank enable signal, BEF# selects the flash memory bank. The WE# signal has to be used with Software Data Protection (SDP) command sequence when controlling the Erase and Program operations in the flash memory bank. The SDP command sequence protects the data stored in the flash memory bank from accidental alteration.

The SST31LF041/041A provide the added functionality of being able to simultaneously read from or write to the SRAM bank while erasing or programming in the flash memory bank. The SRAM memory bank can be read or written while the flash memory bank performs Sector-Erase, Bank-Erase, or Byte-Program concurrently. All flash memory Erase and Program operations will automatically latch the input address and data signals and complete the operation in background without further input stimulus requirement. Once the internally controlled Erase or Program cycle in the flash bank has commenced, the SRAM bank can be accessed for Read or Write.

The SST31LF041/041A devices are suited for applications that use both nonvolatile flash memory and volatile SRAM memory to store code or data. For all system applications, the SST31LF041/041A devices significantly improve performance and reliability, while lowering power consumption, when compared with multiple chip solutions. The

SST31LF041/041A inherently use less energy during Erase and Program than alternative flash technologies. When programming a flash device, the total energy consumed is a function of the applied voltage, current, and time of application. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter Erase time, the total energy consumed during any Erase or Program operation is less than alternative flash technologies. The monolithic ComboMemory eliminates redundant functions when using two separate memories of similar architecture; therefore, reducing the total power consumption.

The SuperFlash technology provides fixed Erase and Program times, independent of the number of Erase/Program cycles that have occurred. Therefore the system software or hardware does not have to be modified or de-rated as is necessary with alternative flash technologies, whose Erase and Program times increase with accumulated Erase/Program cycles.

The SST31LF041/041A devices also improve flexibility by using a single package and a common set of signals to perform functions previously requiring two separate devices. To meet high density, surface mount requirements, the SST31LF041 device is offered in 40-lead TSOP package and the SST31LF041A device is offered in 32-lead TSOP package. See Figures 1 and 2 for the pinouts.

Device Operation

The ComboMemory uses BES# and BEF# to control operation of either the SRAM or the flash memory bank. Bus contention is eliminated as the monolithic device will not recognize both bank enables as being simultaneously active. If both bank enables are asserted (i.e., BEF# and BES# are both low), the BEF# will dominate while the BES# is ignored and the appropriate operation will be executed in the flash memory bank. SST does not recommend that both bank enables be simultaneously asserted. All other address, data, and control lines are shared which minimizes power consumption and area. The device goes into standby when both bank enables are raised to V_{IHC}. See Table 3 for SRAM operation mode selection.

For SST31LF041A only: BES# and OE# share pin 32. During SRAM operation, pin 32 will function as BES#. During flash operation, pin 32 will function as OE#. When pin 32 (OE#/BES#) is high, the data bus is in high impedance state.

SRAM Operation

With BES# low and BEF# high, the SST31LF041/041A operate as a 128K x8 CMOS SRAM with fully static operation requiring no external clocks or timing strobes. The SRAM is mapped into the first 128 KByte address space of the device for 041/041A. Read and Write cycle times are equal.

SRAM Read

The SRAM Read operation of the SST31LF041/041A are controlled by OE# and BES#, both have to be low with WE# high, for the system to obtain data from the outputs. BES# is used for SRAM bank selection. When BES# and BEF# are high, both memory banks are deselected. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when OE# is high. See Figure 3 for the Read cycle timing diagram.

SRAM Write

The SRAM Write operation of the SST31LF041/041A is controlled by WE# and BES#; both have to be low for the system to write to the SRAM. BES# is used for SRAM bank selection. During the Byte-Write operation, the addresses and data are referenced to the rising edge of either BES# or WE#, whichever occurs first. The Write time is measured from the last falling edge to the first rising edge of BES# and WE#. OE# can be V_{IL} or V_{IH}, but no other value, for SRAM Write operations. See Figure 4 for the SRAM Write cycle timing diagram.

Flash Operation

With BEF# active, the SST31LF041/041A operate as a 512K x8 flash memory. The flash memory bank is read using the common address lines, data lines, WE# and OE#. Erase and Program operations are initiated with the JEDEC standard SDP command sequences. Address and data are latched during the SDP commands and internally timed Erase and Program operations. See Table 3 for flash operation mode selection.

Flash Read

The Read operation of the SST31LF041/041A devices are controlled by BEF# and OE#; both have to be low, with WE# high, for the system to obtain data from the outputs. BEF# is used for flash memory bank selection. When BEF# and BES# are high, both banks are deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when OE# is high. See Figure 5 for the Read cycle timing diagram.

Flash Erase/Program Operation

SDP commands are used to initiate the flash memory bank Program and Erase operations of the SST31LF041/041A. SDP commands are loaded to the flash memory bank using standard microprocessor write sequences. A command is loaded by asserting WE# low while keeping BEF# low and OE# high. The address is latched on the falling edge of WE# or BEF#, whichever occurs last. The data is latched on the rising edge of WE# or BEF#, whichever occurs first.

Flash Byte-Program Operation

The flash memory bank of the SST31LF041/041A devices are programmed on a byte-by-byte basis. Before the Program operations, the memory must be erased first. The Program operation consists of three steps. The first step is the three-byte load sequence for Software Data Protection. The second step is to load byte address and byte data. During the Byte-Program operation, the addresses are latched on the falling edge of either BEF# or WE#, whichever occurs last. The data is latched on the rising edge of either BEF# or WE#, whichever occurs first. The third step is the internal Program operation which is initiated after the rising edge of the fourth WE# or BEF#, whichever occurs first. The Program operation, once initiated, will be completed, within 20 µs. See Figures 6 and 7 for WE# and BEF# controlled Program operation timing diagrams and Figure 17 for flowcharts. During the Program operation, the only valid Flash Read operations are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any SDP commands loaded during the internal Program operation will be ignored.

Flash Sector-Erase Operation

The Sector-Erase operation allows the system to erase the flash memory bank on a sector-by-sector basis. The sector architecture is based on uniform sector size of 4 KByte. The Sector-Erase operation is initiated by executing a six-byte command load sequence for Software Data Protection with Sector-Erase command (30H) and sector address (SA) in the last bus cycle. The address lines A_{18}-A_{12} will be used to determine the sector address. The sector address is latched on the falling edge of the sixth WE# pulse, while the command (30H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. The End-of-Erase can be determined using either Data# Polling or Toggle Bit methods. See Figure 10 for timing waveforms. Any SDP commands loaded during the Sector-Erase operation will be ignored.

Flash Bank-Erase Operation

The SST31LF041/041A flash memory bank provides a Bank-Erase operation, which allows the user to erase the entire flash memory bank array to the '1's state. This is useful when the entire bank must be quickly erased. The Bank-Erase operation is initiated by executing a six-byte Software Data Protection command sequence with Bank-Erase command (10H) with address 5555H in the last byte sequence. The internal Erase operation begins with the rising edge of the sixth WE# or BEF# pulse, whichever occurs first. During the internal Erase operation, the only valid Flash Read operations are Toggle Bit and Data# Polling. See Table 4 for the command sequence, Figure 11 for timing diagram, and Figure 20 for the flowchart. Any SDP commands loaded during the Bank-Erase operation will be ignored.

Flash Write Operation Status Detection

The SST31LF041/041A flash memory bank provides two software means to detect the completion of a flash memory bank Write (Program or Erase) cycle, in order to optimize the system Write cycle time. The software detection includes two status bits: Data# Polling (DQ_7) and Toggle Bit (DQ_6). The End-of-Write detection mode is enabled after the rising edge of WE#, which initiates the internal Program or Erase operation. The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit Read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ_7 or DQ_6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

Flash Data# Polling (DQ_7)

When the SST31LF041/041A flash memory bank is in the internal Program operation, any attempt to read DQ_7 will produce the complement of the true data. Once the Program operation is completed, DQ_7 will produce true data. Note that even though DQ_7 may have valid data immediately following the completion of an internal Write operation, the remaining data outputs may still be invalid: valid data on the entire data bus will appear in subsequent successive Read cycles after an interval of 1 µs. During internal Erase operation, any attempt to read DQ_7 will produce a '0'. Once the internal Erase operation is completed, DQ_7 will produce a '1'. The Data# Polling is valid after the rising edge of the fourth WE# (or BEF#) pulse for Program operation. For Sector or Bank-Erase, the Data# Polling is valid after the rising edge of the sixth WE# (or BEF#) pulse. See Figure 8 for Data# Polling timing diagram and Figure 18 for a flowchart.

Flash Toggle Bit (DQ_6)

During the internal Program or Erase operation, any consecutive attempts to read DQ_6 will produce alternating 0s and 1s, i.e., toggling between 0 and 1. When the internal Program or Erase operation is completed, the toggling will stop. The flash memory bank is then ready for the next operation. The Toggle Bit is valid after the rising edge of the fourth WE# (or BE#) pulse for Program operation. For Sector or Bank-Erase, the Toggle Bit is valid after the rising edge of the sixth WE# (or BEF#) pulse. See Figure 9 for Toggle Bit timing diagram and Figure 18 for a flowchart.

Flash Memory Data Protection

The SST31LF041/041A flash memory bank provides both hardware and software features to protect nonvolatile data from inadvertent writes.

Flash Hardware Data Protection

Noise/Glitch Protection: A WE# or BEF# pulse of less than 5 ns will not initiate a Write cycle.

V_{DD} Power Up/Down Detection: The Write operation is inhibited when is less than 1.5V.

Write Inhibit Mode: Forcing OE# low, BEF# high, or WE# high will inhibit the Flash Write operation. This prevents inadvertent writes during power-up or power-down.

Flash Software Data Protection (SDP)

The SST31LF041/041A provide the JEDEC approved Software Data Protection scheme for all flash memory bank data alteration operations, i.e., Program and Erase. Any Program operation requires the inclusion of a series of three-byte sequence. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of six-byte load sequence. The SST31LF041/041A devices are shipped with the Software Data Protection permanently enabled. See Table 4 for the specific software command codes. During SDP command sequence, invalid SDP commands will abort the device to the Read mode, within T_{RC}.

Concurrent Read and Write Operations

The SST31LF041/041A provide the unique benefit of being able to read from or write to SRAM, while simultaneously erasing or programming the flash. The device will ignore all SDP commands when an Erase or Program operation is in progress. This allows data alteration code to be executed from SRAM, while altering the data in flash. The following table lists all valid states. SST does not recommend that both bank enables, BEF# and BES#, be simultaneously asserted.

CONCURRENT READ/WRITE STATE TABLE

Flash	SRAM
Program/Erase	Read
Program/Erase	Write

Note that Product Identification commands use SDP; therefore, these commands will also be ignored while an Erase or Program operation is in progress.

Product Identification

The Product Identification mode identifies the devices as either SST31LF041 or SST31LF041A and the manufacturer as SST. This mode may be accessed by hardware or software operations. The hardware device ID Read operation is typically used by a programmer to identify the correct algorithm for the SST31LF041/041A flash memory banks. Users may wish to use the software Product Identification operation to identify the part (i.e., using the device ID) when using multiple manufacturers in the same socket. For details, see Table 3 for hardware operation or Table 4 for software operation, Figure 12 for the software ID entry and read timing diagram and Figure 19 for the ID entry command sequence flowchart.

TABLE 1: PRODUCT IDENTIFICATION

	Address	Data
Manufacturer's ID	0000H	BFH
Device ID		
SST31LF041	0001H	17H
SST31LF041A	0001H	16H

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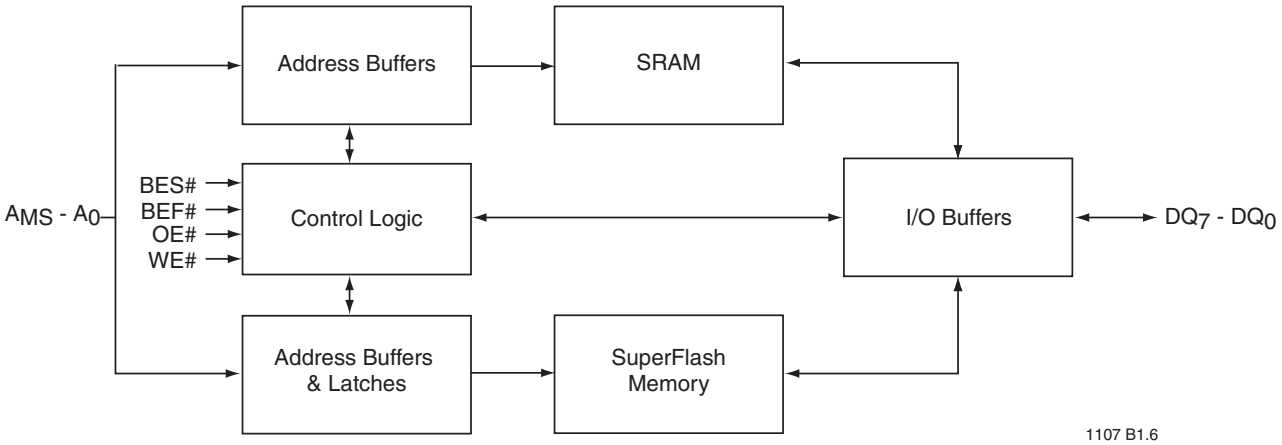
Product Identification Mode Exit/Reset

In order to return to the standard Read mode, the Software Product Identification mode must be exited. Exiting is accomplished by issuing the Exit ID command sequence, which returns the device to the Read operation. Please note that the software reset command is ignored during an internal Program or Erase operation. See Table 4 for software command codes, Figure 13 for timing waveform and Figure 19 for a flowchart.

Design Considerations

SST recommends a high frequency 0.1 µF ceramic capacitor to be placed as close as possible between V_{DD} and V_{SS}, e.g., less than 1 cm away from the V_{DD} pin of the device. Additionally, a low frequency 4.7 µF electrolytic capacitor from V_{DD} to V_{SS} should be placed within 1 cm of the V_{DD} pin.

FUNCTIONAL BLOCK DIAGRAM



A_{MS} = Most Significant Address

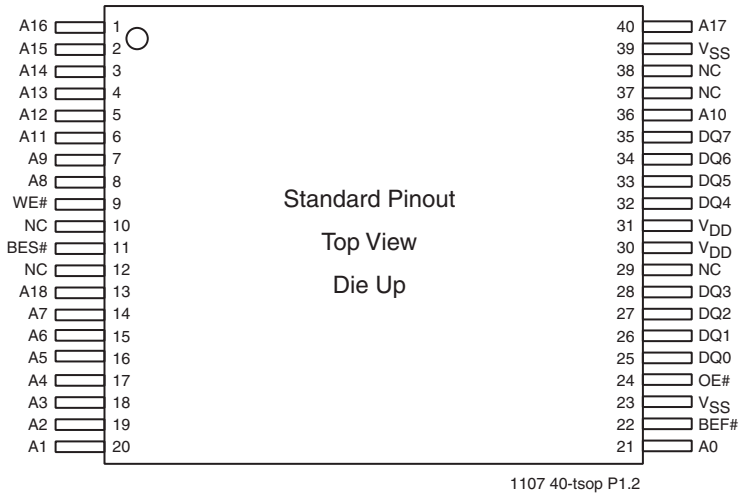


FIGURE 1: PIN ASSIGNMENTS FOR 40-LEAD TSOP (10MM X 14MM) - SSTLF041

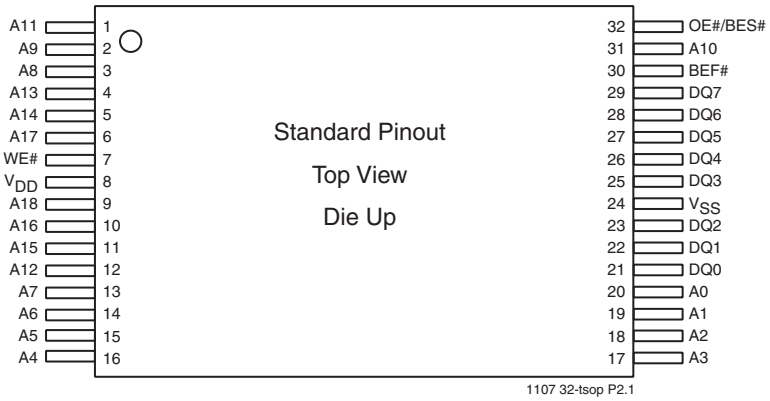


FIGURE 2: PIN ASSIGNMENTS FOR 32-LEAD TSOP (8MM X 14MM) - SSTLF041A

TABLE 2: PIN DESCRIPTION

Symbol	Pin Name	Functions
A_{MS}[1]-A_0	Address Inputs	To provide memory addresses. A_{18}-A_0 to provide flash address A_{16}-A_0 to provide SRAM addresses for SST32LF041/041A During flash Sector-Erase, A_{18}-A_{12} address lines will select the sector.
DQ_7-DQ_0	Data Input/output	To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a flash Erase/Program cycle. The outputs are in tri-state when OE# or BES# and BEF# are high.
BES#	SRAM Memory Bank Enable	To activate the SRAM memory bank when BES# is low. Note: For SST31LF041A, BES# and OE# share pin 32.
BEF#	Flash Memory Bank Enable	To activate the Flash memory bank when BEF# is low.
OE#	Output Enable	To gate the data output buffers. Note: For SST31LF041A, BES# and OE# share pin 32.
WE#	Write Enable	To control the Write operations.
V_{DD}	Power Supply	3.0-3.6V Power Supply
V_{SS}	Ground	

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1. A_{MS} = Most significant address

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TABLE 3: OPERATION MODES SELECTION

Mode	BES#[1]	BEF#[1]	OE#	WE#	A_9	DQ	Address
Flash							
Read	X[2]	V_{IL}	V_{IL}	V_{IH}	A_{IN}	D_{OUT}	A_{IN}
Program	X	V_{IL}	V_{IH}	V_{IL}	A_{IN}	D_{IN}	A_{IN}
Erase	X	V_{IL}	V_{IH}	V_{IL}	X	X	Sector address, XXH for Bank-Erase
SRAM							
Read	V_{IL}	V_{IH}	V_{IL}	V_{IH}	A_{IN}	D_{OUT}	A_{IN}
Write	V_{IL}	V_{IH}	X	V_{IL}	A_{IN}	D_{IN}	A_{IN}
Standby	V_{IHC}	V_{IHC}	X	X	X	High Z	X
Flash Write Inhibit	X	X	V_{IL}	X	X	High Z / D_{OUT}	X
	X	X	X	V_{IH}	X	High Z / D_{OUT}	X
	X	V_{IH}	X	X	X	High Z / D_{OUT}	X
Product Identification							
Hardware Mode	X	V_{IL}	V_{IL}	V_{IH}	V_H	Manufacturer's ID (BFH) Device ID[3]	A_{18}-A_1=V_{IL}, A_0=V_{IL} A_{18}-A_1=V_{IL}, A_0=V_{IH}
Software Mode	X	V_{IL}	V_{IL}	V_{IH}	A_{IN}	ID Code	See Table 4

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1. BES# and BEF# cannot be asserted simultaneously. For SST31LF041A BES# and OE# share pin 32. When flash is active, pin 32 becomes OE#. When flash is inactive, pin 32 becomes BES#.
2. X can be V_{IL} or V_{IH}, but no other value.
3. Device ID 17H for SST31LF041 and 16H for SST31LF041A.

TABLE 4: SOFTWARE COMMAND SEQUENCE

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data
Byte-Program	5555H	AAH	2AAAH	55H	5555H	A0H	BA[2]	Data				
Sector-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA_X[3]	30H
Bank-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Software ID Entry[4,5]	5555H	AAH	2AAAH	55H	5555H	90H						
Software ID Exit	5555H	AAH	2AAAH	55H	5555H	F0H						

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1. Address format A_{14}-A_0 (Hex), Address A_{18}-A_{15} can be V_{IL} or V_{IH}, but no other value, for the Command sequence.
2. BA = Program Byte address
3. SA_X for Sector-Erase; uses A_{18}-A_{12} address lines
4. The device does not remain in Software Product ID mode if powered down.
5. With A_{18}-A_1 = 0; SST Manufacturer's ID = BFH, is read with A_0 = 0,
   SST31LF041 Device ID = 17H, is read with A_0 = 1,
   SST31LF041A Device ID = 16H, is read with A_0 = 1

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Operating Temperature . . . . . -20°C to +85°C
Storage Temperature . . . . . -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential . . . . . -0.5V to V_{DD}+0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential . . . . . -1.0V to V_{DD}+1.0V
Voltage on A_9 Pin to Ground Potential . . . . . -0.5V to 13.2V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Surface Mount Lead Soldering Temperature (3 Seconds) . . . . . 240°C
Output Short Circuit Current[1] . . . . . 50 mA

1. Outputs shorted for no more than one second. No more than one output shorted at a time.

OPERATING RANGE

Range	Ambient Temp	V_{DD}
Commercial	0°C to +70°C	3.0-3.6V
Extended	-20°C to +85°C	3.0-3.6V

AC CONDITIONS OF TEST

Input Rise/Fall Time	5 ns
Output Load	C_L = 30 pF
See Figures 15 and 16	

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TABLE 5: DC OPERATING CHARACTERISTICS (V_{DD} = 3.0-3.6V)

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{DD}	Power Supply Current				Address input = V_{ILT}/V_{IHT}, at f=1/T_{RC} Min, $V_{DD}=V_{DD}$ Max, all DQs open
	Read				OE#=V_{IL}, WE#=V_{IH}
	Flash		12	mA	BEF#=V_{IL}, BES#=V_{IH}
	SRAM		40	mA	BEF#=V_{IH}, BES#=V_{IL}
	Concurrent Operation		55	mA	BEF#=V_{IH}, BES#=V_{IL}
	Write				OE#=V_{IH}, WE#=V_{IL}
	Flash (Program)		15	mA	BEF#=V_{IL}, BES#=V_{IH}
	SRAM		40	mA	BEF#=V_{IH}, BES#=V_{IL}
I_{SB}[1]	Standby V_{DD} Current		30	µA	BEF#=BES#=V_{IHC}, $V_{DD}=V_{DD}$ Max
I_{LI}	Input Leakage Current		1	µA	V_{IN}=GND to V_{DD}, $V_{DD}=V_{DD}$ Max
I_{LO}	Output Leakage Current		1	µA	V_{OUT}=GND to V_{DD}, $V_{DD}=V_{DD}$ Max
V_{IL}	Input Low Voltage		0.4	V	$V_{DD}=V_{DD}$ Min
V_{IH}	Input High Voltage	0.7V_{DD}		V	$V_{DD}=V_{DD}$ Max
V_{IHC}	Input High Voltage (CMOS)	V_{DD}-0.3		V	$V_{DD}=V_{DD}$ Max
V_{OL}	Output Low Voltage		0.2	V	I_{OL}=100 µA, $V_{DD}=V_{DD}$ Min
V_{OH}	Output High Voltage	V_{DD}-0.2		V	I_{OH}=-100 µA, $V_{DD}=V_{DD}$ Min
V_H	Supervoltage for A_9 pin	11.4	12.6	V	BEF#=OE#=V_{IL}, WE#=V_{IH}
I_H	Supervoltage Current for A_9 pin		200	µA	BEF#=OE#=V_{IL}, WE#=V_{IH}, $A_9=V_H$ Max

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1. Specification applies to commercial temperature devices only. This parameter may be higher for extended devices.

TABLE 6: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$[1]	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$[1]	Power-up to Write Operation	100	µs

T6.2 1107

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 7: CAPACITANCE (Ta = 25°C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	6 pF

T7.2 1107

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 8: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

T8.4 1107

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

AC CHARACTERISTICS

TABLE 9: SRAM MEMORY BANK CYCLE TIMING PARAMETERS (V_{DD} = 3.0-3.6V)

Symbol	Parameter	SST31LF041/041A-70		SST31LF041A-300		Units
		Min	Max	Min	Max	
T_{RCS}	Read Cycle Time	70		300		ns
T_{BES}	Bank Enable Access Time		70		300	ns
T_{AAS}	Address Access Time		70		300	ns
T_{OES}[1]	Output Enable Access Time		35		150	ns
T_{BLZS}[2]	BES# to Active Output	0		0		ns
T_{OLZS}[1]	Output Enable to Active Output	0		0		ns
T_{BHZS}[1]	BES# to High-Z Output		25		30	ns
T_{OHZS}[1]	Output Disable to High-Z Output		25		30	ns
T_{OHS}	Output Hold from Address Change	0		10		ns

T9.8 1107

1. No T_{OES} value for SST31LF041A
2. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 10: SRAM MEMORY BANK WRITE CYCLE TIMING PARAMETERS (V_{DD} = 3.0-3.6V)

Symbol	Parameter	SST31LF041/041A-70		SST31LF041A-300		Unit
		Min	Max	Min	Max	
T_{WCS}	Write Cycle Time	70		300		ns
T_{BWS}	Bank Enable to End-of-Write	60		230		ns
T_{AWS}	Address Valid to End-of-Write	60		230		ns
T_{ASTS}	Address Set-up Time	0		0		ns
T_{WPS}	Write Pulse Width	60		200		ns
T_{WRS}	Write Recovery Time	0		0		ns
T_{DSS}	Data Set-up Time	30		150		ns
T_{DHS}	Data Hold from Write Time	0		0		ns

T10.5 1107

TABLE 11: FLASH READ CYCLE TIMING PARAMETERS (V_{DD} = 3.0-3.6V)

Symbol	Parameter	SST31LF041/041A-70		SST31LF041A-300		Units
		Min	Max	Min	Max	
T_{RC}	Read Cycle Time	70		300		ns
T_{BE}	Bank Enable Access Time		70		300	ns
T_{AA}	Address Access Time		70		300	ns
T_{OE}	Output Enable Access Time		40		150	ns
T_{BLZ}[1]	BEF# Low to Active Output	0		0		ns
T_{OLZ}[1]	OE# Low to Active Output	0		0		ns
T_{BHZ}[1]	BEF# High to High-Z Output		15		60	ns
T_{OHZ}[1]	OE# High to High-Z Output		15		60	ns
T_{OH}[1]	Output Hold from Address Change	0		0		ns

T11.5 1107

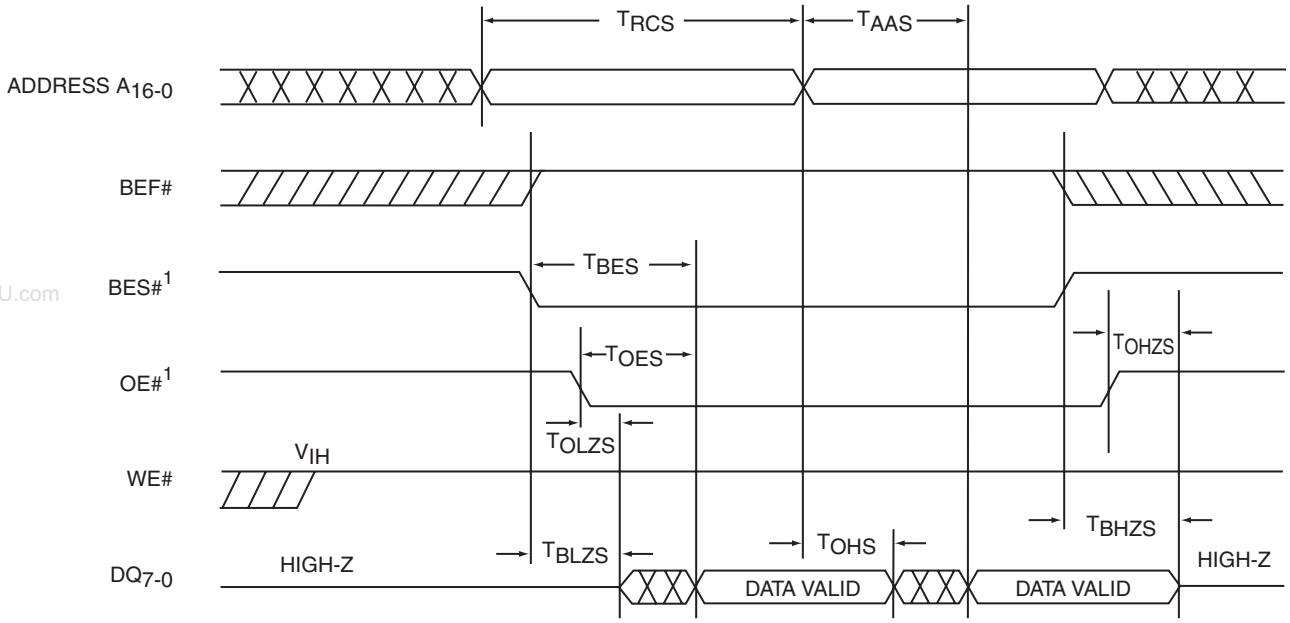
1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Preliminary Specifications

TABLE 12: FLASH PROGRAM/ERASE CYCLE TIMING PARAMETERS (V_{DD} = 3.0-3.6V)

Symbol	Parameter	SST31LF041/041A-70		SST31LF041A-300		Units
		Min	Max	Min	Max	
T_{BP}	Byte-Program Time		20		20	µs
T_{AS}	Address Setup Time	0		0		ns
T_{AH}	Address Hold Time	30		50		ns
T_{BS}	WE# and BEF# Setup Time	0		0		ns
T_{BH}	WE# and BEF# Hold Time	0		0		ns
T_{OES}	OE# High Setup Time	0		0		ns
T_{OEH}	OE# High Hold Time	10		10		ns
T_{BP}	BEF# Pulse Width	40		100		ns
T_{WP}	WE# Pulse Width	40		100		ns
T_{WPH}	WE# Pulse Width High	30		50		ns
T_{BPH}	BEF# Pulse Width High	30		50		ns
T_{DS}	Data Setup Time	40		50		ns
T_{DH}	Data Hold Time	0		0		ns
T_{IDA}	Software ID Access and Exit Time		150		150	ns
T_{SE}	Sector-Erase		25		25	ms
T_{SBE}	Bank-Erase		100		100	ms
T_{BS}	Bank Enable Setup Time for Concurrent Operation	0		0		ns

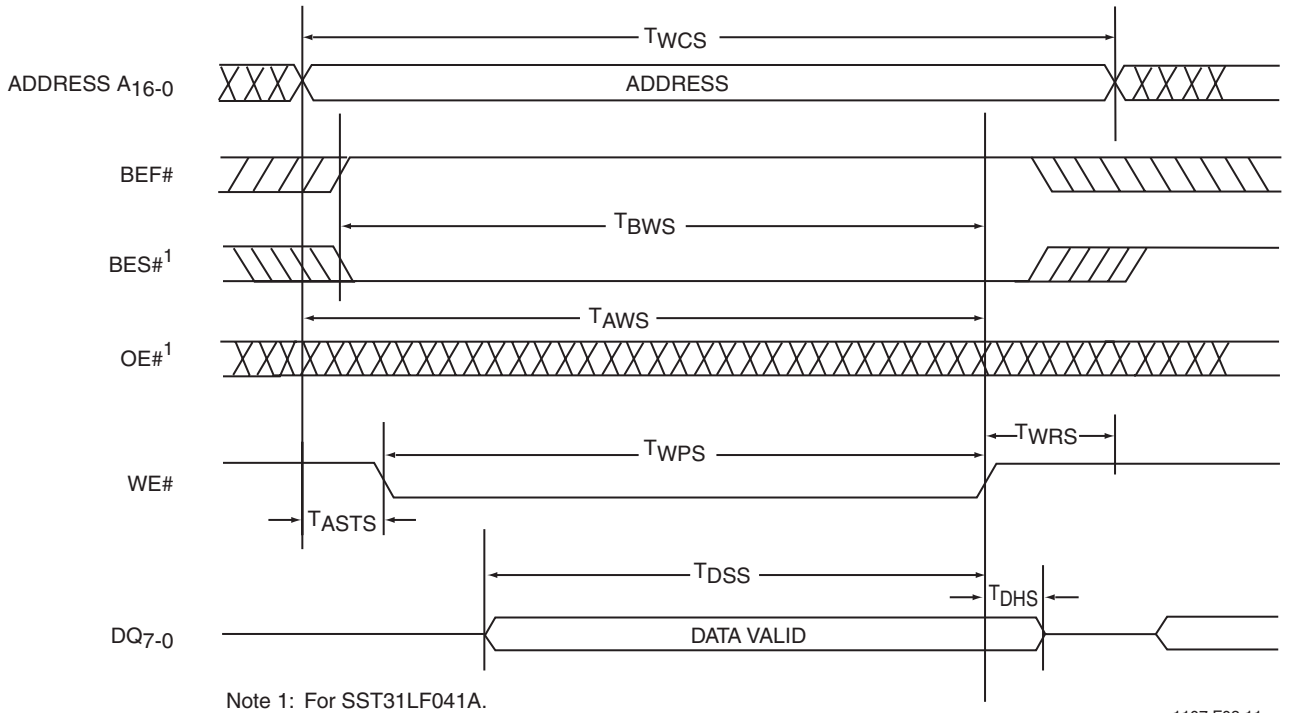
T12.4 1107



Note 1: For SST31LF041A.
BES# and OE# share pin 32. During SRAM operation, pin 32 functions as BES#.

1107 F02.10

FIGURE 3: SRAM READ CYCLE TIMING DIAGRAM



Note 1: For SST31LF041A.
BES# and OE# share pin 32. During SRAM operation, pin 32 functions as BES#.

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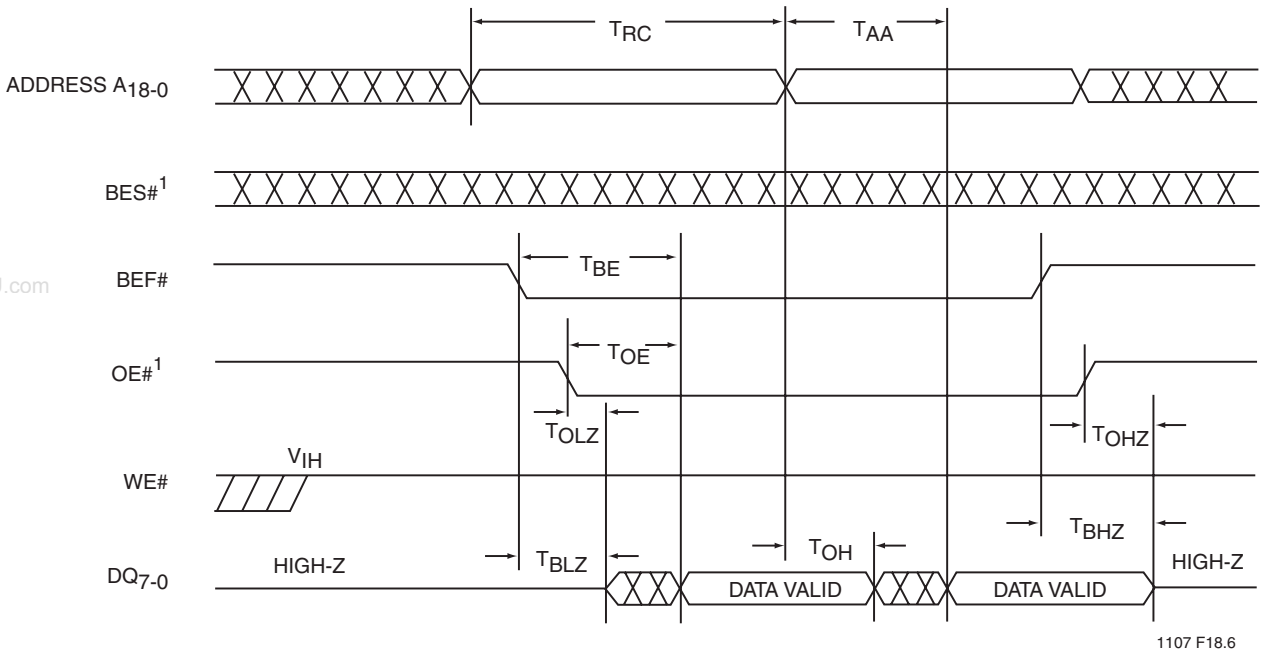
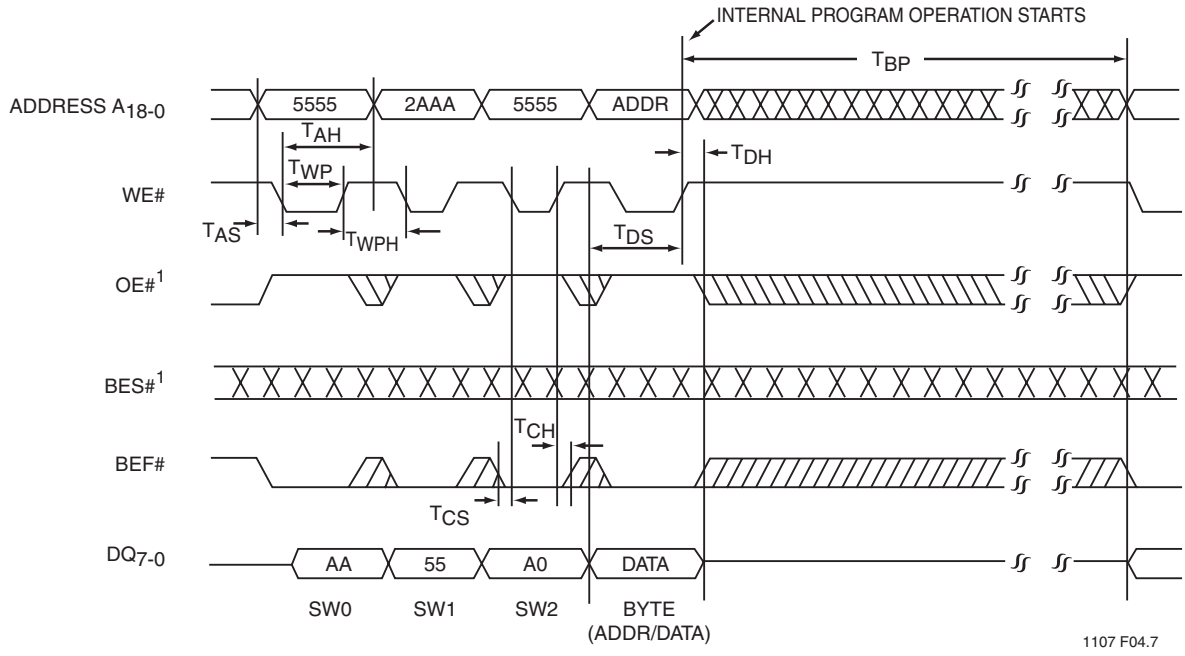
FIGURE 4: SRAM WRITE CYCLE TIMING DIAGRAM



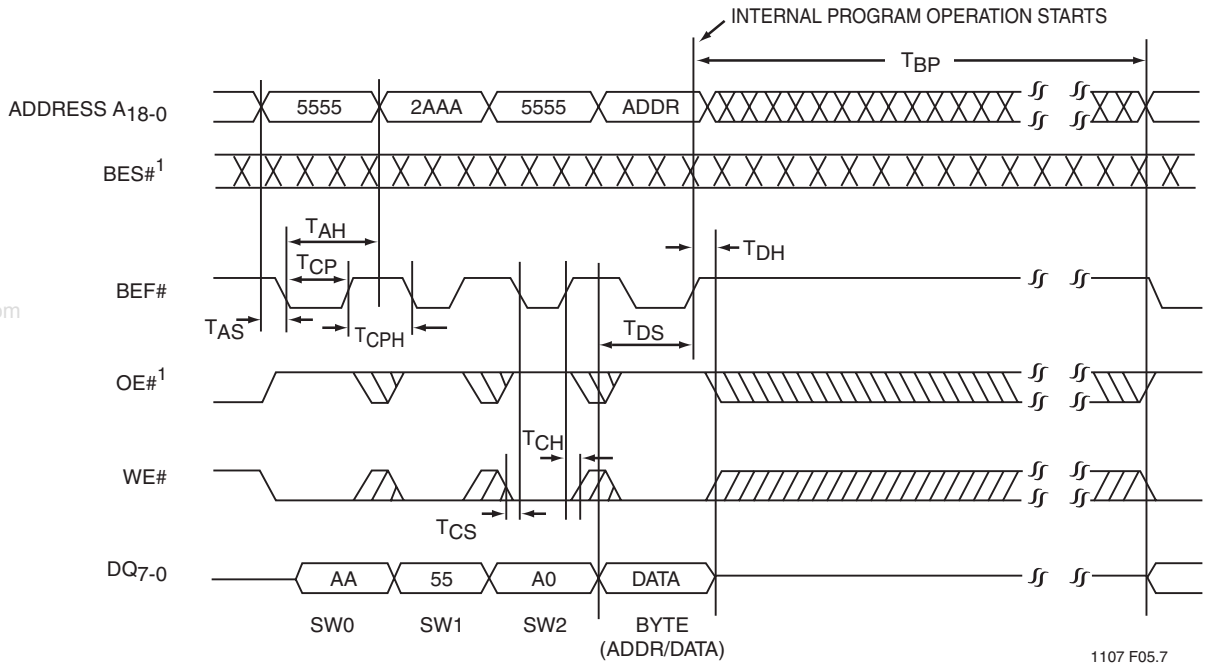
Note 1. For SST31LF041A, BES# and OE# share pin 32. During Flash operation, pin 32 functions as OE#.

FIGURE 5: FLASH READ CYCLE TIMING DIAGRAM



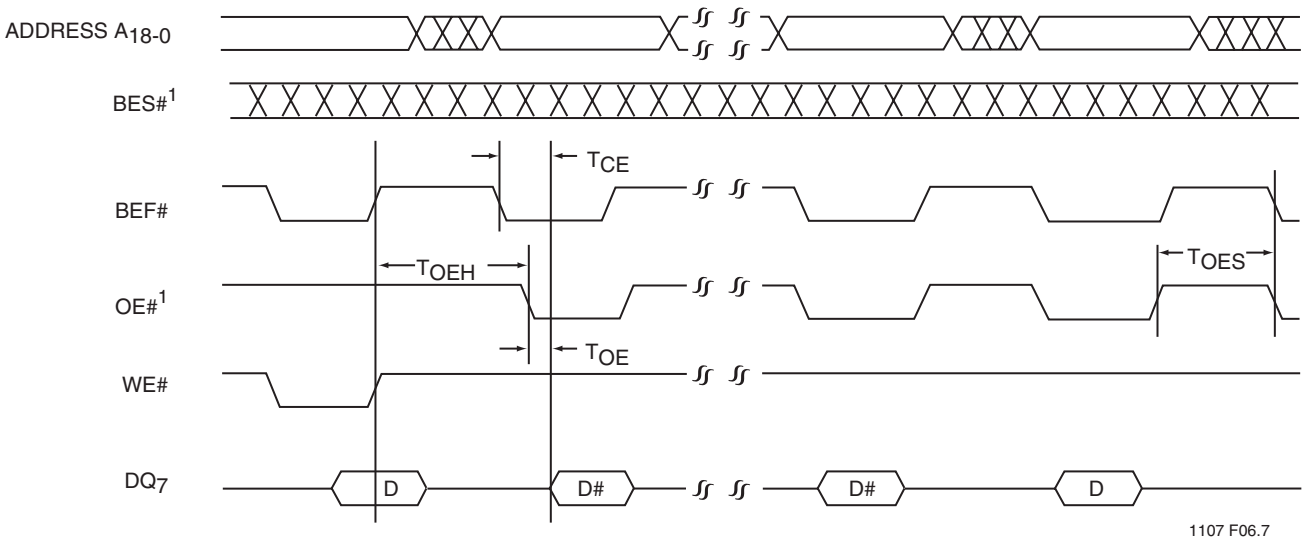
Note 1. For SST31LF041A, BES# and OE# share pin 32. During Flash operation, pin 32 functions as OE#.

FIGURE 6: FLASH WE# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM



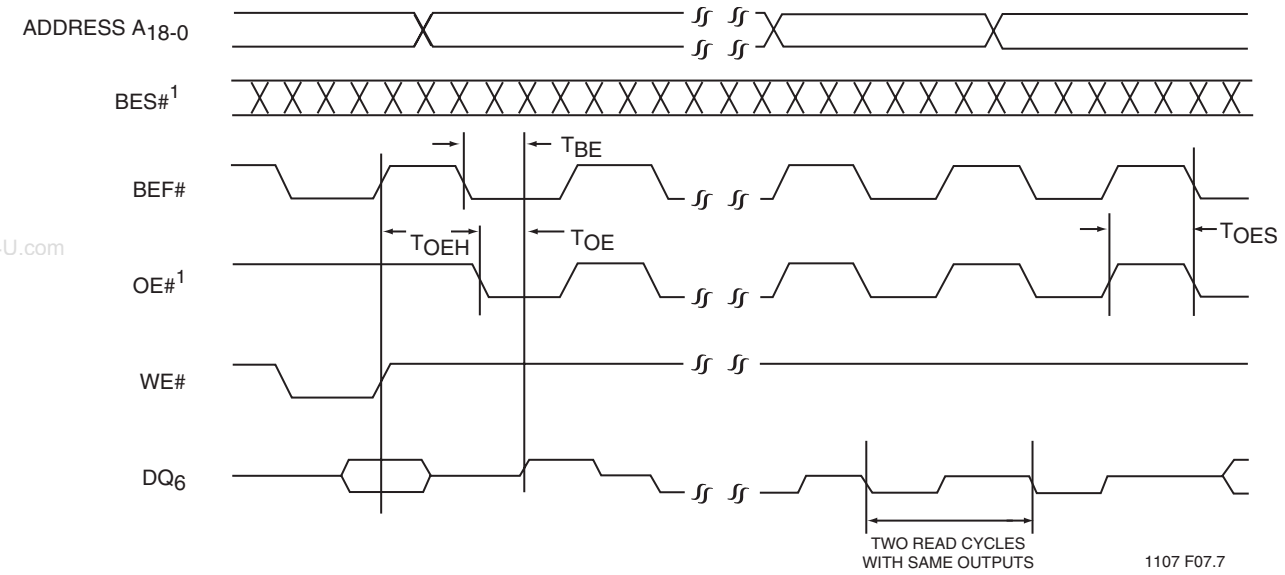
Note 1. For SST31LF041A, BES# and OE# share pin 32. During Flash operation, pin 32 functions as OE#.

FIGURE 7: BEF# CONTROLLED FLASH PROGRAM CYCLE TIMING DIAGRAM



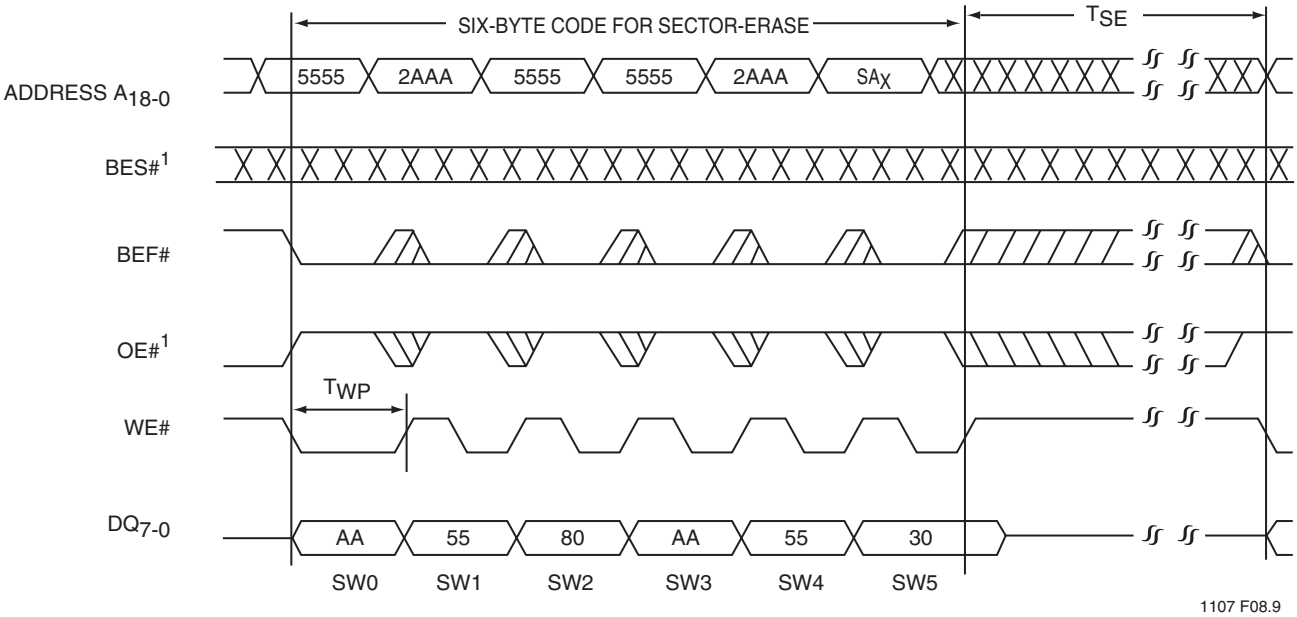
Note 1. For SST31LF041A, BES# and OE# share pin 32. During Flash operation, pin 32 functions as OE#.

FIGURE 8: FLASH DATA# POLLING TIMING DIAGRAM



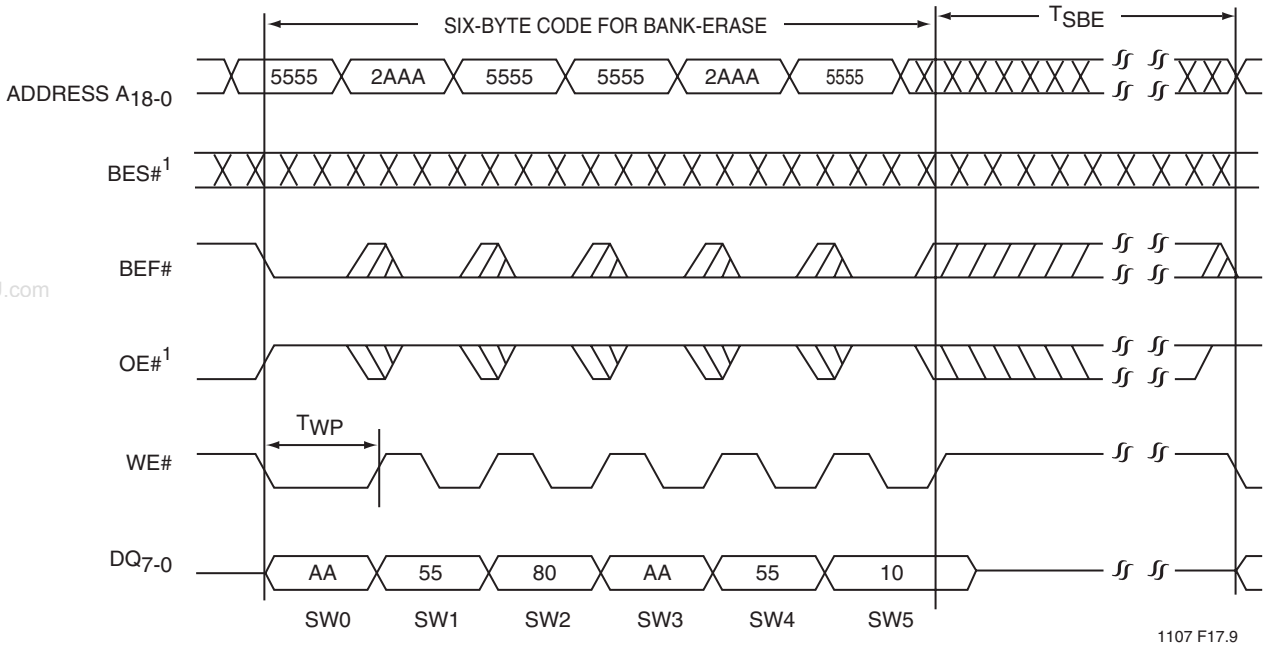
Note 1. For SST31LF041A, BES# and OE# share pin 32. During Flash operation, pin 32 functions as OE#.

FIGURE 9: FLASH TOGGLE BIT TIMING DIAGRAM



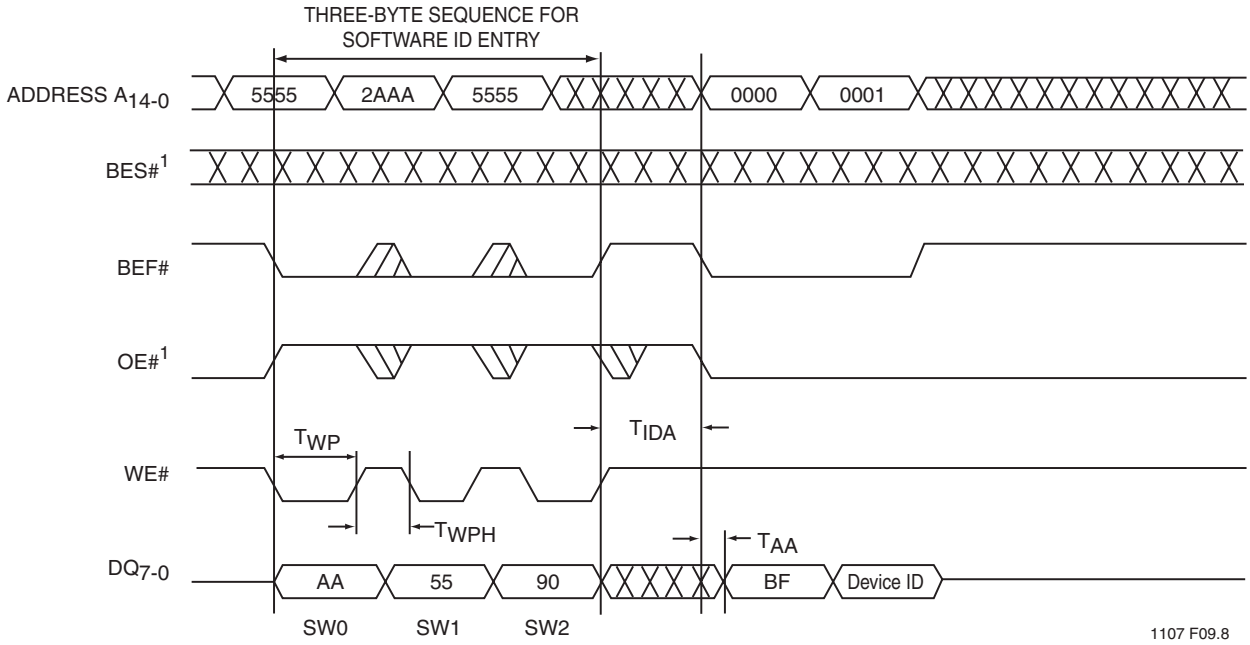
Note: The device also supports BEF# controlled Sector-Erase operation. The WE# and BEF# signals are interchangeable as long as minimum timings are met. (See Table 12)
SA_X = Sector Address
Note 1. For SST31LF041A, BES# and OE# share pin 32. During Flash operation, pin 32 functions as OE#.

FIGURE 10: WE# CONTROLLED FLASH SECTOR-ERASE TIMING DIAGRAM



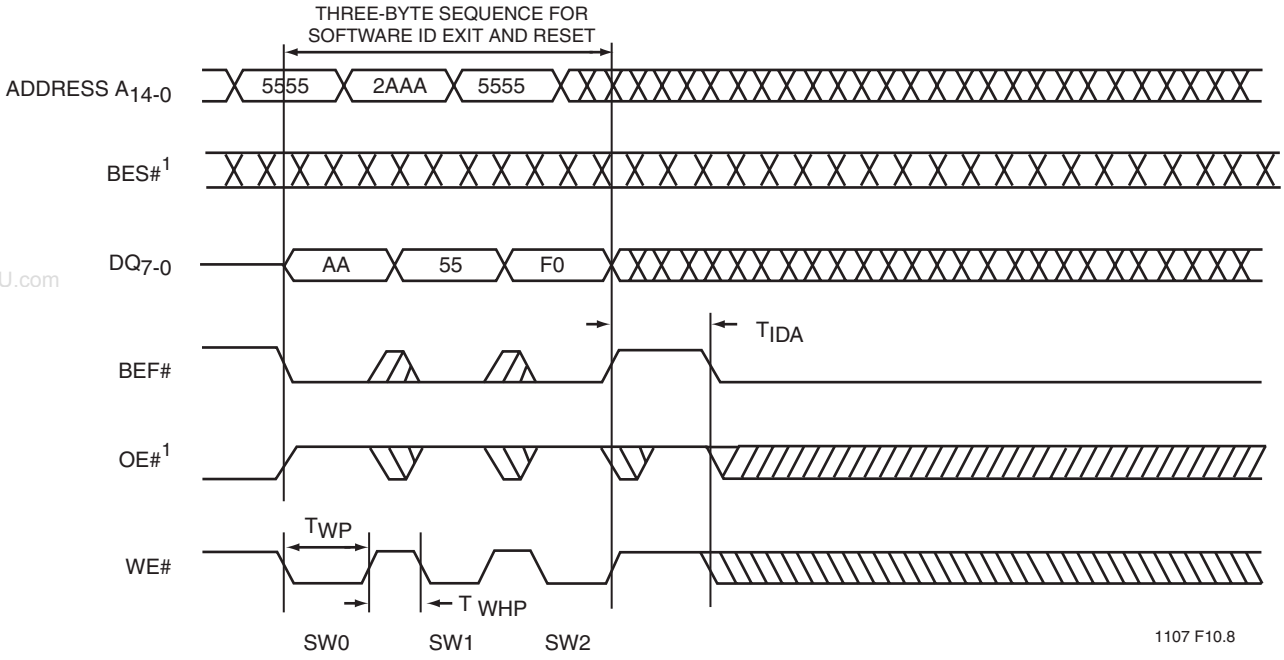
Note: The device also supports BEF# controlled Bank-Erase operation. The WE# and BEF# signals are interchangeable as long as minimum timings are met. (See Table 12)
Note 1. For SST31LF041A, BES# and OE# share pin 32. During Flash operation, pin 32 functions as OE#.

FIGURE 11: WE# CONTROLLED FLASH BANK-ERASE TIMING DIAGRAM



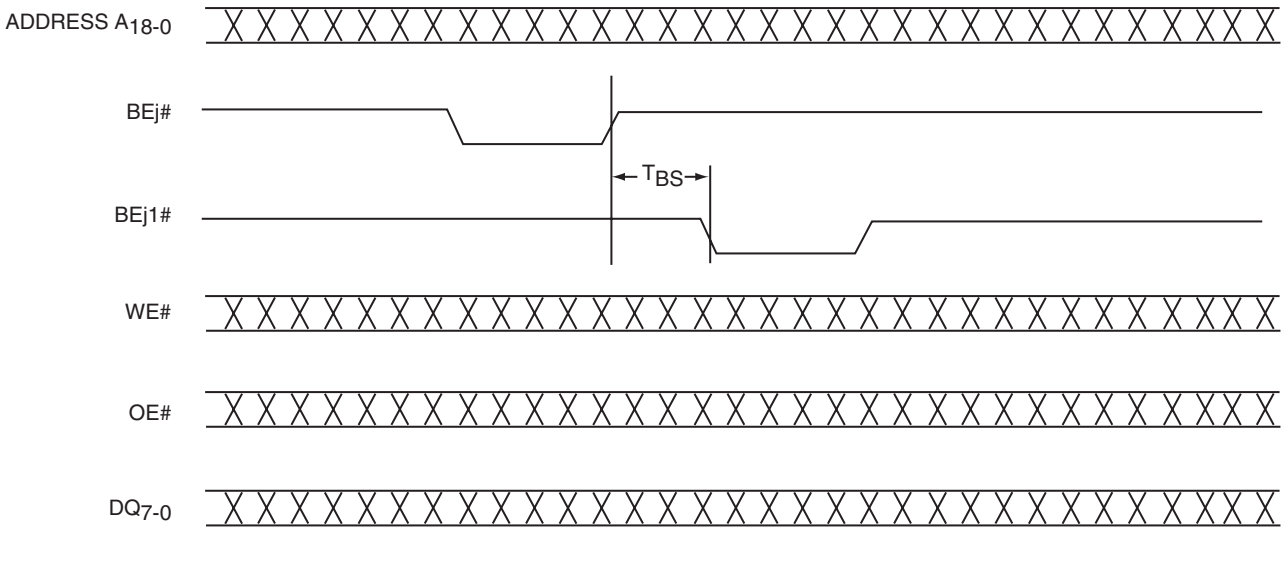
Note 1. For SST31LF041A, BES# and OE# share pin 32. During Flash operation, pin 32 functions as OE#.
Note: Device ID = 16H for SST31LF041A and 17H for SST31LF041.

FIGURE 12: FLASH SOFTWARE ID ENTRY AND READ



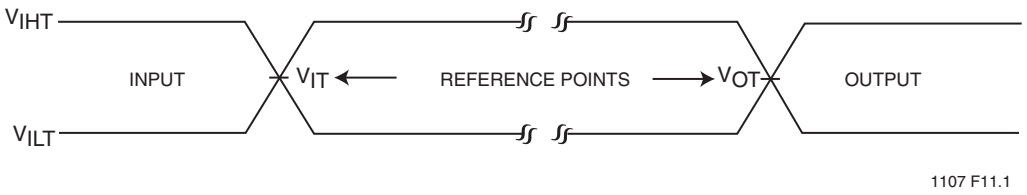
Note 1. For SST31LF041A, BES# and OE# share pin 32. During Flash operation, pin 32 functions as OE#.

FIGURE 13: FLASH SOFTWARE ID EXIT AND RESET



Note: j = F or S
j1 = S or F

FIGURE 14: TIMING DIAGRAM FOR ALTERNATING BETWEEN FLASH/SRAM AND SRAM/FLASH



AC test inputs are driven at V_{IHT} (0.9 V_{DD}) for a logic "1" and V_{ILT} (0.1 V_{DD}) for a logic "0". Measurement reference points for inputs and outputs are V_{IT} (0.5 V_{DD}) and V_{OT} (0.5 V_{DD}). Input rise and fall times (10% ↔ 90%) are <5 ns.

Note: V_{IT} - V_{INPUT} Test
V_{OT} - V_{OUTPUT} Test
V_{IHT} - V_{INPUT} HIGH Test
V_{ILT} - V_{INPUT} LOW Test

FIGURE 15: AC INPUT/OUTPUT REFERENCE WAVEFORMS

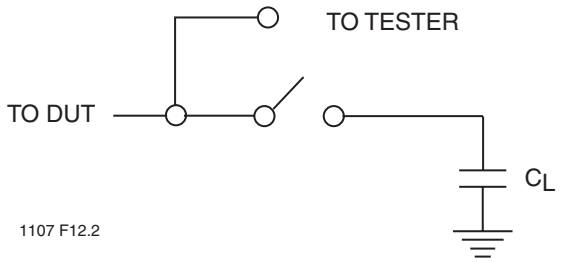


FIGURE 16: A TEST LOAD EXAMPLE

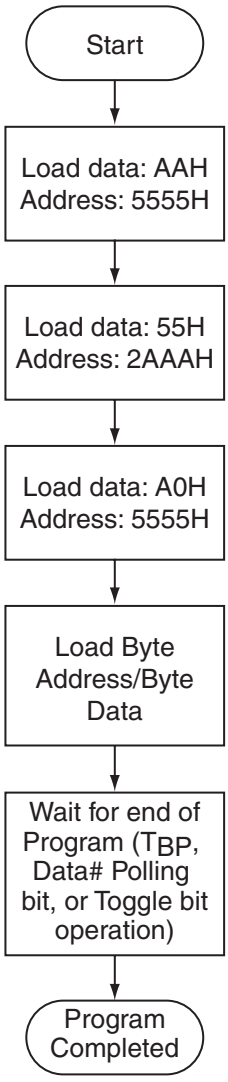


FIGURE 17: BYTE-PROGRAM ALGORITHM

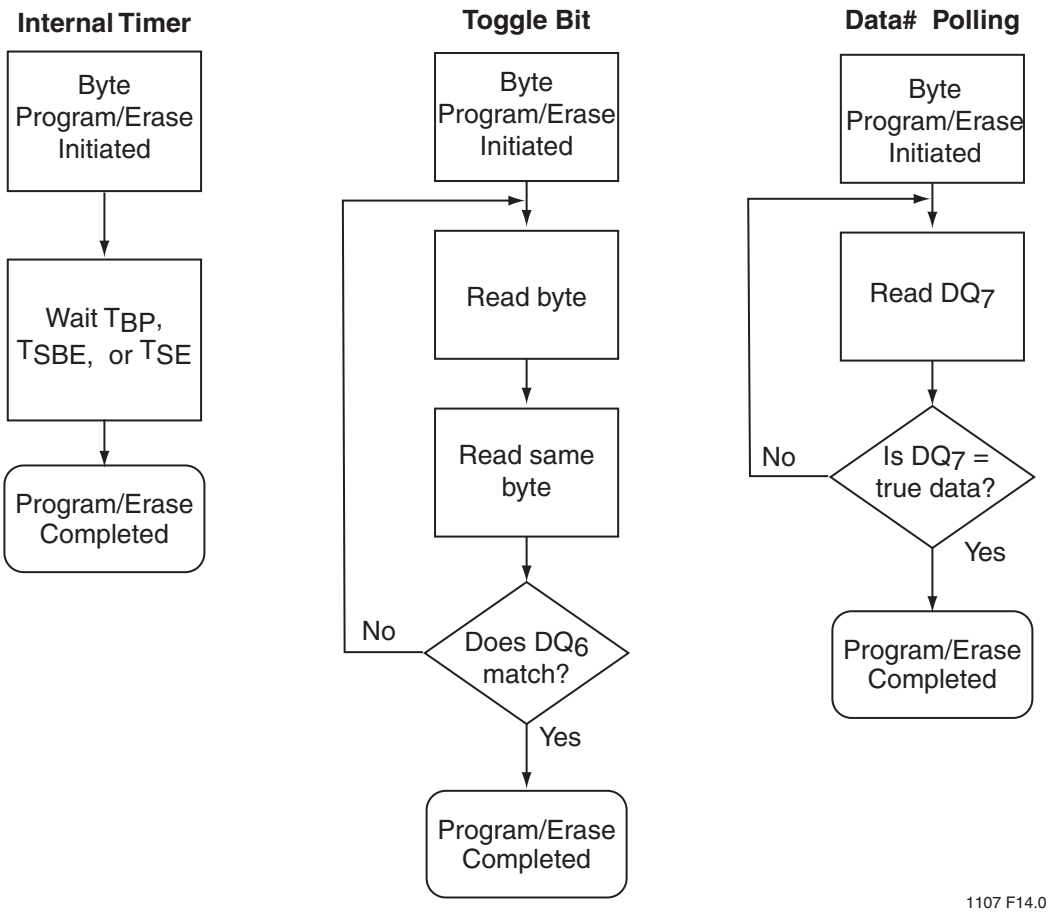


FIGURE 18: WAIT OPTIONS

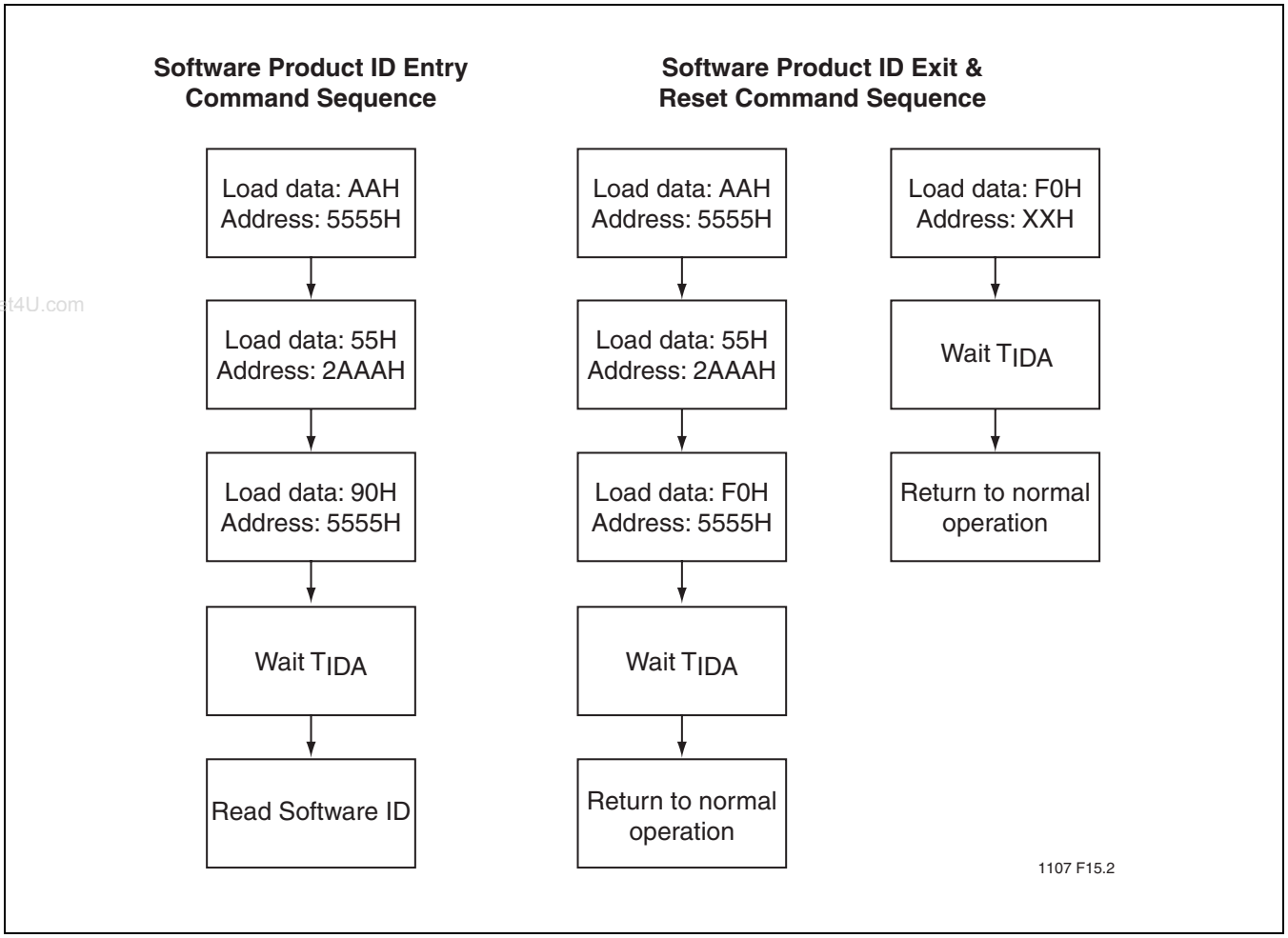


FIGURE 19: SOFTWARE PRODUCT COMMAND FLOWCHARTS

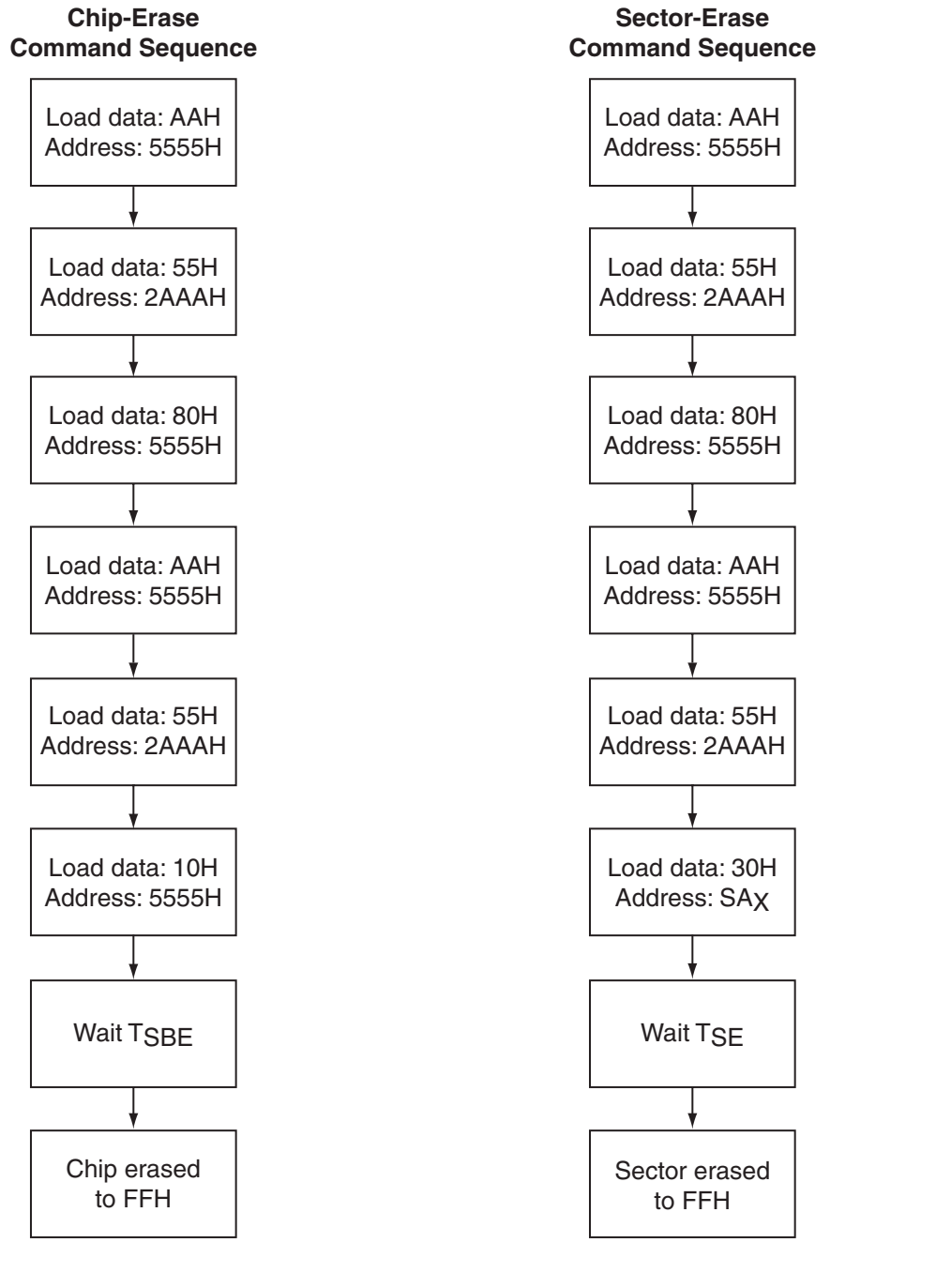
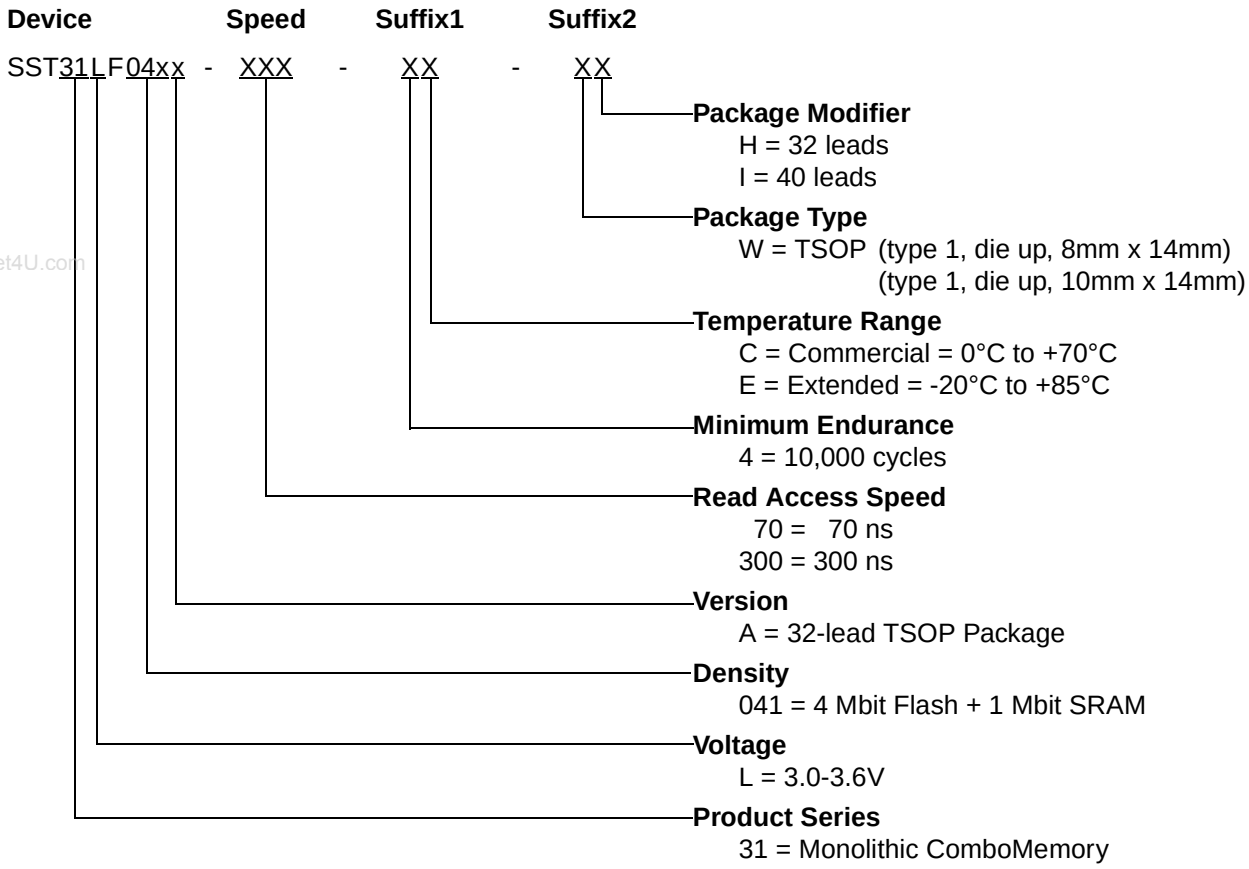


FIGURE 20: ERASE COMMAND SEQUENCE

Preliminary Specifications

PRODUCT ORDERING INFORMATION



Valid combinations for SST31LF041

SST31LF041-70-4C-WI

SST31LF041-70-4E-WI

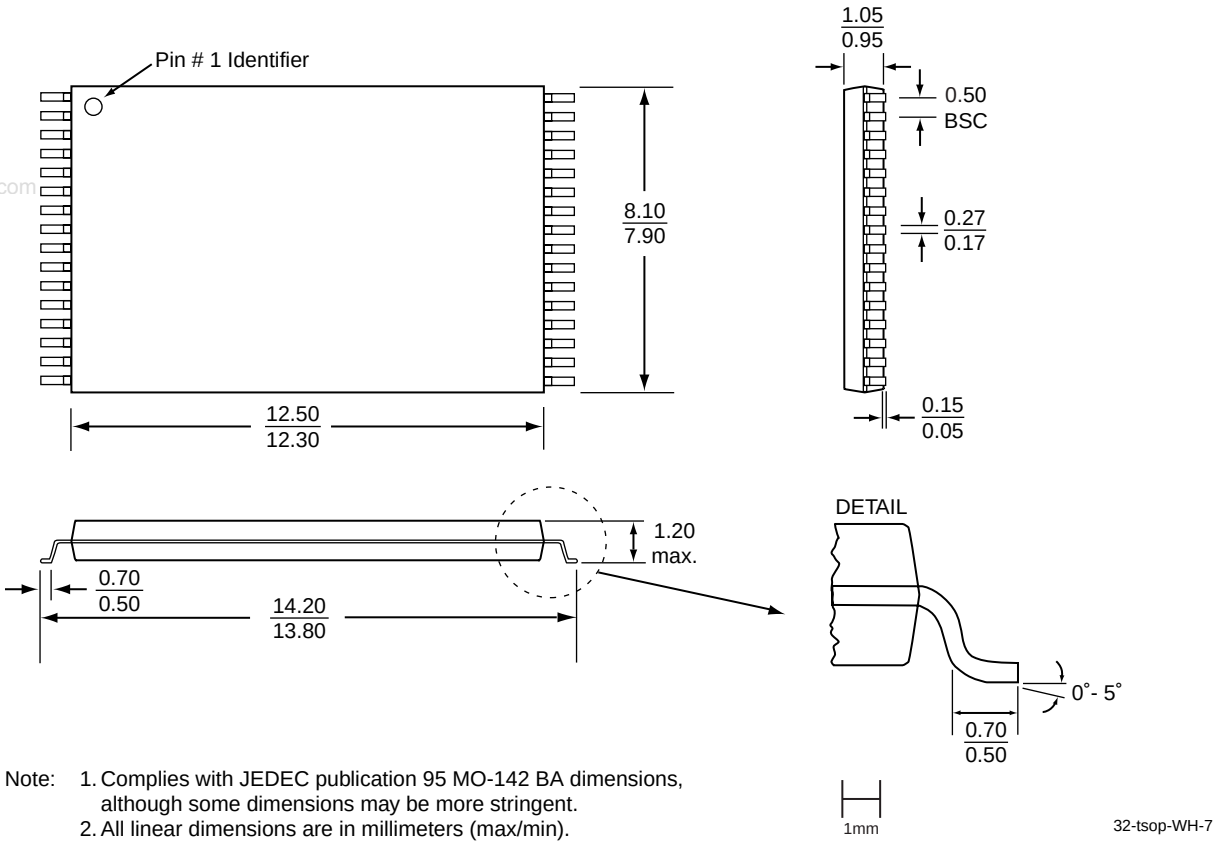
Valid combinations for SST31LF041A

SST31LF041A-70-4C-WH
SST31LF041A-300-4C-WH

SST31LF041A-70-4E-WH
SST31LF041A-300-4E-WH

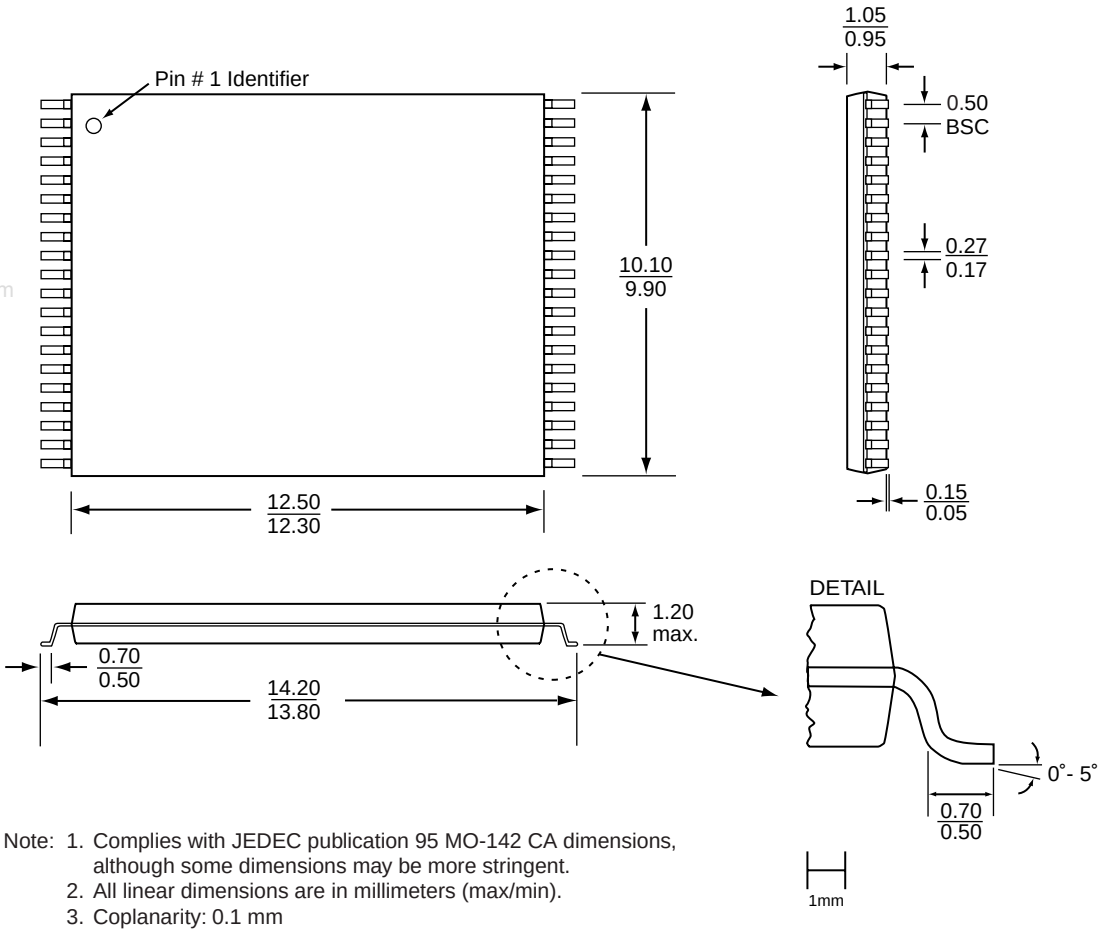
Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

PACKAGING DIAGRAMS



Note:
1. Complies with JEDEC publication 95 MO-142 BA dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in millimeters (max/min).
3. Coplanarity: 0.1 mm
4. Maximum allowable mold flash is 0.15 mm at the package ends, and 0.25 mm between leads.

32-LEAD THIN SMALL OUTLINE PACKAGE (TSOP) 8MM X 14MM
SST PACKAGE CODE: WH



Note: 1. Complies with JEDEC publication 95 MO-142 CA dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in millimeters (max/min).
3. Coplanarity: 0.1 mm
4. Maximum allowable mold flash is 0.15 mm at the package ends, and 0.25 mm between leads.

40-tsop-WI-7

40-LEAD THIN SMALL OUTLINE PACKAGE (TSOP) 10MM X 14MM
SST PACKAGE CODE: WI

TABLE 13: REVISION HISTORY

Number	Description	Date
03	• 2002 Data Book	Feb 2002
04	• Removed the 256 SRAM parts (SST31LF043/043A) and associated MPNs • Corrected the Test Conditions for I_{DD} in Table 5 on page 10 • Added Revision History	Sep 2003
05	• 2004 Data Book	Dec 2003