SST440 SERIES

Siliconix incorporated

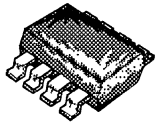
N-Channel JFET Pairs

The SST440 Series are monolithic pairs of JFETs mounted in a single SO-8 package. The SST440 Series features high speed amplification (slew rate), high gain (typically > 6 mS), and low gate leakage (typically < 1 pA). This performance makes these devices perfect for use as wideband differential amplifiers in demanding test and measurement applications. Finally, its SO-8 package is available in tape and reel to support automated assembly. (See Section 8.)

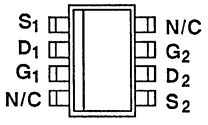
For additional design information please see performance curves NNZ, which are located in Section 7.

PART NUMBER	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_G MAX (pA)	$\lvert V_{GS_1} - V_{GS_2} \rvert$ MAX (mV)
SST440	-25	4.5	-500	10
SST441	-25	4.5	-500	20

SO-8



TOP VIEW



SIMILAR PRODUCTS

- TO-71, See U440 Series
- TO-78, See U443 Series
- Low Noise, See SST404 Series
- Chips, Order U44XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMIT	UNITS
Gate-Drain Voltage		V_{GD}	-25	V
Gate-Source Voltage		V_{GS}	-25	
Forward Gate Current		I_G	50	mA
Power Dissipation	Per Side	P_D	300	mW
	Total		500	
Power Derating	Per Side		2.4	mW/°C
	Total		4	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature		T_{stg}	-55 to 150	
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

ELECTRICAL CHARACTERISTICS[1]				LIMITS				
				SST440		SST441		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-35	-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA	-3.5	-1	-6	-1	-6	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	15	6	30	6	30	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-1		-500		-500	pA
		V_{GS} = -15 V, V_{DS} = 0 V, T_A = 125°C	-0.2					nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 5 mA	-1		-500		-500	pA
		V_{DG} = 10 V, I_D = 5 mA, T_A = 125°C	-0.2					nA
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 5 mA, f = 1 kHz	6	4.5	9	4.5	9	mS
Common-Source Output Conductance	g_{os}		20		200		200	µS
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 5 mA, f = 100 MHz	5.5					mS
Common-Source Output Conductance	g_{os}		30					µS
Common-Source Input Capacitance	C_{iss}	V_{DG} = 10 V, I_D = 5 mA, f = 1 MHz	3.5					pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1					pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 5 mA, f = 10 kHz	4					$nV/\sqrt{Hz}$
MATCHING								
Differential Gate-Source Voltage	$\lvert V_{GS1}-V_{GS2}\rvert$	V_{DG} = 10 V, I_D = 5 mA	7		10		20	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	V_{DG} = 10 V, I_D = 5 mA, T = -55 to 25°C	10					µV/°C
		V_{DG} = 10 V, I_D = 5 mA, T = 25 to 125°C	10					µV/°C
Saturation Drain Current Ratio	$\frac{I_{DSS1}}{I_{DSS2}}$	V_{DS} = 10 V, V_{GS} = 0 V	0.98					
Transconductance Ratio	$\frac{g_{fs1}}{g_{fs2}}$	V_{DG} = 10 V, I_D = 5 mA, f = 1 kHz	0.98					
Common Mode Rejection Ratio	CMRR	V_{DD} = 5 to 10 V, I_D = 5 mA	90					dB

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.

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