

# SSTU32865

## 1.8 V 28-bit 1:2 registered buffer with parity for DDR2 RDIMM applications

Rev. 02 — 28 September 2004

Product data sheet

### 1. General description

The SSTU32865 is a 1.8 V 28-bit 1:2 register specifically designed for use on two rank by four (2R × 4) and similar high-density Double Data Rate 2 (DDR2) memory modules. It is similar in function to the JEDEC-standard 14-bit DDR2 register, but integrates the functionality of the normally required two registers in a single package, thereby freeing up board real-estate and facilitating routing to accommodate high-density Dual In-line Memory Module (DIMM) designs.

The SSTU32865 also integrates a parity function, which accepts a parity bit from the memory controller, compares it with the data received on the D-inputs and indicates whether a parity error has occurred on its open-drain  $\overline{\text{PTYERR}}$  pin (active-LOW).

The SSTU32865 is packaged in a 160-ball, 12 × 18 grid, 0.65 mm ball pitch, thin profile fine-pitch ball grid array (TFBGA) package, which—while requiring a minimum 9 mm × 13 mm of board space—allows for adequate signal routing and escape using conventional card technology.

### 2. Features

- 28-bit data register supporting DDR2
- Fully compliant to JEDEC standard JESD82-9
- Supports 2 rank by 4 DIMM density by integrating equivalent functionality of two JEDEC-standard DDR2 registers (i.e. 2 × SSTU32864 or 2 × SSTU32866)
- Parity checking function across 22 input data bits
- Parity out signal
- Controlled output impedance drivers enable optimal signal integrity and speed
- Exceeds JESD82-9 speed performance (1.8 ns max. single-bit switching propagation delay, 2.0 ns max. mass-switching)
- Supports up to 450 MHz clock frequency of operation
- Optimized pinout for high-density DDR2 module design
- Chip-selects minimize power consumption by gating data outputs from changing state
- Supports Stub Series Terminated Logic SSTL\_18 data inputs
- Differential clock (CK and  $\overline{\text{CK}}$ ) inputs
- Supports Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS) switching levels on the control and  $\overline{\text{RESET}}$  inputs
- Single 1.8 V supply operation
- Available in 160-ball 9 mm × 13 mm, 0.65 mm ball pitch TFBGA package

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### 3. Applications

- High-density (e.g. 2 rank by 4) DDR2 registered DIMMs
- DDR2 Registered DIMMs (RDIMM) desiring parity checking functionality

### 4. Ordering information

Table 1: Ordering information

| Type number   | Solder process                        | Package  |  |          |
|---------------|---------------------------------------|----------|--|----------|
|               |                                       | Name     | Description  | Version  |
| SSTU32865ET/G | Pb-free (SnAgCu solder ball compound) | TFBGA160 | plastic thin fine-pitch ball grid array package; 160 balls; body $9 \times 13 \times 0.8$ mm | SOT802-1 |
| SSTU32865ET   | SnPb solder ball compound             | TFBGA160 | plastic thin fine-pitch ball grid array package; 160 balls; body $9 \times 13 \times 0.8$ mm | SOT802-1 |



5. Functional diagram

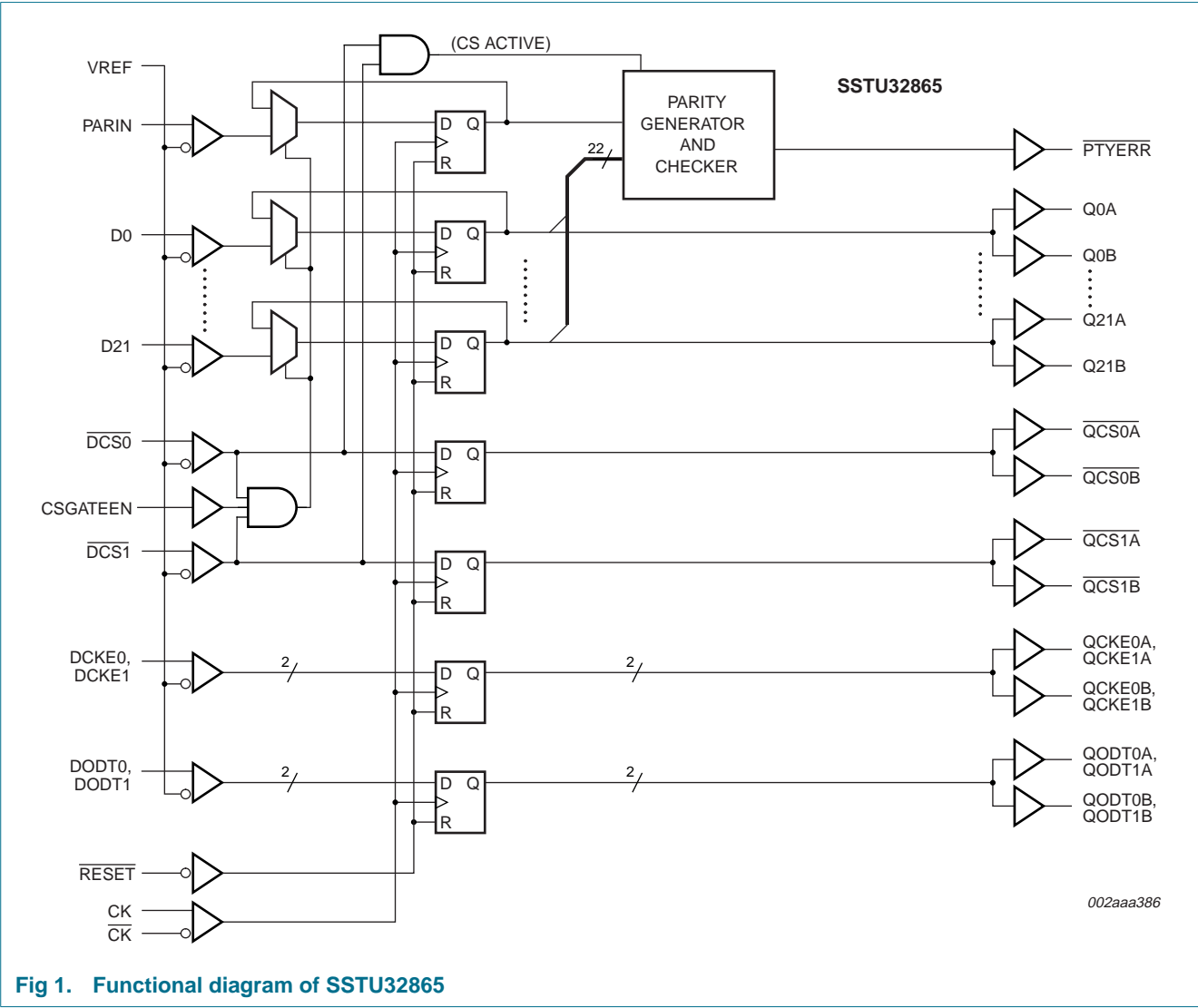


Fig 1. Functional diagram of SSTU32865

6. Pinning information

6.1 Pinning

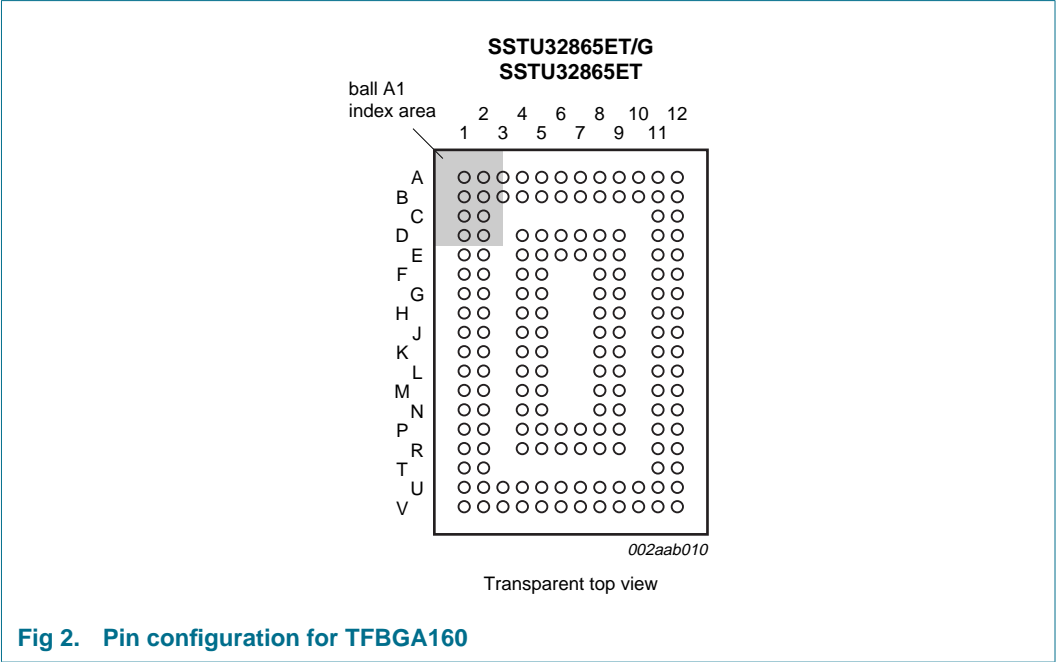


Fig 2. Pin configuration for TFBGA160

|   | 1                         | 2                        | 3      | 4                          | 5      | 6      | 7      | 8    | 9    | 10   | 11                        | 12                        |
|---|---------------------------|--------------------------|--------|----------------------------|--------|--------|--------|------|------|------|---------------------------|---------------------------|
| A | VREF                      | n.c.                     | PARIN  | n.c.                       | n.c.   | QCKE1A | QCKE0A | Q21A | Q19A | Q18A | Q17B                      | Q17A                      |
| B | D1                        | D2                       | n.c.   | n.c.                       | n.c.   | QCKE1B | QCKE0B | Q21B | Q19B | Q18B | QODT0B                    | QODT0A                    |
| C | D3                        | D4                       |        |                            |        |        |        |      |      |      | QODT1B                    | QODT1A                    |
| D | D6                        | D5                       |        | VDDL                       | GND    | n.c.   | n.c.   | GND  | GND  |      | Q20B                      | Q20A                      |
| E | D7                        | D8                       |        | VDDL                       | GND    | VDDL   | VDDR   | GND  | GND  |      | Q16B                      | Q16A                      |
| F | D11                       | D9                       |        | VDDL                       | GND    |        |        | VDDR | VDDR |      | Q1B                       | Q1A                       |
| G | D18                       | D12                      |        | VDDL                       | GND    |        |        | VDDR | VDDR |      | Q2B                       | Q2A                       |
| H | CSGATEEN                  | D15                      |        | VDDL                       | GND    |        |        | GND  | GND  |      | Q5B                       | Q5A                       |
| J | CK                        | $\overline{\text{DCS0}}$ |        | GND                        | GND    |        |        | VDDR | VDDR |      | $\overline{\text{QCS0B}}$ | $\overline{\text{QCS0A}}$ |
| K | $\overline{\text{CK}}$    | $\overline{\text{DCS1}}$ |        | VDDL                       | VDDL   |        |        | GND  | GND  |      | $\overline{\text{QCS1B}}$ | $\overline{\text{QCS1A}}$ |
| L | $\overline{\text{RESET}}$ | D14                      |        | GND                        | GND    |        |        | VDDR | VDDR |      | Q6B                       | Q6A                       |
| M | D0                        | D10                      |        | GND                        | GND    |        |        | GND  | GND  |      | Q10B                      | Q10A                      |
| N | D17                       | D16                      |        | VDDL                       | VDDL   |        |        | VDDR | VDDR |      | Q9B                       | Q9A                       |
| P | D19                       | D21                      |        | GND                        | VDDL   | VDDL   | VDDR   | VDDR | GND  |      | Q11B                      | Q11A                      |
| R | D13                       | D20                      |        | GND                        | VDDL   | VDDL   | GND    | GND  | GND  |      | Q15B                      | Q15A                      |
| T | DODT1                     | DODT0                    |        |                            |        |        |        |      |      |      | Q14B                      | Q14A                      |
| U | DCKE0                     | DCKE1                    | m.c.l. | $\overline{\text{PTYERR}}$ | m.c.h. | Q3B    | Q12B   | Q7B  | Q4B  | Q13B | Q0B                       | Q8B                       |
| V | VREF                      | m.c.l.                   | m.c.l. | n.c.                       | m.c.h. | Q3A    | Q12A   | Q7A  | Q4A  | Q13A | Q0A                       | Q8A                       |

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160-ball, 12 × 18 grid; top view.

An empty cell indicates no ball is populated at that grid point.

n.c. denotes a no-connect (ball present but not connected to the die).

m.c.l. denotes a pin that must be connected LOW.

m.c.h. denotes a pin that must be connected HIGH.

**Fig 3. Ball mapping**

## 6.2 Pin description

Table 2: Pin description

| Symbol                          | Pin  | Type         | Description   |
|---------------------------------|--|--------------|---|
| <b>Ungated inputs</b>           |  |              |   |
| DCKE0, DCKE1                    | U1, U2   | SSTL_18      | DRAM function pins not associated with Chip Select.   |
| DODT0, DODT1                    | T2, T1   |              |   |
| <b>Chip Select gated inputs</b> |  |              |   |
| D0 to D21                       | M1, B1, B2, C1, C2, D2, D1, E1, E2, F2, M2, F1, G2, R1, L2, H2, N2, N1, G1, P1, R2, P2                 | SSTL_18      | DRAM inputs, re-driven only when Chip Select is LOW.  |
| <b>Chip Select inputs</b>       |  |              |   |
| DCS0, DCS1                      | J2, K2   | SSTL_18      | DRAM Chip Select signals. These pins initiate DRAM address/command decodes, and as such at least one will be LOW when a valid address/command is present. The register can be programmed to re-drive all D-inputs only (CSGATEEN = HIGH) when at least one Chip Select input is LOW.  |
| <b>Re-driven outputs</b>        |  |              |   |
| Q0A to Q21A                     | V11, F12, G12, V6, V9, H12, L12, V8, V12, N12, M12, P12, V7, V10, T12, R12, E12, A12, A10, A9, D12, A8 | SSTL_18      | Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.  |
| Q0B to Q21B                     | U11, F11, G11, U6, U9, H11, L11, U8, U12, N11, M11, P11, U7, U10, T11, R11, E11, A11, B10, B9, D11, B8 |              |   |
| QCS0A, QDS1A, QCS0B, QCS1B      | J12, K12, J11, K11   |              |   |
| QCKE0A, QCKE1A, QCKE0B, QCKE1B  | A7, A6, B7, B6   |              |   |
| QODT0A, QODT1A, QODT0B, QODT1B  | B12, C12, B11, C11   |              |   |
| <b>Parity input</b>             |  |              |   |
| PARIN                           | A3   | SSTL_18      | Parity input for the D0 to D21 inputs. Arrives one clock cycle after the corresponding data input.  |
| <b>Parity error</b>             |  |              |   |
| PTYERR                          | U4   | open drain   | When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs. PTYERR will be active for two clock cycles, and delayed by an additional clock cycle for compatibility with final parity out timing on the industry-standard DDR2 register with parity (in JEDEC definition). |
| <b>Program inputs</b>           |  |              |   |
| CSGATEEN                        | H1   | 1.8 V LVCMOS | Chip Select Gate Enable. When HIGH, the D0 to D21 inputs will be latched only when at least one Chip Select input is LOW during the rising edge of the clock. When LOW, the D0 to D21 inputs will be latched and redriven on every rising edge of the clock.  |

Table 2: Pin description ...continued

| Symbol                      | Pin   | Type             | Description  |
|-----------------------------|---|------------------|--|
| <b>Clock inputs</b>         |   |                  |  |
| CK, $\overline{\text{CK}}$  | J1, K1  | SSTL_18          | Differential master clock input pair to the register. The register operation is triggered by a rising edge on the positive clock input (CK).   |
| <b>Miscellaneous inputs</b> |   |                  |  |
| m.c.l.                      | U3, V2, V3  |                  | Must be connected to a logic LOW   |
| m.c.h.                      | U5, V5  |                  | Must be connected to a logic HIGH.   |
| $\overline{\text{RESET}}$   | L1  | 1.8 V<br>LVCMOS  | Asynchronous reset input. When LOW, it causes a reset of the internal latches, thereby forcing the outputs LOW. $\overline{\text{RESET}}$ also resets the $\overline{\text{PTYERR}}$ signal. |
| VREF                        | A1, V1  | 0.9 V<br>nominal | Input reference voltage for the SSTL_18 inputs. Two pins (internally tied together) are used for increased reliability.  |
| VDDL                        | D4, E4, E6, F4, G4, H4, K4,<br>K5, N4, N5, P5, P6, R5, R6   |                  | power supply voltage   |
| VDDR                        | E7, F8, F9, G8, G9, J8, J9,<br>L8, L9, N8, N9, P7, P8   |                  | power supply voltage   |
| GND                         | D5, D8, D9, E5, E8, E9, F5,<br>G5, H5, H8, H9, J4, J5, K8,<br>K9, L4, L5, M4, M5, M8, M9,<br>P4, P9, R4, R7, R8, R9 |                  | ground   |
| n.c.                        | A2, A4, A5, B3, B4, B5, D6,<br>D7, V4   |                  | ball present but not connected to die  |

## 7. Functional description

### 7.1 Function table

Table 3: Function table (each flip-flop)

| Inputs |               |               |               |               |               |                  | Outputs <sup>[1]</sup> |                |                |                |
|--------|---------------|---------------|---------------|---------------|---------------|------------------|------------------------|----------------|----------------|----------------|
| RESET  | DCS0          | DCS1          | CSGATEEN      | CK            | CK            | Dn, DODTn, DCKEn | Qn                     | QCS0           | QCS1           | QODTn, QCKEn   |
| H      | L             | L             | X             | ↑             | ↓             | L                | L                      | L              | L              | L              |
| H      | L             | L             | X             | ↑             | ↓             | H                | H                      | L              | L              | H              |
| H      | L             | L             | X             | L or H        | L or H        | X                | Q <sub>0</sub>         | Q <sub>0</sub> | Q <sub>0</sub> | Q <sub>0</sub> |
| H      | L             | H             | X             | ↑             | ↓             | L                | L                      | L              | H              | L              |
| H      | L             | H             | X             | ↑             | ↓             | H                | H                      | L              | H              | H              |
| H      | L             | H             | X             | L or H        | L or H        | X                | Q <sub>0</sub>         | Q <sub>0</sub> | Q <sub>0</sub> | Q <sub>0</sub> |
| H      | H             | L             | X             | ↑             | ↓             | L                | L                      | H              | L              | L              |
| H      | H             | L             | X             | ↑             | ↓             | H                | H                      | H              | L              | H              |
| H      | H             | L             | X             | L or H        | L or H        | X                | Q <sub>0</sub>         | Q <sub>0</sub> | Q <sub>0</sub> | Q <sub>0</sub> |
| H      | H             | H             | L             | ↑             | ↓             | L                | L                      | H              | H              | L              |
| H      | H             | H             | L             | ↑             | ↓             | H                | H                      | H              | H              | H              |
| H      | H             | H             | L             | L or H        | L or H        | X                | Q <sub>0</sub>         | Q <sub>0</sub> | Q <sub>0</sub> | Q <sub>0</sub> |
| H      | H             | H             | H             | ↑             | ↓             | L                | Q <sub>0</sub>         | H              | H              | L              |
| H      | H             | H             | H             | ↑             | ↓             | H                | Q <sub>0</sub>         | H              | H              | H              |
| H      | H             | H             | H             | L or H        | L or H        | X                | Q <sub>0</sub>         | Q <sub>0</sub> | Q <sub>0</sub> | Q <sub>0</sub> |
| L      | X or floating | X or floating | X or floating | X or floating | X or floating | X or floating    | L                      | L              | L              | L              |

[1] Q<sub>0</sub> is the previous state of the associated output.

Table 4: Parity and standby function table

| Inputs |               |               |               |               |                             |                      | Output                   |
|--------|---------------|---------------|---------------|---------------|-----------------------------|----------------------|--------------------------|
| RESET  | DCS0          | DCS1          | CK            | CK            | Σ of inputs = H (D0 to D21) | PARIN <sup>[1]</sup> | PTYERR <sup>[2][3]</sup> |
| H      | L             | H             | ↑             | ↓             | even                        | L                    | H                        |
| H      | L             | H             | ↑             | ↓             | odd                         | L                    | L                        |
| H      | L             | H             | ↑             | ↓             | even                        | H                    | L                        |
| H      | L             | H             | ↑             | ↓             | odd                         | H                    | H                        |
| H      | H             | L             | ↑             | ↓             | even                        | L                    | H                        |
| H      | H             | L             | ↑             | ↓             | odd                         | L                    | L                        |
| H      | H             | L             | ↑             | ↓             | even                        | H                    | L                        |
| H      | H             | L             | ↑             | ↓             | odd                         | H                    | H                        |
| H      | H             | H             | ↑             | ↓             | X                           | X                    | PTYERR <sub>0</sub>      |
| H      | X             | X             | L or H        | L or H        | X                           | X                    | PTYERR <sub>0</sub>      |
| L      | X or floating | X or floating | X or floating | X or floating | X or floating               | X or floating        | H                        |

[1] PARIN arrives one clock cycle after the data to which it applies. All Dn inputs must be driven to a known state for parity to be calculated correctly.



- [2] This condition assumes  $\overline{\text{PTYERR}}$  is HIGH at the crossing of CK going HIGH and  $\overline{\text{CK}}$  going LOW. If  $\overline{\text{PTYERR}}$  is LOW, it stays latched LOW for two clock cycles or until  $\overline{\text{RESET}}$  is driven LOW.  
CSGATEEN is 'don't care' for  $\overline{\text{PTYERR}}$ .
- [3]  $\overline{\text{PTYERR}}_0$  is the previous state of output  $\overline{\text{PTYERR}}$ .

## 7.2 Functional information

This 28-bit 1:2 registered buffer with parity is designed for 1.7 V to 1.9 V  $V_{\text{DD}}$  operation.

All clock and data inputs are compatible with the JEDEC standard for SSTL\_18. The control inputs are LVCMOS. All outputs are 1.8 V CMOS drivers that have been optimized to drive the DDR2 DIMM load.

The SSTU32865 operates from a differential clock (CK and  $\overline{\text{CK}}$ ). Data are registered at the crossing of CK going HIGH, and  $\overline{\text{CK}}$  going LOW.

The device supports low-power standby operation. When the reset input ( $\overline{\text{RESET}}$ ) is LOW, the differential input receivers are disabled, and undriven (floating) data, clock and reference voltage ( $V_{\text{REF}}$ ) inputs are allowed. In addition, when  $\overline{\text{RESET}}$  is LOW all registers are reset, and all outputs except  $\overline{\text{PTYERR}}$  are forced LOW. The LVCMOS  $\overline{\text{RESET}}$  input must always be held at a valid logic HIGH or LOW level.

To ensure defined outputs from the register before a stable clock has been supplied,  $\overline{\text{RESET}}$  must be held in the LOW state during power-up.

In the DDR2 RDIMM application,  $\overline{\text{RESET}}$  is specified to be completely asynchronous with respect to CK and  $\overline{\text{CK}}$ . Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the data outputs will be driven LOW quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers. As long as the data inputs are LOW, and the clock is stable during the time from the LOW-to-HIGH transition of  $\overline{\text{RESET}}$  until the input receivers are fully enabled, the design of the SSTU32865 ensures that the outputs remain LOW, thus ensuring no glitches on the output.

The device monitors both  $\overline{\text{DCS0}}$  and  $\overline{\text{DCS1}}$  inputs and will gate the Qn outputs from changing states when both  $\overline{\text{DCS0}}$  and  $\overline{\text{DCS1}}$  are HIGH. If either  $\overline{\text{DCS0}}$  or  $\overline{\text{DCS1}}$  input is LOW, the Qn outputs will function normally. The  $\overline{\text{RESET}}$  input has priority over the  $\overline{\text{DCS0}}$  and  $\overline{\text{DCS1}}$  control and will force the Qn outputs LOW and the  $\overline{\text{PTYERR}}$  output HIGH. If the  $\overline{\text{DCSn}}$ -control functionality is not desired, then the CSGATEEN input can be hardwired to ground, in which case, the setup-time requirement for  $\overline{\text{DCSn}}$  would be the same as for the other Dn data inputs.

The SSTU32865 includes a parity checking function. The SSTU32865 accepts a parity bit from the memory controller at its input pin PARIN, compares it with the data received on the Dn inputs (with either  $\overline{\text{DCS0}}$  or  $\overline{\text{DCS1}}$  active) and indicates whether a parity error has occurred on its open-drain  $\overline{\text{PTYERR}}$  pin (active LOW).

### 7.3 Functional differences to SSTU32864

The SSTU32865 for its basic register functionality, signal definition and performance is based upon the industry-standard SSTU32864, but provides key operational features which differ (at least in part) from the industry-standard register in the following aspects:

#### 7.3.1 Chip Select (CS) gating of key inputs ( $\overline{DCS0}$ , $\overline{DCS1}$ , CSGATEEN)

As a means to reduce device power, the internal latches will only be updated when one or both of the CS inputs are active (LOW) and CSGATEEN HIGH at the rising edge of the clock. The 22 'Chip-Select-gated' input signals associated with this function include addresses (ADDR0 to ADDR15, BA0 to BA2), and RAS, CAS, WE, with the remaining signals (CS, CKE, ODT) continuously re-driven at the rising edge of every clock as they are independent of CS. The CS gating function can be disabled by tying CSGATEEN LOW, enabling all internal latches to be updated on every rising edge of the clock.

**Table 5: Chip Select gating mode**

| Mode       | Signal name      | Description   |
|------------|------------------|---|
| Gating     | CSGATEEN<br>HIGH | Registers only re-drive signals to the DRAMs when Chip Select inputs are LOW.                               |
| Non-gating | CSGATEEN<br>LOW  | Registers always re-drive signals on every clock cycle, independent of the state of the Chip Select inputs. |

#### 7.3.2 Parity error checking and reporting

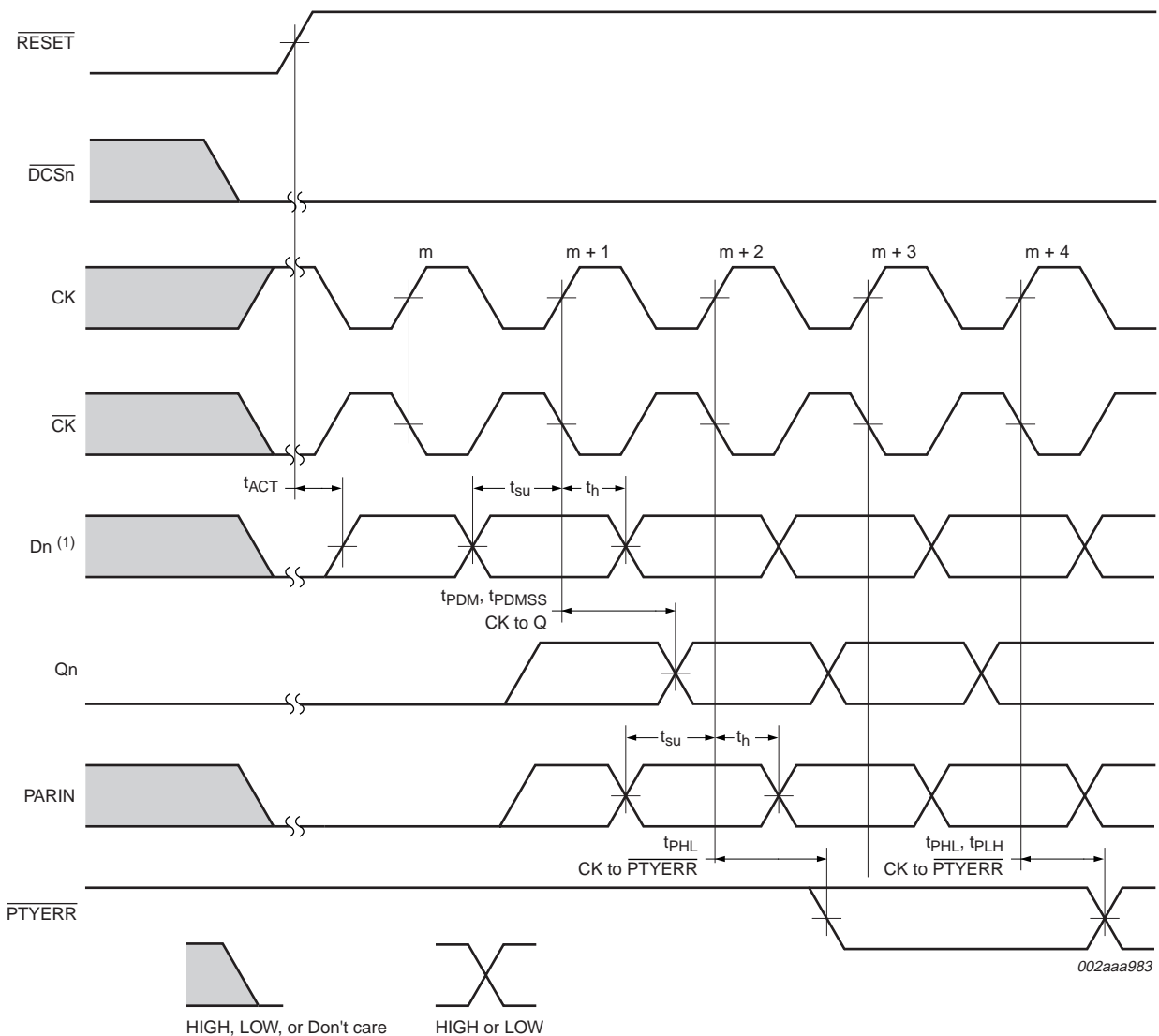
The SSTU32865 incorporates a parity function, whereby the signal received on input pin PARIN is received as parity to the register, one clock cycle later than the CS-gated inputs. The received parity bit is then compared to the parity calculated across these same inputs by the register parity logic to verify that the information has not been corrupted. The 22 CS-gated input signals will be latched and re-driven on the first clock, and any error will be reported one clock cycle later via the  $\overline{PTYERR}$  output pin (driven LOW for two consecutive clock cycles).  $\overline{PTYERR}$  is an open-drain output, allowing multiple modules to share a common signal pin for reporting the occurrence of a parity error during a valid command cycle (coincident with the re-driven signals). This output is driven LOW for two consecutive clock cycles to allow the memory controller sufficient time to sense and capture the error even. A LOW state on  $\overline{PTYERR}$  indicates that a parity error has occurred.

#### 7.3.3 Reset ( $\overline{RESET}$ )

Similar to the  $\overline{RESET}$  pin on the industry-standard SSTU32864, this pin is used to clear all internal latches and all outputs will be driven LOW quickly except the  $\overline{PTYERR}$  output, which will be floated (and will normally default HIGH by their external pull-up).

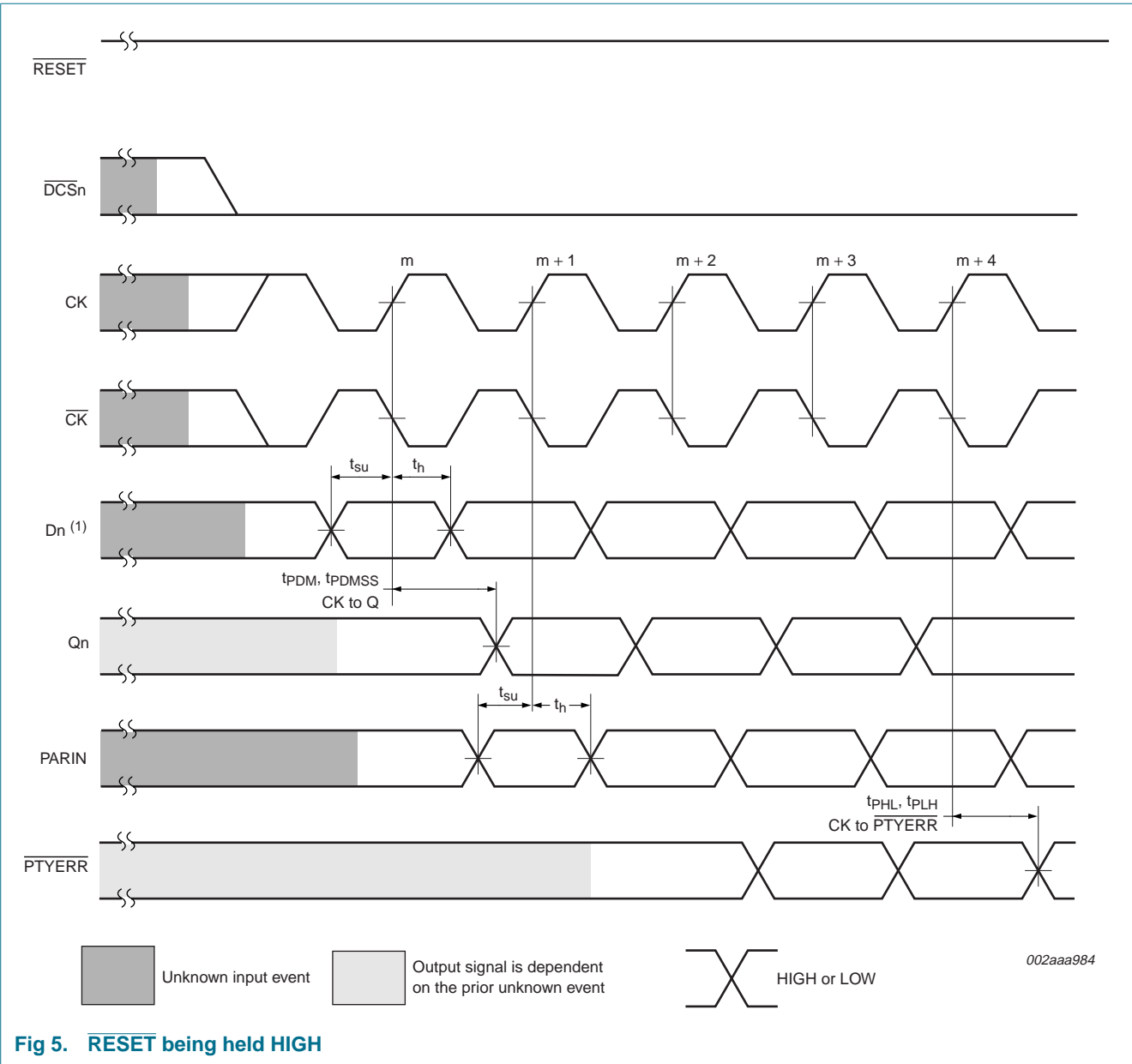
#### 7.3.4 Power-up sequence

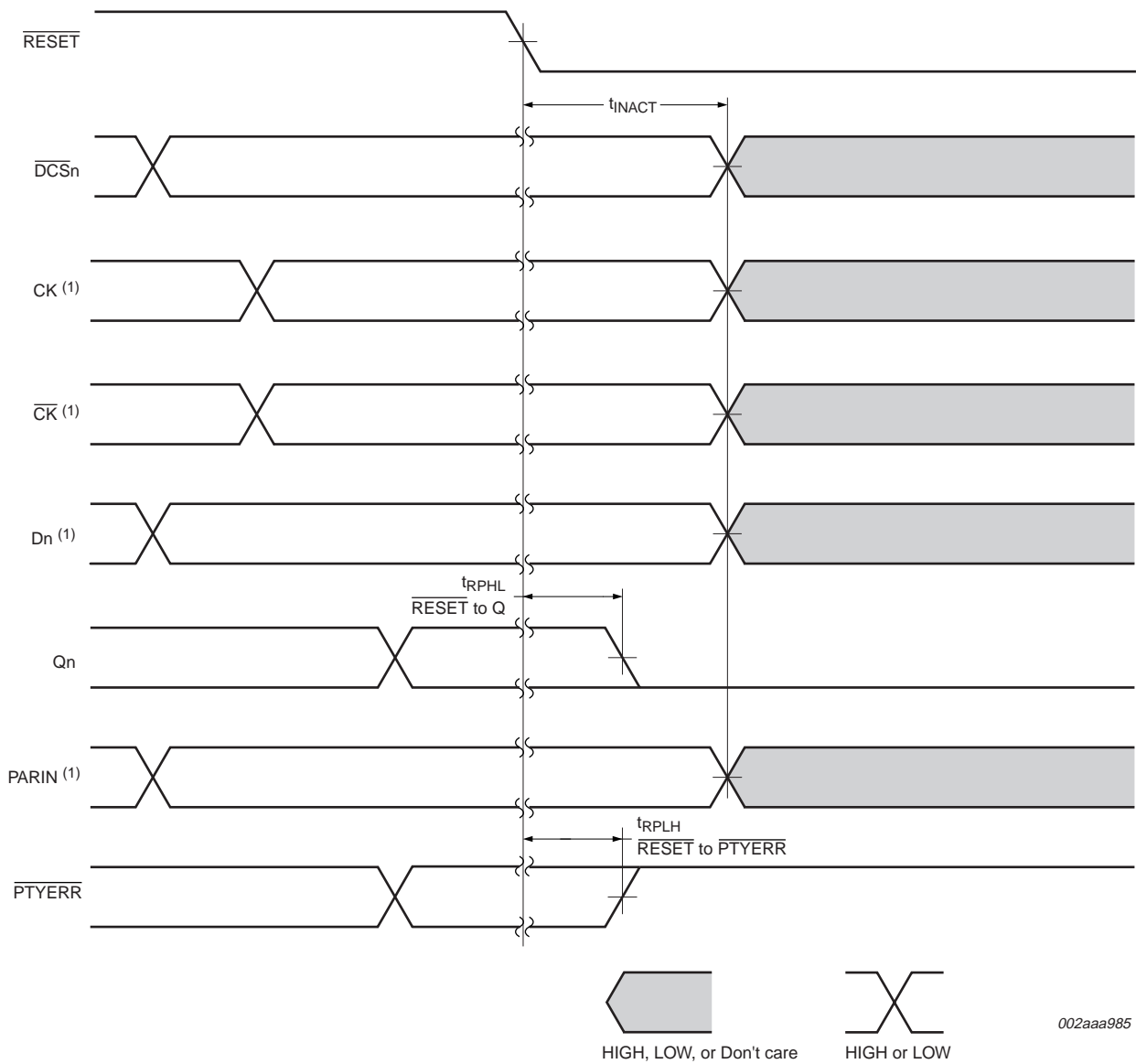
The reset function for the SSTU32865 is similar to that of the SSTU32864 except that the  $\overline{PTYERR}$  signal is also cleared and will be held clear (HIGH) for three consecutive clock cycles.



- (1) After  $\overline{\text{RESET}}$  is switched from LOW to HIGH, all data and PARIN input signals must be set and held LOW for a minimum time of  $t_{\text{ACT(max)}}$  to avoid false error.

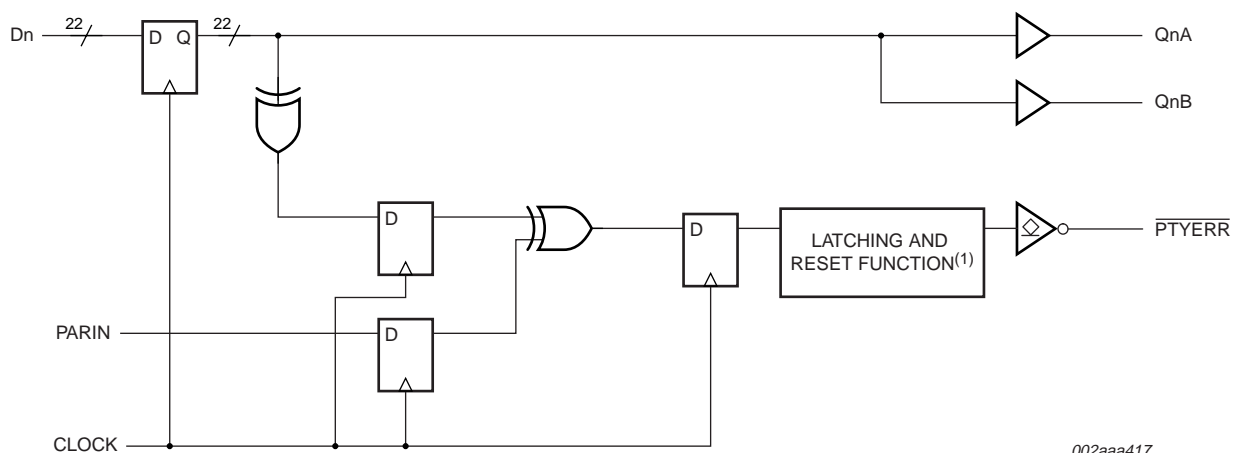
Fig 4.  $\overline{\text{RESET}}$  switches from LOW to HIGH





(1) After  $\overline{\text{RESET}}$  is switched from HIGH to LOW, all data and clock input signals must be set and held at valid logic levels (not floating) for a minimum time of  $t_{\text{INACT(max)}}$ .

**Fig 6.  $\overline{\text{RESET}}$  switches from HIGH to LOW**



(1) This function holds the error for two cycles. For details, see [Section 7 "Functional description"](#) and [Figure 4 "RESET switches from LOW to HIGH"](#).

**Fig 7. Parity logic diagram**

## 8. Limiting values

**Table 6: Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol    | Parameter   | Conditions                                      | Min      | Max            | Unit |
|-----------|---|---|----------|----------------|------|
| $V_{DD}$  | supply voltage                                      |   | -0.5     | +2.5           | V    |
| $V_I$     | receiver input voltage                              |   | [2] -0.5 | +2.5           | V    |
| $V_O$     | driver output voltage                               |   | [2] -0.5 | $V_{DD} + 0.5$ | V    |
| $I_{IK}$  | input clamp current                                 | $V_I < 0\text{ V}$ or $V_I > V_{DD}$            | -        | -50            | mA   |
| $I_{OK}$  | output clamp current                                | $V_O < 0\text{ V}$ or $V_O > V_{DD}$            | -        | $\pm 50$       | mA   |
| $I_O$     | continuous output current                           | $0\text{ V} < V_O < V_{DD}$                     | -        | $\pm 50$       | mA   |
| $I_{CCC}$ | continuous current through each $V_{DD}$ or GND pin |   | -        | $\pm 100$      | mA   |
| $T_{stg}$ | storage temperature                                 |   | -65      | +150           | °C   |
| $V_{esd}$ | electrostatic discharge voltage                     | Human Body Model (HBM); 1.5 k $\Omega$ ; 100 pF | 2        | -              | kV   |
|           |   | Machine Model (MM); 0 $\Omega$ ; 200 pF         | 200      | -              | V    |

[1] Stresses beyond those listed under 'absolute maximum ratings' may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under 'recommended operating conditions' is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

## 9. Recommended operating conditions

**Table 7: Recommended operating conditions**

| Symbol       | Parameter                                 | Conditions                 | Min                           | Typ                  | Max                       | Unit |
|--------------|---|----------------------------|-------------------------------|----------------------|---------------------------|------|
| $V_{DD}$     | supply voltage                            |                            | 1.7                           | -                    | 1.9                       | V    |
| $V_{REF}$    | reference voltage                         |                            | $0.49 \times V_{DD}$          | $0.50 \times V_{DD}$ | $0.51 \times V_{DD}$      | V    |
| $V_{TT}$     | termination voltage                       |                            | $V_{REF} - 40\text{ mV}$      | $V_{REF}$            | $V_{REF} + 40\text{ mV}$  | V    |
| $V_I$        | input voltage                             |                            | 0                             | -                    | $V_{DD}$                  | V    |
| $V_{IH(AC)}$ | AC HIGH-level input voltage               | data inputs (Dn)           | [1] $V_{REF} + 250\text{ mV}$ | -                    | -                         | V    |
| $V_{IL(AC)}$ | AC LOW-level input voltage                | data inputs (Dn)           | [1] -                         | -                    | $V_{REF} - 250\text{ mV}$ | V    |
| $V_{IH(DC)}$ | DC HIGH-level input voltage               | data inputs (Dn)           | [1] $V_{REF} + 125\text{ mV}$ | -                    | -                         | V    |
| $V_{IL(DC)}$ | DC LOW-level input voltage                | data inputs (Dn)           | [1] -                         | -                    | $V_{REF} - 125\text{ mV}$ | V    |
| $V_{IH}$     | HIGH-level input voltage                  | $\overline{\text{RESET}}$  | [2] $0.65 \times V_{DD}$      | -                    | -                         | V    |
| $V_{IL}$     | LOW-level input voltage                   | $\overline{\text{RESET}}$  | [2] -                         | -                    | $0.35 \times V_{DD}$      | V    |
| $V_{ICR}$    | common mode input voltage range           | CK, $\overline{\text{CK}}$ | 0.675                         | -                    | 1.125                     | V    |
| $V_{ID}$     | differential input voltage                | CK, $\overline{\text{CK}}$ | 600                           | -                    | -                         | mV   |
| $I_{OH}$     | HIGH-level output current                 |                            | -                             | -                    | -8                        | mA   |
| $I_{OL}$     | LOW-level output current                  |                            | -                             | -                    | 8                         | mA   |
| $T_{amb}$    | operating ambient temperature in free air |                            | 0                             | -                    | +70                       | °C   |

[1] The differential inputs must not be floating, unless  $\overline{\text{RESET}}$  is LOW.

[2] The  $\overline{\text{RESET}}$  input of the device must be held at valid logic levels (not floating) to ensure proper device operation.

## 10. Characteristics

**Table 8: Characteristics**

Over recommended operating conditions, unless otherwise noted.

| Symbol    | Parameter  | Conditions   | Min | Typ | Max     | Unit          |
|-----------|--|--|-----|-----|---------|---------------|
| $V_{OH}$  | HIGH-level output voltage                              | $I_{OH} = -6 \text{ mA}$ ; $V_{DD} = 1.7 \text{ V}$  | 1.2 | -   | -       | V             |
| $V_{OL}$  | LOW-level output voltage                               | $I_{OL} = 6 \text{ mA}$ ; $V_{DD} = 1.7 \text{ V}$   | -   | -   | 0.5     | V             |
| $I_I$     | input current  | all inputs; $V_I = V_{DD}$ or GND;<br>$V_{DD} = 1.9 \text{ V}$   | -   | -   | $\pm 5$ | $\mu\text{A}$ |
| $I_{DD}$  | static standby current                                 | $\overline{\text{RESET}} = \text{GND}$ ; $V_{DD} = 1.9 \text{ V}$  | -   | -   | 100     | $\mu\text{A}$ |
|           | static operating current                               | $\overline{\text{RESET}} = V_{DD}$ ; $V_{DD} = 1.9 \text{ V}$ ;<br>$V_I = V_{IH(AC)}$ or $V_{IL(AC)}$  | -   | -   | 40      | mA            |
| $I_{DDD}$ | dynamic operating current per MHz, clock only          | $\overline{\text{RESET}} = V_{DD}$ ;<br>$V_I = V_{IH(AC)}$ or $V_{IL(AC)}$ ; CK and $\overline{\text{CK}}$ switching at 50 % duty cycle.<br>$I_O = 0 \text{ mA}$ ; $V_{DD} = 1.8 \text{ V}$  | -   | 16  | -       | $\mu\text{A}$ |
|           | dynamic operating current per MHz, per each data input | $\overline{\text{RESET}} = V_{DD}$ ;<br>$V_I = V_{IH(AC)}$ or $V_{IL(AC)}$ ; CK and $\overline{\text{CK}}$ switching at 50 % duty cycle. One data input switching at half clock frequency, 50 % duty cycle.<br>$I_O = 0 \text{ mA}$ ; $V_{DD} = 1.8 \text{ V}$ | -   | 19  | -       | $\mu\text{A}$ |
| $C_i$     | input capacitance, data inputs                         | $V_I = V_{REF} \pm 250 \text{ mV}$ ; $V_{DD} = 1.8 \text{ V}$  | 2.5 | -   | 3.5     | pF            |
|           | input capacitance, CK and $\overline{\text{CK}}$       | $V_{ICR} = 0.9 \text{ V}$ ; $V_{ID} = 600 \text{ mV}$ ;<br>$V_{DD} = 1.8 \text{ V}$  | 2   | -   | 3       | pF            |
|           | input capacitance, $\overline{\text{RESET}}$           | $V_I = V_{DD}$ or GND; $V_{DD} = 1.8 \text{ V}$  | 3   | -   | 5       | pF            |



**Table 9: Timing requirements**

Over recommended operating conditions, unless otherwise noted.

| Symbol             | Parameter  | Conditions                                  | Min     | Typ | Max | Unit |
|--------------------|--|---|---------|-----|-----|------|
| $f_{\text{clock}}$ | clock frequency  |   | -       | -   | 450 | MHz  |
| $t_W$              | pulse duration, CK, $\overline{\text{CK}}$ HIGH or LOW |   | 1       | -   | -   | ns   |
| $t_{\text{ACT}}$   | differential inputs active time                        |   | [1] [2] | -   | 10  | ns   |
| $t_{\text{INACT}}$ | differential inputs inactive time                      |   | [1] [3] | -   | 15  | ns   |
| $t_{\text{su}}$    | setup time, Chip Select                                | DCS0, DCS1 valid before clock switching     | 0.7     | -   | -   | ns   |
|                    | setup time, Data                                       | Dn valid before clock switching             | 0.5     | -   | -   | ns   |
|                    | setup time, PARIN                                      | PARIN before CK and $\overline{\text{CK}}$  | 0.5     | -   | -   | ns   |
| $t_h$              | hold time  | input to remain valid after clock switching | 0.5     | -   | -   | ns   |
|                    | hold time, PARIN                                       | PARIN after CK and $\overline{\text{CK}}$   | 0.5     | -   | -   | ns   |

[1] This parameter is not necessarily production tested.

[2] Data inputs must be active below a minimum time of  $t_{\text{ACT(max)}}$  after  $\overline{\text{RESET}}$  is taken HIGH.[3] Data and clock inputs must be held at valid levels (not floating) a minimum time of  $t_{\text{INACT(max)}}$  after  $\overline{\text{RESET}}$  is taken LOW.**Table 10: Switching characteristics**

Over recommended operating conditions, unless otherwise noted.

| Symbol             | Parameter                                 | Conditions   | Min      | Typ | Max | Unit |
|--------------------|---|--|----------|-----|-----|------|
| $f_{\text{MAX}}$   | maximum input clock frequency             |  | 450      | -   | -   | MHz  |
| $t_{\text{PDM}}$   | propagation delay                         | CK and $\overline{\text{CK}}$ to output                      | [1] 1.41 | -   | 1.8 | ns   |
| $t_{\text{LH}}$    | LOW-to-HIGH delay                         | CK and $\overline{\text{CK}}$ to $\overline{\text{PTYERR}}$  | 1.2      | -   | 3   | ns   |
| $t_{\text{HL}}$    | HIGH-to-LOW delay                         | CK and $\overline{\text{CK}}$ to $\overline{\text{PTYERR}}$  | 1        | -   | 3   | ns   |
| $t_{\text{PLH}}$   | LOW-to-HIGH propagation delay             | from $\overline{\text{RESET}}$ to $\overline{\text{PTYERR}}$ | -        | -   | 3   | ns   |
| $t_{\text{PDMSS}}$ | propagation delay, simultaneous switching | CK and $\overline{\text{CK}}$ to output                      | [1] [2]  | -   | 2.0 | ns   |
| $t_{\text{PHL}}$   | propagation delay                         | $\overline{\text{RESET}}$ to output                          | -        | -   | 3   | ns   |

[1] Includes 350 ps of test-load transmission line delay.

[2] This parameter is not necessarily production tested.

**Table 11: Output edge rates**

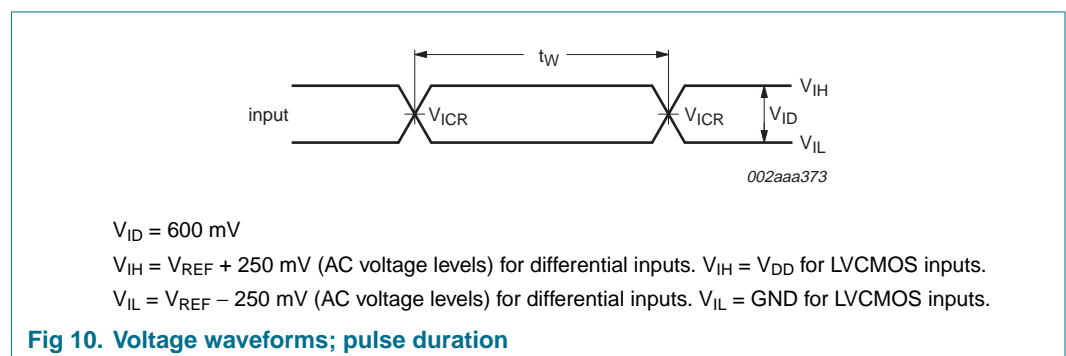
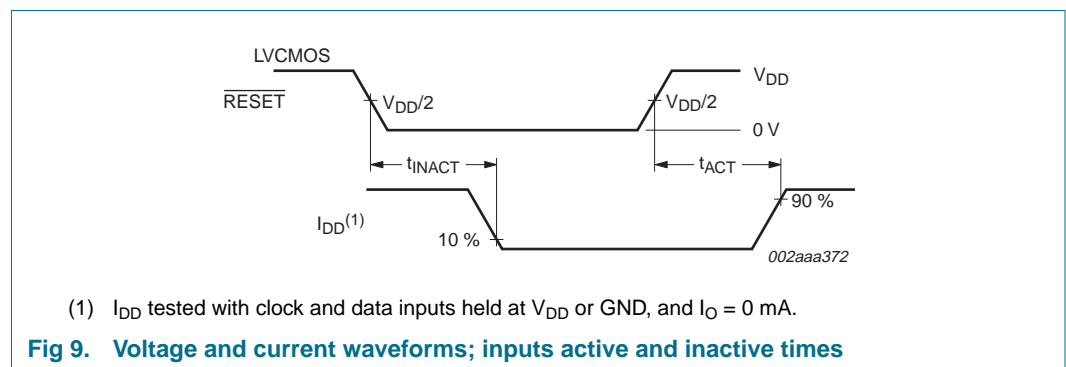
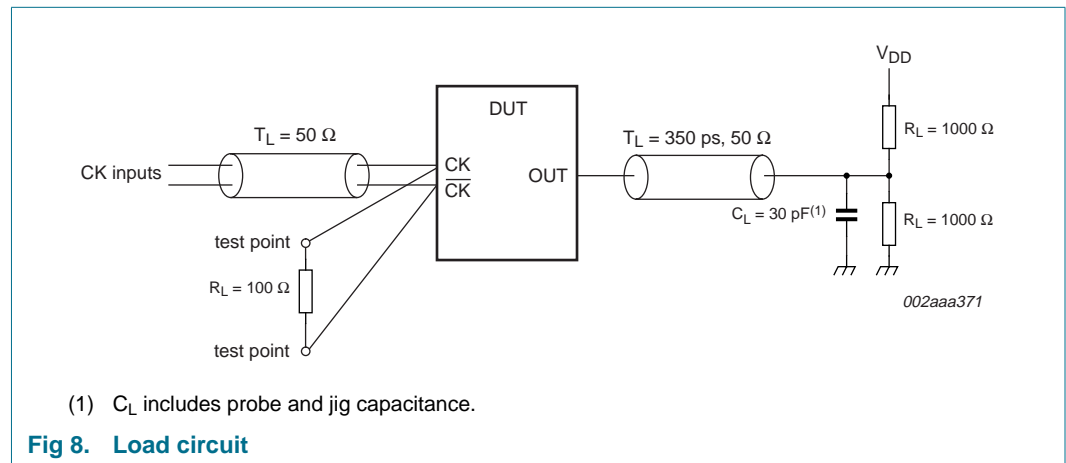
Over recommended operating conditions, unless otherwise noted.

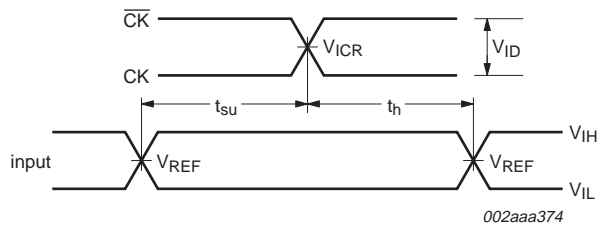
| Symbol           | Parameter   | Conditions | Min | Typ | Max | Unit |
|------------------|---|------------|-----|-----|-----|------|
| $dV/dt_r$        | rising edge slew rate                               |            | 1   | -   | 4   | V/ns |
| $dV/dt_f$        | falling edge slew rate                              |            | 1   | -   | 4   | V/ns |
| $dV/dt_{\Delta}$ | absolute difference between $dV/dt_r$ and $dV/dt_f$ |            | -   | -   | 1   | V/ns |

## 11.1 Test circuit

All input pulses are supplied by generators having the following characteristics: Pulse Repetition Rate (PRR)  $\leq 10$  MHz;  $Z_0 = 50 \Omega$ ; input slew rate = 1 V/ns  $\pm 20$  %, unless otherwise specified.

The outputs are measured one at a time with one transition per measurement.





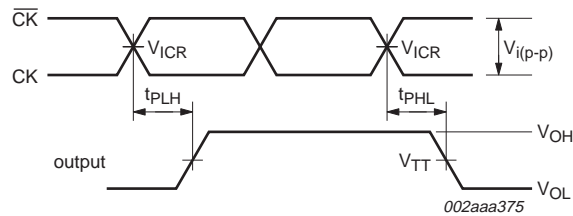
$$V_{ID} = 600 \text{ mV}$$

$$V_{REF} = V_{DD}/2$$

$V_{IH} = V_{REF} + 250 \text{ mV}$  (AC voltage levels) for differential inputs.  $V_{IH} = V_{DD}$  for LVCMOS inputs.

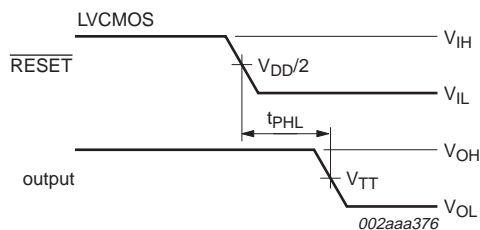
$V_{IL} = V_{REF} - 250 \text{ mV}$  (AC voltage levels) for differential inputs.  $V_{IL} = \text{GND}$  for LVCMOS inputs.

**Fig 11. Voltage waveforms; setup and hold times**



$t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{PD}$ .

**Fig 12. Voltage waveforms; propagation delay times (clock to output)**



$t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{PD}$ .

$V_{IH} = V_{REF} + 250 \text{ mV}$  (AC voltage levels) for differential inputs.  $V_{IH} = V_{DD}$  for LVCMOS inputs.

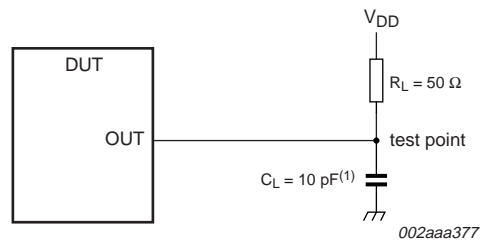
$V_{IL} = V_{REF} - 250 \text{ mV}$  (AC voltage levels) for differential inputs.  $V_{IL} = \text{GND}$  for LVCMOS inputs.

**Fig 13. Voltage waveforms; propagation delay times (reset to output)**

## 11.2 Output slew rate measurement

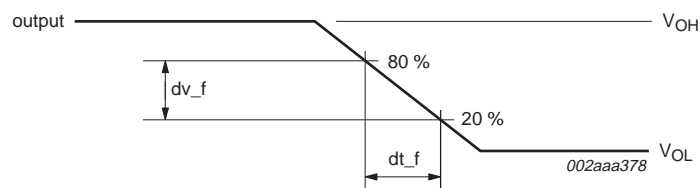
$$V_{DD} = 1.8 \text{ V} \pm 0.1 \text{ V.}$$

All input pulses are supplied by generators having the following characteristics:  
 $PRR \leq 10 \text{ MHz}$ ;  $Z_0 = 50 \Omega$ ; input slew rate =  $1 \text{ V/ns} \pm 20 \%$ , unless otherwise specified.

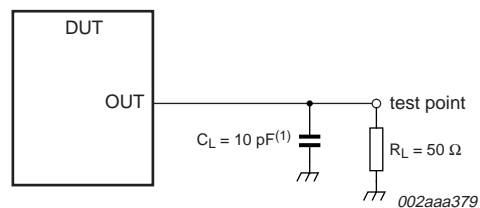


(1)  $C_L$  includes probe and jig capacitance.

**Fig 14. Load circuit, HIGH-to-LOW slew rate measurement**

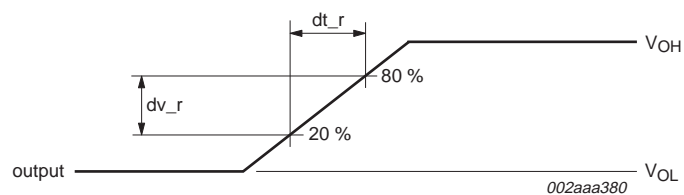


**Fig 15. Voltage waveforms, HIGH-to-LOW slew rate measurement**



(1)  $C_L$  includes probe and jig capacitance.

**Fig 16. Load circuit, LOW-to-HIGH slew rate measurement**

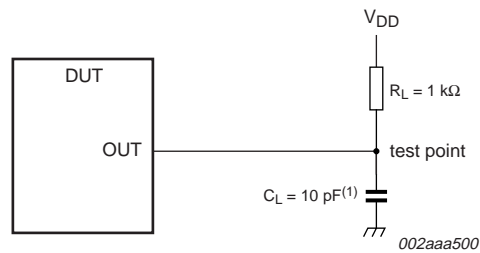


**Fig 17. Voltage waveforms, LOW-to-HIGH slew rate measurement**

### 11.3 Error output load circuit and voltage measurement

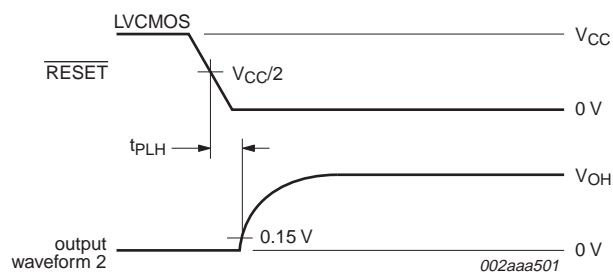
$$V_{DD} = 1.8 \text{ V} \pm 0.1 \text{ V.}$$

All input pulses are supplied by generators having the following characteristics:  
 $PRR \leq 10 \text{ MHz}$ ;  $Z_0 = 50 \Omega$ ; input slew rate =  $1 \text{ V/ns} \pm 20 \%$ , unless otherwise specified.

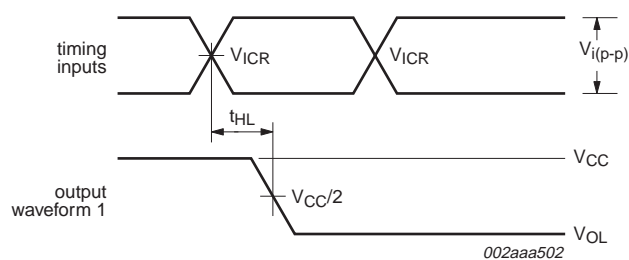


(1)  $C_L$  includes probe and jig capacitance.

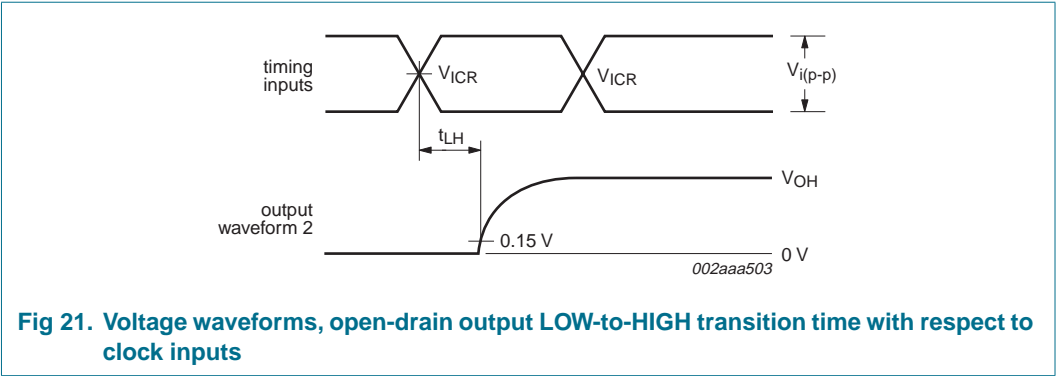
**Fig 18. Load circuit, error output measurements**



**Fig 19. Voltage waveforms, open-drain output LOW-to-HIGH transition time with respect to RESET input**



**Fig 20. Voltage waveforms, open-drain output HIGH-to-LOW transition time with respect to clock inputs**



12. Package outline

TFBGA160: plastic thin fine-pitch ball grid array package; 160 balls; body 9 x 13 x 0.8 mm SOT802-1

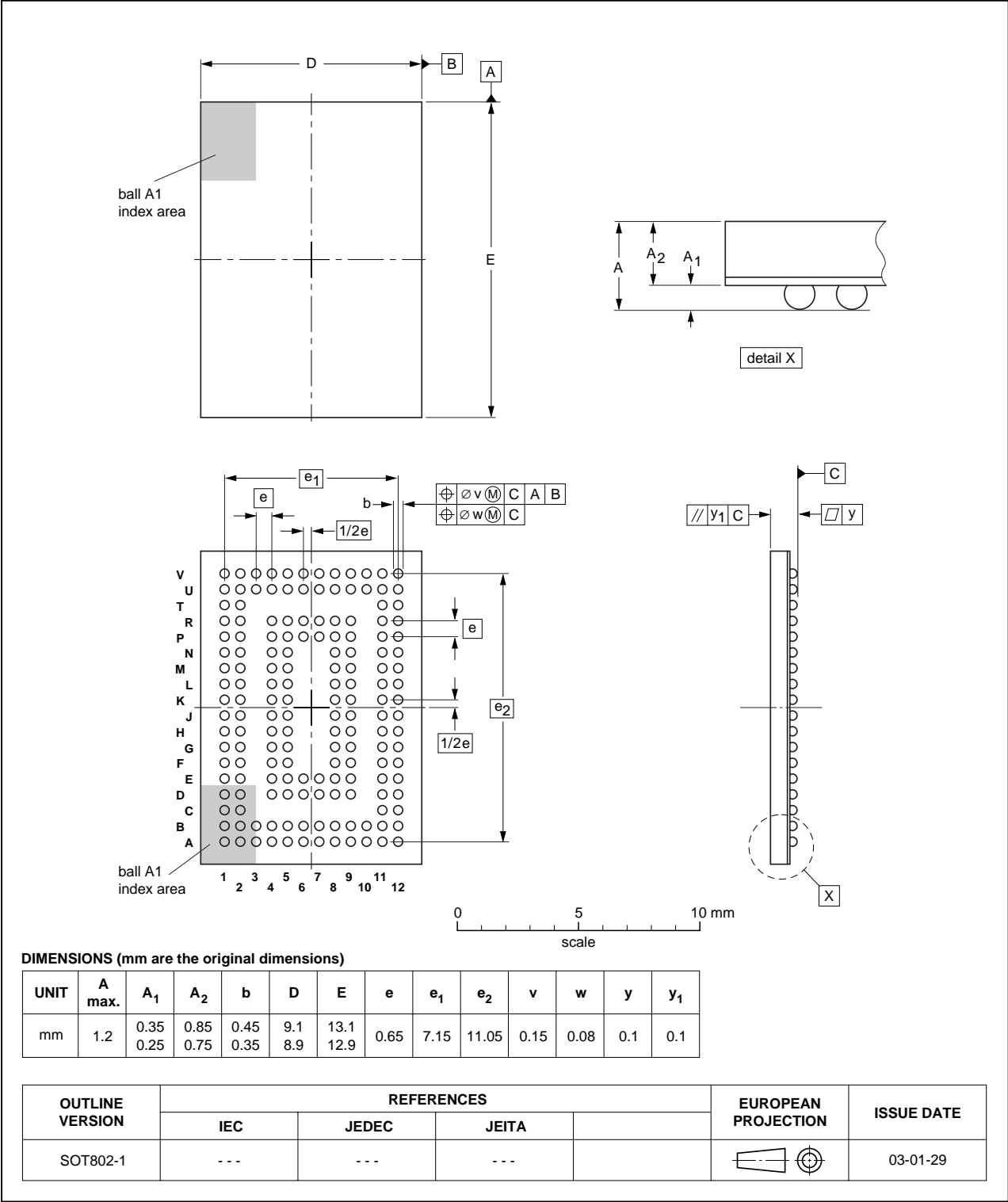


Fig 22. Package outline SOT802-1 (TFBGA160)

## 13. Soldering

### 13.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

### 13.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness  $\geq 2.5$  mm
  - for packages with a thickness  $< 2.5$  mm and a volume  $\geq 350$  mm<sup>3</sup> so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness  $< 2.5$  mm and a volume  $< 350$  mm<sup>3</sup> so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

### 13.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;



- smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

### 13.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

### 13.5 Package related soldering information

**Table 12: Suitability of surface mount IC packages for wave and reflow soldering methods**

| Package <sup>[1]</sup>   | Soldering method                   |                       |
|--|------------------------------------|-----------------------|
|  | Wave                               | Reflow <sup>[2]</sup> |
| BGA, HTSSON..T <sup>[3]</sup> , LBGA, LFBGA, SQFP, SSOP..T <sup>[3]</sup> , TFBGA, VFBGA, XSON | not suitable                       | suitable              |
| DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS           | not suitable <sup>[4]</sup>        | suitable              |
| PLCC <sup>[5]</sup> , SO, SOJ  | suitable                           | suitable              |
| LQFP, QFP, TQFP  | not recommended <sup>[5] [6]</sup> | suitable              |
| SSOP, TSSOP, VSO, VSSOP  | not recommended <sup>[7]</sup>     | suitable              |
| CWQCCN..L <sup>[8]</sup> , PMFP <sup>[9]</sup> , WQCCN..L <sup>[8]</sup>                       | not suitable                       | not suitable          |

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

- [4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
- [5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- [6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- [7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
- [8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.
- [9] Hot bar soldering or manual soldering is suitable for PMFP packages.

## 14. Revision history

Table 13: Revision history

| Document ID    | Release date   | Data sheet status  | Change notice | Doc. number    | Supersedes   |
|----------------|--|--------------------|---------------|----------------|--------------|
| SSTU32865_2    | 20040928   | Product data sheet | -             | 9397 750 13799 | SSTU32865-01 |
| Modifications: | <ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors.</li> <li><a href="#">Section 1 "General description"</a>: acronym TFBGA defined.</li> <li><a href="#">Section 2 "Features"</a>: acronym SSTL defined.</li> <li>Additional features added to <a href="#">Section 2 "Features"</a></li> <li><a href="#">Section 6 "Pinning information"</a> <ul style="list-style-type: none"> <li>change 'MCL' to 'm.c.l.' and 'MCH' to 'm.c.h.'</li> <li>add descriptions for VDDL and VDDR in <a href="#">Table 2 "Pin description"</a></li> <li>added <a href="#">Figure 2 "Pin configuration for TFBGA160"</a></li> <li>added <a href="#">Figure 3 "Ball mapping"</a> (replaces Table 2 "Ball mapping")</li> </ul> </li> <li><a href="#">Table 3 "Function table (each flip-flop)"</a> and <a href="#">Table 4 "Parity and standby function table"</a> moved to <a href="#">Section 7.1 on page 8</a>.</li> <li><a href="#">Table 3 "Function table (each flip-flop)"</a>: add <a href="#">Table note 1</a> and its reference at 'Outputs'.</li> <li><a href="#">Table 4 "Parity and standby function table"</a>: <ul style="list-style-type: none"> <li><a href="#">Table note 2</a>: change 'This transition assumes ...' to 'This condition assumes ...'.</li> <li>Add <a href="#">Table note 3</a>.</li> </ul> </li> <li><a href="#">Section 7.3.4 "Power-up sequence"</a>: add '(HIGH)' after '... and will be held clear'.</li> <li><a href="#">Table 6 "Limiting values"</a>: <ul style="list-style-type: none"> <li>Symbol <math>V_i</math> changed to <math>V_I</math>; Symbol <math>V_o</math> changed to <math>V_O</math>.</li> <li>Symbols <math>ESD_{HBM}</math> and <math>ESD_{MM}</math> replaced with <math>V_{esd}</math> (added model types under "Conditions")</li> </ul> </li> <li><a href="#">Table 7 "Recommended operating conditions"</a>: <ul style="list-style-type: none"> <li>change <math>V_{IH}</math> (for data inputs) to <math>V_{IH(AC)}</math> and <math>V_{IH(DC)}</math>; condition changed to 'data inputs (Dn)'</li> <li>change <math>V_{IL}</math> (for data inputs) to <math>V_{IL(AC)}</math> and <math>V_{IL(DC)}</math>; condition changed to 'data inputs (Dn)'</li> <li>Table note split into 2 notes; references added.</li> </ul> </li> <li><a href="#">Table 8 "Characteristics"</a> <ul style="list-style-type: none"> <li>change <math>I_{DDD}</math> Parameter from "dynamic operating current ..." to "dynamic operating current per MHz ..."; change Unit from "<math>\mu A/MHz</math>" to "<math>\mu A</math>".</li> <li>change Typical value for <math>I_{DDD}</math> (clock only) from TBD to 16 <math>\mu A</math></li> <li>change Typical value for <math>I_{DDD}</math> (per each data input) from TBD to 19 <math>\mu A</math></li> </ul> </li> <li><a href="#">Table 9 "Timing requirements"</a>: <ul style="list-style-type: none"> <li>change symbol <math>f_{CLOCK}</math> to <math>f_{clock}</math></li> <li>change <math>f_{clock}</math> maximum value from 270 MHz to 450 MHz</li> <li>change symbol <math>t_{SU}</math> to <math>t_{su}</math>; under 'Conditions', change 'Chip Select' to '<math>\overline{DCS0}</math>, <math>\overline{DCS1}</math>'.</li> <li>change symbol <math>t_H</math> to <math>t_h</math></li> </ul> </li> <li><a href="#">Table 10 "Switching characteristics"</a>: <ul style="list-style-type: none"> <li>change <math>f_{MAX}</math> minimum value from 270 MHz to 450 MHz</li> <li>change <math>t_{PDM}</math> maximum value from 2.15 ns to 1.8 ns</li> <li>change <math>t_{PDMSS}</math> maximum value from 2.35 ns to 2.0 ns</li> </ul> </li> <li><a href="#">Section 11.1 "Test circuit"</a>: acronym PRR defined; titles for <a href="#">Figure 12</a> and <a href="#">Figure 13</a> modified.</li> </ul> |                    |               |                |              |
| SSTU32865-01   | 20040705   | Product data       | -             | 9397 750 10942 | -            |

## 15. Data sheet status

| Level | Data sheet status <sup>[1]</sup> | Product status <sup>[2] [3]</sup> | Definition   |
|-------|----------------------------------|-----------------------------------|--|
| I     | Objective data                   | Development                       | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.  |
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