DATA SHEET

SSTV16857

14-bit SSTL_2 registered driver with differential clock inputs

Product data
Supersedes data of 2002 Jun 05

2002 Sep 27

Philips Semiconductors

14-bit SSTL_2 registered driver with differential clock inputs

SSTV16857

FEATURES

- Stub-series terminated logic for 2.5 V V_{DDQ} (SSTL_2)
- Optimized for DDR (Double Data Rate) SDRAM applications
- Inputs compatible with JESD8–9 SSTL_2 specifications.
- Flow-through architecture optimizes PCB layout
- ESD classification testing is done to JEDEC Standard JESD22. Protection exceeds 2000 V to HBM per method A114.
- Latch-up testing is done to JEDEC Standard JESD78, which exceeds 100 mA.
- Same form, fit, and function as SSTL16877
- Full DDR 200/266 solution @ 2.5 V when used with PCKV857
- See SSTV16856 for driver/buffer version with mode select.
- Available in TSSOP-48, TVSOP-48 and 56 ball VFBGA packages

DESCRIPTION

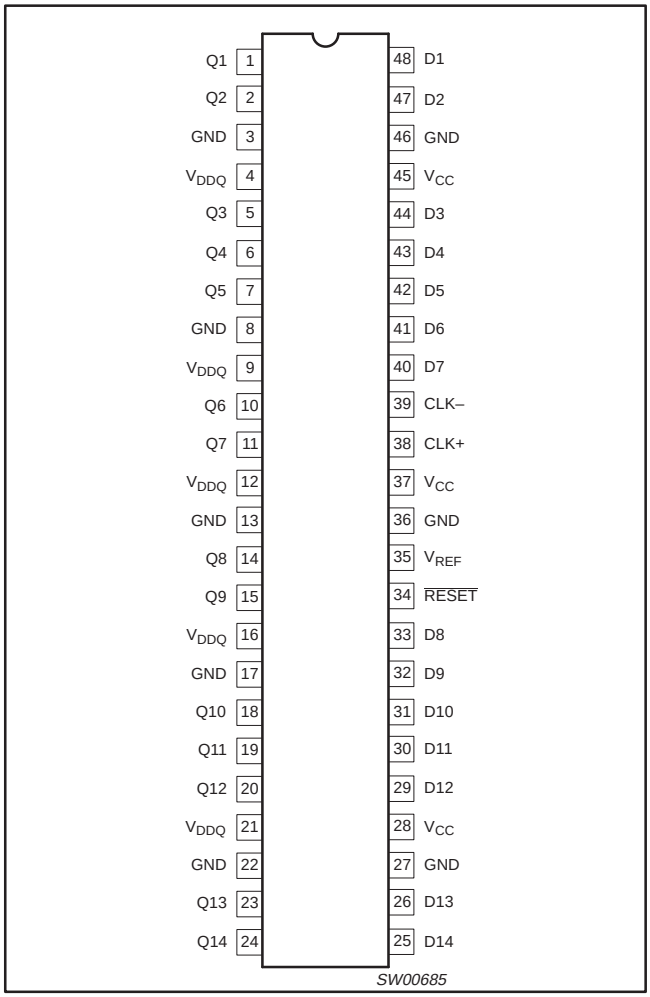
The SSTV16857 is a 14-bit SSTL_2 registered driver with differential clock inputs, designed to operate between 2.3 V and 2.7 V. V_{DDQ} must not exceed V_{CC}. Inputs are SSTL_2 type with V_{REF} normally at 0.5*V_{DDQ}. The outputs support class I which can be used for standard stub-series applications or capacitive loads. Master reset ($\overline{RESET}$) asynchronously resets all registers to zero.

The SSTV16857 is intended to be incorporated into standard DIMM (Dual In-Line Memory Module) designs defined by JEDEC, such as DDR (Double Data Rate) SDRAM or SDRAM II Memory Modules. Different from traditional SDRAM, DDR SDRAM transfers data on both clock edges (rising and falling), thus doubling the peak bus bandwidth. A DDR DRAM rated at 133 MHz will have a burst rate of 266 MHz. The modules require between 23 and 27 registered control and address lines, so two 14-bit wide devices will be used on each module. The SSTV16857 is intended to be used for SSTL_2 input and output signals.

The device data inputs consist of differential receivers. One differential input is tied to the input pin while the other is tied to a reference input pad, which is shared by all inputs.

The clock input is fully differential to be compatible with DRAM devices that are installed on the DIMM. However, since the control inputs to the SDRAM change at only half the data rate, the device must only change state on the positive transition of the CLK signal. In order to be able to provide defined outputs from the device even before a stable clock has been supplied, the device must support an asynchronous input pin (reset), which when held to the LOW state will assume that all registers are reset to the LOW state and all outputs drive a LOW signal as well.

PIN CONFIGURATION



QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay; CLK to Qn	C_L = 30 pF; V_{DDQ} = 2.5 V	2.4	ns
C_I	Input capacitance	V_{CC} = 2.5 V	2.9	pF

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
48-Pin Plastic TSSOP	0 to +70 °C	SSTV16857DGG	SOT362-1
48-Pin Plastic TSSOP (TVSOP)	0 to +70 °C	SSTV16857DGV	SOT480-1
56-Ball Plastic VFBGA	0 to +70 °C	SSTV16857EV	SOT702-1

PIN DESCRIPTION

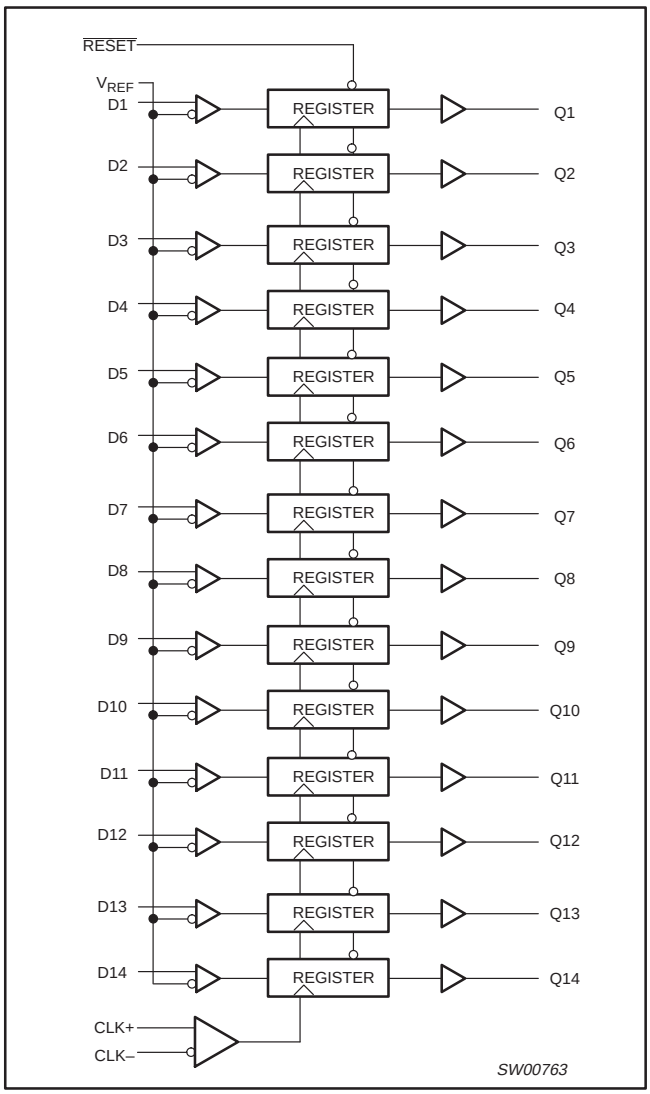
PIN NUMBER	SYMBOL	NAME AND FUNCTION
34	$\overline{RESET}$	LVCMOS asynchronous master reset (Active LOW)
48, 47, 44, 43, 42, 41, 40, 33, 32, 31, 30, 29, 26, 25	D1 – D14	SSTL_2 data inputs
1, 2, 5, 6, 7, 10, 11, 14, 15, 18, 19, 20, 23, 24	Q1 – Q14	SSTL_2 data outputs
35	V_{REF}	SSTL_2 input reference level
3, 8, 13, 17, 22, 27, 36, 46	GND	Ground (0 V)
28, 37, 45	V_{CC}	Positive supply voltage
4, 9, 12, 16, 21	V_{DDQ}	Output supply voltage
38 39	CLK+ CLK–	Differential clock inputs

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{RESET}$	$\overline{CLK}$	CLK	D	Q
L	X	X	X	L
H	↓	↑	H	H
H	↓	↑	L	L
H	L or H	L or H	X	Q_0

H = High voltage level
L = High voltage level
↓ = High-to-Low transition
↑ = Low-to-High transition
X = Don't care

LOGIC DIAGRAM



BALL CONFIGURATION

	1	2	3	4	5	6
A	Q1	NC	NC	NC	NC	D1
B	GND	Q2	V_{CC}	V_{CC}	D2	GND
C	Q4	Q3	Q5	D5	D3	D4
D	V_{CC}	GND	Q6	CLK–	D6	D7
E	V_{CC}	Q7			CLK+	V_{CC}
F	GND	Q8			V_{REF}	GND
G	V_{CC}	GND	Q9	$\overline{\text{RESET}}$	D9	D8
H	Q11	Q12	Q10	D10	D12	D11
J	GND	Q13	V_{CC}	V_{CC}	D13	GND
K	Q14	NC	NC	NC	NC	D14

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ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITION	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage		–0.5	+4.6	V
I_{IK}	DC input diode current	$V_I < 0$	—	–50	mA
V_I	DC input voltage[3]		–0.5	V_{DDQ} + 0.5	V
I_{OK}	DC output diode current	$V_O < 0$	—	–50	mA
V_{OUT}	DC output voltage[3]		–0.5	V_{DDQ} + 0.5	V
I_{OUT}	DC output current	V_O = 0 to V_{DDQ}	—	±50	mA
	Continuous current[4]	V_{CC}, V_{DDQ}, or GND	—	±100	
T_{stg}	Storage temperature range[2]		–65	+150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
4. The continuous current at V_{CC}, V_{DDQ}, or GND should not exceed ±100 mA.

RECOMMENDED OPERATING CONDITIONS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		2.3	2.5	2.7	V
V_{DDQ}	Output supply voltage		2.3	2.5	2.7	V
V_{REF}	Reference voltage (V_{REF} = 0.5 x V_{DDQ})		1.15	1.25	1.35	V
V_{TT}	Termination voltage		V_{REF} – 40 mV	V_{REF}	V_{REF} + 40 mV	V
V_I	Input voltage		0	—	V_{CC}	V
V_{IH}	AC HIGH-level input voltage	All inputs	V_{REF} + 350 mV	—	—	V
V_{IL}	AC LOW-level input voltage	All inputs	—	—	V_{REF} – 350 mV	V
V_{IH}	DC HIGH-level input voltage	All inputs	V_{REF} + 180 mV	—	V_{DDQ} + 0.5 V	V
V_{IL}	DC LOW-level input voltage	All inputs	V_{SS} – 0.5 V	—	V_{REF} – 180 mV	V
I_{OH}	HIGH-level output current		—	—	–20	mA
I_{OL}	LOW-level output current		—	—	20	mA
T_{amb}	Operating free-air temperature range		0	—	70	°C

NOTE:
1. Unused control inputs must be held HIGH or LOW to prevent them from floating.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = 0 to +70 °C			
				MIN	TYP[2]	MAX	
V_{IK}	I/O supply voltage	V_{CC} = 2.3 V; I_I = –18 mA		—	—	–1.2	V
V_{OH}	HIGH level output voltage	V_{CC} = 2.3 V to 2.7 V; I_{OH} = –100 µA		V_{CC} – 0.2	—	—	V
		V_{CC} = 2.3 V; I_{OH} = –16 mA		1.95	—	—	
V_{OL}	LOW level output voltage	V_{CC} = 2.3 V to 2.7 V; I_{OL} = 100 µA		—	—	0.2	V
		V_{CC} = 2.3 V; I_{OL} = 16 mA		—	—	0.35	
V_{CMR}	CLK, $\overline{CLK}$	Common mode range for reliable performance		0.97	—	1.53	V
V_{PP}	CLK, $\overline{CLK}$	Minimum peak-to-peak input to ensure logic state		360	—	—	mV
I_I	Data inputs, $\overline{RESET}$	V_{CC} = 2.7 V; V_I = 1.7 V or 0.8 V	V_{REF} = 1.15 V or 1.35 V	—	0.01	±5	µA
		V_{CC} = 2.7 V; V_I = 2.7 V or 0 V		—	0.01	±5	
	CLK, $\overline{CLK}$	V_{CC} = 2.7 V; V_I = 1.7 V or 0.8 V	V_{REF} = 1.15 V or 1.35 V	—	0.05	±5	µA
		V_{CC} = 2.7 V; V_I = 2.7 V or 0 V		—	0.05	±5	
	V_{REF}	V_{CC} = 2.7 V	V_{REF} = 1.15 V or 1.35 V	—	0.05	±5	µA
I_{CC}	Quiescent supply current CLK and $\overline{CLK}$ in opposite state[1]	V_{CC} = 2.7 V; V_I = 1.7 V or 0.8 V	$\overline{RESET}$ = GND	—	0.5	10	µA
		V_{CC} = 2.7 V; V_I = 2.7 V or 0 V	$\overline{RESET}$ = V_{CC}	—	10	25	mA

NOTES:
1. When CLK and $\overline{CLK}$ are HIGH, typical I_{CC} = 25 mA.
2. All typical values are at V_{CC} = 2.5 V and T_{amb} = 25 °C (unless otherwise specified).

TIMING REQUIREMENTS

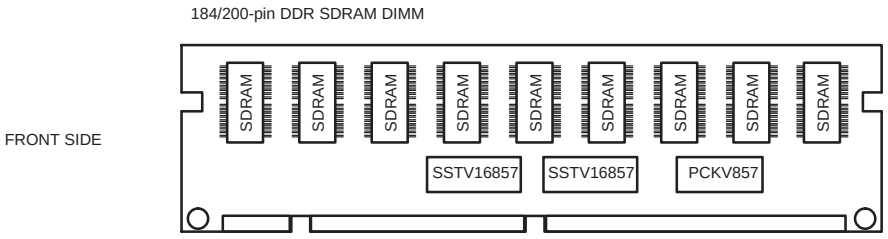
Over recommended operating conditions; T_{amb} = 0 to +70 °C (unless otherwise noted) (see Figure 1)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			V_{CC} = 2.5 V ±0.2 V		
			MIN	MAX	
f_{clock}	Clock frequency		—	200	MHz
t_w	Pulse duration, CLK, $\overline{CLK}$ HIGH or LOW		1.0	—	ns
t_{su}	Setup time	Data before CLK↑, $\overline{CLK}$↓	0.2	—	ns
		$\overline{RESET}$ HIGH before CLK↑, $\overline{CLK}$↓	0.8	—	
t_h	Hold time		0.75	—	ns

SWITCHING CHARACTERISTICS

Over recommended operating conditions; T_{amb} = 0 to +70 °C; V_{DDQ} = 2.3 – 2.7 V and V_{DDQ} does not exceed V_{CC}.
Class I, $V_{REF} = V_{TT} = V_{DDQ} \times 0.5$ and C_L = 10 pF (unless otherwise noted) (see Figure 1)

SYMBOL	FROM (INPUT)	TO (OUTPUT)	LIMITS		UNIT
			V_{CC} = 2.5 V ±0.2 V		
			MIN	MAX	
f_{max}	Maximum clock frequency		200	—	MHz
t_{PLH}/t_{PHL}	CLK and $\overline{CLK}$	Q	1.0	2.8	ns
t_{PHL}	$\overline{RESET}$	Q	2.0	4.0	ns



The PLL clock distribution device and SSTV registered drivers reduce signal loads on the memory controller and prevent timing delays and waveform distortions that would cause unreliable operation

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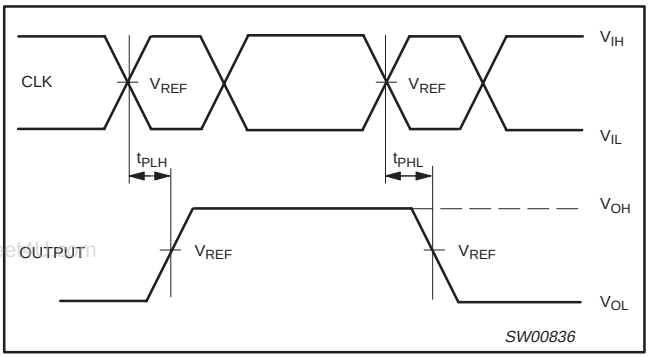
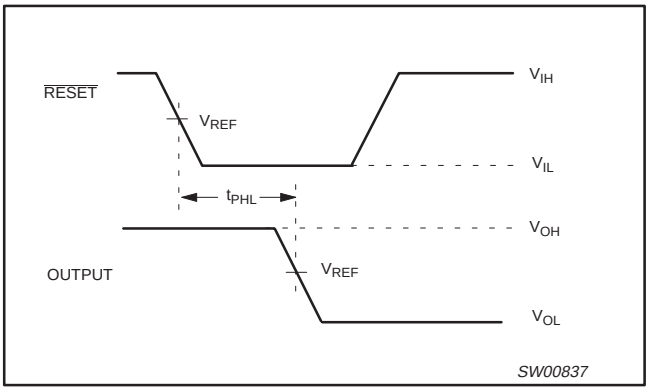
PARAMETER MEASUREMENT INFORMATION

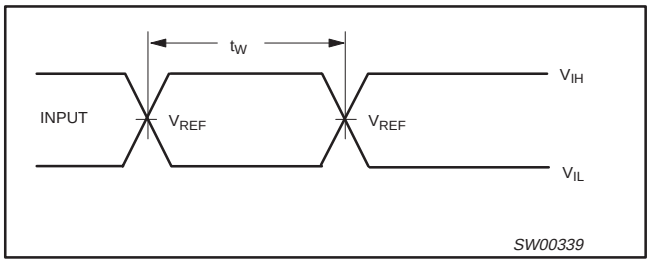
AC WAVEFORMS



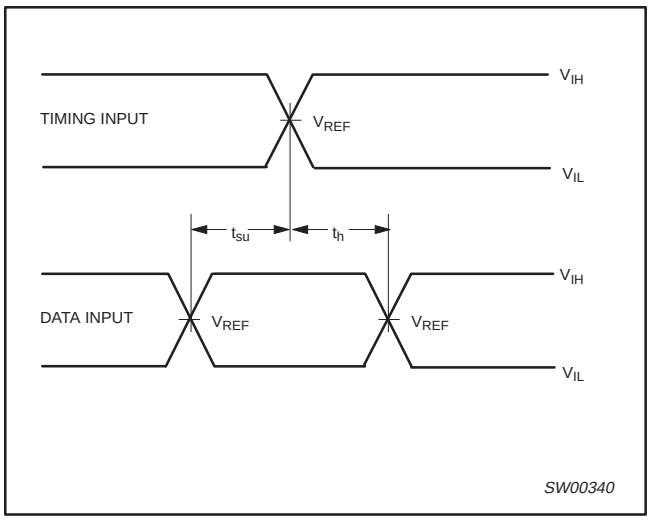
Waveform 1. Propagation delay times



Waveform 2. Propagation delay $\overline{RESET}$ to output.



Waveform 3. Pulse duration



Waveform 4. Setup and hold times

TEST CIRCUIT

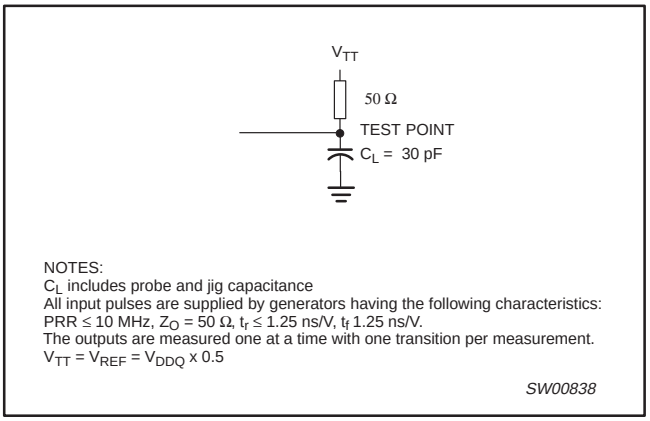
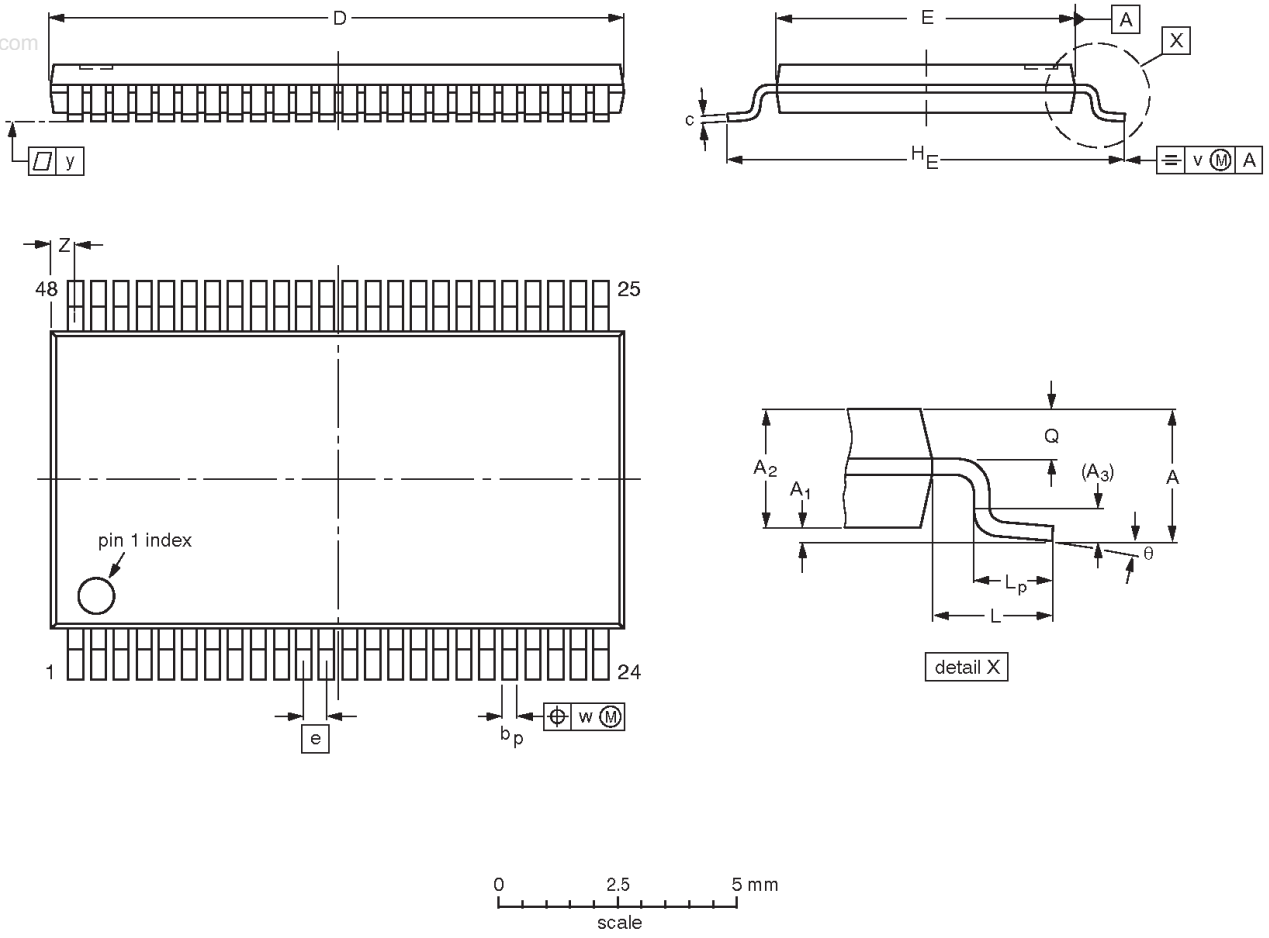


Figure 1. Load circuitry

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm SOT362-1



DIMENSIONS (mm are the original dimensions).

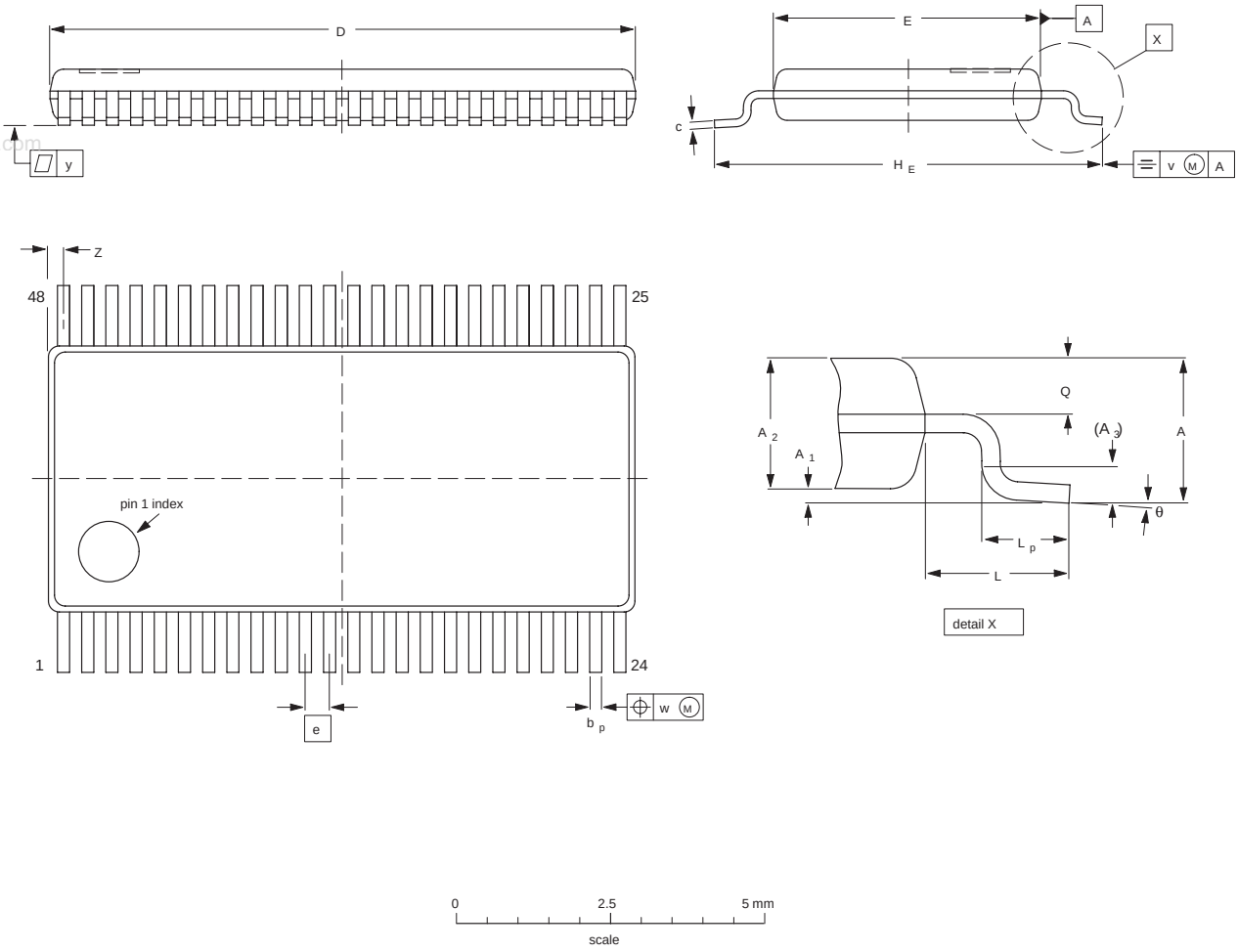
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT362-1		MO-153					~~95-02-10~~ 99-12-27

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 4.4 mm; lead pitch 0.4 mm **SOT480-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A 1	A 2	A 3	b p	c	D (1)	E (2)	e	H E	L	L p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.85	0.25	0.23 0.13	0.20 0.09	9.80 9.60	4.50 4.30	0.40	6.60 6.20	1.00	0.70 0.50	0.40 0.30	0.20	0.07	0.08	0.40 0.10	8° 0°

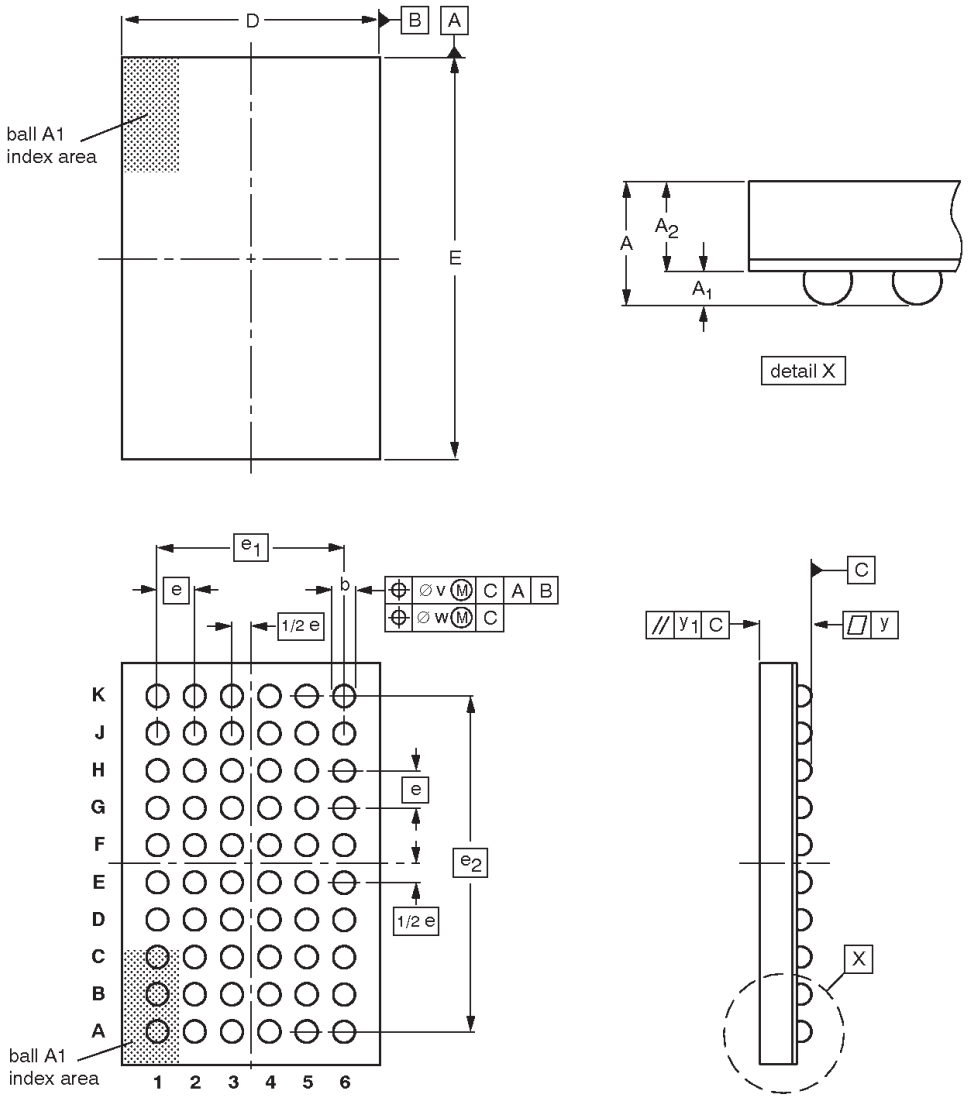
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

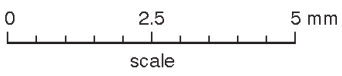
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT480–1		MO–153				~~97–03–20~~ 99–12–27

VFBGA56: plastic very thin fine-pitch ball grid array package; 56 balls; body 4.5 x 7 x 0.65 mm **SOT702-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1	0.3 0.2	0.7 0.6	0.45 0.35	4.6 4.4	7.1 6.9	0.65	3.25	5.85	0.15	0.08	0.08	0.1



OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT702-1		MO-225				~~01-06-25~~ 02-08-08

REVISION HISTORY

Rev	Date	Description
_6	2002 Sep 27	Product data (9397 750 10412); sixth version supersedes Product data fifth version, 2002 Jun 05. Engineering Change Notice: 853 2224 28989 (2002 Sep 26). Modifications: Package type changed from SSTV16857EC to SSTV16857EV.
_5	2002 Jun 05	Product data (9397 750 09942); fifth version.

Data sheet status

Data sheet status[1]	Product status[2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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