Description

The ST0524D25 is an uni-directional TVS diode array, utilizing leading monolithic silicon technology to provide fast response time and low ESD clamping voltage, making this device an ideal solution for protecting voltage sensitive high-speed data lines. The ST0524D25 has an ultra-low capacitance with a typical value at 0.3pF, and complies with the IEC 61000-4-2 (ESD) standard with ±15kV air and ±8kV contact discharge. It is assembled into an flow through lead-free DFN package. The small size, ultra-low capacitance and high ESD surge protection make ST0524D25 an ideal choice to protect cell phone, digital video interfaces and other high speed ports.

Mechanical Characteristics

- Package: DFN2510-10
- Lead Finish: NiPdAu
- Case Material: “Green” Molding Compound.
- UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 3 per J-STD-020
- Terminal Connections: See Diagram Below
- Marking Information: See Below

Features

- Low capacitance: 0.30pF typical（I/O to I/O)
- Ultra low leakage: nA level
- Low operating voltage: 5V
- Low clamping voltage
- 10-pin leadless package
- Complies with following standards:
  - IEC 61000-4-2 (ESD) immunity test
    - Air discharge: ±18kV
    - Contact discharge: ±10kV
  - IEC61000-4-4 (EFT) 40A (5/50ns)
  - IEC61000-4-5 (Lightning) 5A (8/20μs)
- RoHS Compliant

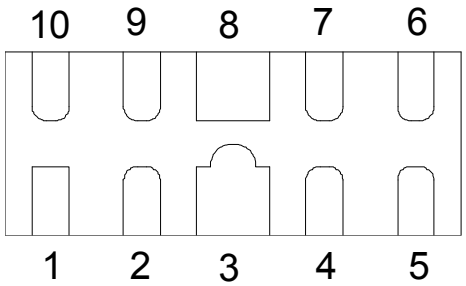
Applications

- Cellular Handsets and Accessories
- Display Ports
- MDDI Ports
- USB Ports
- Digital Video Interface (DVI)
- PCI Express and Serial SATA Ports

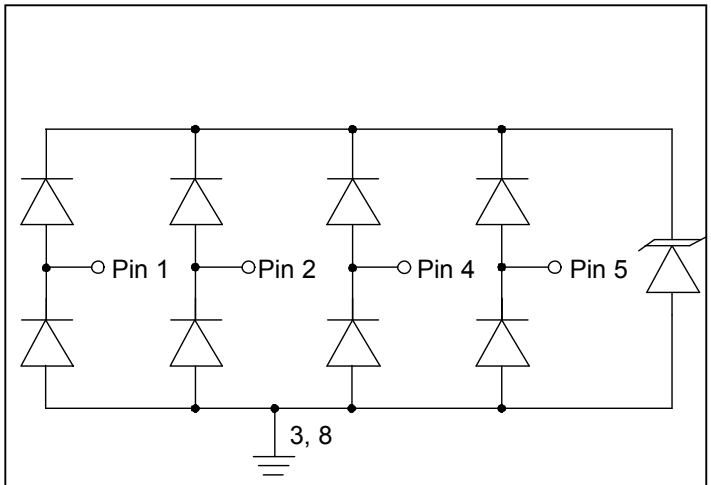
Ordering Information

Part Number	Packaging	Reel Size
ST0524D25	3000/Tape & Reel	7 inch

PIN Identification and Configuration



Circuit Diagram



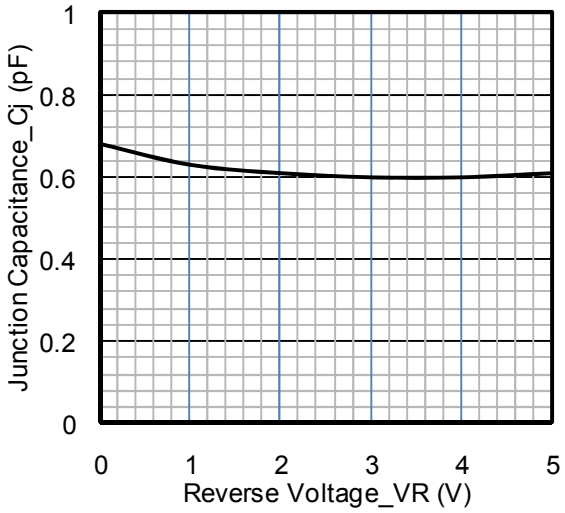
Absolute Maximum Ratings (TA=25˚C unless otherwise specified)

Parameter	Symbol	Value	Unit
Peak Pulse Power (8/20μs)	Ppk	150	W
Peak Pulse Current (8/20μs)	I_{PP}	5	A
ESD per IEC 61000−4−2 (Air) ESD per IEC 61000−4−2 (Contact)	V_{ESD}	±18 ±10	kV
Operating Temperature Range	T_J	−55 to +125	°C
Storage Temperature Range	Tstg	−55 to +150	°C

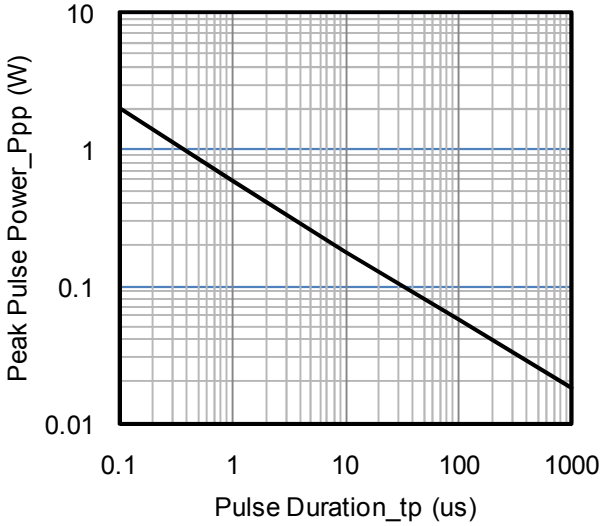
Electrical Characteristics (TA=25˚C unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse Working Voltage	V_{RWM}			5	V	
Breakdown Voltage	V_{BR}	6.4		9	V	I_T = 1mA
Reverse Leakage Current	I_R			0.5	uA	V_{RWM} = 5V
Clamping Voltage	V_C			15	V	I_{PP} = 1A (8 x 20μs pulse)
Junction Capacitance	C_J		0.3	0.4	pF	VR = 0V, f = 1MHz, beween I/O pins
Junction Capacitance	C_J			0.8	pF	VR = 0V, f = 1MHz, any I/O to ground

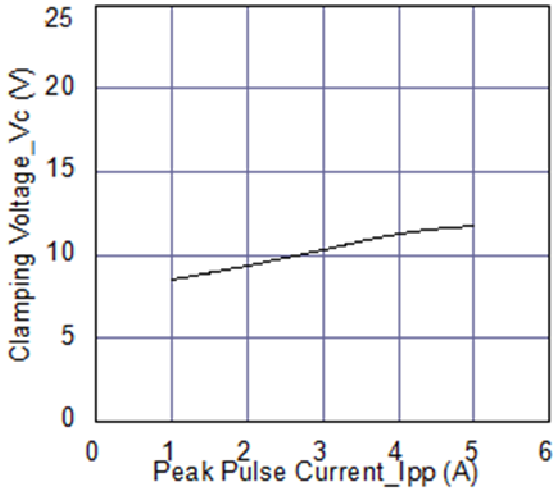
Typical Performance Characteristics (TA=25°C unless otherwise specified)



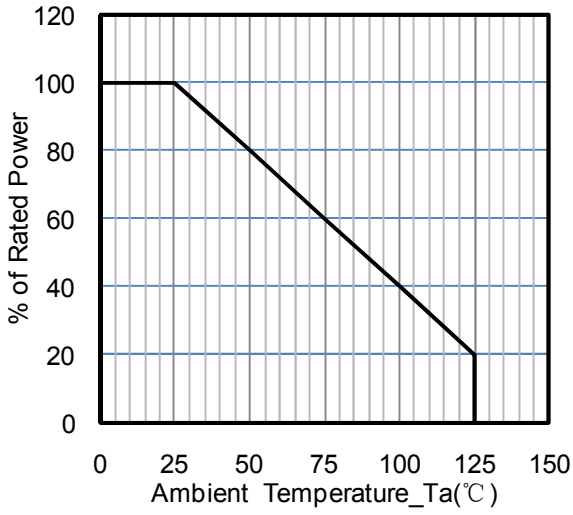
Junction Capacitance vs. Reverse Voltage



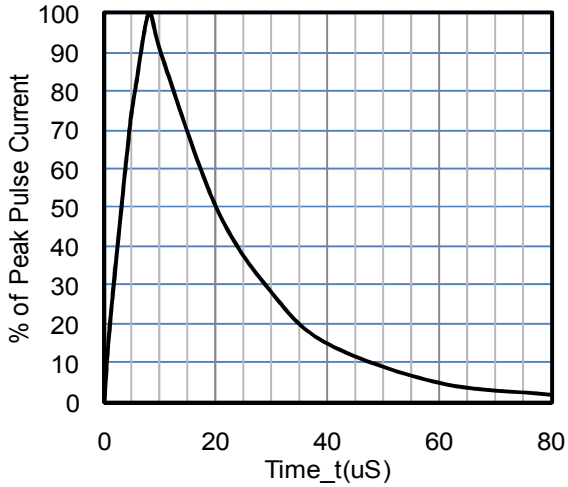
Peak Pulse Power vs. Pulse Time



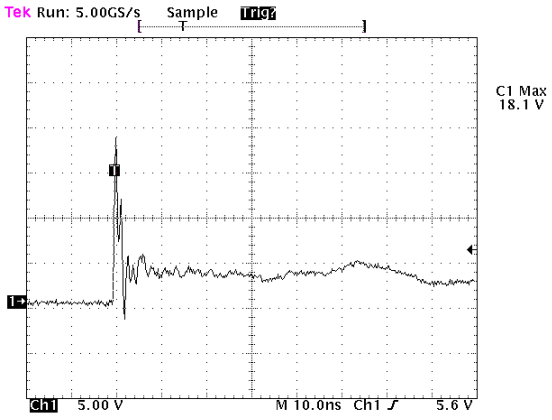
Clamping Voltage vs. Peak Pulse Current



Power Derating Curve



8 X 20uS Pulse Waveform



ESD Clamping Voltage

8 kV Contact per IEC61000−4−2

Applications Information

Design Recommendations for HDMI Protection

Adding external ESD protection to HDMI ports can be challenging. First, ESD protection devices have an inherent junction capaci tance. Furthermore, adding even a small amount of capacitance will cause the impedance of the differential pair to drop. Second, large packages and land pattern requirements cause discontinuities that adversely affect signal integrity. The ST0524D25 are specifi cally designed for protection of high-speed interfaces such as HDMI. They present <0.4pF capacitance between the pairs while being rated to handle >±8kV ESD contact discharges (>±15kV air discharge) as outlined in IEC 61000-4-2. Each device is in a leadless DFN package that is less than 1.1mm wide. They are designed such that the traces flow straight through the device. The narrow package and flow-through design reduces discontinuities and minimizes impact on signal integrity. This becomes even more critical as signal speeds increase.

Pin Configuration

Figure 1 is an example of how to route the high speed differential traces through the ST0524D25. The solid line represents the PCB trace. The PCB traces are used to connect the pin pairs for each line (pin 1 to pin 10, pin 2 to pin 9, pin 4 to pin 7, pin 5 to pin 6). For example, line 1 enters at pin 1 and exits at Pin 10 and the PCB trace connects pin 1 and 10 together. This is true for lines connected at pins 2, 4, and 5 also. Ground is connected at pins 3 and 8. One large ground pad should be used in lieu of two separate pads.

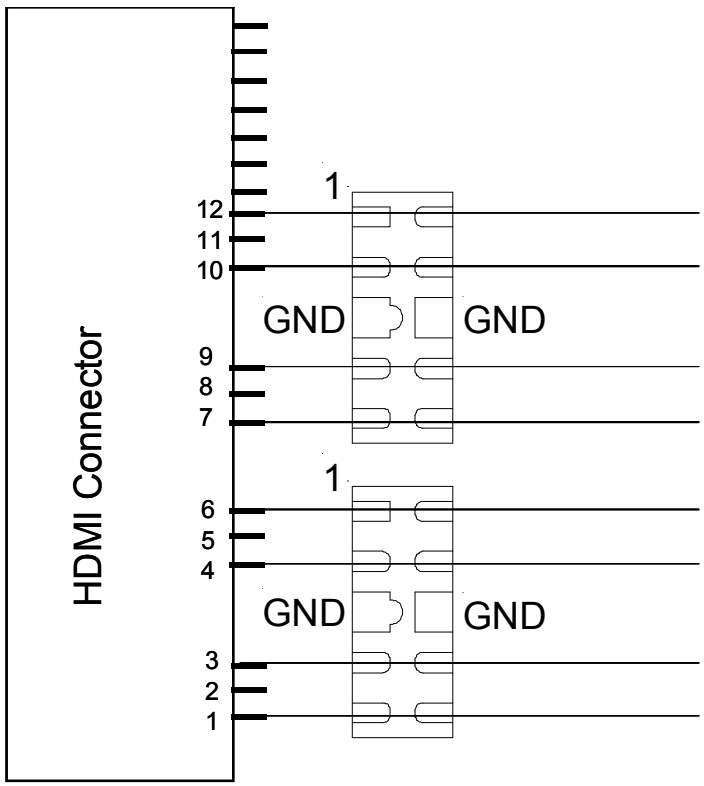
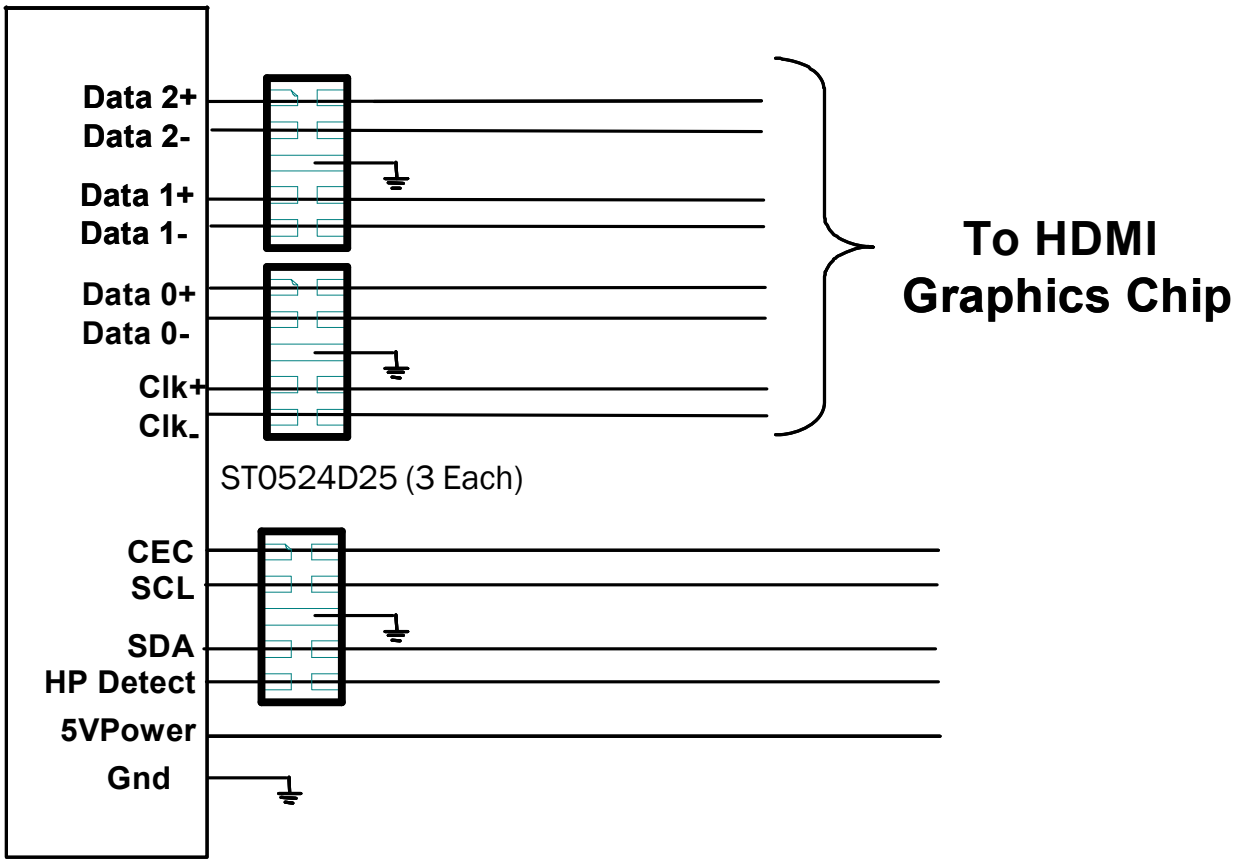
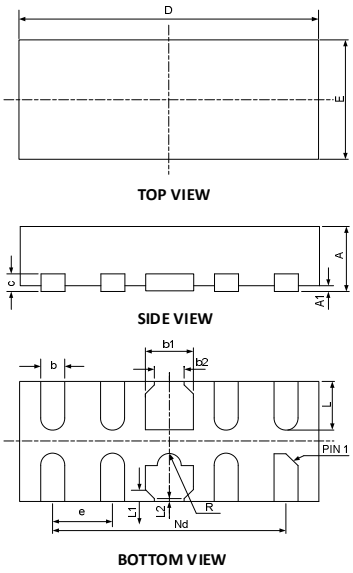


Figure 1. Flow Through Layout Using ST0524D25

HDMI Protection

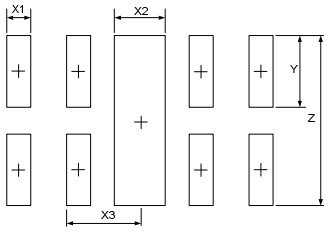


DFN2510-10 Package Outline Drawing



SYM	DIMENSIONS					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.45	0.50	0.55	0.018	0.020	0.022
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
b1	0.35	0.40	0.45	0.014	0.016	0.018
b2	0.20	0.25	0.30	0.008	0.010	0.012
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.45	2.50	2.55	0.098	0.100	0.102
e	0.50BSC			0.020BSC		
Nd	2.00BSC			0.080BSC		
E	0.95	1.00	1.05	0.038	0.040	0.042
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.075REF			0.003REF		
L2	0.050REF			0.002REF		
h	0.08	0.12	0.15	0.003	0.005	0.006
R	0.05	0.10	0.15	0.002	0.004	0.006

Suggested Land Pattern



SYM	DIMENSIONS	
	MILLIMETERS	INCHES
X1	0.200	0.008
X2	0.400	0.016
X3	0.500	0.020
Y	0.600	0.024
Z	1.400	0.056

Contact Information

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