STANSON

ST1004SRG

N Channel Enhancement Mode MOSFET

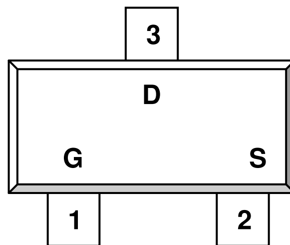
2.0A

DESCRIPTION

ST1004SRG is the N-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. The process is especially to improve the overall efficiency of DC/DC conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(on)}$ and fast switching speed.

PIN CONFIGURATION

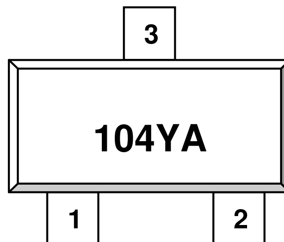
SOT-23



1.Gate 2.Source 3.Drain

PART MARKING

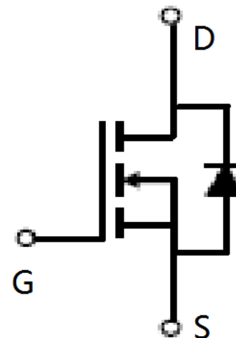
SOT-23



Y: Year Code A: Process Code

FEATURE

- 100V/1.0A, $R_{DS(ON)}$ = 310mΩ @VGS = 10V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23 package design



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ABSOULTE MAXIMUM RATINGS (Ta = 25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	100	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current=150℃)	T_A=25℃ T_A=70℃	I_D	3.0 2.0	A
Pulsed Drain Current		I_{DM}	10	A
Power Dissipation	T_A=25℃ T_A=70℃	P_D	1.25 0.8	W
Operation Junction Temperature		T_J	150	℃
Storgae Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	100	℃/W

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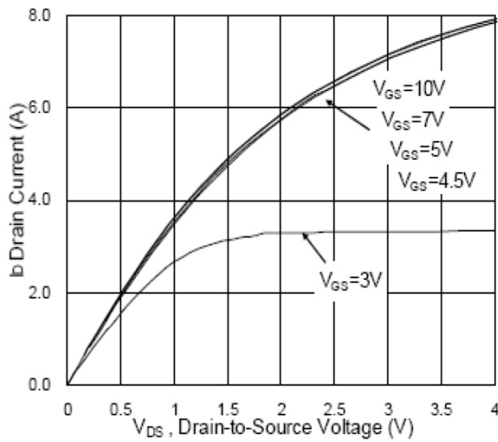
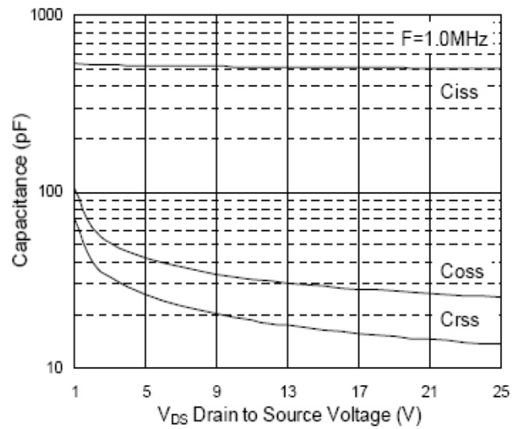
ELECTRICAL CHARACTERISTICS (Ta = 25℃ Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250uA	100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=VGS, I_D=250uA	1.0		2.5	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V, V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=80V, V_{GS}=0V			1	uA
		V_{DS}=80V, V_{GS}=0V T_J=125℃			5	
On-State Drain Current	$I_{D(on)}$	V_{DS}≧5V,V_{GS}=10V	3.0			A
Drain-source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=2.0A V_{GS}=4.5V,I_D=1.0A		0.26 0.29	0.31 0.32	Ω
Forward Transconductance	g_{fs}	V_{DS}=5V,I_D=3.6V		2.4		S
Diode Forward Voltage	V_{SD}	I_S=1.0A,V_{GS}=0V			1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=80V V_{GS}=10V I_D≡5.0A		9	13	nC
Gate-Source Charge	Q_{gs}			2		
Gate-Drain Charge	Q_{gd}			1.4		
Input Capacitance	C_{iss}	V_{DS}=25V V_{GS}=0V F=1MHz		508		pF
Output Capacitance	C_{oss}			29		
Reverse Transfer Capacitance	C_{rss}			16.5		
Turn-On Time	$t_{d(on)}$	V_{DD}=50V R_L=10Ω I_D=3.0A V_{GEN}=10V R_G=3.3Ω		12		nS
	t_r			21.5		
Turn-Off Time	$t_{d(off)}$			11.2		
	t_f			18.8		

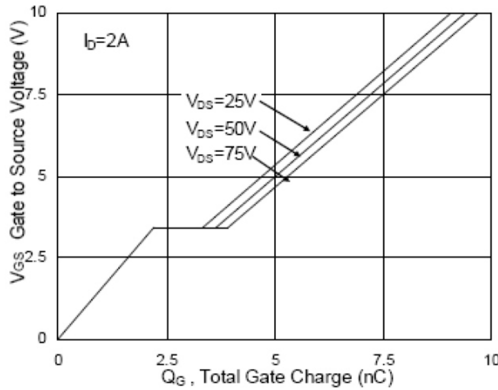
TYPICAL CHARACTERICTICS (25℃ Unless noted)



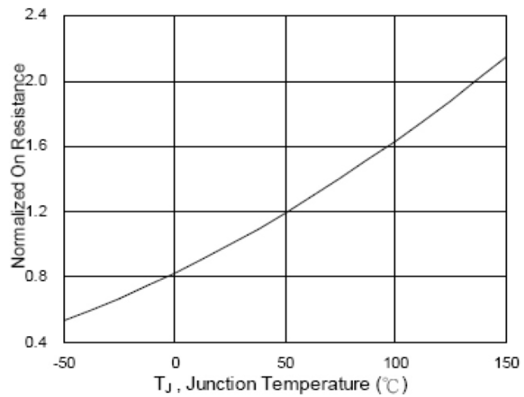
Output Characteristics



Capacitance



Gate Charge



On-Resistance vs. Junction Temperature

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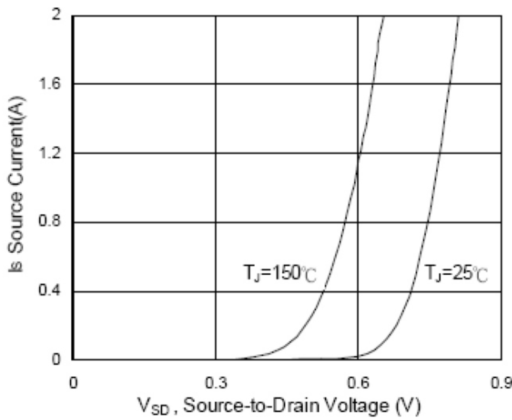
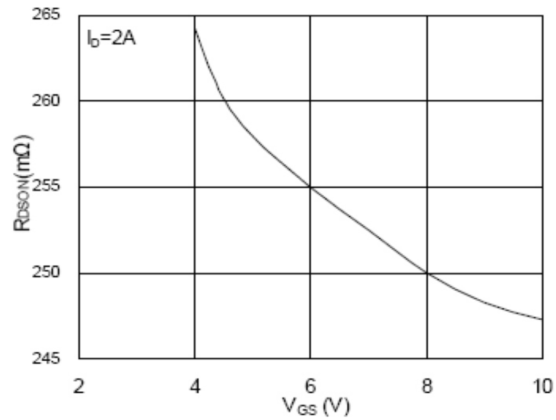
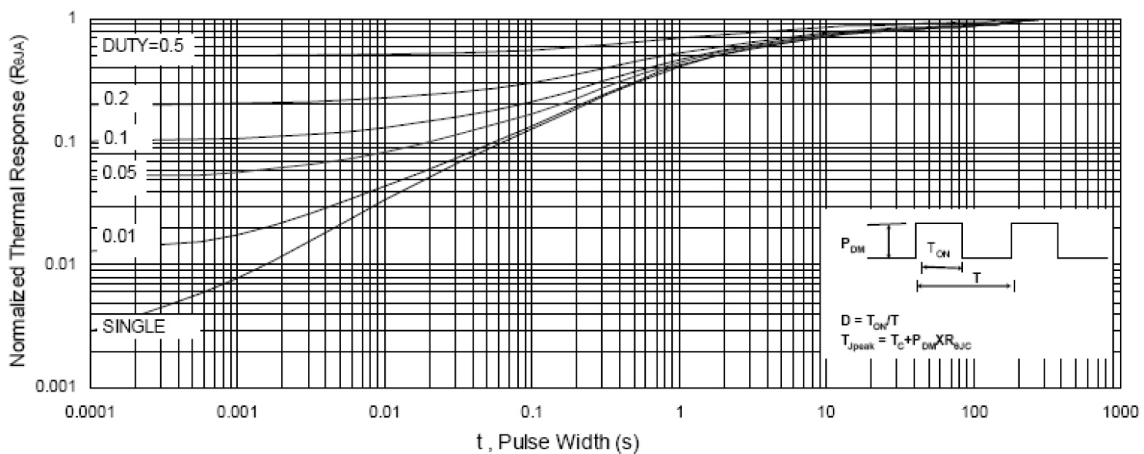
TYPICAL CHARACTERICTICS (25℃ Unless noted)



Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-Source Voltage



Normalized Thermal Transient Impedance, Junction to Foot

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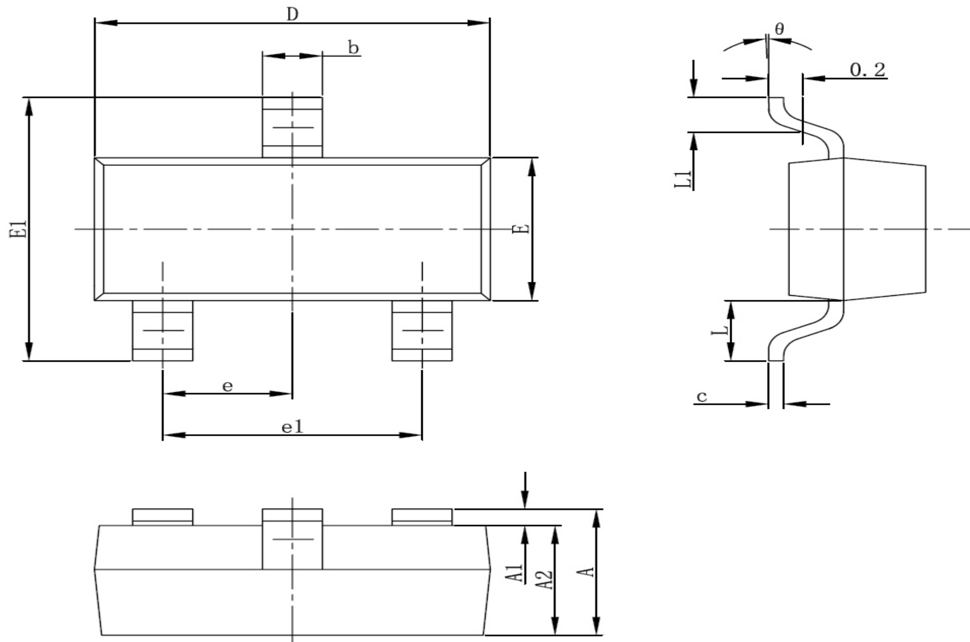
SOT-23 PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.550REF		0.022REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

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