ST1536/1530

Touch Screen Controller

Datasheet

Version 1.1

2012/02/02

Note: Sitronix Technology Corp. reserves the right to change the contents in this document without prior notice. This is not a final specification. Some parameters are subject to change.

1 INTRODUCTION

The ST1536/1530 is a mutual capacitive sensing controller for small size projected capacitive touch screen. It is a RISC microcontroller with capacitor charge, capacitor sensing, slave I2C interface, general purpose I/O and embedded non-volatile memory.

Internal program and cooperating digital circuit covert finger / capacitor stylus data into button pressing or multiple coordination information for application. The maximum fingers identification ability is up to five.

The ST1536/1530 uses low profile QFN package and support ITO electrode on glass or film substrate. Hence, slim and small touch panel module is realizable.

And more, the ability of reducing electromagnetic interference of ST1536/1530 makes it suitable for modern touch screen application which contain a vivid and high density display, like smart phone, portable navigation device and touch-enabled media player, etc..

FEATURES

- **MCU based mutual sensing touch controller**
- **Operation voltage**
  – VDD = 2.4V ~ 3.6V
  – IOVDD = 1.8V ~ 3.3V
- **Temperature: -40℃ ~ 85℃**
- **Interface**
  – I2C (slave)
- **Sensor input: 32 + 4**
  – Maximum 32 channels for touch matrix sensing
  – Maximum 4 channels for touch key sensing
  – All configurable
- **Single finger handwriting**
- **five fingers detection**
- **Capacitive Sensor**
  – Mutual-capacitance sensing
  – Max. loading: 30 kOhm/60pF
  – Report Rate : 100Hz
  – Hardware noise reduction
  – Waterproof circuit
- **Power Consumption**
  – Normal mode:13mA (Sensor dependent)
  – Idle mode: 5mA (@20Hz)
  – Power down: 5uA
- **Package**
  – I2C interface

IC	ST1536	ST1530
Package	QFN 6x6	QFN 5x5
Sensor	32+4	30

APPLICATIONS

- **Cell phones**
- **PDAs**
- **Portable instruments**
- **Touch screen monitors**
- **Electrical papers**
- **Gaming machines**
- **Pointing devices**
- **PC peripherals**

2 PACKAGE INFORMATION

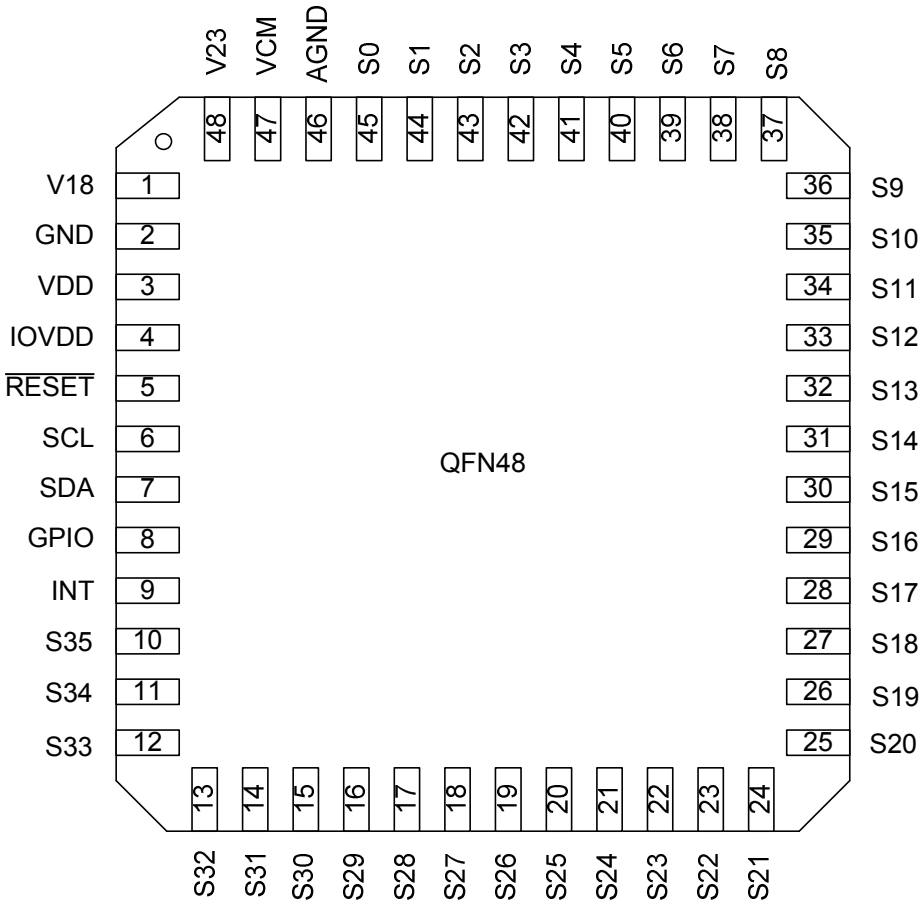


Figure 2-1 ST1536 Package Pin Configuration (QFN48)

Table 2-1 ST1536 Package Signal Descriptions (QFN48)

Pin #	Pin Name	Description
1	V18	Core power, connect to 4.7uF capacitor
2	GND	logic Ground
3	VDD	Power supply
4	IOVDD	I/O power supply
5	$\overline{\text{RESET}}$	System reset signal input, active low
6	SCL	I2C: serial clock
7	SDA	I2C: serial data
8	GPIO	General purpose input/output
9	INT	Report coordinate to host
45~10	S0~S35	Touch sensor input
46	AGND	Analog Ground
47	VCM	Common mode voltage, connect to 0.1uF
48	V23	Core power, connect to 4.7uF capacitor

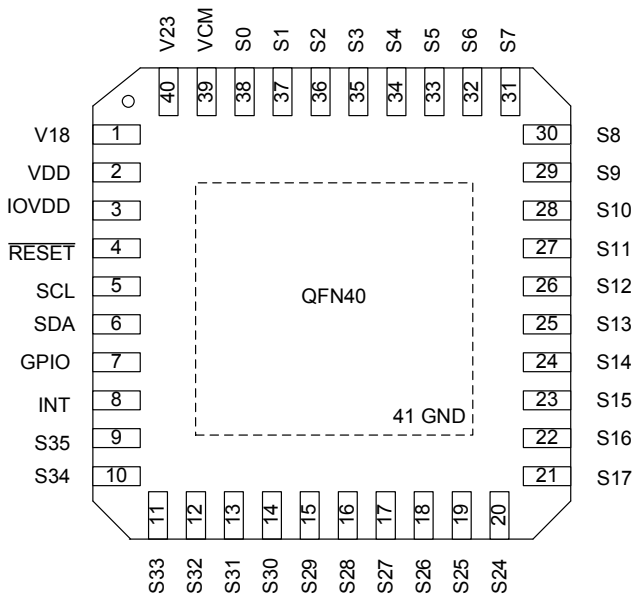


Figure 2-2 ST1530 Package Pin Configuration (QFN40)

Table 2-2 ST1530 Package Signal Descriptions (QFN40)

Pin #	Pin Name	Description
1	V18	Core power, connect to 4.7uF capacitor
2	VDD	Power supply
3	IOVDD	I/O Power supply
4	$\overline{\text{RESET}}$	System reset signal input, active low
5	SCL	I2C: serial clock
6	SDA	I2C: serial data
7	GPIO	General purpose input/output
8	INT	Report coordinate to host
38~9	S0~S35	Touch sensor input, except S18~S23
39	VCM	Common mode voltage, connect to 0.1uF
40	V23	Core power, connect to 4.7uF capacitor
41	GND	Ground, In the bottom of chip

3 SYSTEM MANAGEMENT

3.1 Power Down

In power down mode, all of the clocks of ST1536/1530 are stopped. The way to exit power down mode is by a hardware reset or I2C.

3.2 Reset

Master can reset ST1536/1530 through $\overline{\text{RESET}}$ pin. $\overline{\text{RESET}}$ pin is low active and needs hold low for 1us to take effect.

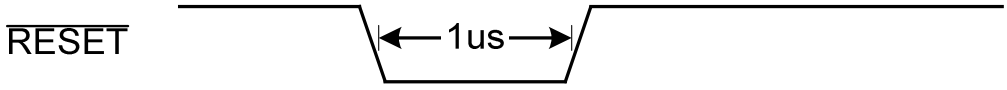


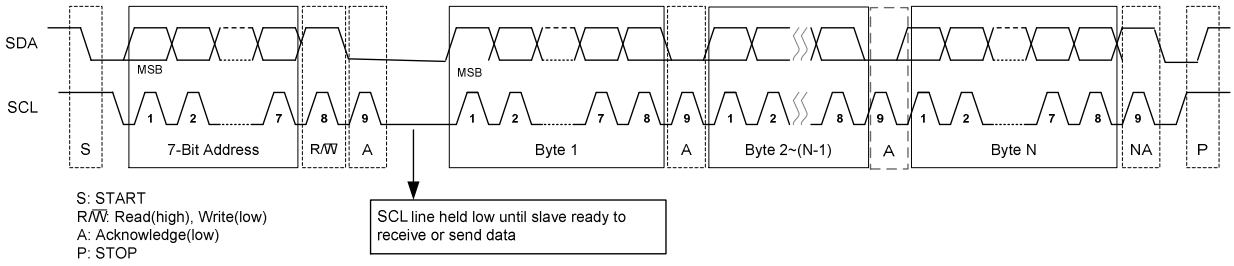
Figure 3-1 $\overline{\text{RESET}}$ Pin Low Pulse Width

4 DIGITAL INTERFACE

4.1 I2C Slave Interface

ST1536/1530 equipped with I2C provide two wires, serial data (SDA) and serial clock (SCL), to carry information transfers at up to 400 kbit/s(Fast mode). ST1536/1530 plays a slave role in I2C transfer. Both SDA and SCL are bidirectional lines, connected to IOVDD via pull-up resistors. All transactions begin with a START (S) and can be terminated by a STOP (P). 7-Bit address follows START to recognize device. Each bye is 8-bit length and followed by an acknowledge bit. A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.

Read



Write

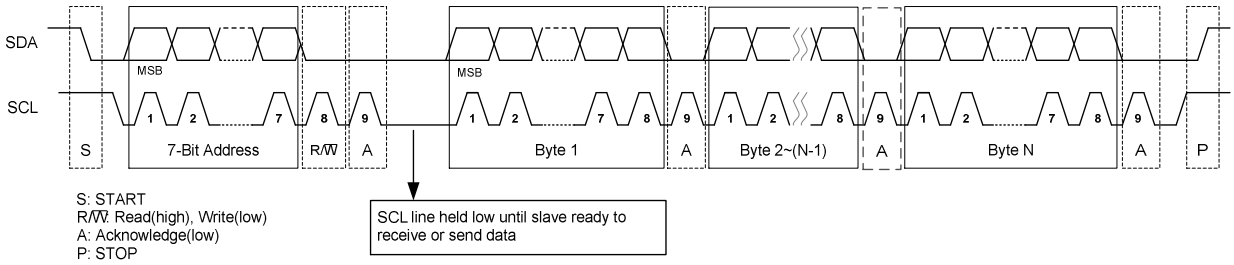


Figure 4-1 I2C Waveform

5 ELECTRICAL CHARACTERISTIC

5.1 DC Electrical Characteristics

Table 5-1 System DC Electrical Characteristics

Condition: VDD = IOVDD = 3.3V, T_A = 25°C, unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
VDD	V_{VDD}	2.4	3.3	3.6	V	
IOVDD	V_{IOVDD}	1.8	3	3.3	V	
Operating Current	I_{NML}	-	13	-	mA	
Power Down Current	I_{PD}	-	5	-	uA	
Input High Voltage	V_{IH}	1.2	-	2.0	V	IOVDD correlate
Input Low Voltage	V_{IL}	0.64	-	1.3	V	IOVDD correlate
Input Pull Up Resistor	R_{PU}	-	60	-	KOhm	
Output Driving Current	I_{DRV}	-	45	-	mA	V_{OH}=0.7xIOVDD
Output Sinking Current	I_{SINK}	-	75	-	mA	V_{OL}=0.3xIOVDD
Low Voltage Reset	V_{LVR}	-	1.6	-	V	

5.2 AC Electrical Characteristics

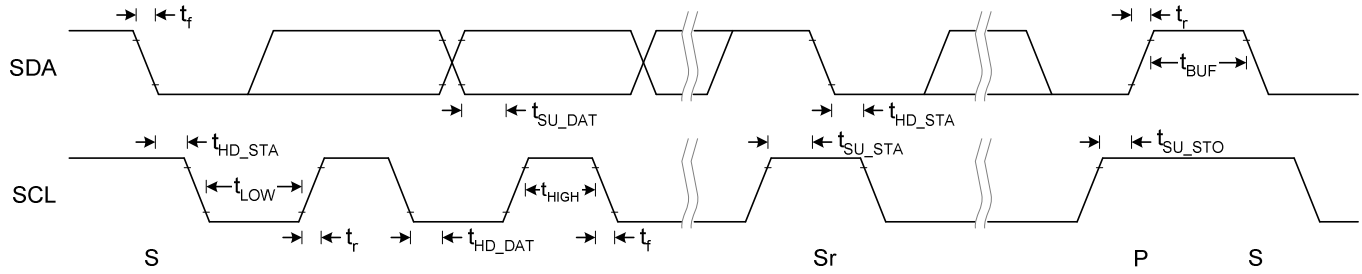


Figure 5-1 I2C Fast Mode Timing

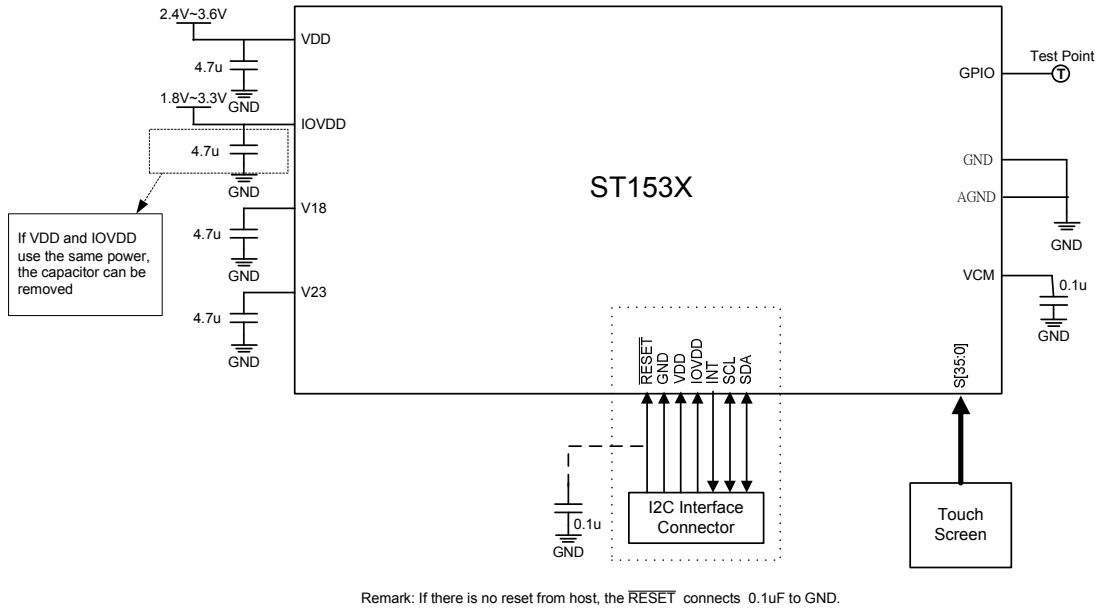
Table 5-2 I2C Fast Mode Timing Characteristic

Conditions: VDD = IOVDD = 3.3V, GND = 0V, T_A = 25°C

Symbol	Parameter	Rating			Unit
		Min.	Typ.	Max.	
f_{SCL}	SCL clock frequency	0	-	400	kHz
t_{LOW}	Low period of the SCL clock	1.3	-	-	us
t_{HIGH}	High period of the SCL clock	0.6	-	-	us
t_f	Signal falling time	-	-	300	ns
t_r	Signal rising time	-	-	300	ns
t_{SU_STA}	Set up time for a repeated START condition	0.6	-	-	us
t_{HD_STA}	Hold time (repeated) START condition. After this period, the first clock pulse is generated	0.6	-	-	us
t_{SU_DAT}	Data set up time	100	-	-	ns

t_{HD_DAT}	Data hold time	0	-	0.9	us
t_{SU_STO}	Set up time for STOP condition	0.6	-	-	us
t_{BUF}	Bus free time between a STOP and START condition	1.3	-	-	us
C_b	Capacitive load for each bus line	-	-	400	pF

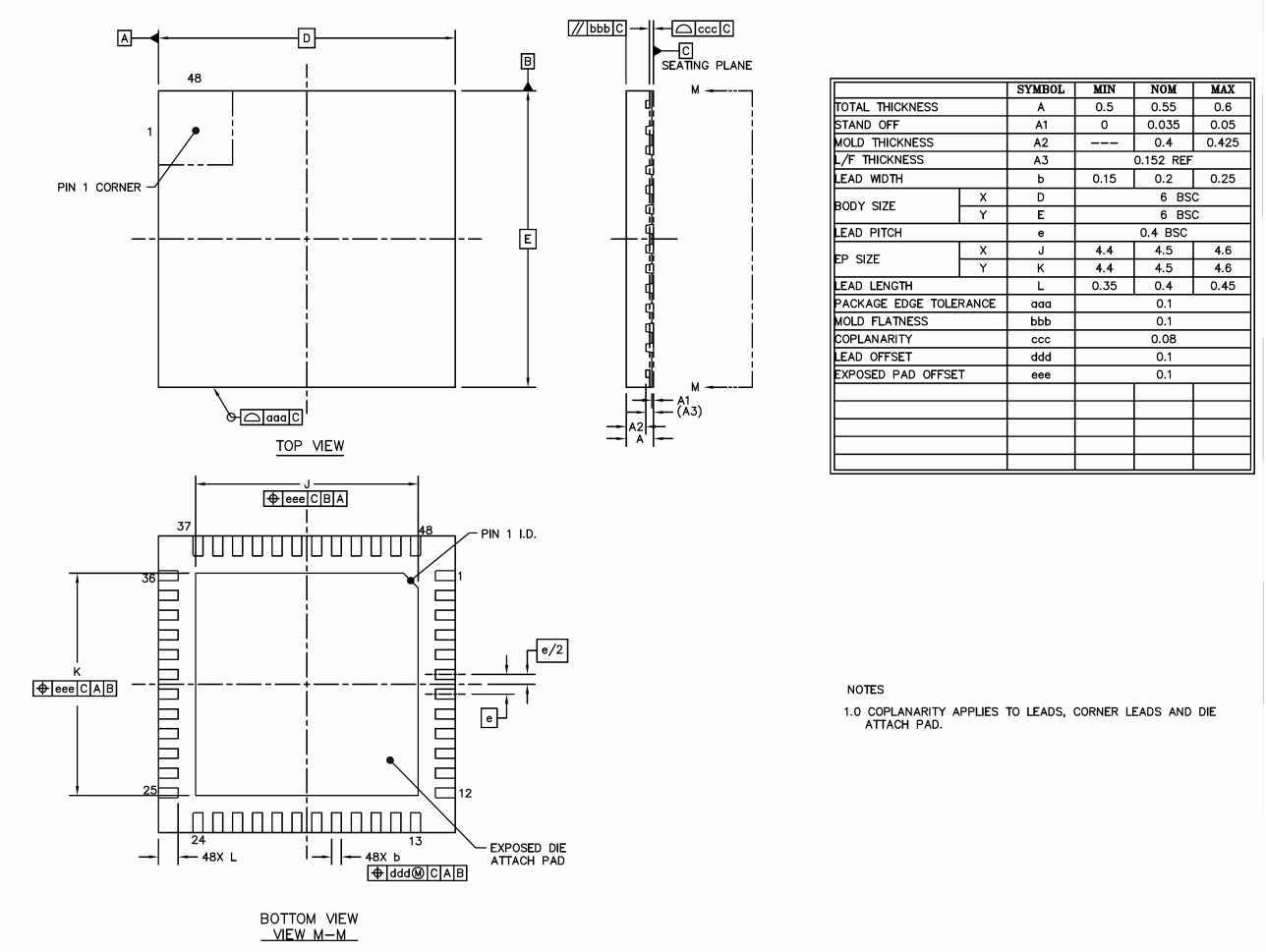
6 APPLICATION CIRCUITS



Remark: If there is no reset from host, the $\overline{\text{RESET}}$ connects 0.1uF to GND.

Figure 6-1 Application Circuit

7 PACKAGE DIMENSION

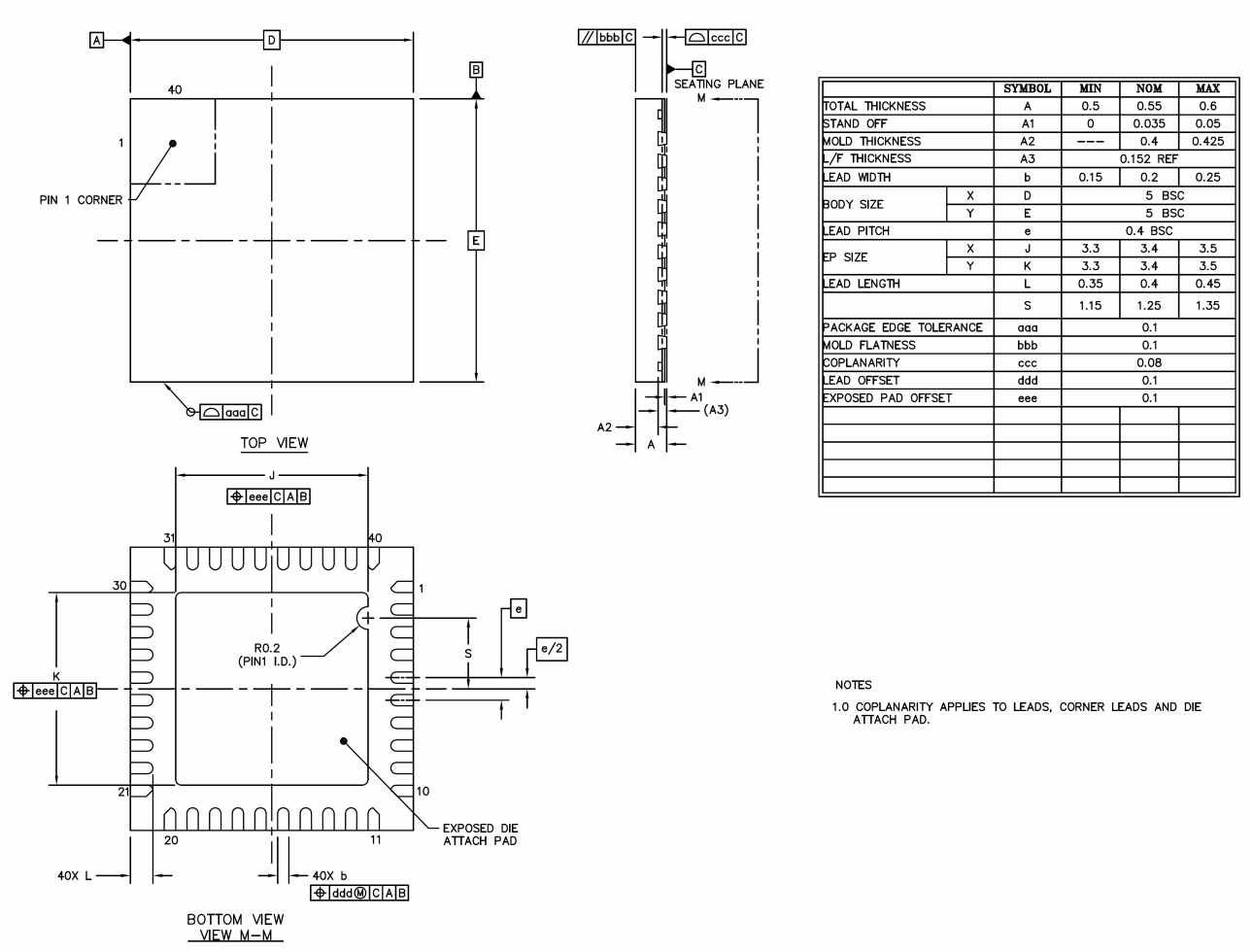


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.5	0.55	0.6
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.4	0.425
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		6 BSC	
	Y	E		6 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	J	4.4	4.5	4.6
	Y	K	4.4	4.5	4.6
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

Figure 7-1 ST1536 Package Dimension (QFN48)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.5	0.55	0.6
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.4	0.425
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	J	3.3	3.4	3.5
	Y	K	3.3	3.4	3.5
LEAD LENGTH		L	0.35	0.4	0.45
		S	1.15	1.25	1.35
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

Figure 7-2 ST1530 Package Dimension (QFN40)

8 REVISION

REVISION	DESCRIPTION	PAGE	DATE
0.1	■ First release		2011/10/14
0.2	■ modify features ■ modify Reset description ■ Add DC Electrical Characteristics Value ■ Modify application circuit	3 6 8 10	2011/12/16
1.0	■ Remove “Preliminary”		2011/12/21
1.1	■ modify features ■ modify DC Electrical Characteristics Value ■ Modify application circuit	3 8 10	2012/02/02