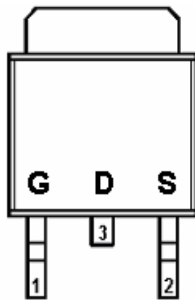


DESCRIPTION

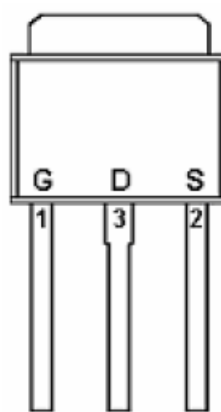
ST16N10 is the N-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. The ST16N10 has been designed specially to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

PIN CONFIGURATION (D-PAK)

TO-252



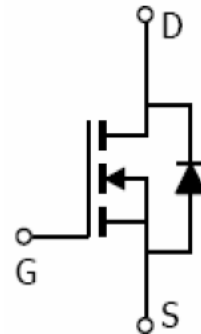
TO-251



FEATURE

- 100V/ 10A, $R_{DS(ON)} = 140m\Omega$ @ $V_{GS} = 10V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- TO-252, TO-251 package design

PART MARKING



Y: Year Code A: Process Code

**ST16N10**

N Channel Enhancement Mode MOSFET

16.0A

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	VDSS	100	V
Gate-Source Voltage	VGSS	±20	V
Continuous Drain Current (TJ=150°C)	ID	16.0	A
		12.0	
TA=25°C TA=100°C			
Pulsed Drain Current	IDM	60	A
Continuous Source Current (Diode Conduction)	IS	16	A
Power Dissipation	PD	79	W
TA=25°C			
Operation Junction Temperature	TJ	150	°C
Storage Temperature Range	TSTG	-55/150	°C
Thermal Resistance-Junction to Ambient	RθJA	110	°C/W


ST16N10


N Channel Enhancement Mode MOSFET

16.0A

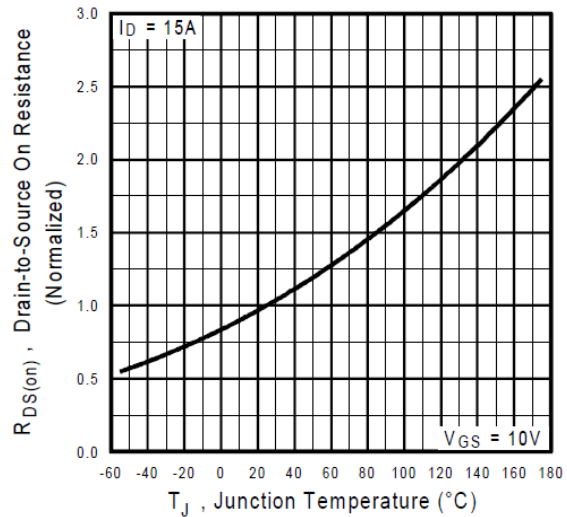
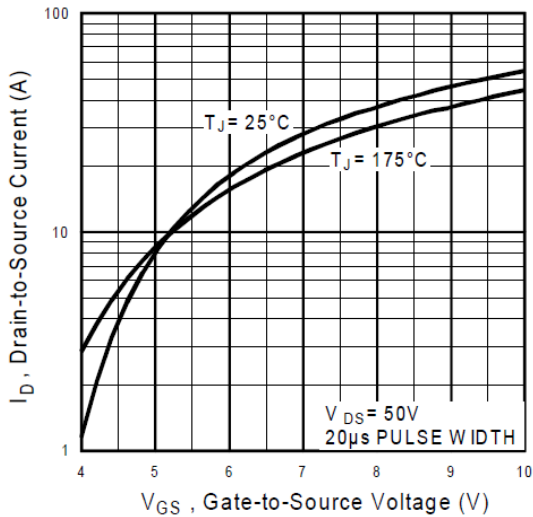
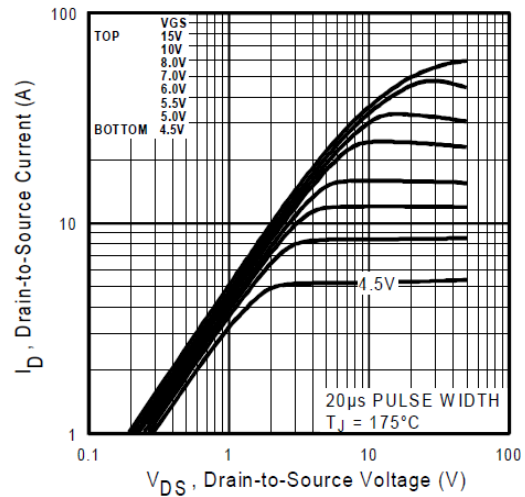
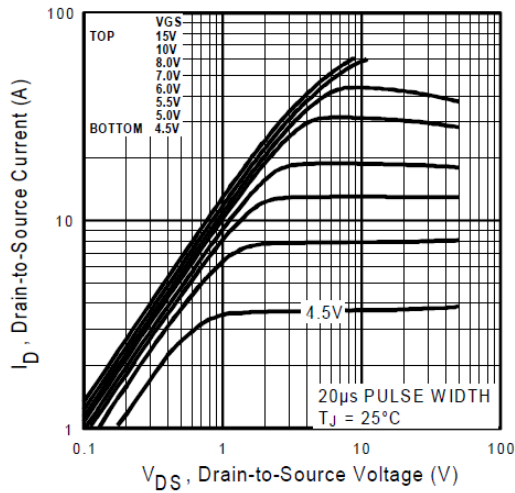
ELECTRICAL CHARACTERISTICS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0		4.0	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V$			25	uA
		$V_{DS}=80V, V_{GS}=0V$ $T_J=150^{\circ}C$			250	
On-State Drain Current	$I_{D(on)}$	$V_{DS}\geq 5V, V_{GS}=10V$	60			A
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=16A$			140	mΩ
Forward Transconductance	gfs	$V_{DS}=50V, I_D=9.0A$	6.4			S
Diode Forward Voltage	V_{SD}	$I_S=9.0A, V_{GS}=0V$			1.3	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=80V, V_{GS}=10V$ $I_D=9.0A$			44	nC
Gate-Source Charge	Q_{gs}				6.2	
Gate-Drain Charge	Q_{gd}				21	
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V$ $F=1MHz$		640		pF
Output Capacitance	C_{oss}			160		
Reverse TransferCapacitance	C_{rss}			88		
Turn-On Time	$t_{d(on)}$ t_r	$V_{DD}=50V, R_D=5.5\Omega$ $I_D=9.0A, V_{GEN}=10V$ $R_G=12\Omega$		6.4		nS
Turn-Off Time	$t_{d(off)}$ t_f			27		
				37		
				25		

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TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

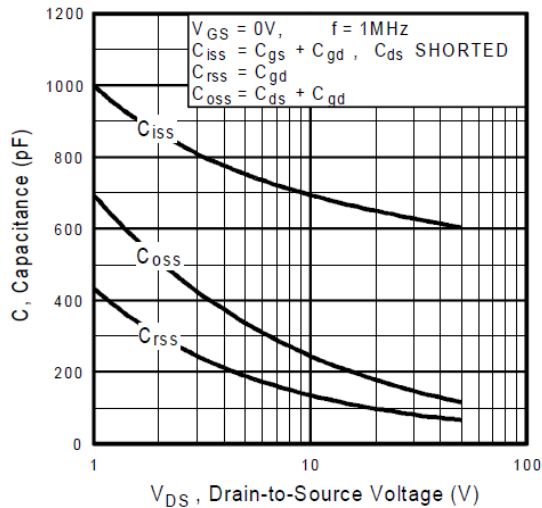


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

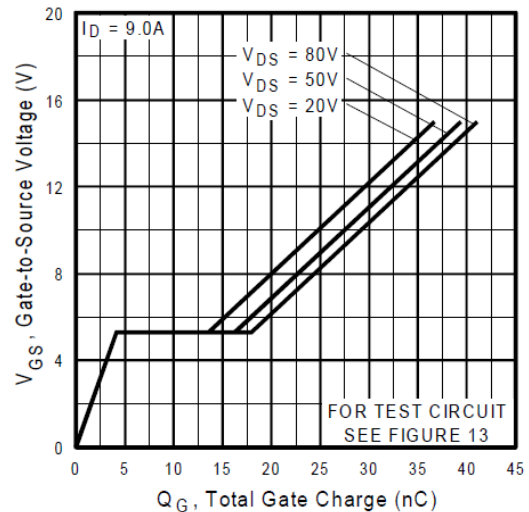


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

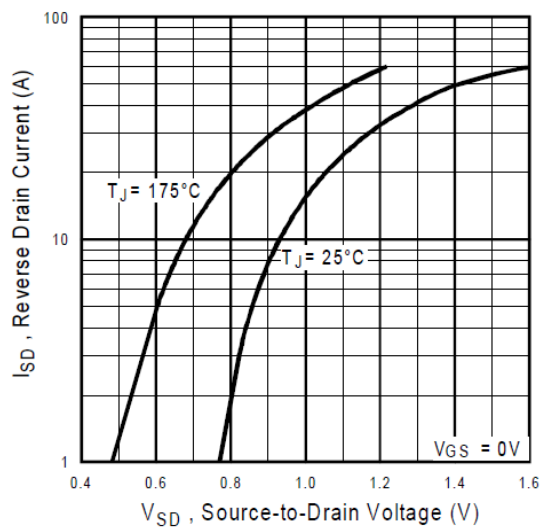


Fig 7. Typical Source-Drain Diode Forward Voltage

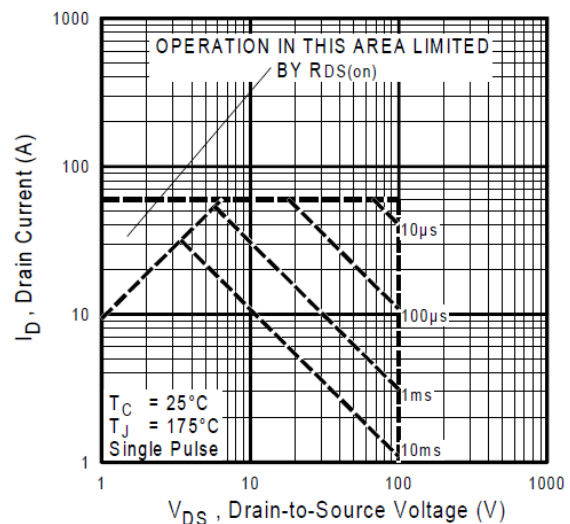


Fig 8. Maximum Safe Operating Area

TYPICAL CHARACTERISTICS

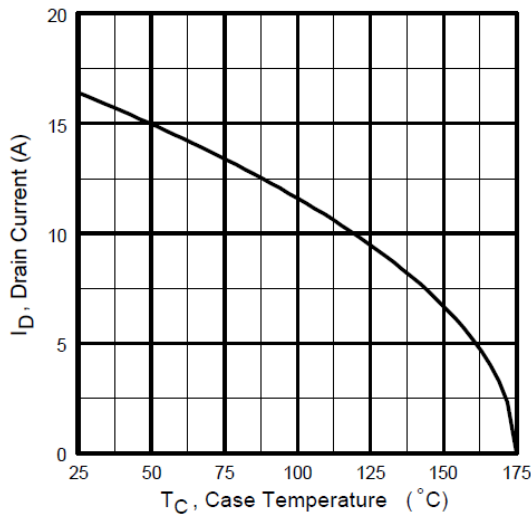


Fig 9. Maximum Drain Current Vs. Case Temperature

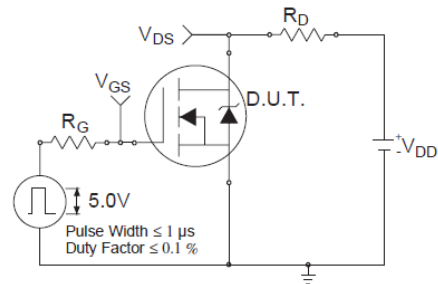


Fig 10a. Switching Time Test Circuit

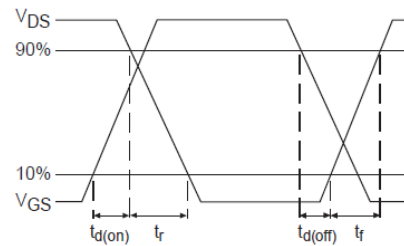


Fig 10b. Switching Time Waveforms

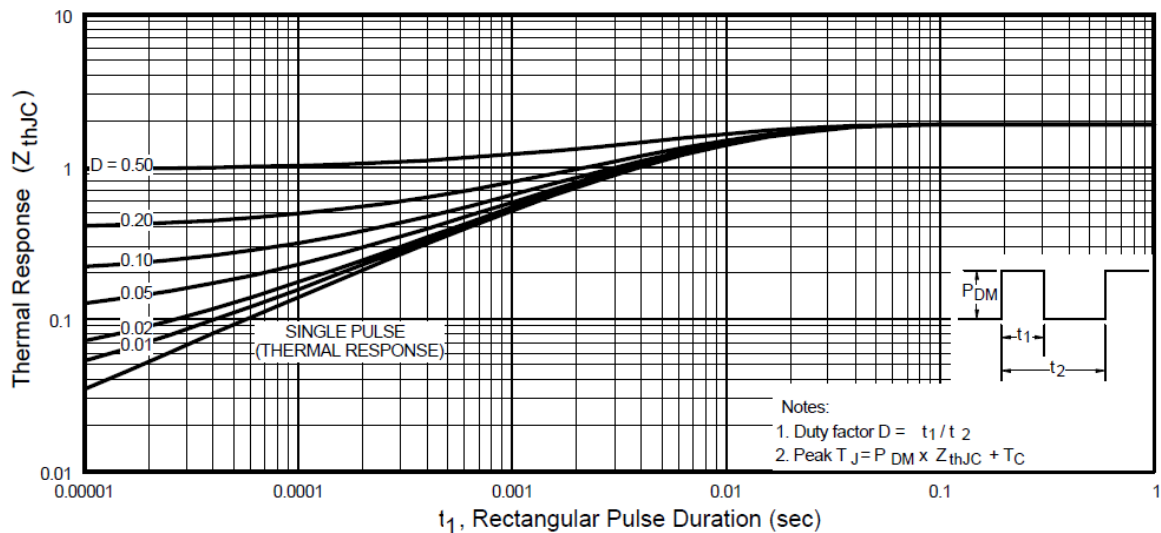
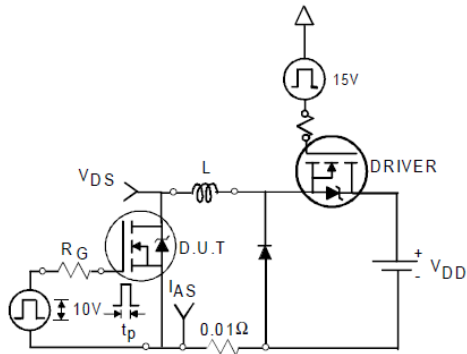
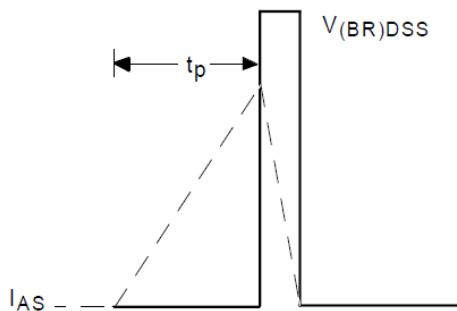
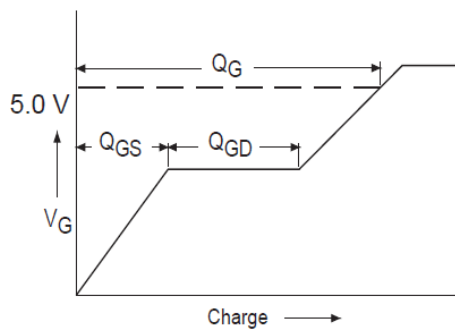
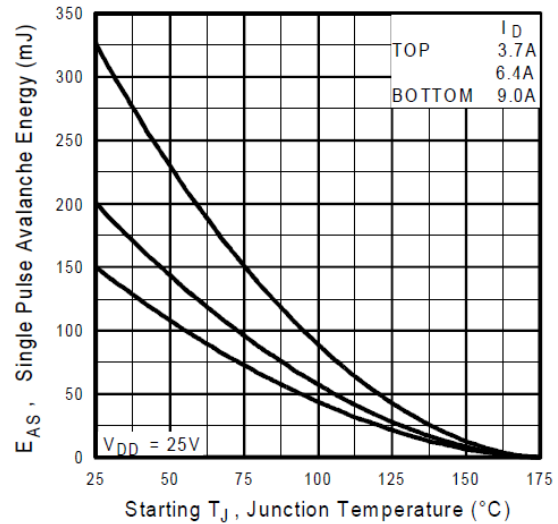
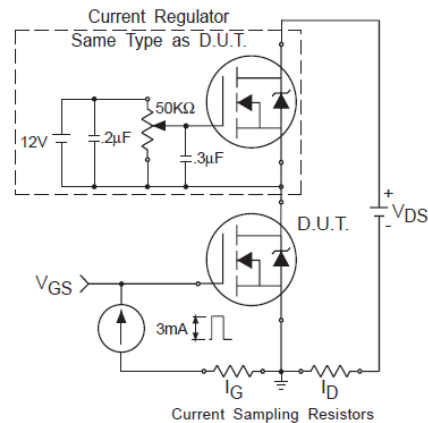


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case


Fig 12a. Unclamped Inductive Test Circuit

Fig 12b. Unclamped Inductive Waveforms

Fig 13a. Basic Gate Charge Waveform

Fig 12c. Maximum Avalanche Energy Vs. Drain Current

Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit

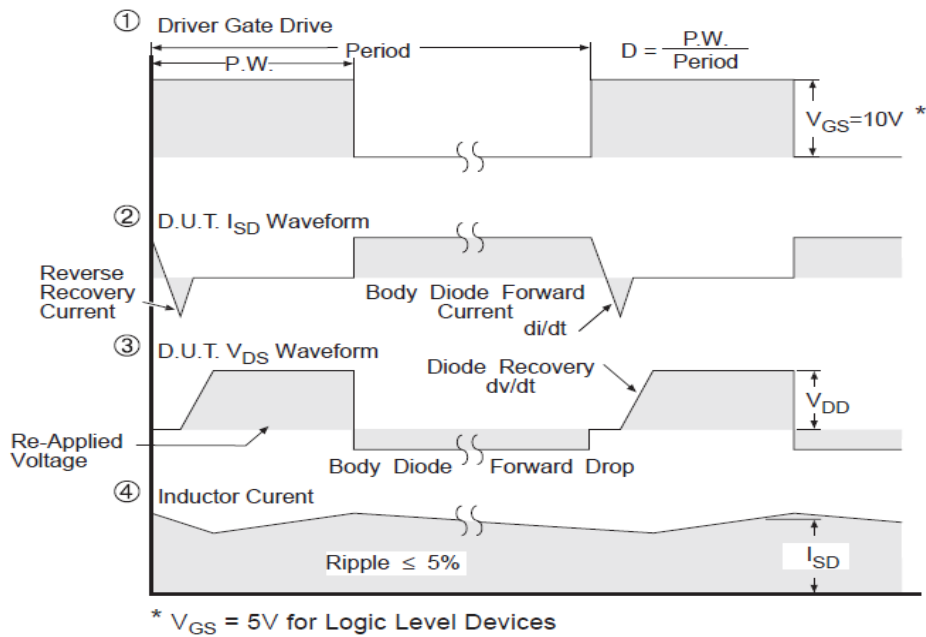
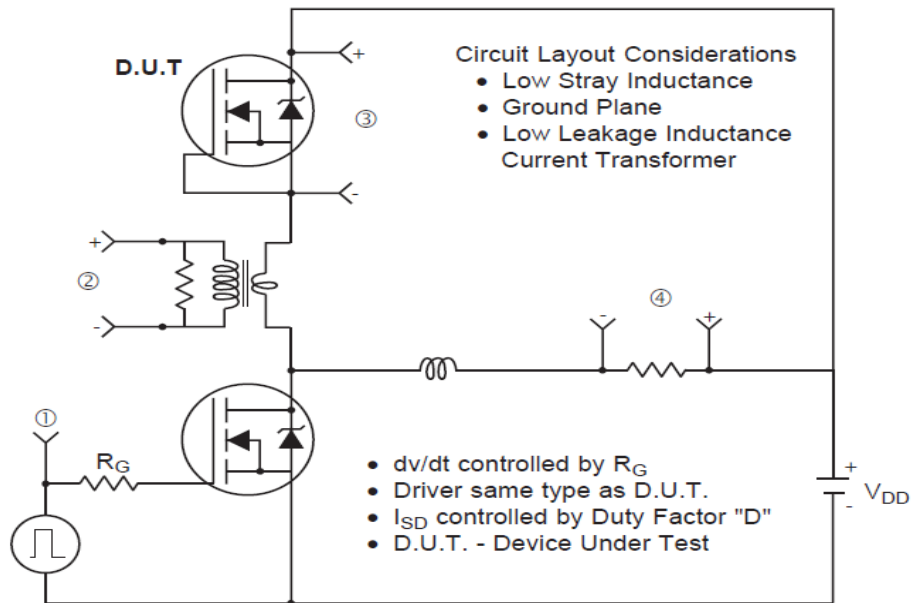
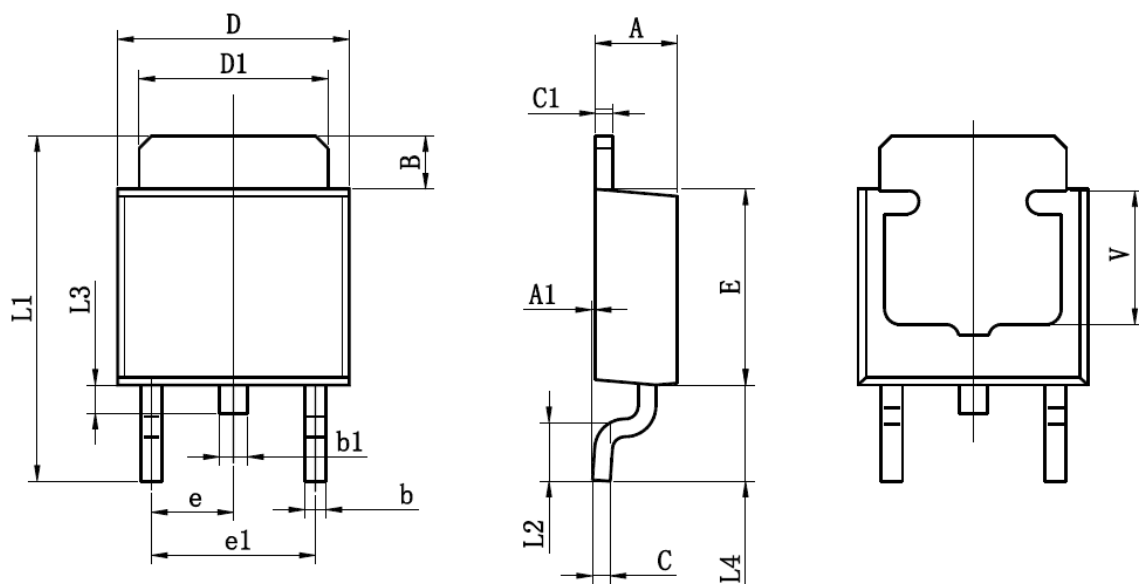
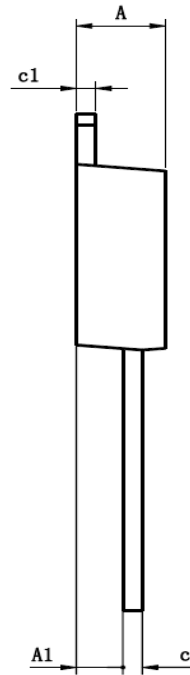
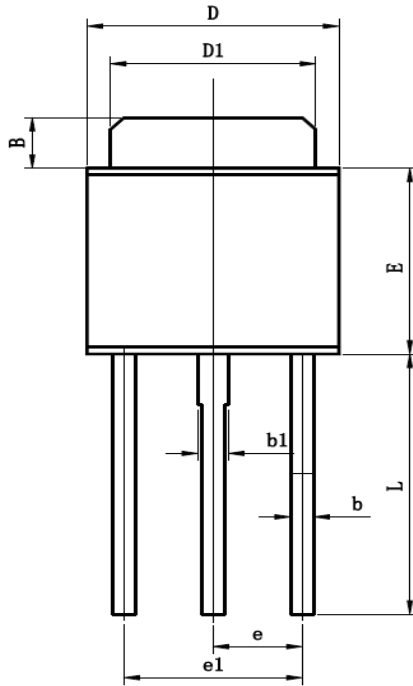


Fig 14. For N-Channel HEXFETS

TO-252-2L PACKAGE OUTLINE SOP-8P


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300TYP		0.091TYP	
e1	4.500	4.700	0.177	0.185
L1	9.500	9.900	0.374	0.390
L2	1.400	1.780	0.055	0.070
L3	0.650	0.950	0.026	0.037
L4	2.550	2.900	0.100	0.114
V	3.80REF		0.150REF	

TO-251 PACKAGE OUTLINE SOP-8P


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.200	2.400	0.087	0.094
A1	1.020	1.270	0.040	0.050
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300TYP		0.091TYP	
e1	4.500	4.700	0.177	0.185
L	7.500	7.900	0.295	0.311