

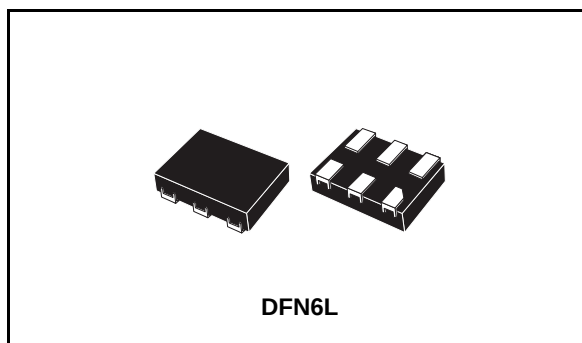


ST1G3236

1-bit dual supply bus transceiver level translator with A-side series resistor

Features

- High speed: $t_{PD} = 4.0\text{ns}$ (Max.) at $T_A = 85^\circ\text{C}$
- Low power dissipation:
 $I_{CCA} = I_{CCB} = 5\mu\text{A}$ (Max.) at $T_A = 85^\circ\text{C}$
- Balanced propagation delays:
 $t_{PLH} \cong t_{PHL}$
- Power-down protection on inputs and outputs
- 26Ω series resistor on A-side outputs
- Operating voltage range:
 - $V_{CCA}(\text{Opr}) = 1.2\text{V}$ to 3.6V
 - $V_{CCB}(\text{Opr}) = 1.2\text{V}$ to V_{CCA}
- Latch-up performance exceeds 100mA per JESD 78, Class II
- ESD performance exceeds JESD22
 - 2000-V Human-body model (A114-A)



Description

The ST1G3236 is a dual supply low voltage CMOS 1-bit bus Transceiver fabricated with sub-micron silicon gate and five-layer metal wiring C2MOS technology. Designed for use as an interface between a 3.3V bus and a 2.5V or 1.2V bus in mixed supply systems of 3.3V/1.2V, 3.3V/2.5V and 2.5V/1.8V, the ST1G3236 achieves high speed operation while maintaining low power dissipation. V_{CCA} and V_{CCB} can be powered from 1.2V to 3.6V respectively. The DIR pin is designed to track V_{CCB} .

The device is intended for two-way asynchronous communication between data buses and the direction of data transmission is determined by DIR inputs.

All inputs are equipped with protection circuits against static discharge, giving them 2kV ESD immunity and transient excess voltage.

Table 1. Device summary

Order code	Package	Packaging
ST1G3236DTR	DFN6L (1.2x1mm)	Tape and Reel

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1 Device summary

1.1 Pin settings

Figure 1. Logic diagram

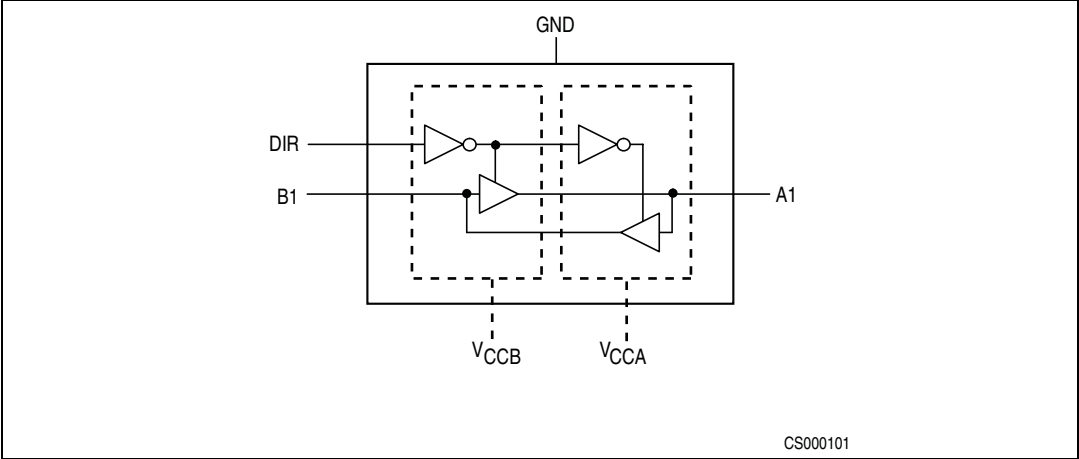
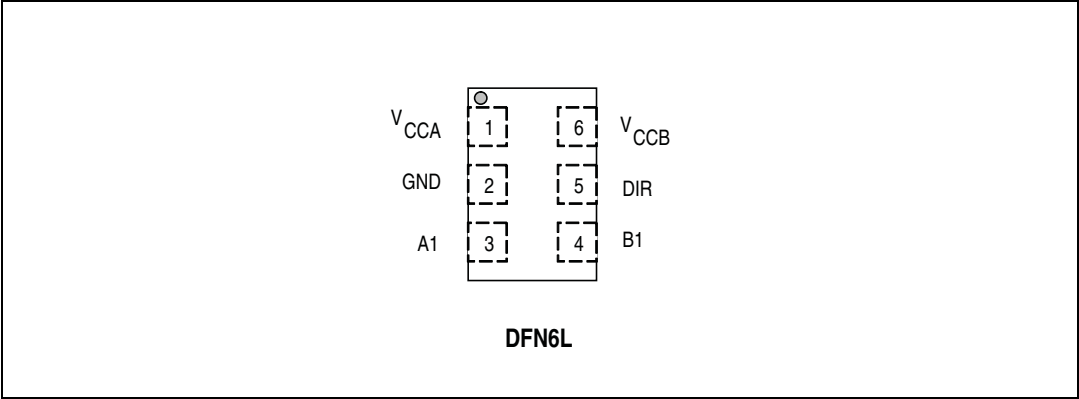


Figure 2. Pin connection (top through view)



1.2 Pin description

Table 1. Pin description

Pin N°	Symbol	Name and function
1	V _{CCA}	Positive supply voltage
2	GND	Ground (0V)
3	A1	Data Inputs/Outputs
4	B1	Data Inputs/Outputs
5	DIR	Directional controls
6	V _{CCB}	Positive supply voltage

2 Pin connection

Figure 3. Input and output equivalent circuit

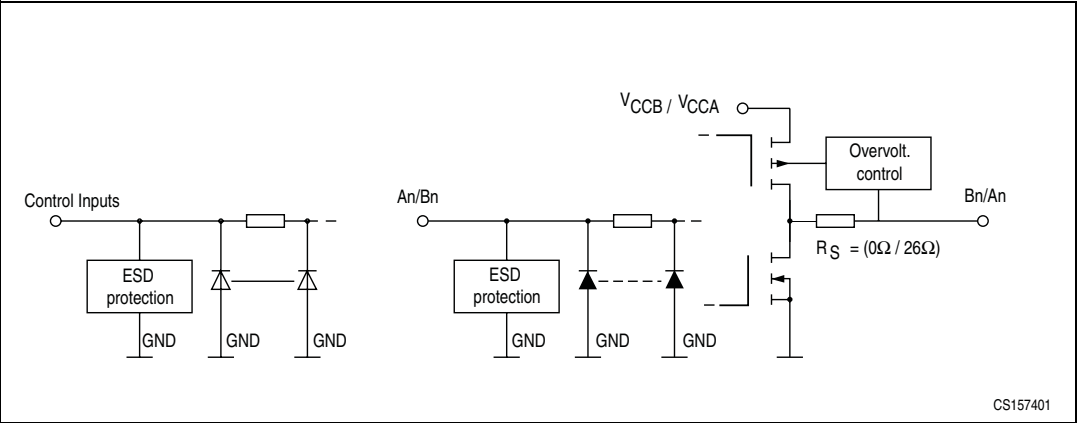


Table 2. Truth table

Dir input	Function	
	Bus A	Bus B
L	Output	Input
H	Input	Output

3 Maximum rating

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CCA}	Output supply voltage	-0.5 to 4.6	V
V_{CCB}	Input supply voltage	-0.5 to + 4.6	V
V_I	DC input voltage	-0.5 to +4.6	V
V_{IOA}	DC output voltage	-0.5 to $V_{CCA} + 0.5$	V
V_{IOB}	DC output voltage	-0.5 to $V_{CCB} + 0.5$	V
I_{IK}	DC input diode current	-20	mA
I_{OK}	DC output diode current	-50	mA
I_{OA}	DC output current	± 50	mA
I_{OB}	DC output current	± 50	mA
I_{CCA}	DC V_{CCA} or ground current	± 100	mA
I_{CCB}	DC V_{CCB} or ground current	± 100	mA
P_d	Power dissipation	200	mW
T_{stg}	Storage temperature	-65 to +150	°C
T_L	Lead temperature (10 sec)	260	°C

3.1 Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Value	Unit
V_{CCA}	Supply voltage	1.2 to 3.6	V
$V_{CCB}^{(1)}$	Supply voltage	1.2 to V_{CCA}	V

Table 4. Recommended operating conditions

Symbol	Parameter		Value	Unit
V_I	Input voltage (DIR)		0 to V_{CCB}	V
$V_{I/OA}$	I/O voltage		0 to V_{CCA}	V
$V_{I/OB}$	I/O voltage		0 to V_{CCB}	V
T_{op}	Operating temperature		-40 to 85	°C
$dt/dv^{(2)}$	Input Rise and Fall Time	$V_{CCB} = 3.0$ to $3.6V$	0 to 10	ns/V
		$V_{CCB} = 2.3$ to $2.7V$	0 to 20	ns/V
		$V_{CCB} = 1.2$ to $1.95V$	0 to 100	ns/V

1. V_{CCB} must be lower than V_{CCA}
2. V_{IN} from 0.8V to 2.0V at $V_{CC} = 3.0V$

4 Electrical characteristics

Table 5. DC specification for V_{CCA}

Symbol	Parameter	Test condition			Value				Unit
		V _{CCB} (V)	V _{CCA} (V)		T _A = 25 °C		-40 to 85 °C		
					Min	Max	Min	Max	
V _{IHA}	High level input voltage (A1)	1.2 to V _{CCA}	1.2 to 1.95		0.65 V _{CCA}		0.65 V _{CCA}		V
			1.95 to 2.7		1.6		1.6		
			2.7 to 3.6		2		2		
V _{ILA}	Low level input voltage (A1)	1.2 to V _{CCA}	1.2 to 1.95			0.35V _{CCA}		0.35 V _{CCA}	V
			1.95 to 2.7			0.7		0.8	
			2.7 to 3.6			0.8		0.8	
V _{OHA}	High level output voltage	1.2 to V _{CCA}	1.2 to 3.6V	I _O =-100μA	V _{CCA} - 0.2		V _{CCA} - 0.2		V
			3.0	I _O =-10mA	2.5		2.5		
			2.3	I _O =-6mA	1.8		1.8		
			1.65	I _O =-4mA	1.25		1.25		
			1.4	I _O =-2mA	1.1		1.1		
			1.2	I _O =-1mA	0.95		0.95		
V _{OLA}	Low level output voltage	1.2 to V _{CCA}	1.2 to 3.6V	I _O =-100μA		0.2		0.2	V
			3.0	I _O =-10mA		0.55		0.55	
			2.3	I _O =-6mA		0.40		0.40	
			1.65	I _O =-4mA		0.40		0.40	
			1.4	I _O =-2mA		0.30		0.30	
			1.2	I _O =-1mA		0.25		0.25	
I _{IA}	Input leakage current	2.7	3.3	V _I =V _{CCA} or GND		±0.5		±5	μA
		1.4	2.7	V _{IA} =3.6V or GND		±0.5		±5	μA

Table 5. DC specification for V_{CCA} (continued)

Symbol	Parameter	Test condition			Value				Unit
		V _{CCB} (V)	V _{CCA} (V)		T _A = 25 °C		-40 to 85 °C		
					Min	Max	Min	Max	
I _{OFF}	Power OFF leakage current	0	0	V _{IA} =GND to 3.6V V _{IB} =GND to 3.6V DIR=GND to 3.6V		±1.0		±10	μA
I _{CCtA}	Quiescent supply current	1.2V	1.2 to 3.6V	V _{IA} =V _{CCA} or GND		0.5		5	μA
		1.2 to 3.6V	3.6	V _{IB} =V _{CCB} or GND DIR =A to B					
ΔI _{CCtA}	Maximum quiescent supply current/input	2.7V	3.3V	V _{IA} =V _{CCA} to 0.6V				0.75	μA
		1.8	3.3	V _{IB} =V _{CCB} or GND					
		1.8	2.7						

Table 6. DC specification for V_{CCB}

Symbol	Parameter	Test condition			Value				Unit
		V _{CCB} (V)	V _{CCA} (V)		T _A = 25 °C		-40 to 85 °C		
					Min	Max	Min	Max	
V _{IHB}	High level input voltage (A1)	1.2	V _{CCB} to 3.6V		0.65 V _{CCB}		0.65 V _{CCB}		V
		1.8			1.2		1.2		
		2.5			1.6		1.6		
		3.3			2		2		
V _{ILB}	Low level input voltage (B1, DIR)	1.2	V _{CCB} to 3.6V			0.35 V _{CCB}		0.35 V _{CCB}	V
		1.8				0.6		0.6	
		2.5				0.7		0.7	
		3.3				1.0		1.0	

Table 6. DC specification for V_{CCB} (continued)

Symbol	Parameter	Test condition			Value				Unit
		V _{CCB} (V)	V _{CCA} (V)		T _A = 25 °C		-40 to 85 °C		
					Min	Max	Min	Max	
V _{OHB}	High level output voltage	1.2 to 3.6V	V _{CCB} to 3.6V	I _O =-100μA		V _{CCB} -0.2		V _{CCB} -0.2	V
		3.0		I _O =-10mA		2.5		2.5	
		2.3		I _O =-6mA		1.8		1.8	
		1.65		I _O =-4mA		1.25		1.25	
		1.4		I _O =-2mA		1.1		1.1	
		1.2		I _O =-1mA		0.95		0.95	
V _{OLB}	Low level output voltage	1.2 to 3.6V	V _{CCB} to 3.6V	I _O =-100μA		0.2		0.2	V
		3.0		I _O =-10mA		0.55		0.55	
		2.3		I _O =-6mA		0.40		0.40	
		1.65		I _O =-4mA		0.40		0.40	
		1.4		I _O =-2mA		0.30		0.30	
		1.2		I _O =-1mA		0.25		0.25	
I _{IB}	Input leakage current	2.7	3.3	V _{IB} =V _{CC} or GND		±0.5		±5	μA
		1.4	2.7	V _{IB} =3.6V or GND		±0.5		±5	μA
I _{CCIB}	Quiescent supply current	1.2 to V _{CCA}	1.2 to 3.6	V _{IA} =V _{CC} _A or GND V _{IB} =V _{CC} _B or GND DIR =B to A		0.5		5	μA
ΔI _{CCIB}	Maximum quiescent supply current/input (B1, DIR)	2.7	3.3	V _{IB} =V _{CCB} to 0.6V	-	-	-	0.75	μA
		1.8	3.3		-	-	-		
		1.8	2.7	V _{IA} =V _{CCB} or GND	-	-	-		

Table 7. AC electrical characteristics

Symbol	Parameter	Test condition			Value			Unit
		V _{CCB} (V)	V _{CCA} (V)		-40 to 85 °C			
					Min	Typ	Max	
t _{PLH} t _{PHL}	Propagation delay time An to Bn	1.8 ± 0.15	2.5 ± 0.2	C _L = 30 pF R _L = 500Ω	1.0		4	ns
		1.8 ± 0.15	3.3 ± 0.3		1.0		3.5	
		2.5 ± 0.2	3.3 ± 0.3		1.0		2.8	
		1.8 ± 0.15	2.5 ± 0.2	C _L = 10 pF	1.0		3.8	
		1.8 ± 0.15	3.3 ± 0.3		1.0		3.4	
		2.5 ± 0.2	3.3 ± 0.3		1.0		2.7	
t _{PLH} t _{PHL}	Propagation delay time Bn to An	1.8 ± 0.15	2.5 ± 0.2	C _L = 30 pF R _L = 500 Ω	1.0		4.5	ns
		1.8 ± 0.15	3.3 ± 0.3		1.0		4	
		2.5 ± 0.2	3.3 ± 0.3		1.0		3	
		1.8 ± 0.15	2.5 ± 0.2	C _L = 10 pF	1.0		4.5	
		1.8 ± 0.15	3.3 ± 0.3		1.0		4	
		2.5 ± 0.2	3.3 ± 0.3		1.0		3	
t _{PZL} t _{PZH}	Output enable time DIR to An	1.8 ± 0.15	2.5 ± 0.2	C _L = 30 pF R _L = 500Ω		6		ns
		1.8 ± 0.15	3.3 ± 0.3			6		
		2.5 ± 0.2	3.3 ± 0.3			6		
t _{PZL} t _{PZH}	Output enable time DIR to Bn	1.8 ± 0.15	2.5 ± 0.2	C _L = 30 pF R _L = 500Ω		6		ns
		1.8 ± 0.15	3.3 ± 0.3			6		
		2.5 ± 0.2	3.3 ± 0.3			6		

Table 8. Capacitance characteristics

Symbol	Parameter	Test condition			Value					Unit
		V _{CCB} (V)	V _{CCA} (V)		T _A = 25 °C			-40 to 85 °C		
					Min	Typ	Max	Min	Max	
C _{INB}	Input capacitance	open	open			6				pF
C _{I/O}	I/O capacitance	2.5	3.3			6				pF
C _{PD}	Power dissipation capacitance	2.5	3.3	f = 10MHz		29				pF
		1.8	3.3			29				pF

Note: 1 C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/4$ (per circuit)

5 Test circuit

Figure 4. Test circuit

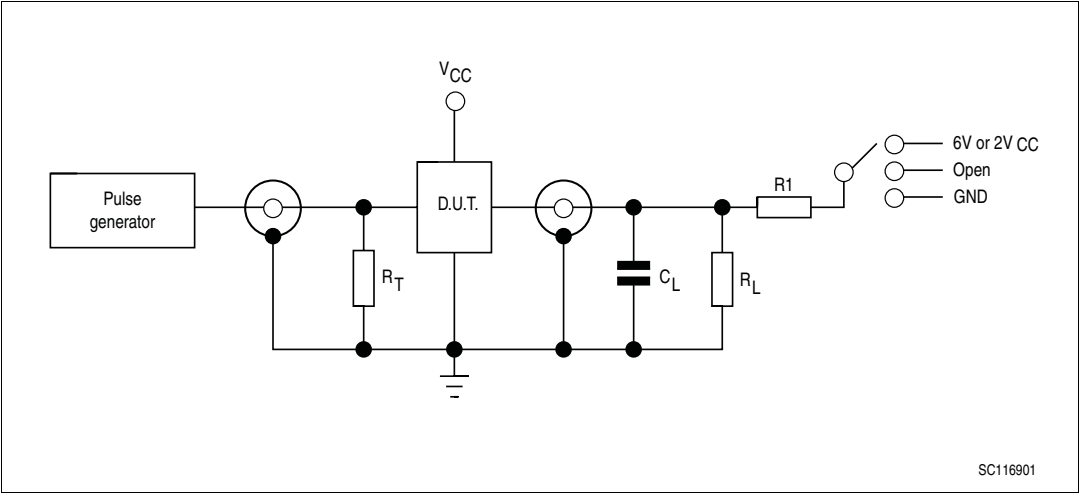


Table 9. Test circuit

Test		Switch
t_{PLH} , t_{PHL}	$C_L \approx 30\text{pF}$; $R_L \approx 500\Omega$	Open

$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

6 Waveforms

Figure 5. Waveform - propagation delay (f=1 MHz, 50% duty cycle)

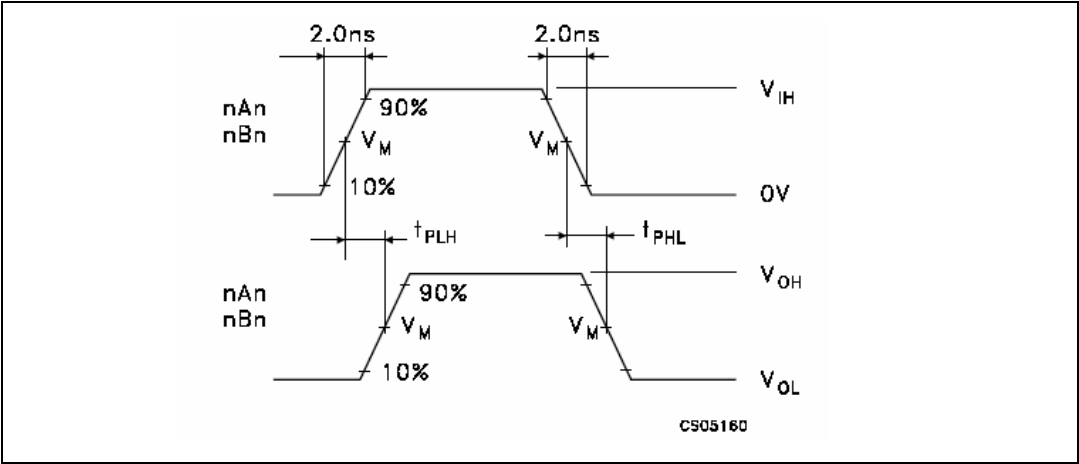
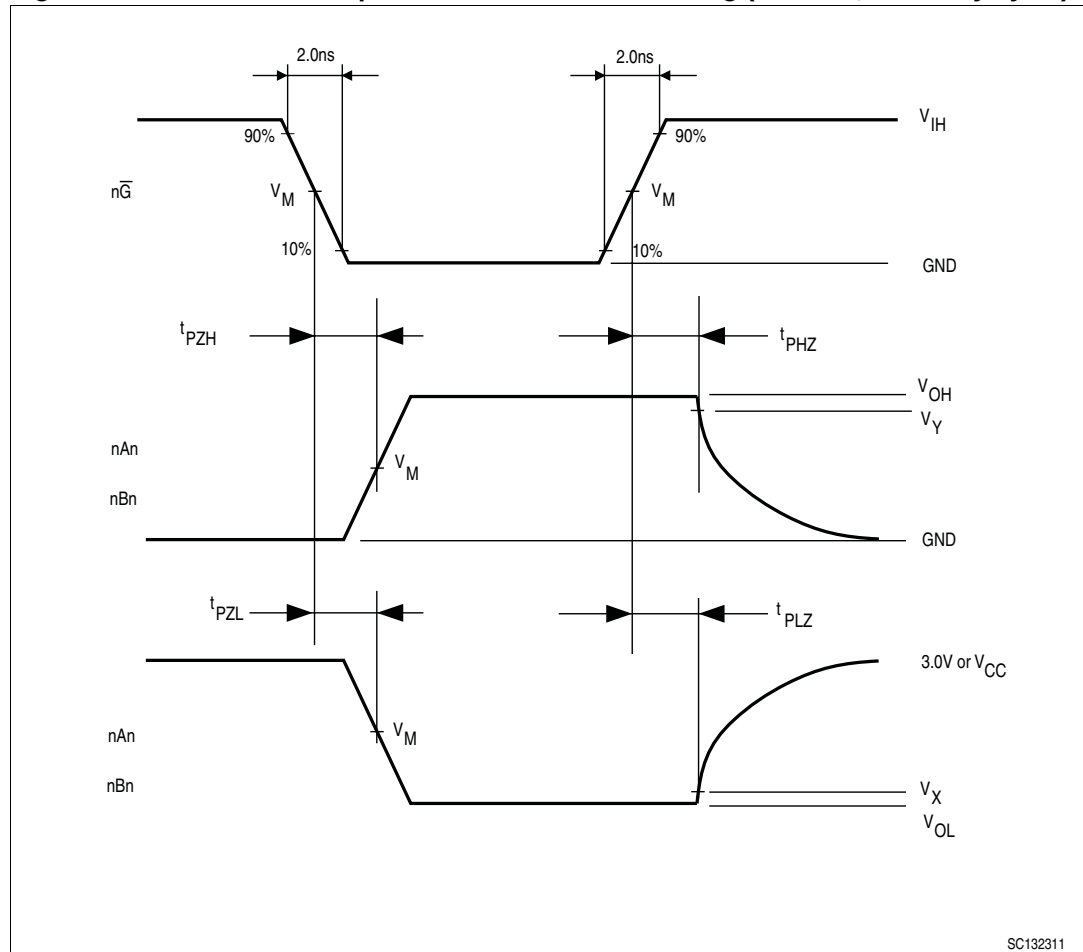


Table 10. Waveform symbol value

Symbol	V _{CC}		
	3.0 to 3.6V	2.3 to 2.7V	1.65 to 1.95V
V _{IH}	V _{CC}	V _{CC}	V _{CC}
V _M	1.5V	V _{CC} /2	V _{CC} /2
V _X	V _{OL} +0.3V	V _{OL} +0.15V	V _{OL} +0.15V
V _Y	V _{OH} -0.3V	V _{OH} -0.15V	V _{OH} -0.15V

Figure 6. Waveform - Output Enable and Disable timing (f=1 MHz, 50% duty cycle)



7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 7. DFN6 (1.2x1mm) package outline

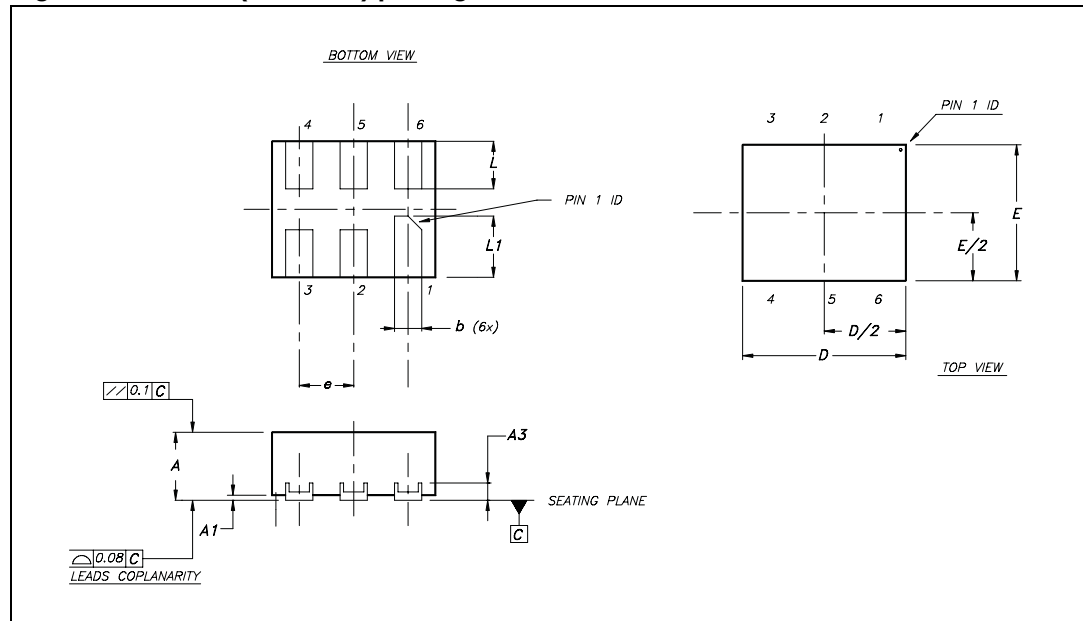


Table 11. DFN6L (1.2x1mm) mechanical data

Symbol	millimeters		
	Min	Typ	Max
A	0.45	0.50	0.55
A1	0	0.02	0.05
A3		0.127	
b	0.15	0.20	0.25
D	1.15	1.20	1.25
E	0.95	1	1.05
e		0.40	
L	0.30	0.35	0.40
L1	0.40	0.45	0.50

The diagram shows a stepped pyramid structure with the following dimensions and labels:

- Top Level:** A central rectangular block labeled **1** with a width of **0.25 (6x)** and a height of **0.50**. It is flanked by two smaller rectangular blocks labeled **2** and **3**, each with a width of **0.40**. The total width of the top level is **0.80**.
- Bottom Level:** Three rectangular blocks labeled **4**, **5**, and **6** are positioned below the top level. Block **4** is on the left, **5** is in the center, and **6** is on the right. The total width of the bottom level is **0.525**. The height of the bottom level is **0.40 (5x)**.
- Overall Dimensions:** The total height of the structure is **1.05**, which is the sum of the top level height (**0.50**) and the bottom level height (**0.40**).

[illegible]

Figure 10. Reel for carrier tape information

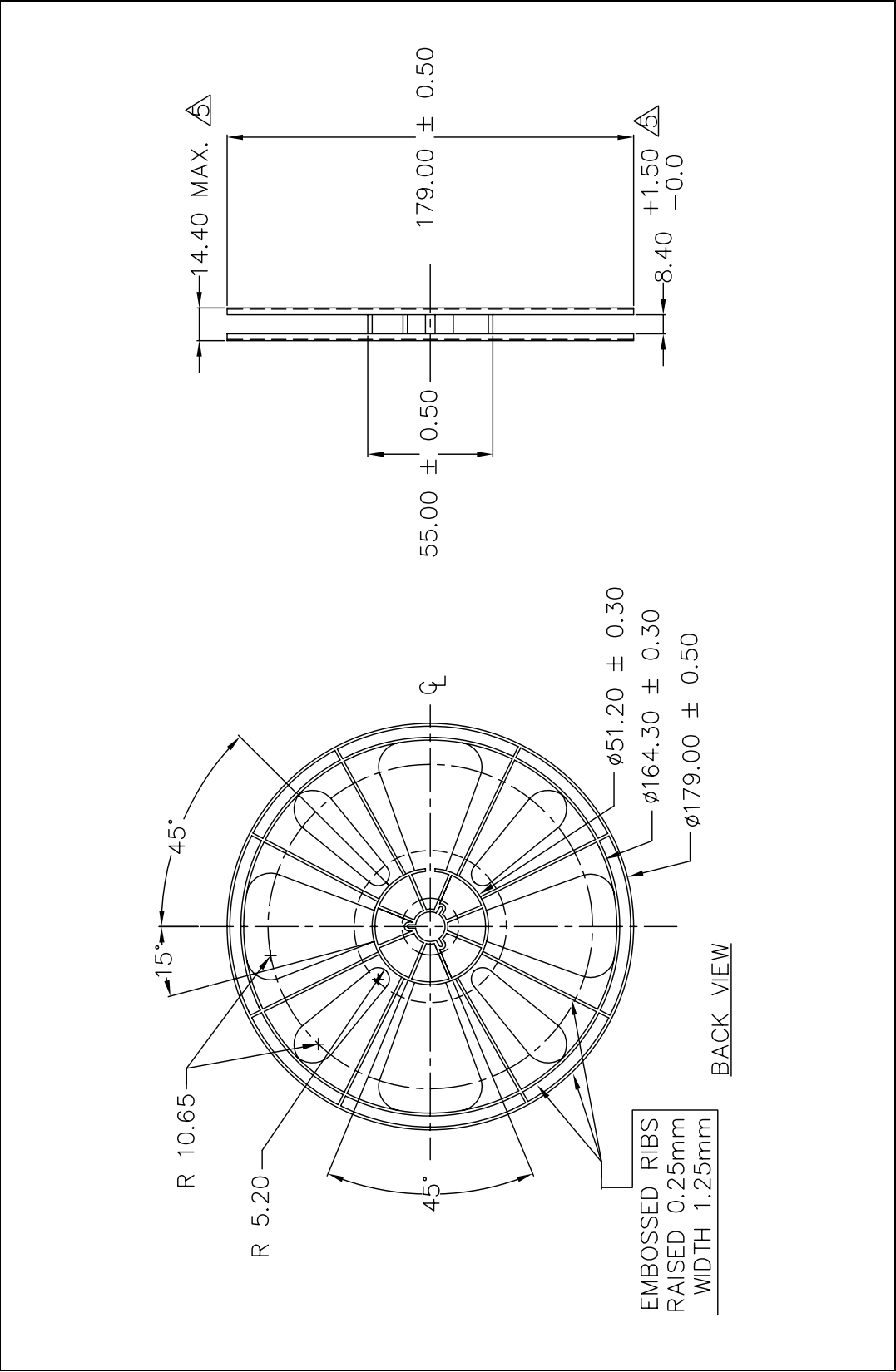
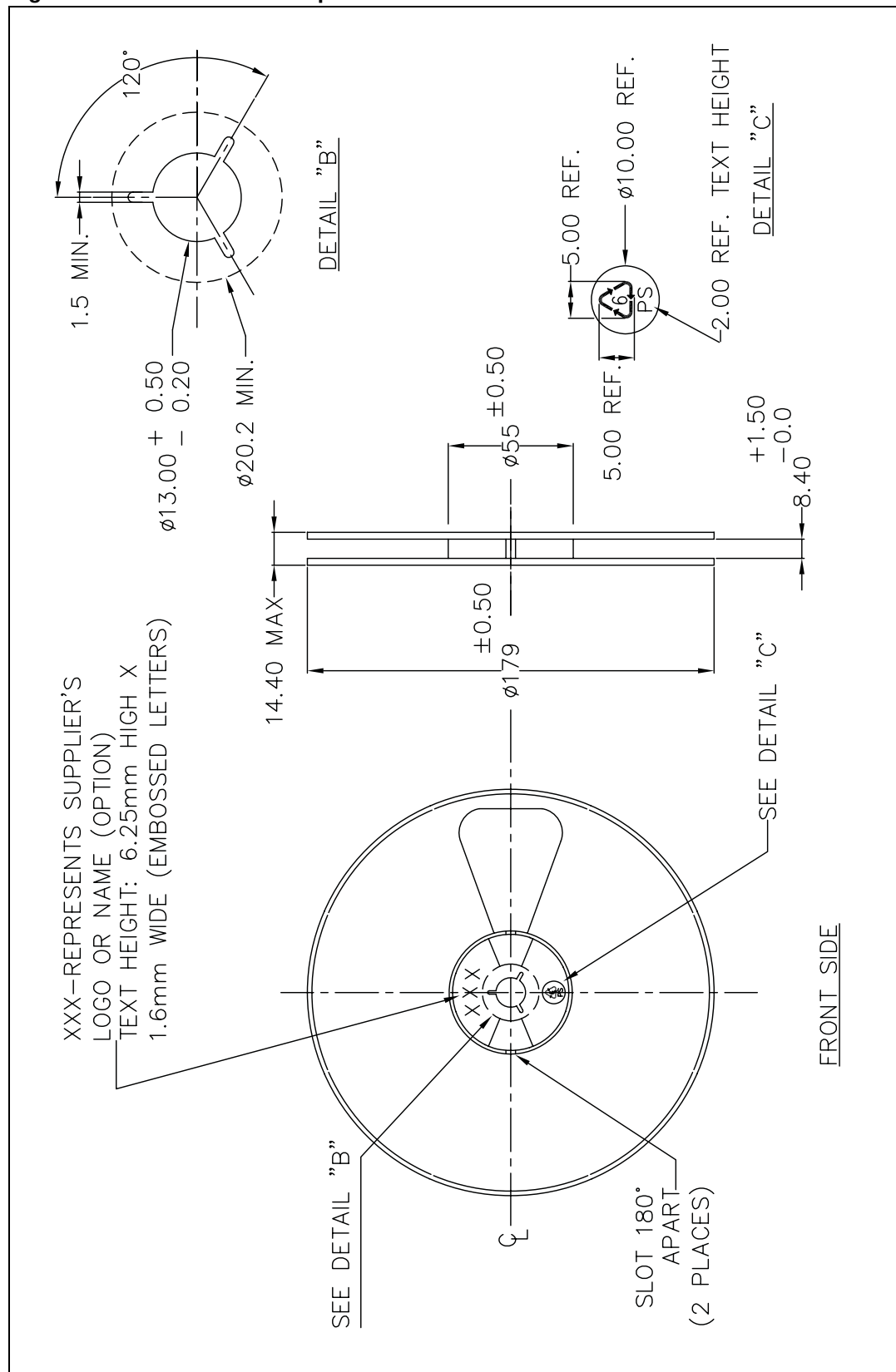


Figure 11. Reel for carrier tape information



8 Revision history

Table 12. Revision history

Date	Revision	Changes
25-July-2007	1	First release.

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