



ST21NFCA

Near field communication microcontroller

Data Brief

Features

ST21NFCA operating modes supported:

- Card emulation
- Reader
- Peer-to-peer communication

Hardware features

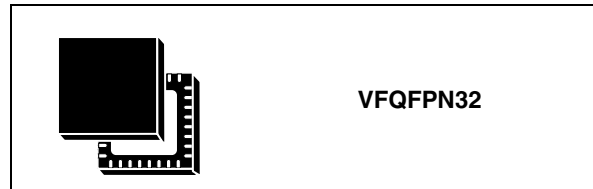
- Enhanced 8/16-bit CPU core with 16 Mbytes linear addressable memory
- 112 Kbytes of User ROM
- 4 Kbytes of RAM
- 36 Kbytes of EEPROM including 64 bytes User OTP area
- High integrated analog front end (AFE) for RF transmission and reception including automatic card and field detection modes
- Three 8-bit timers with interrupt capability
- Battery Off and Battery Low modes supported in Card Emulation mode
- Optimized power consumption modes
- SIM and ST21NFCA power management functions

RF communications

- ISO/IEC 14443 A&B
- ISO/IEC 15693
- ISO/IEC 18000-3 Mod1
- ECMA340 (NFCIP-1)
- Supports FeliCa™ cards as described in ECMA340 specification
- All RF communications are available in card and reader modes

Communication interfaces

- Single Wire Protocol (SWP) interface
- I²C Slave interface
- SPI Slave interface
- Asynchronous receiver transmitter ISO/IEC 7816-3 master interface supporting T=0 and T=1 protocols



Security features

- True random number generator
- ISO/IEC 3309 CRC calculation block
- Unique serial number on each die
- Hardware DES accelerator

Electrical characteristics

- Standby current: < 75 µA (typ.)
- Card emulation: < 8 mA in normal mode
- Standby current for Reader mode: ~200 µA in Card Detection mode
- Reader mode: < 70 mA (typ.)
- 3V power supply
- Supports Class B and C for UICC

Software features

- Includes all drivers supporting the handling and host protocols for contact and contactless interfaces
- Includes complete firmware driving switch modes between operating modes and host controller interface functions (HCI)

Validation tools

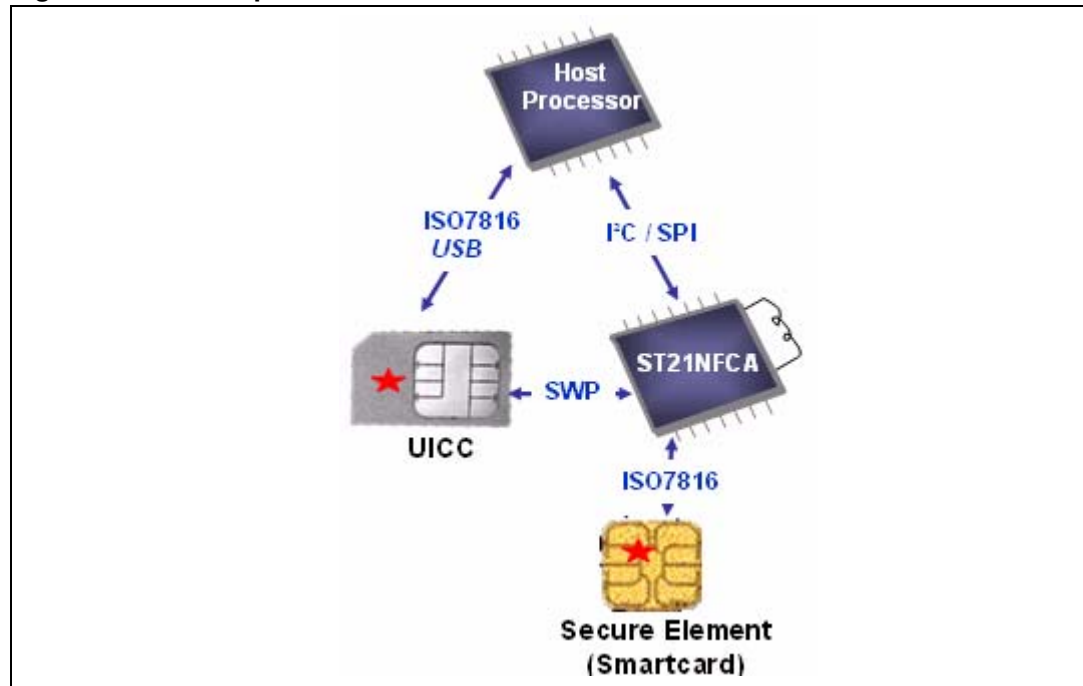
An evaluation and debugging board is available for complete integration.

1 Description

The ST21NFCA is a single chip designed for supporting 13.56 MHz contactless communication, including Near Field Communication (NFC) functions in the three operating modes: card emulation, reader and peer-to-peer communication.

The ST21NFCA is designed for an optimized integration on a mobile phone with the communication links shown in *Figure 1*.

Figure 1. Mobile phone communication links



This product is based on an advanced Smartcard ST21 microcontroller with 36 Kbytes of EEPROM, 112 Kbytes of User ROM and 4 Kbytes of RAM and includes an integrated RF Analog Front End (AFE) supporting all the contactless proximity (ISO/IEC 14443, Calypso V1 Radio Protocol (B'), ECMA340 (NFCIP-1), and vicinity (ISO/IEC15693, ISO/IEC18000-3Mod1) standards.

The ST21NFCA system-on-chip combines a complete hardware capability for 13.56 MHz contactless communication with an useful embedded firmware which handles:

- ISO/IEC 14443 A&B, Calypso V1 Radio Protocol (B'), ECMA340 (NFCIP-1), ISO/IEC 15693, ISO/IEC18000-3Mod1 in card emulation modes as well as reader modes
- Switch modes between operating modes and RF modes
- Host Controller Interface functions (HCI based on the ETSI specification)

In addition, the embedded firmware and associated macrocells support handling and protocol for the various interfaces:

- Single Wire Protocol (SWP) interface fully compliant with ETSI TS 102 613 Release 7
- I²C Slave interface fully compliant with NXP specification
- SPI Slave interface fully compliant with Freescale specification
- Asynchronous Receiver Transmitter in master configuration supporting ISO/IEC 7816-3 T=0 and T=1 protocols

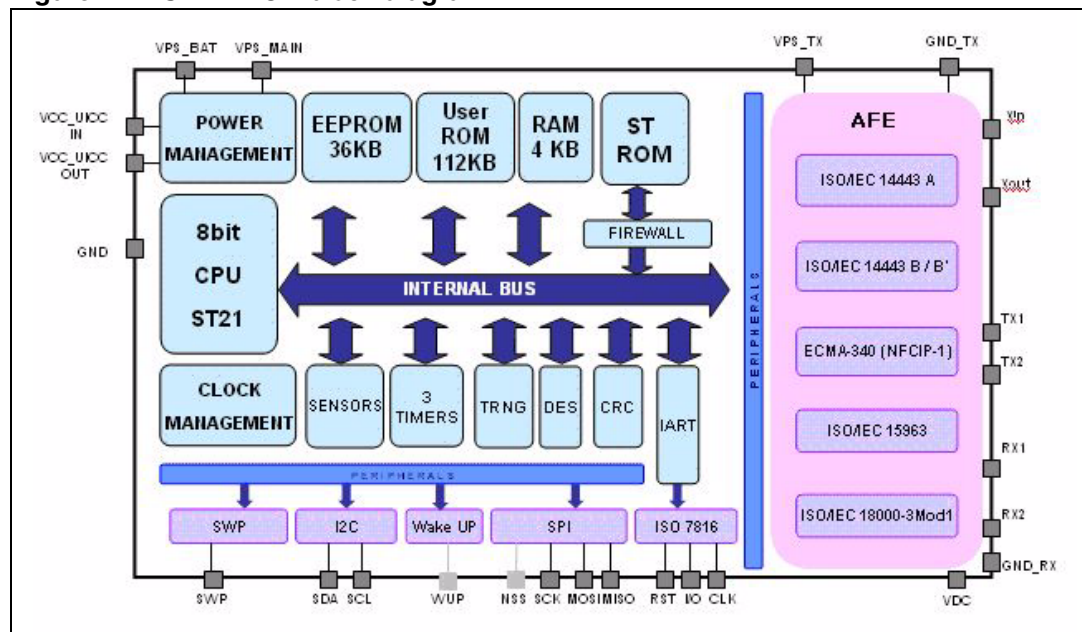
The ST21NFCA is a serial access circuit based on a 8/16-bit CPU core. Operations will be synchronized with an internally generated clock issued by the Clock Generator module. The internal speed of the device is fully software programmable.

The CPU includes the Arithmetic Logic Unit (ALU), the control logic and registers controlled by the ST21NFCA firmware. The CPU interfaces with the on-chip RAM, ROM and EEPROM memories via a 24-bit internal bus offering 16 MBytes of linear addressing space.

This device also includes a True Random Number Generator (TRNG), three 8-bit fully programmable timers, a Cyclic Redundancy Check (CRC3309) module, and a Data Encryption Standard (DES) accelerator.

Thanks to an enhanced power switch system, the ST21NFCA is able to support several power supply sources ("Battery On", Battery Low and Battery Off" modes) which manages the power management of the device and its associated UICC.

Figure 2. ST21NFCA block diagram



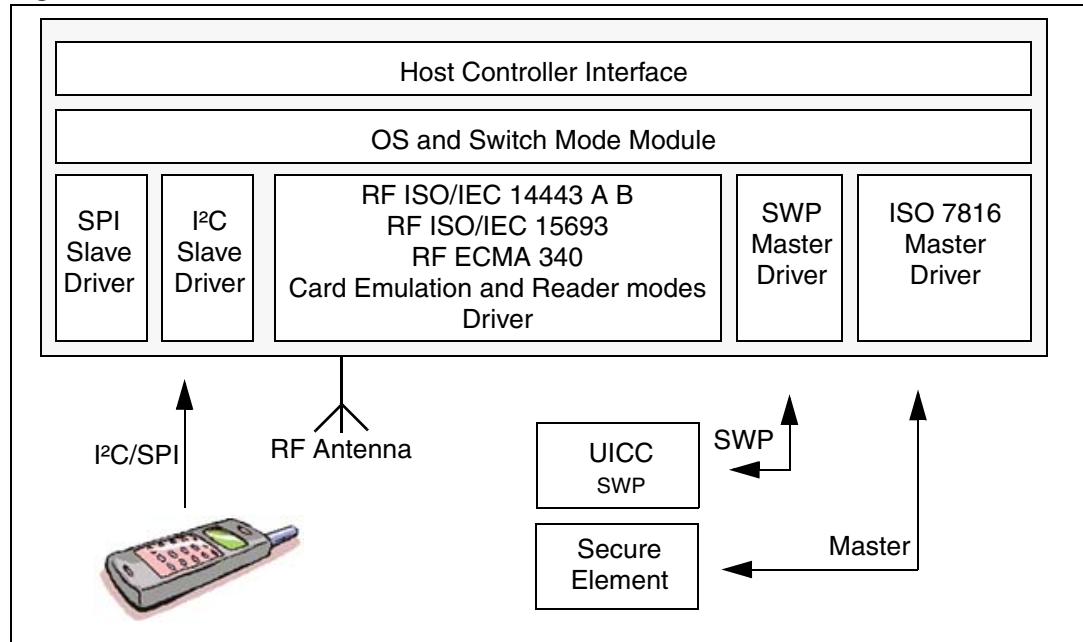
1.1 Firmware description

The ST21NFCA is a system on chip solution able to be compliant with NFC communication system embedded in a mobile phone.

The firmware is developed in several modules:

- Host Controller Interface based on the ETSI specification managing the gates related to the different protocols, the pipe between gates, the power management system, etc.
- The Operating System (OS) is the core of the system responsible for dispatching commands to the Host Controller Interface.
- The Switch Mode module manages the operating modes and the switching between all RF modes.
- Low-level drivers including:
 - ISO/IEC 7816 in Master mode
 - SPI in Slave mode
 - I²C in Slave mode
 - SWP in Master mode
 - RF drivers for all vicinity and proximity standards in Card Emulation and Reader modes
- Low-level contact and contactless I/O protocols:
 - T=0 and T=1 as defined in the ISO/IEC 7816 specification
 - T=CL as defined in the ISO/IEC 14443-A,-B specification
 - SHDLC as defined in the ETSI SWP specification

Figure 3. Firmware architecture overview



2 Revision history

Table 1. Document revision history

| Date | Revision | Changes |
|------------|----------|------------------|
| 8-Feb-2008 | 1 | Initial release. |

ST21NFCA

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