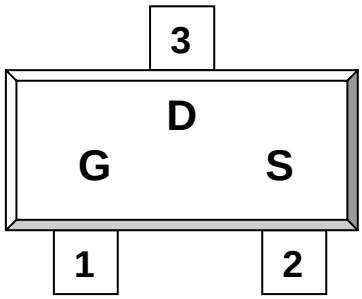
P Channel Enchancement Mode MOSFET ST2303

-1.7A

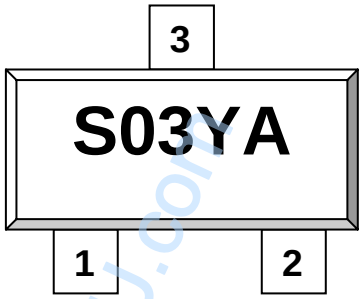
DESCRIPTION

The ST2303 is the P-Channel logic enhancement mode power field effect transistor are produced using high cell density, DMOS trench technology.
This high density process is especially tailored to minimize on-state resistance.
These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other batter powered circuits, and low in-line power loss are needed in a very small outine surface mount package.

PIN CONFIGURATION
SOT-23-3L



1.Gate 2.Source 3.Drain



S: Subcontractor Y: Year Code W: Process Code

FEATURE

- -30V/-2.6A, $R_{DS(ON)}$ = 130m-ohm @VGS = -10V
- -30V/-2.0A, $R_{DS(ON)}$ = 180m-ohm @VGS = -4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23-3L package design

STANSON TECHNOLOGY
120 Bentley Square, Mountain View, Ca 94040 USA
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ABSOULTE MAXIMUM RATINGS (Ta = 25°C Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	-30	V
Gate-Source Voltage		V_{GSS}	+20	V
Continuous Drain Current (TJ=150°C)	T_A=25°C T_A=70°C	I_D	-2.6 -2.0	A
Pulsed Drain Current		I_{DM}	-10	A
Continuous Source Current (Diode Conduction)		I_S	-1.25	A
Power Dissipation	T_A=25°C T_A=70°C	P_D	1.25 0.8	W
Operation Junction Temperature		T_J	150	°C
Storgae Temperature Range		T_{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	100	°C/W

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ELECTRICAL CHARACTERISTICS (Ta = 25℃ Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=-10uA	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250uA	-1.0		-3.0	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=+20V			+100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-30V,V_{GS}=0V			-1	uA
		V_{DS}=-30V,V_{GS}=0V T_J=55℃			-10	
On-State Drain Current	$I_{D(on)}$	V_{DS}≦-5V,V_{GS}=-10V	-6			A
Drain-source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V,I_D=-2.6A V_{GS}=-4.5V,I_D=-2.0A		0.095 0.125	0.130 0.180	Ω
Forward Transconductance	g_{fs}	V_{DS}=-10V,I_D=-1.7V		2.4		S
Diode Forward Voltage	V_{SD}	I_S=-1.25A,V_{GS}=0V		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Qg	V_{DS}=-15V,V_{GS}=-10V I_D≡-1.7A		5.8	10	nC
Gate-Source Charge	Qgs			0.8		
Gate-Drain Charge	Qgd			1.5		
Input Capacitance	Ciss	V_{DS}=-15V,V_{GS}=0V F=1MHz		226		PF
Output Capacitance	Coss			87		
Reverse Transfer Capacitance	Crss			19		
Turn-On Time	$t_{d(on)}$	V_{DD}=-15V,R_L=15Ω I_D=-1.0A,V_{GEN}=-10V R_G=6Ω		9	20	nS
	t_r			9	20	
Turn-Off Time	$t_{d(off)}$			18	35	
	t_f			6	20	

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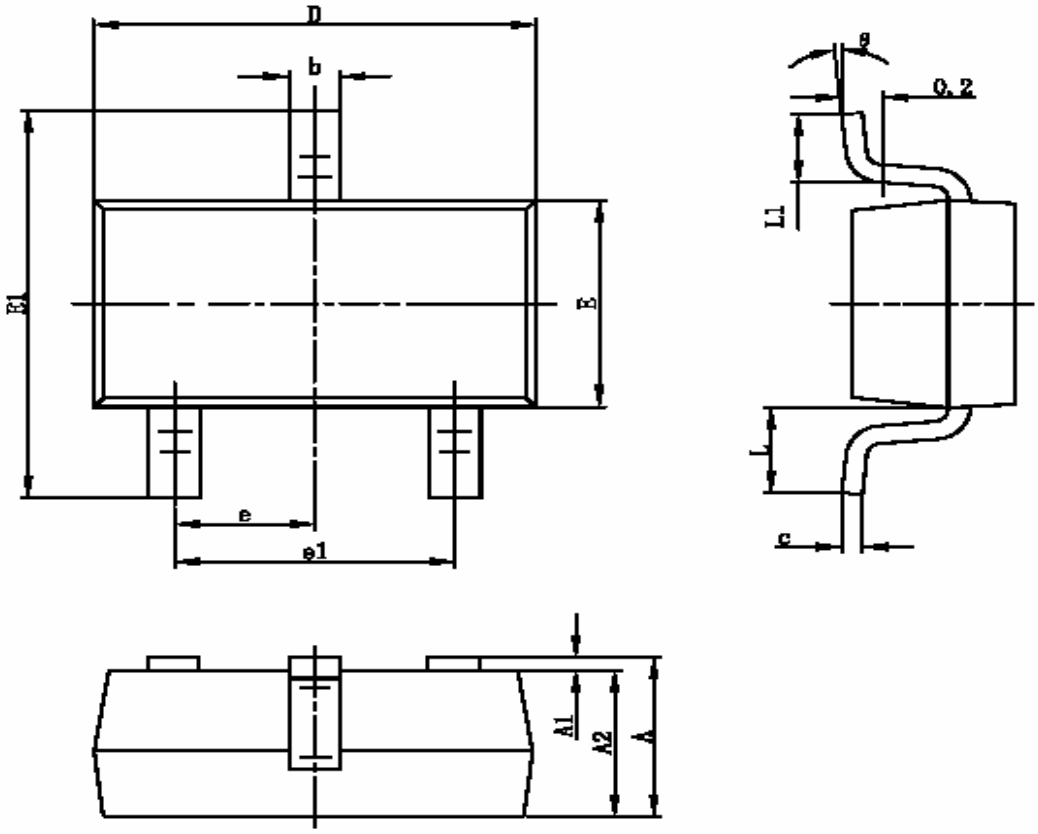
SOT-23-3L PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

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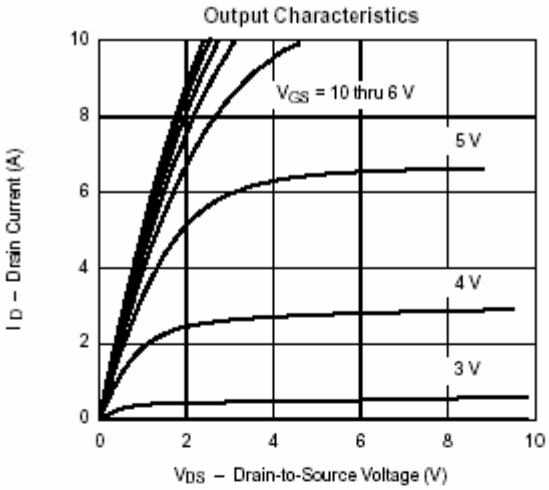

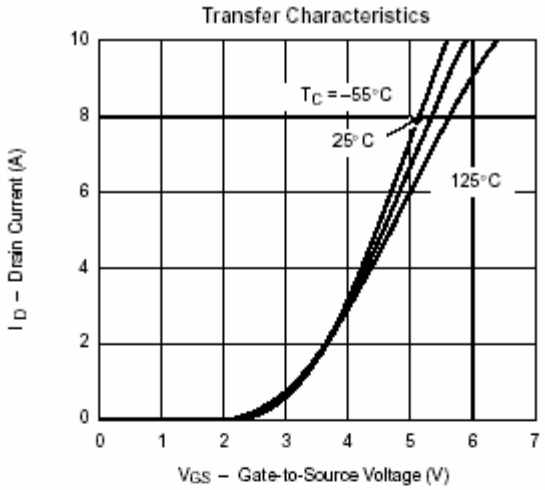

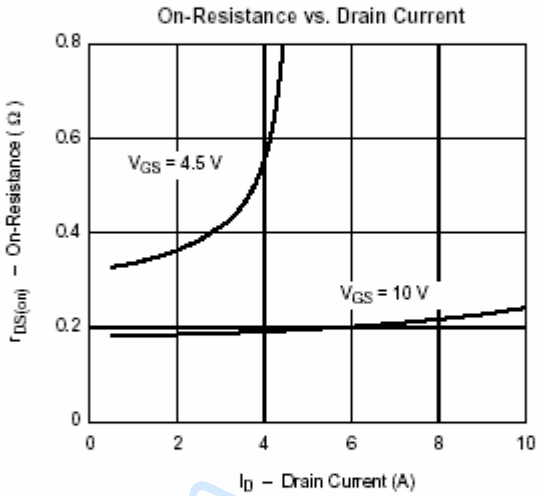

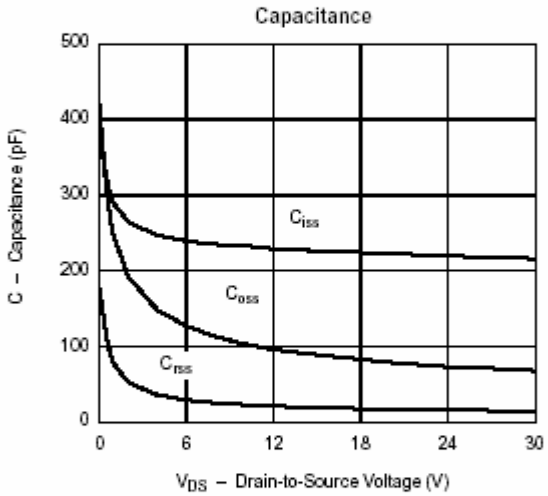

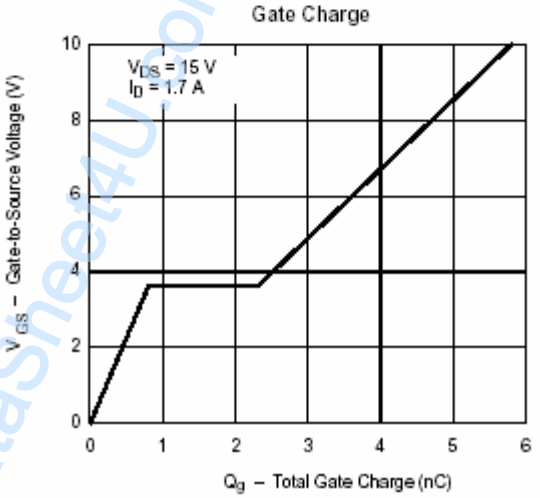

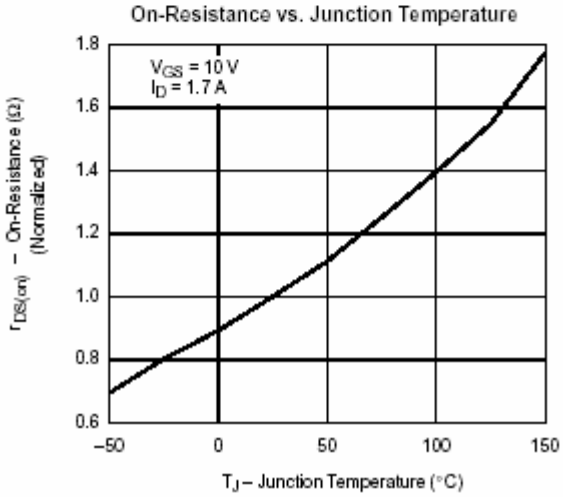

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