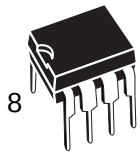
SGS-THOMSON MICROELECTRONICS

ST24LC21

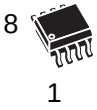
1Kb (x8) DUAL MODE SERIAL EEPROM for VESA Plug&Play

NOT FOR NEW DESIGN

- 1 MILLION ERASE/WRITE CYCLES
- 40 YEARS DATA RETENTION
- 2.5V to 5.5V SINGLE SUPPLY VOLTAGE
- 400k Hz COMPATIBILITY OVER the FULL RANGE of SUPPLY VOLTAGE
- TWO WIRE SERIAL INTERFACE I^2C BUS COMPATIBLE
- PAGE WRITE (up to 8 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES
- ***ST24LC21 is replaced by the ST24LC21B***

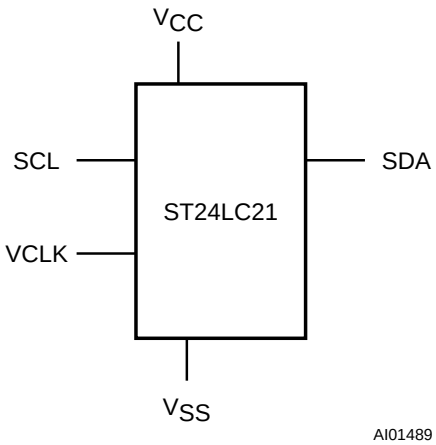


PSDIP8 (B)
0.25mm Frame



SO8 (M)

Figure 1. Logic Diagram



DESCRIPTION

The ST24LC21 is a 1K bit electrically erasable programmable memory (EEPROM), organized by 8 bits. This device can operate in two modes: Transmit Only mode and I^2C bidirectional mode. When powered, the device is in Transmit Only mode with EEPROM data clocked out from the rising edge of the signal applied on VCLK.

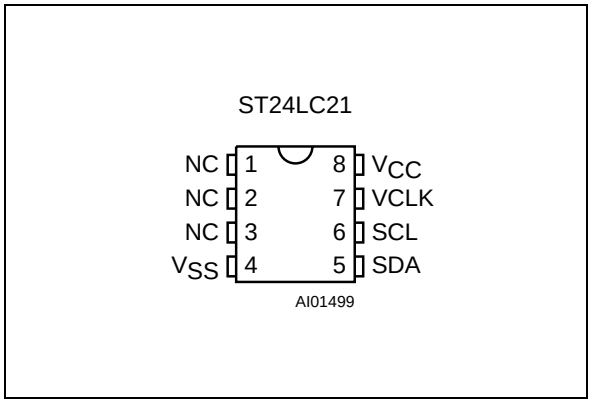
The device will switch to the I^2C bidirectional mode upon the falling edge of the signal applied on SCL pin. The ST24LC21 cannot switch from the I^2C bidirectional mode to the Transmit Only mode (except when the power supply is removed). The device operates with a power supply value as low as 2.5V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

Table 1. Signal Names

SDA	Serial Data Address Input/Output
SCL	Serial Clock (I^2C mode)
V_{CC}	Supply Voltage
V_{SS}	Ground
VCLK	Clock Transmit only mode

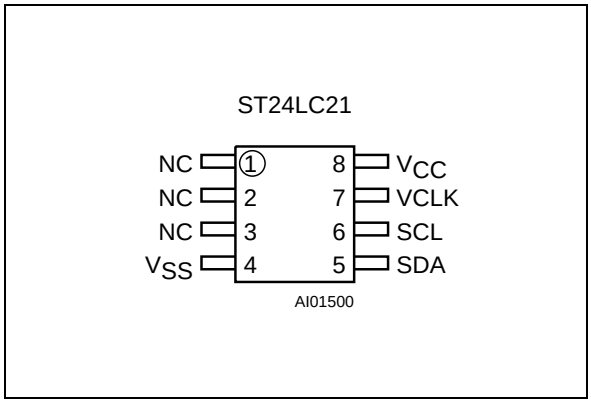
This is information on a product still in production but not recommended for new designs.

Figure 2A. DIP Pin Connections



Warning: NC = Not Connected

Figure 2B. SO Pin Connections



Warning: NC = Not Connected

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1	0 to 70	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

Table 3. Device Select Code

	Device Code				Chip Enable			$\overline{RW}$
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	X	X	X	$R\overline{W}$

Note: The MSB b7 is sent first.
X = 0 or 1.

Figure 3. Transmit Only Mode Waveforms

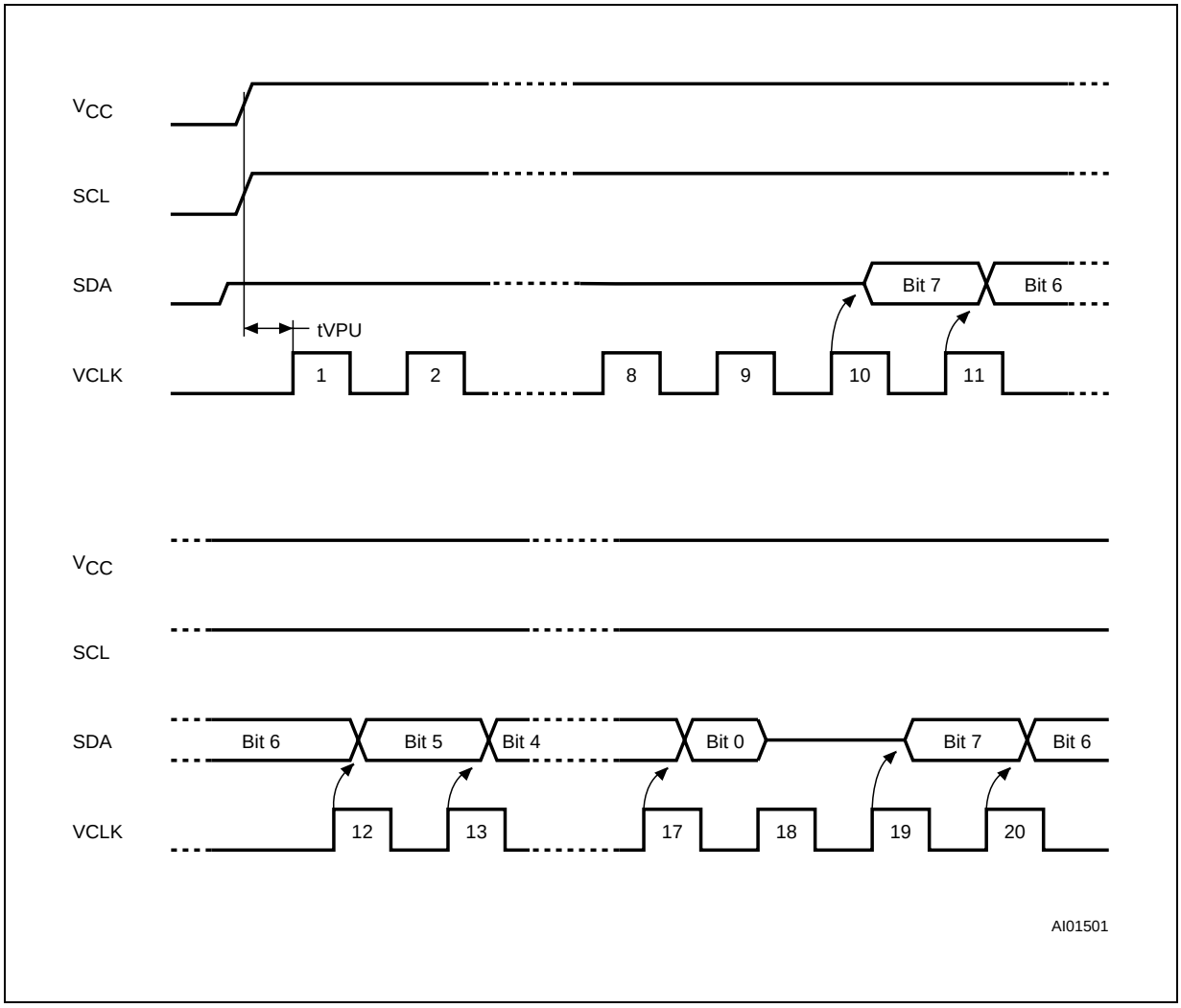
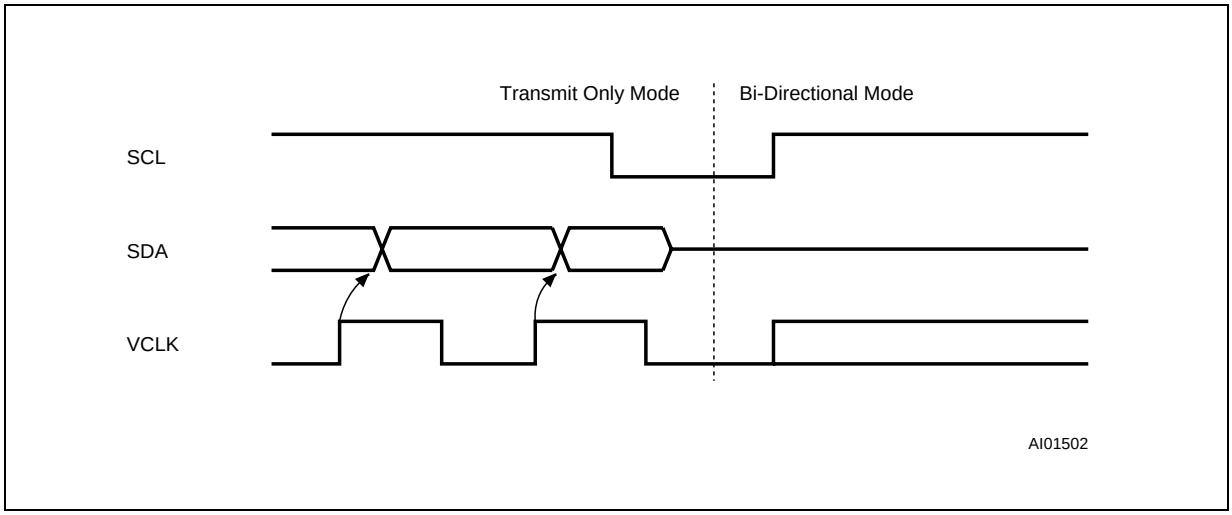


Table 4. Operating Modes

Mode	$\overline{RW}$ bit	VCLK	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, $R\overline{W}$ = '1'
Random Address Read	'0'	X	1	START, Device Select, $R\overline{W}$ = '0', Address,
	'1'	X		reSTART, Device Select, $R\overline{W}$ = '1'
Sequential Read	'1'	X	1 to 128	Similar to Current or Random Mode
Byte Write	'0'	V_{IH}	1	START, Device Select, $R\overline{W}$ = '0'
Page Write	'0'	V_{IH}	8	START, Device Select, $R\overline{W}$ = '0'

Note: X = V_{IH} or V_{IL}

Figure 4. Transition Mode Waveforms



Transmit Only Mode

After a Power-up, the device is in the Transmit Only mode. A proper initialization sequence must supply nine clock pulses on the VCLK pin (in order to internally synchronize the device). During this initialization sequence, the SDA pin is in high impedance. On the rising edge of the tenth pulse applied on VCLK pin, the device will output the first bit of byte located at address 00h (most significant bit first).

A byte is clocked out (on SDA pin) with nine clock pulses on VCLK: 8 clock pulses for the data byte and one extra clock pulse for a Don't Care bit.

As long as the SCL pin is held high, each byte of the memory array is transmitted serially on the SDA pin with an automatic address increment.

When the last byte is transmitted, the address counter will roll-over to location 00h.

I^2C Bidirectional Mode

The device can be switched from Transmit Only mode to I^2C Bidirectional mode by applying a valid high to low transition on the SCL pin (see Figure 4).

When the device is in the I2C Bidirectional mode, the VCLK input enables (or inhibits) the execution of any write instruction: if VCLK = 1, write instructions are executed; if VCLK = 0, write instructions are not executed.

The device is compatible with the I^2C standard, two wire serial interface which uses a bi-directional data bus and serial clock. The device carries a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition.

The device behaves as a slave device in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 7 bits (identification code 1010XXX), plus one read/write bit and terminated by an acknowledge bit.

When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Until the V_{CC} voltage has reached the POR threshold value, the internal reset is active, all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

SIGNAL DESCRIPTIONS

I²C Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 5).

Transmit Only Clock (VCLK). The VCLK input pin is used to synchronize data out when the ST24LC21 is in Transmit Only mode. The VCLK input offers also a Write Enable (active high) function when the ST24LC21 is in I²C bidirectional mode.

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 5).

DEVICE OPERATION

I²C Bus Background

The ST24LC21 supports the I²C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24LC21 are always slave devices in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24LC21 continuously monitor the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24LC21 and the bus master. A STOP condition at the end of a Read command forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successfull data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse period the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Figure 5. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I²C Bus

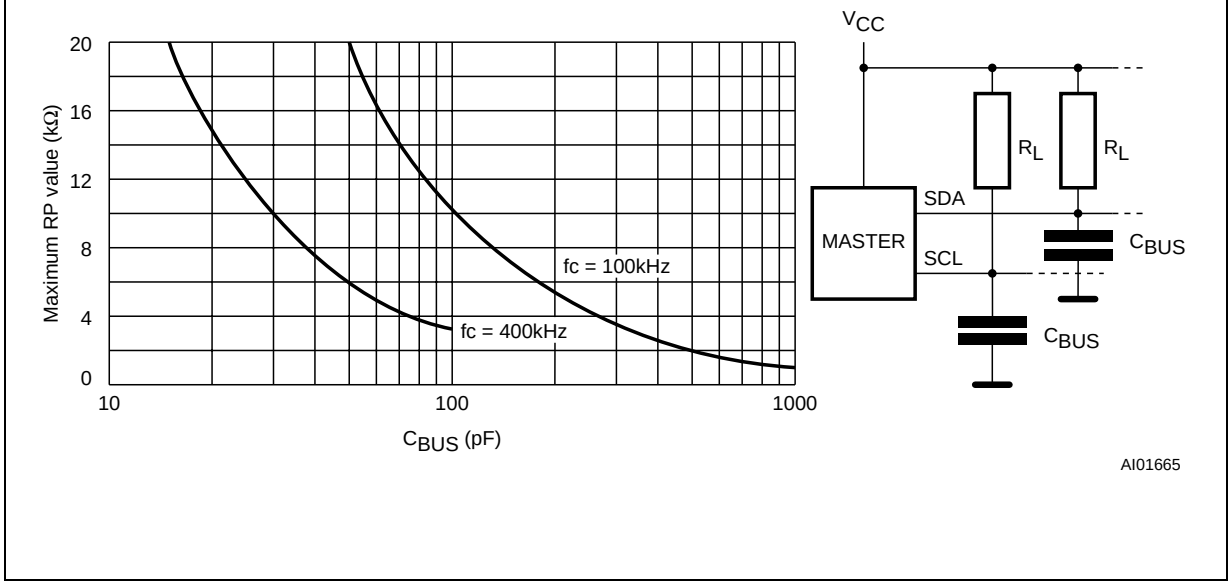


Table 5. Input Parameters (1) (T_A = 25 °C, f = 100 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
t_{LP}	Low-pass filter input time constant (SDA and SCL)			300	ns

Note: 1. Sampled only, not 100% tested.

Table 6. DC Characteristics
(T_A = 0 to 70 °C; V_{CC} = 2.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current	V_{CC} = 5V, f_C = 400kHz (Rise/Fall time < 10ns)		2	mA
	Supply Current	V_{CC} = 2.5V, f_C = 400kHz		1	mA
I_{CC1}	Supply Current (Standby)	V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5V		100	µA
		V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5V, f_C = 400kHz		300	µA
I_{CC2}	Supply Current (Standby)	V_{IN} = V_{SS} or V_{CC}, V_{CC} = 2.5V		5	µA
		V_{IN} = V_{SS} or V_{CC}, V_{CC} = 2.5V, f_C = 400kHz		50	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (VCLK)	$2.5V \le V_{CC} \le 4V$	–0.3	0.2 V_{CC}	V
		V_{CC} > 4V	–0.3	0.8	V
V_{IH}	Input High Voltage (VCLK)		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA		0.4	V
		I_{OL} = 6mA, V_{CC} = 5V		0.6	V

Table 7. AC Characteristics, I^2C Bidirectional Mode for Clock Frequency = 400kHz
(T_A = 0 to 70 °C; V_{CC} = 2.5V to 5.5V)

Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2} (1)	t_R	Clock Rise Time		300	ns
t_{CL1CL2} (1)	t_F	Clock Fall Time		300	ns
t_{DH1DH2} (1)	t_R	SDA Rise Time	20	300	ns
t_{DL1DL2} (1)	t_F	SDA Fall Time	20	300	ns
t_{CHDX} (2)	$t_{SU:STA}$	Clock High to Input Transition	600		ns
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		ns
t_{DLCL}	$t_{HD:STA}$	Input Low to Clock Low (START)	600		ns
t_{CLDX}	$t_{HD:DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1.3		µs
t_{DXCX}	$t_{SU:DAT}$	Input Transition to Clock Transition	100		ns
t_{CHDH}	$t_{SU:STO}$	Clock High to Input High (STOP)	600		ns
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	1.3		µs
t_{CLQV}	t_{AA}	Clock Low to Data Out Valid	200	900	ns
t_{CLQX}	t_{DH}	Clock Low to Data Out Transition	200		ns
f_C	f_{SCL}	Clock Frequency		400	kHz
t_W	t_{WR}	Write Time		10	ms

Notes: 1. Sampled only, not 100% tested.
2. For a reSTART condition, or following a write cycle.

Data Input. During data input the ST24LC21 sample the SDA bus signal on the rising edge of the clock SCL. Note that for correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Memory Addressing. To start communication between the bus master and the slave ST24LC21, the master must initiate a START condition. Following this, the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the device select code (7 bits) and a READ or WRITE bit. The 4 most significant bits of the device select code are the device type identifier, corresponding to the I^2C bus definition. For these memories the 4 bits are fixed as 1010b. The following 3 bits are Don't Care. The 8th bit sent is the read or write bit ($\overline{RW}$), this bit is set to '1' for read and '0' for write operations. If a match is found, the corresponding memory will acknowledge the identification on the SDA bus during the 9th bit time.

Write Operations

Following a START condition the master sends a device select code with the $\overline{RW}$ bit reset to '0'. The memory acknowledges this and waits for a byte address. After receipt of the byte address the device again responds with an acknowledge.

In I^2C bidirectional mode, any write command with VCLK = 0 will not modify data and will be acknowledged on data bytes, as shown in Figure 11.

Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the memory. The master then terminates the transfer by generating a STOP condition.

Page Write. The Page Write mode allows up to 8 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the most significant memory address bits are the same. The master sends from one up to 8 bytes of data, which are each acknowledged by the memory.

Table 8. AC Characteristics, I^2C Bidirectional Mode for Clock Frequency = 100kHz
(T_A = 0 to 70 °C; V_{CC} = 2.5V to 5.5V)

Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		1	µs
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		1	µs
t_{DL1DL1}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU:STA}$	Clock High to Input Transition	4.7		µs
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4		µs
t_{DLCL}	$t_{HD:STA}$	Input Low to Clock Low (START)	4		µs
t_{CLDX}	$t_{HD:DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{DXCX}	$t_{SU:DAT}$	Input Transition to Clock Transition	250		ns
t_{CHDH}	$t_{SU:STO}$	Clock High to Input High (STOP)	4.7		µs
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	4.7		µs
t_{CLQV} (2)	t_{AA}	Clock Low to Next Data Out Valid	0.3	3.5	µs
t_{CLQX}	t_{DH}	Data Out Hold Time	300		ns
f_C	f_{SCL}	Clock Frequency		100	kHz
t_W	t_{WR}	Write Time		10	ms

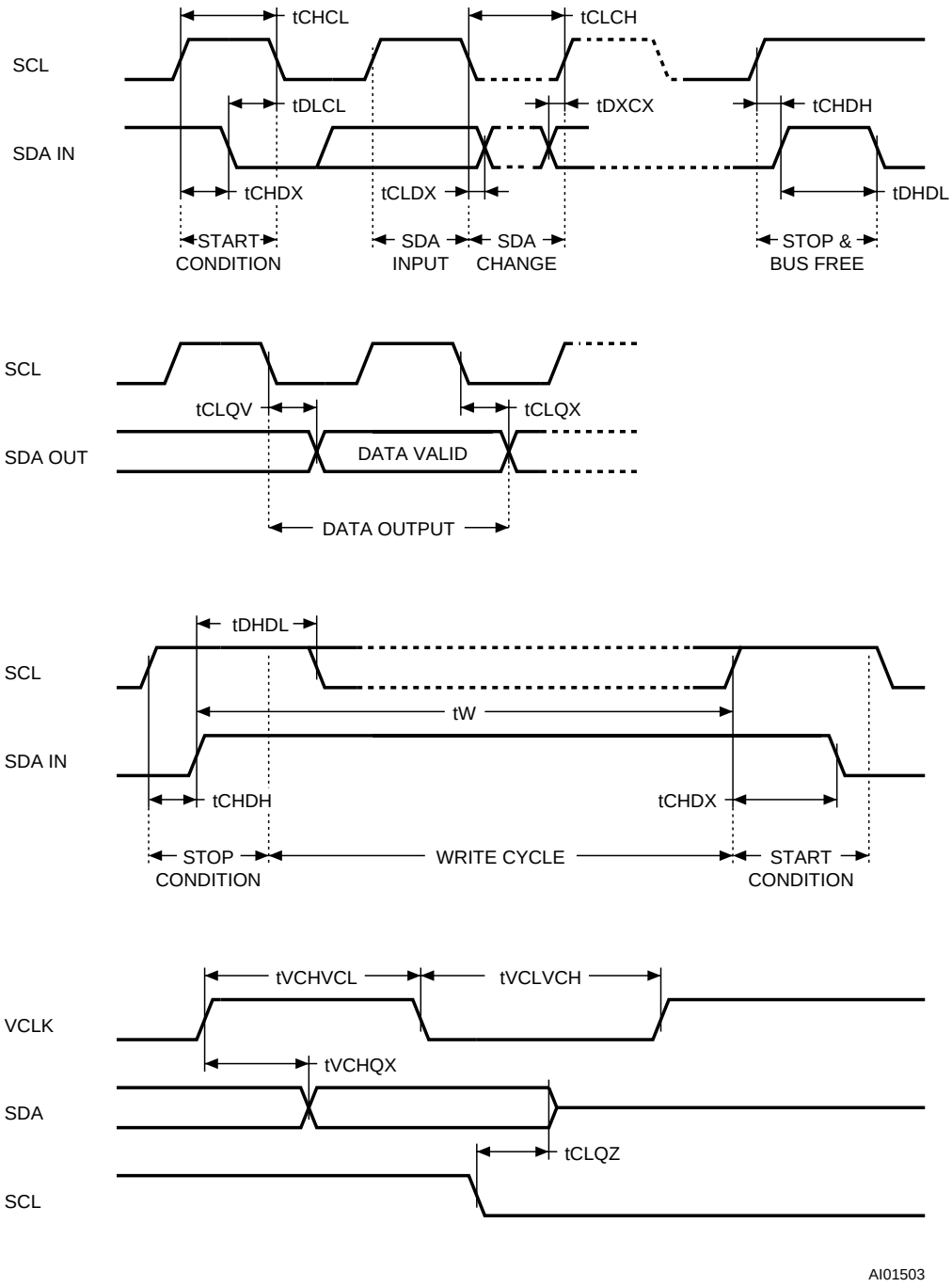
Notes: 1. For a reSTART condition, or following a write cycle.
2. The minimum value delays the falling/rising edge of SDA away from SCL = 1 in order to avoid unwanted START and/or STOP conditions.

Table 9. AC Characteristics, Transmit-only Mode
(T_A = 0 to 70 °C; V_{CC} = 2.5V to 5.5V)

Symbol	Alt	Parameter	Min	Max	Unit
t_{VCHQX}	t_{VAA}	Output Valid from VCLK		500	ns
t_{VCHVCL}	t_{VHIGH}	VCLK High Time	600		ns
t_{VCLVCH}	t_{VLOW}	VCLK Low Time	1.3		µs
t_{CLQZ}	t_{VHZ}	Mode Tansition Time		500	ns
t_{VPU} (1,2)		Transmit-only Power-up Time	0		ns
t_{VH1VH2} (2)	t_R	VCLK Rise Time		1	µs
t_{VL1VL2} (2)	t_F	VCLK Fall Time		1	µs

Notes: 1. Refer to Figure 3.
2. Sampled only, not 100% tested.

Figure 6. AC Waveforms



AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages SDA, SCL	$0.2V_{CC}$ to $0.8V_{CC}$
Input Pulse Voltages V_{CLK}	0.4V to 2V
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 7. AC Testing Input Output Waveforms

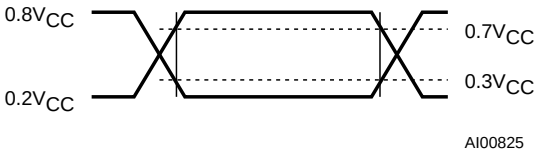


Figure 8. I²C Bus Protocol

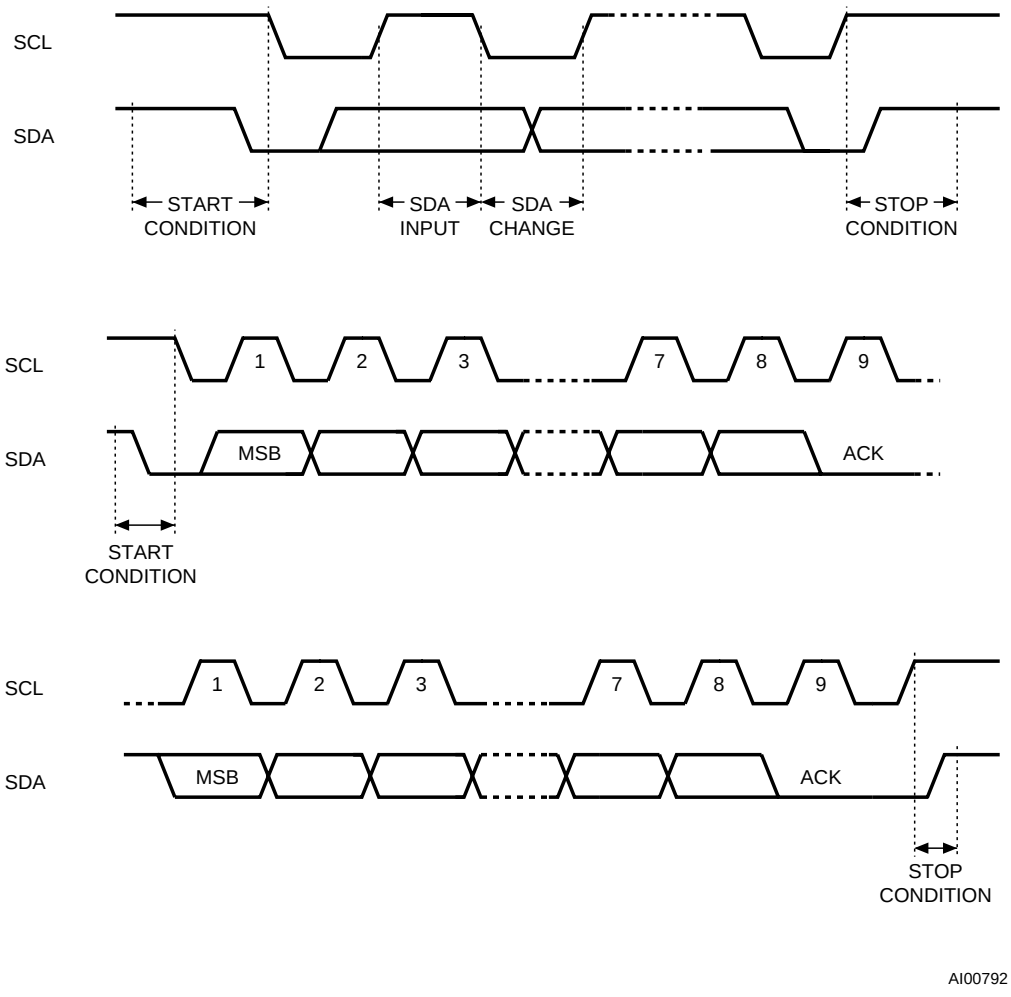
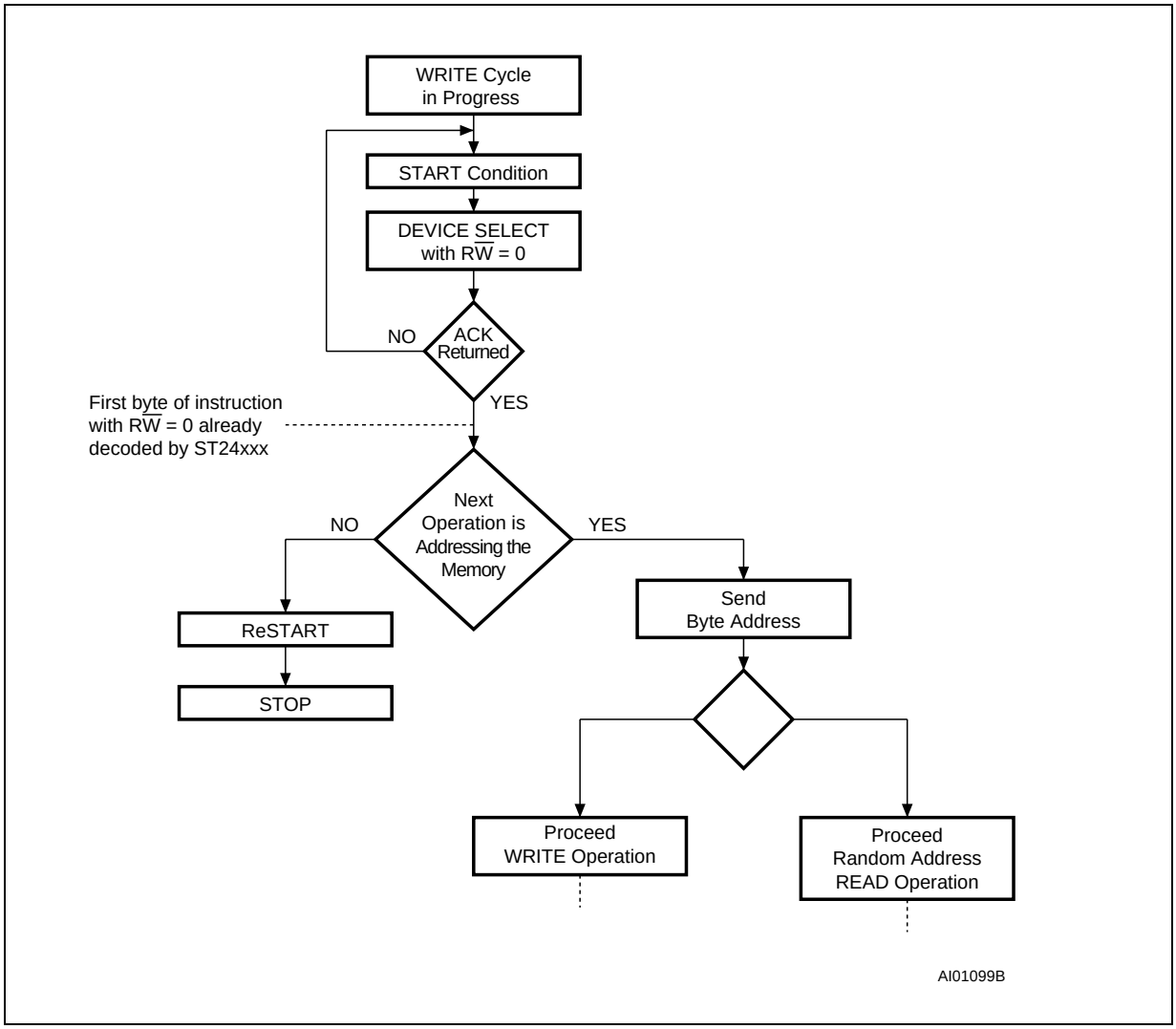


Figure 9. Write Cycle Polling using ACK



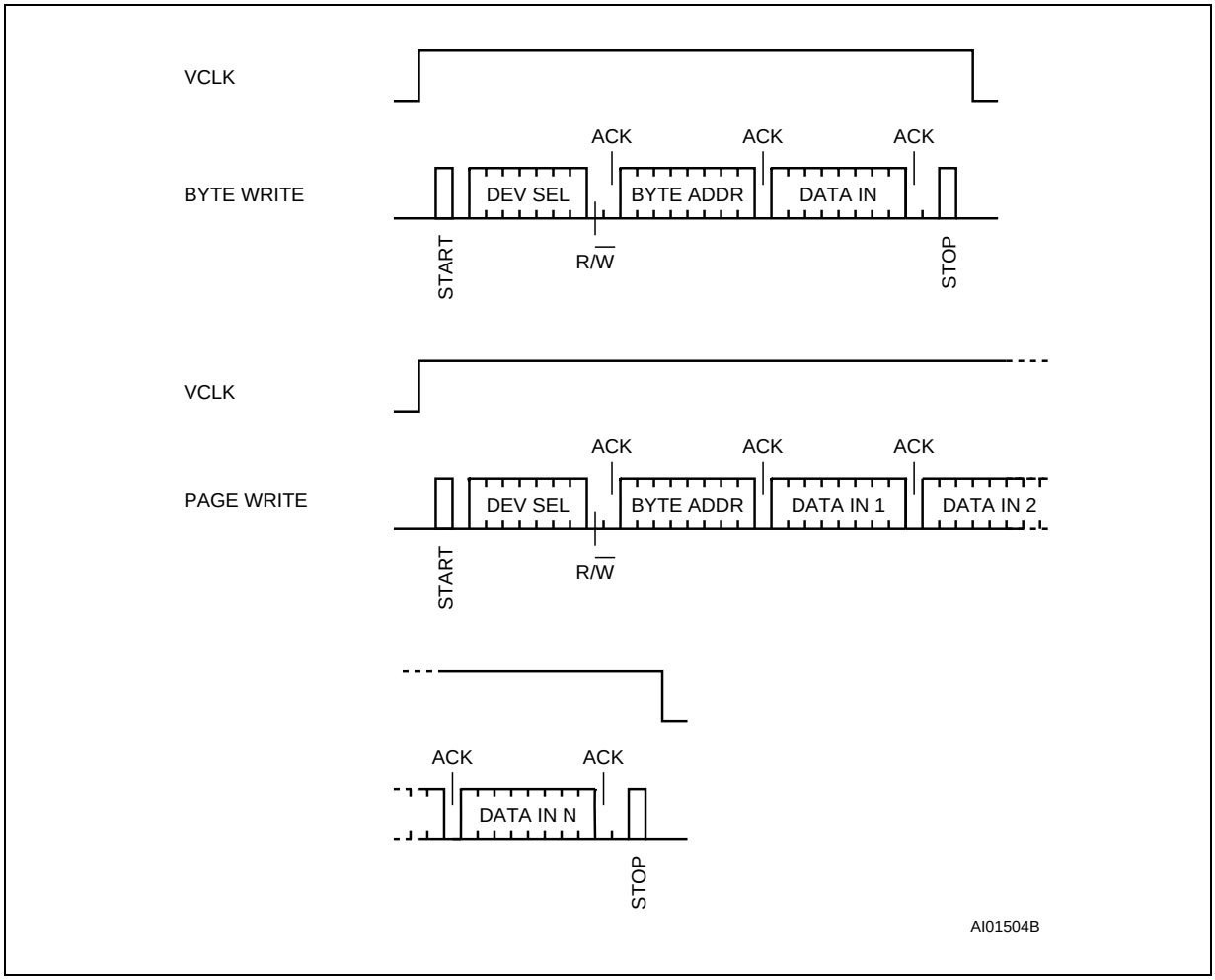
DEVICE OPERATIONS (cont'd)

After each byte is transfered, the internal byte address counter (3 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten. Note that, for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the memory will not respond to any request.

Minimizing System Delays by Polling On ACK. During the internal write cycle, the memory disconnects itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the write time (t_W) is given in the AC Characteristics table, since the typical time is shorter, the time seen by the system may be reduced by an ACK polling sequence issued by the master. The sequence is as follows:

– Initial condition: a Write is in progress (see Figure 9).
– Step 1: the Master issues a START condition followed by a Device Select byte (1st byte of the new instruction).
– Step 2: if the memory is busy with the internal write cycle, no ACK will be returned and the master goes back to Step 1. If the memory has terminated the internal write cycle, it will respond with an ACK, indicating that the memory is ready to receive the second part of the next instruction (the first byte of this instruction was already sent during Step 1).

Figure 10. Write Modes Sequence



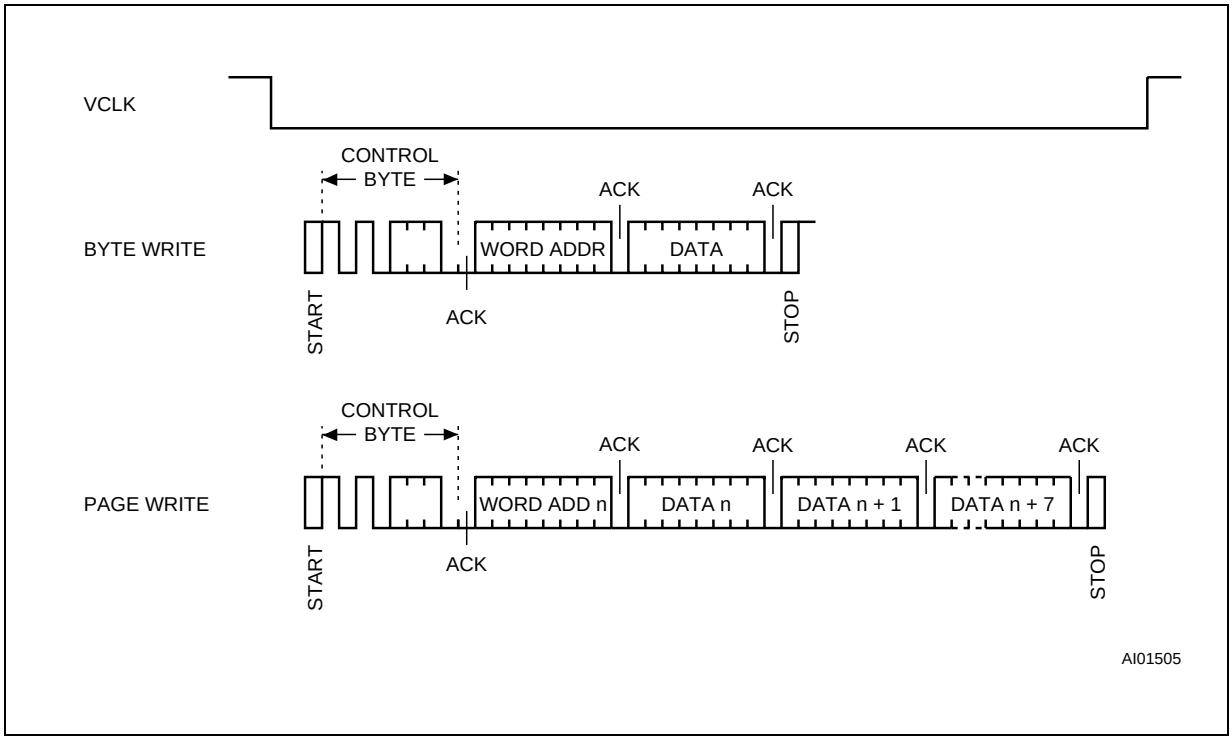
Read Operations

On delivery, the memory content is set at all "1's" (or FFh).

Current Address Read. The memory has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a memory address with the R$\overline{W}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the address into the address counter, see Figure 12. This is followed by another START condition from the master and the byte address is repeated with the R$\overline{W}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

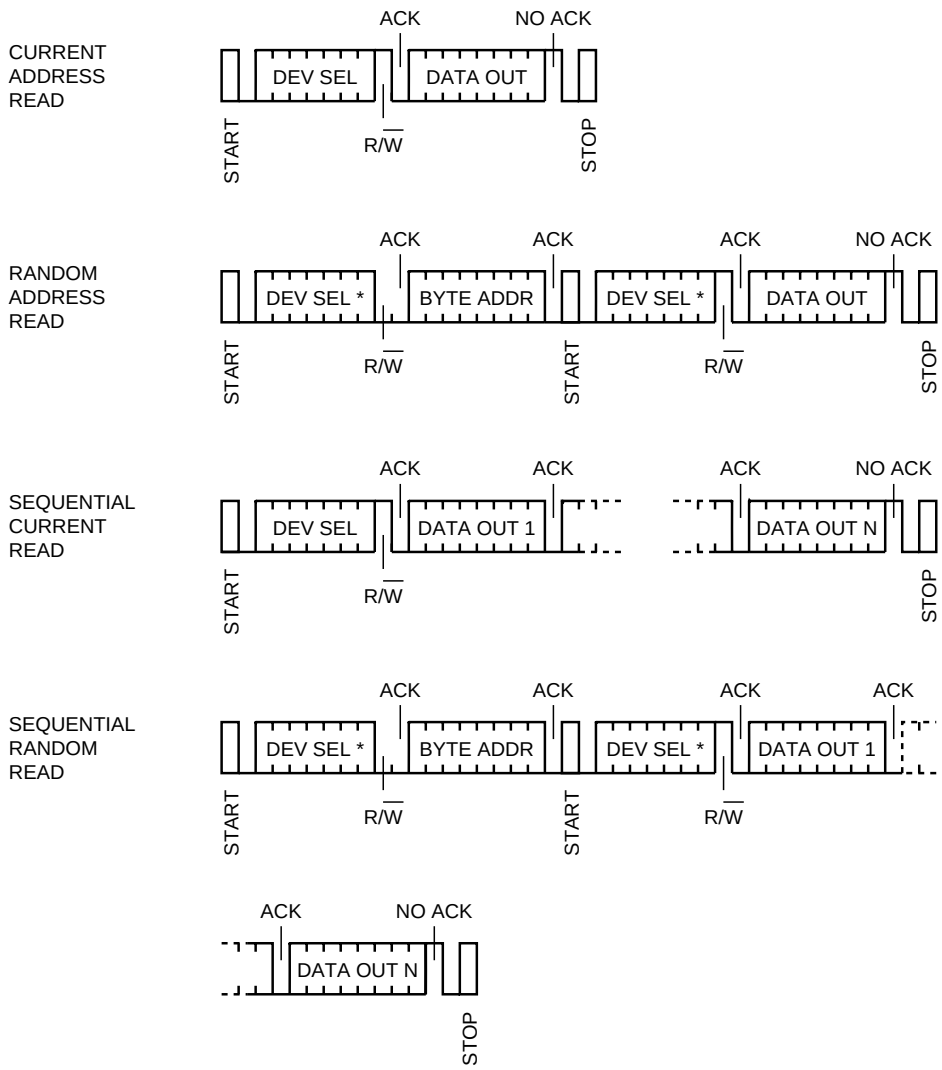
Figure 11. Inhibited Write when V_{CLK} = 0



Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte output, but MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll- over' and the memory will continue to output data.

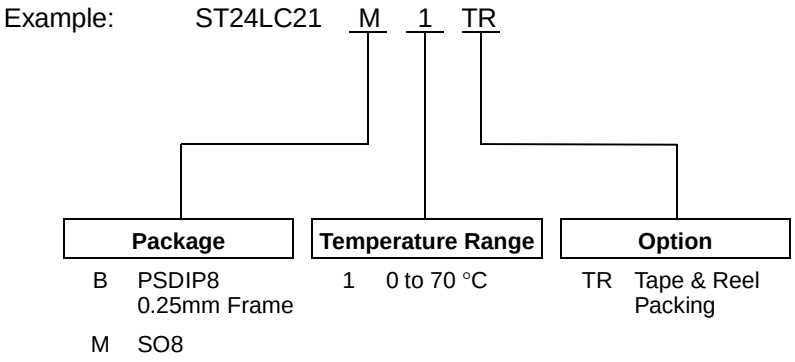
Acknowledge in Read Mode. In all read modes the ST24LC21 wait for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST24LC21 terminate the data transfer and switches to a standby state.

Figure 12. Read Modes Sequence



Note: * The 7 Most Significant bits of DEV SEL bytes of a Random Read (1st byte and 3rd byte) must be identical.

ORDERING INFORMATION SCHEME



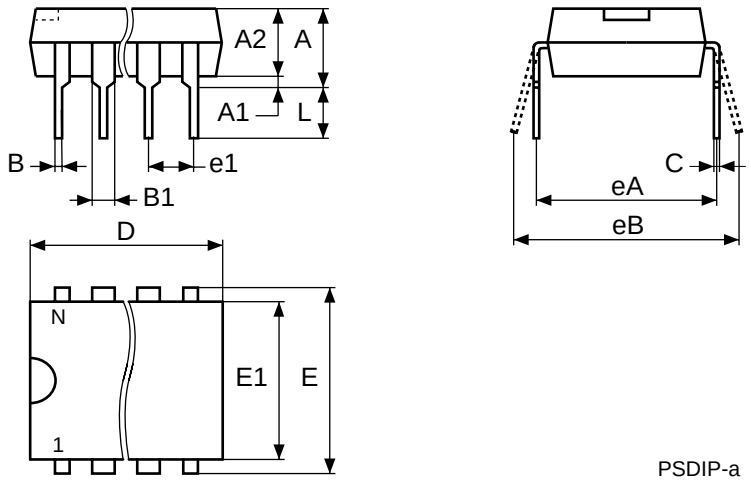
Devices are shipped from the factory with the memory content set at all "1's" (FFh).

For a list of available options (Package, etc...) or for further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		

PSDIP8



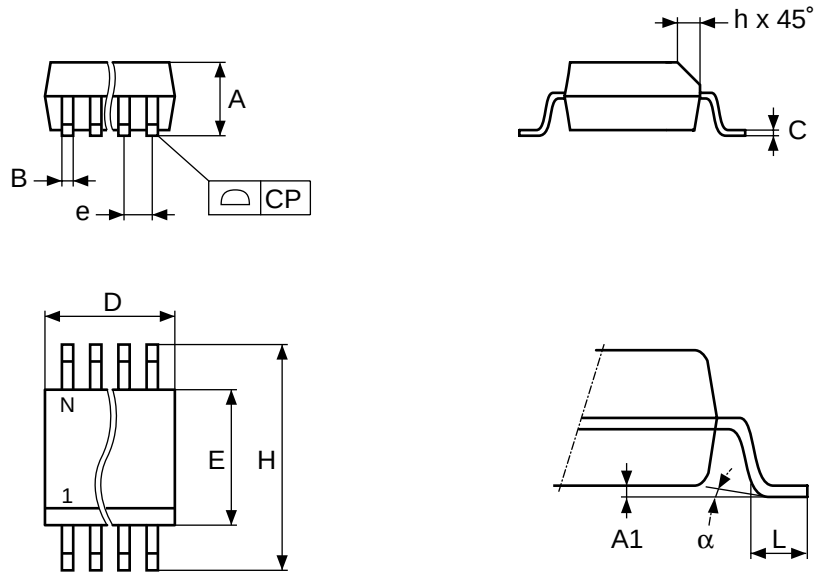
PSDIP-a

Drawing is not to scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

SO8



SO-a

Drawing is not to scale