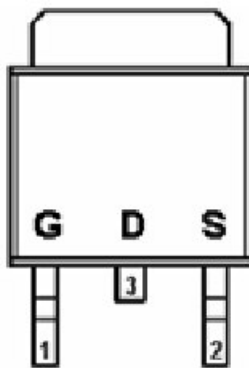


DESCRIPTION

ST25N10 is the N-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. The ST16N10 has been designed specially to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

PIN CONFIGURATION (D-PAK)

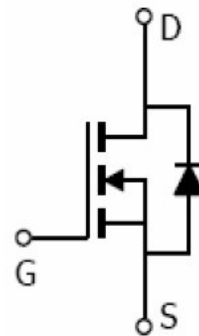
TO-252



FEATURE

- 100V/12.0A, $R_{DS(ON)} = 40m\Omega$ @ $V_{GS} = 10V$
100V/10.0A, $R_{DS(ON)} = 45m\Omega$ @ $V_{GS} = 4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- TO-252 package design

PART MARKING



Y: Year Code A: Week Code
P: Process Code X: Produces Code

**ST25N10**

N Channel Enhancement Mode MOSFET

25.0A

SOULTE MAXIMUM RATINGS (Ta = 25°C Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		VDSS	100	V
Gate-Source Voltage		VGSS	±20	V
Continuous Drain Current (TJ=150°C)	TA=25°C TA=100°C	ID	25.0 16.0	A
Pulsed Drain Current		IDM	75	A
Continuous Source Current (Diode Conduction)		IS	25	A
Power Dissipation	TA=25°C	PD	79	W
Operation Junction Temperature		TJ	150	°C
Storage Temperature Range		TSTG	-55/150	°C
Thermal Resistance-Junction to Ambient		RθJA	110	°C/W


ST25N10


N Channel Enhancement Mode MOSFET

25.0A

ELECTRICAL CHARACTERISTICS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =250mA	100			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250uA	2.0		4.0	V
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =80V, V _{GS} =0V			1	uA
		V _{DS} =80V, V _{GS} =0V T _J =85℃			100	
Drain-source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =12A V _{GS} =4.5V, I _D =10A		32 38	40 45	mΩ
Forward Transconductance	g _{fs}	V _{DS} =50V, I _D =9.0A		35		S
Diode Forward Voltage	V _{SD}	I _S =9.0A, V _{GS} =0V			1.2	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =50V, V _{GS} =10V I _D =12A		50		nC
Gate-Source Charge	Q _{gs}			13.5		
Gate-Drain Charge	Q _{gd}			11		
Input Capacitance	C _{iss}	V _{DS} =30V, V _{GS} =0V F=1MHz		2000		pF
Output Capacitance	C _{oss}			450		
Reverse TransferCapacitance	C _{rss}			260		
Turn-On Time	t _{d(on)} tr	V _{DD} =50V, R _D = 30Ω I _D =1.0A, V _{GEN} =10V R _G =6Ω		25		nS
Turn-Off Time	t _{d(off)} tf			18		
				60		
				78		

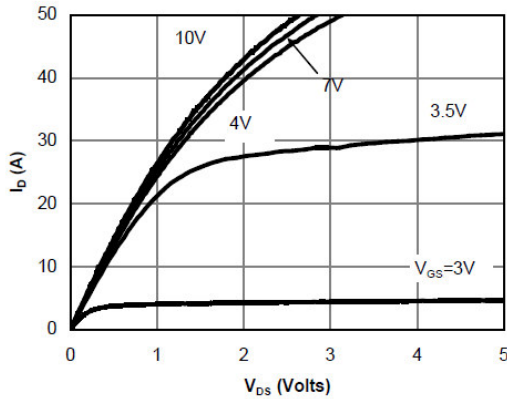
TYPICAL CHARACTERISTICS


Figure 1: On-Region Characteristics (Note E)

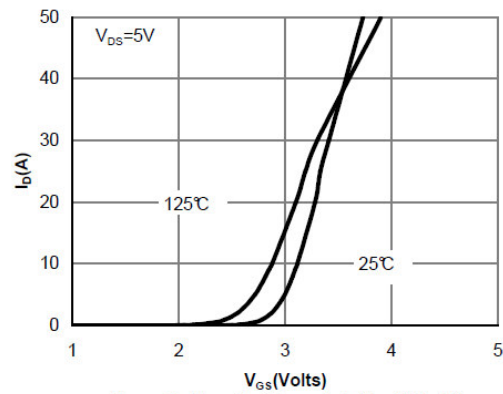


Figure 2: Transfer Characteristics (Note E)

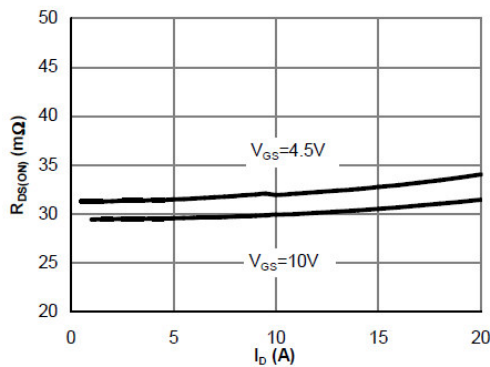


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

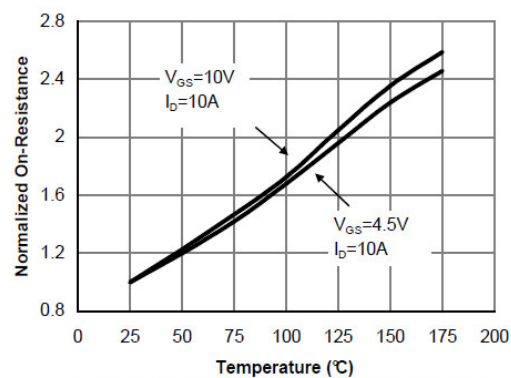


Figure 4: On-Resistance vs. Junction Temperature (Note E)

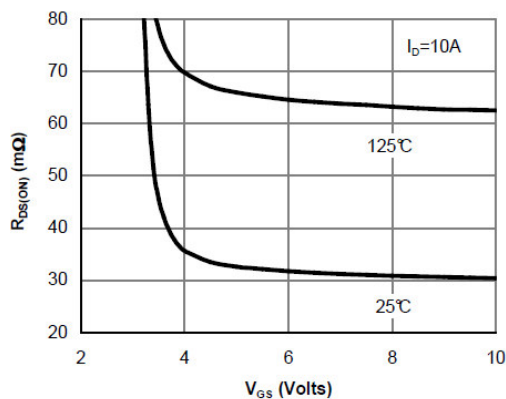


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

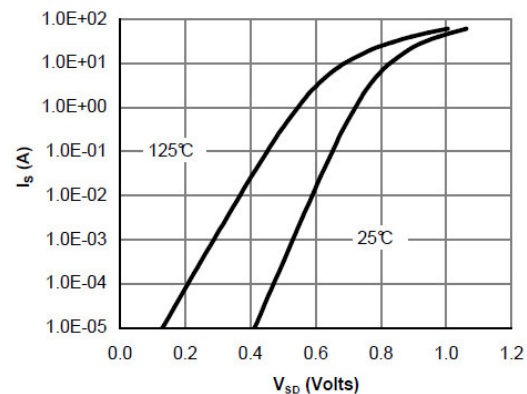


Figure 6: Body-Diode Characteristics (Note E)

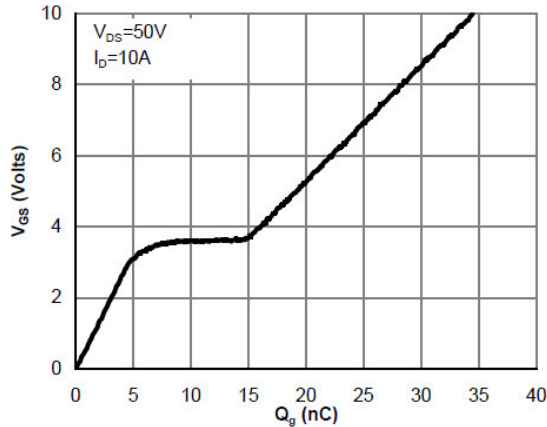


Figure 7: Gate-Charge Characteristics

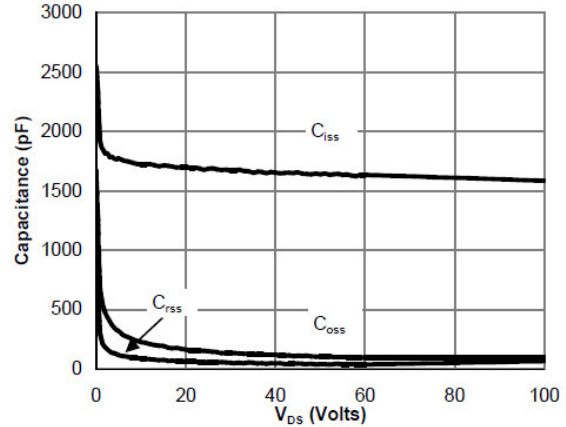


Figure 8: Capacitance Characteristics

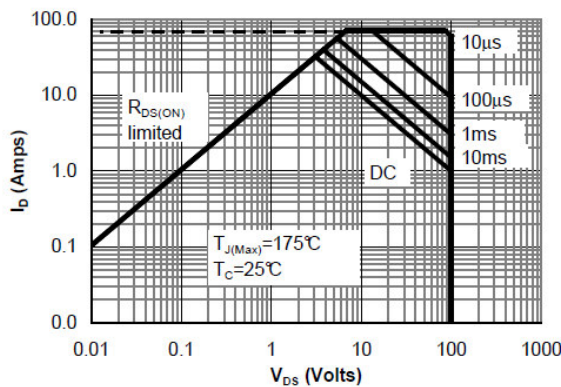


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

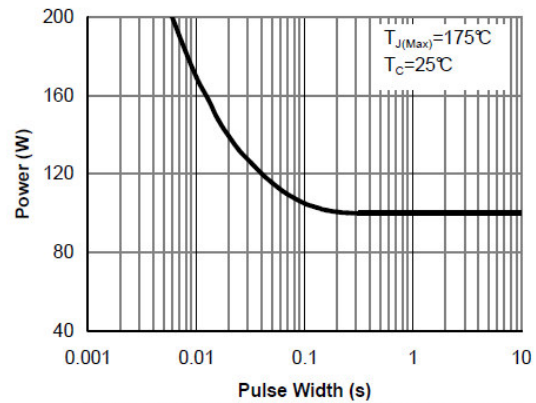


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

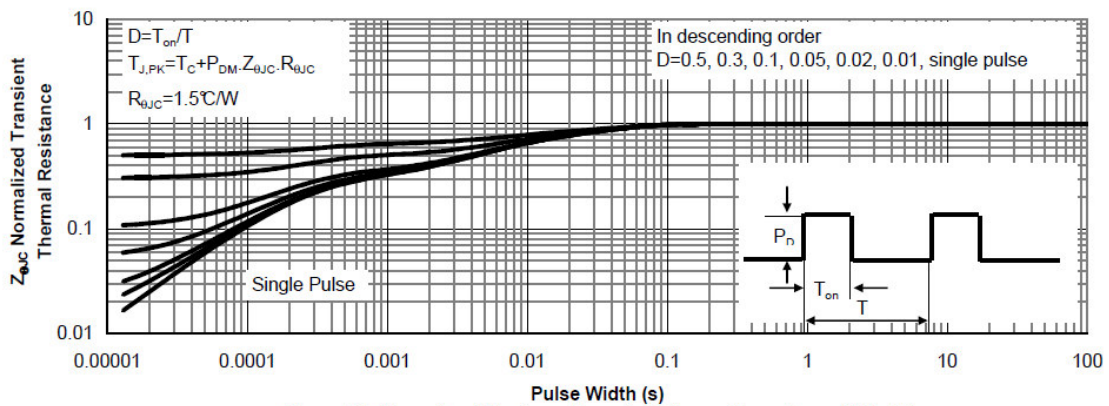
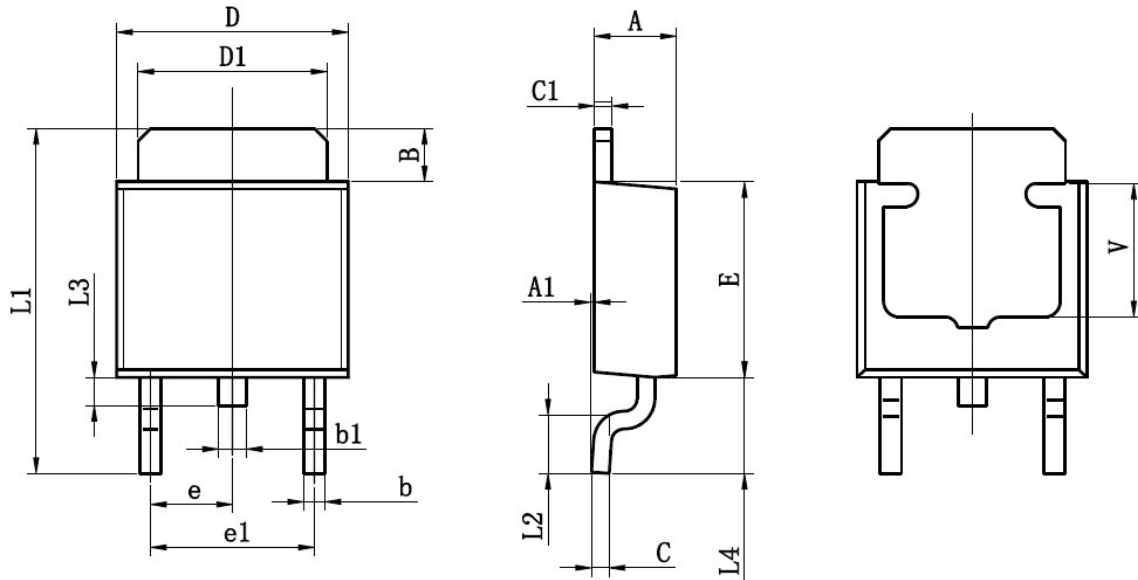


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TO-252-2L PACKAGE OUTLINE SOP-8P


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300TYP		0.091TYP	
e1	4.500	4.700	0.177	0.185
L1	9.500	9.900	0.374	0.390
L2	1.400	1.780	0.055	0.070
L3	0.650	0.950	0.026	0.037
L4	2.550	2.900	0.100	0.114
V	3.80REF		0.150REF	