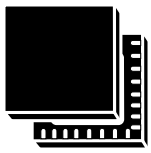
ST25R3916

High performance NFC universal device and EMVCo reader

Datasheet - production data



VFQFPN32 (5x5 mm)

Features

- Operating modes
  - Reader/writer
  - Card emulation
  - Active and passive peer to peer
- RF communication
  - NFC-A / ISO14443A up to 848 kbit/s
  - NFC-B / ISO14443B up to 848 kbit/s
  - NFC-F / Felica™ up to 424 kbit/s
  - NFC-V / ISO15693 up to 53 kb/s
  - NFC-A / ISO14443A and NFC-F / FeliCa™ card emulation
  - Active and passive peer to peer initiator and target modes, up to 424 kbit/s
  - Low level modes to implement MIFARE® Classic compliant or other custom protocols
- Hardware features
  - Dynamic power output (DPO) controls the field strength to stay within given limits
  - Active wave shaping (AWS) reduces over- and under-shoots
  - Noise suppression receiver (NSR) allows reception in noisy environment
  - Automatic antenna tuning (AAT) via variable capacitor
  - Integrated EMVCo compliant EMD handling
  - Automatic gain control and squelch feature to maximize SNR
  - Low power capacitive and inductive card detection
  - Low power NFC active and passive target modes
  - Adjustable ASK modulation depth, from 5 to 40%
  - Integrated regulators to boost system PSRR
  - AM/PM and I/Q demodulator with baseband channel summation or automatic channel selection
  - Possibility to drive two independent single ended antennas
  - Measurement of antenna voltage amplitude and phase, RSSI, on-chip supply and regulated voltages
- External communication interfaces
  - 512 byte FIFO
  - Serial peripheral interface (SPI) up to 10 Mbit/s
  - I2C with up to 400 kbit/s in Fast-mode, 1 Mbit/s in Fast-mode Plus, and 3.4 Mbit/s in High-speed mode
- Electrical characteristics
  - Wide supply voltage range, from 2.4 to 5.5 V
  - Wide peripheral communication supply range, from 1.65 to 5.5 V
  - Wide temperature range, from -40 to +125 °C
  - Quartz oscillator capable of operating with 27.12 MHz crystal with fast start-up

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1 Applications

The ST25R3916 is suitable for a wide range of NFC and HF RFID applications, among them

- NFC Forum compliant NFC universal device
- EMVCo compliant contactless payment terminal
- ISO14443 and ISO15693 compliant general purpose NFC device
- FeliCa™ reader / writer
- Supports of all five NFC Forum Tag types in reader mode
- Supports all common proprietary protocols, such as Kovio, CTS, B’

2 Description

The ST25R3916 is a high performance NFC universal device supporting NFC initiator, NFC target, NFC reader and NFC card emulation modes.

The ST25R3916 includes an advanced analog front end (AFE) and a highly integrated data framing system for ISO 18092 passive and active initiator, ISO 18092 passive and active target, NFC-A/B (ISO 14443A/B) reader including higher bit rates, NFC-F (FeliCa™) reader, NFC-V (ISO 15693) reader up to 53 kbps, NFC-A and NFC-F card emulation and NFC-A and NFC-F card emulation.

Special stream and transparent modes of the AFE and framing system can be used to implement other custom protocols such as MIFARE® Classic in reader or card emulation mode.

The ST25R3916 features high RF output power to directly drive antennas at high efficiency.

The ST25R3916 also includes several features, which make it incomparable for low power applications. It contains a low power capacitive sensor to detect the presence of a card without switching on the reader field. Additionally, the presence of a card can still be detected by performing a measurement of the amplitude or phase of the antenna signal. It also contains a low power RC oscillator and wake-up timer to automatically wake-up the ST25R3916 after a selected time period and check for a presence of a tag using one or more techniques of low power detection of card presence (capacitive, phase or amplitude).

The ST25R3916 is designed to operate from a wide power supply range (from 2.4 to 5.5 V), and a wide peripheral IO voltage range (from 1.65 to 5.5 V).

Due to this combination of high RF output power, low power modes, and wide supply range the ST25R3916 is perfectly suited for infrastructure NFC applications.

2.1 System diagram

Figure 1 and *Figure 2* show the minimum system configuration for, respectively, single ended and differential antenna configurations. Both include the EMC filter.

Figure 1. Minimum system configuration - Single sided antenna driving

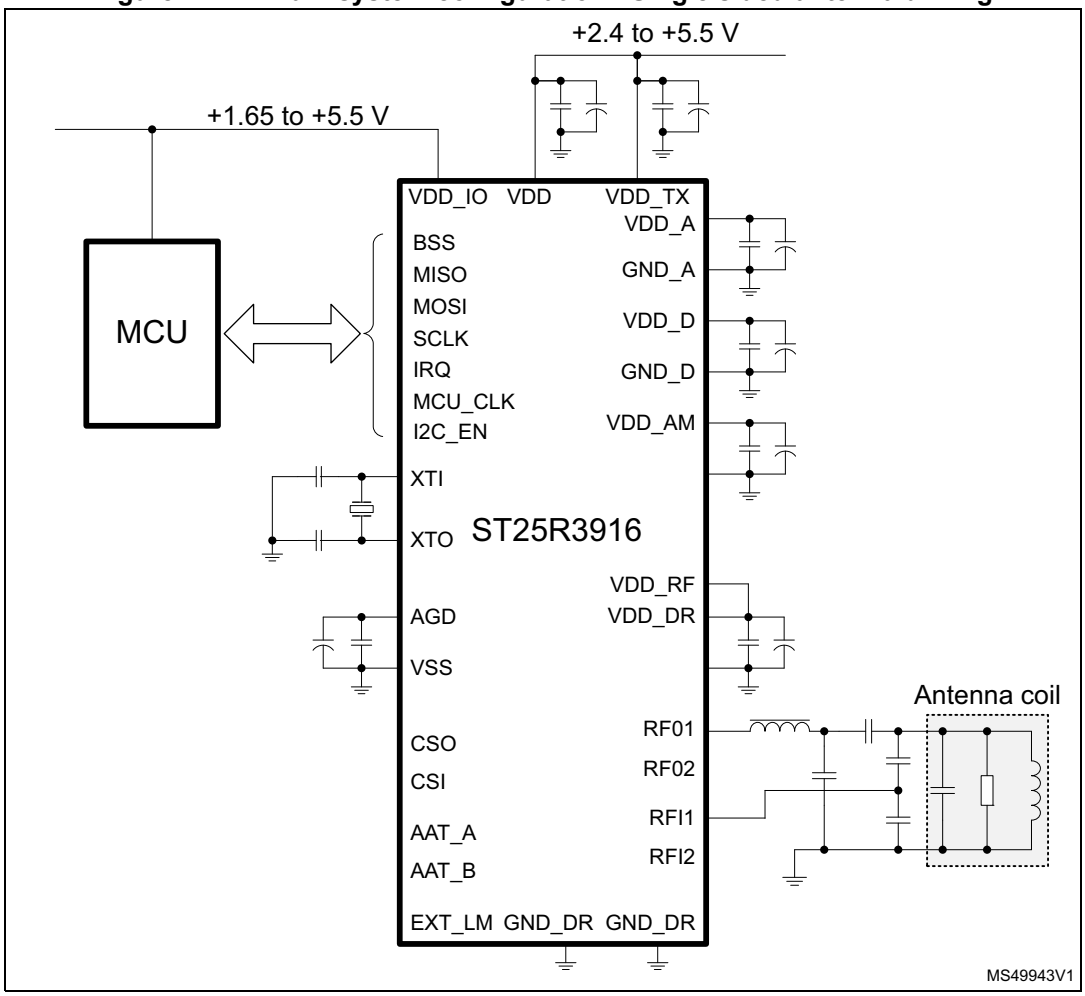
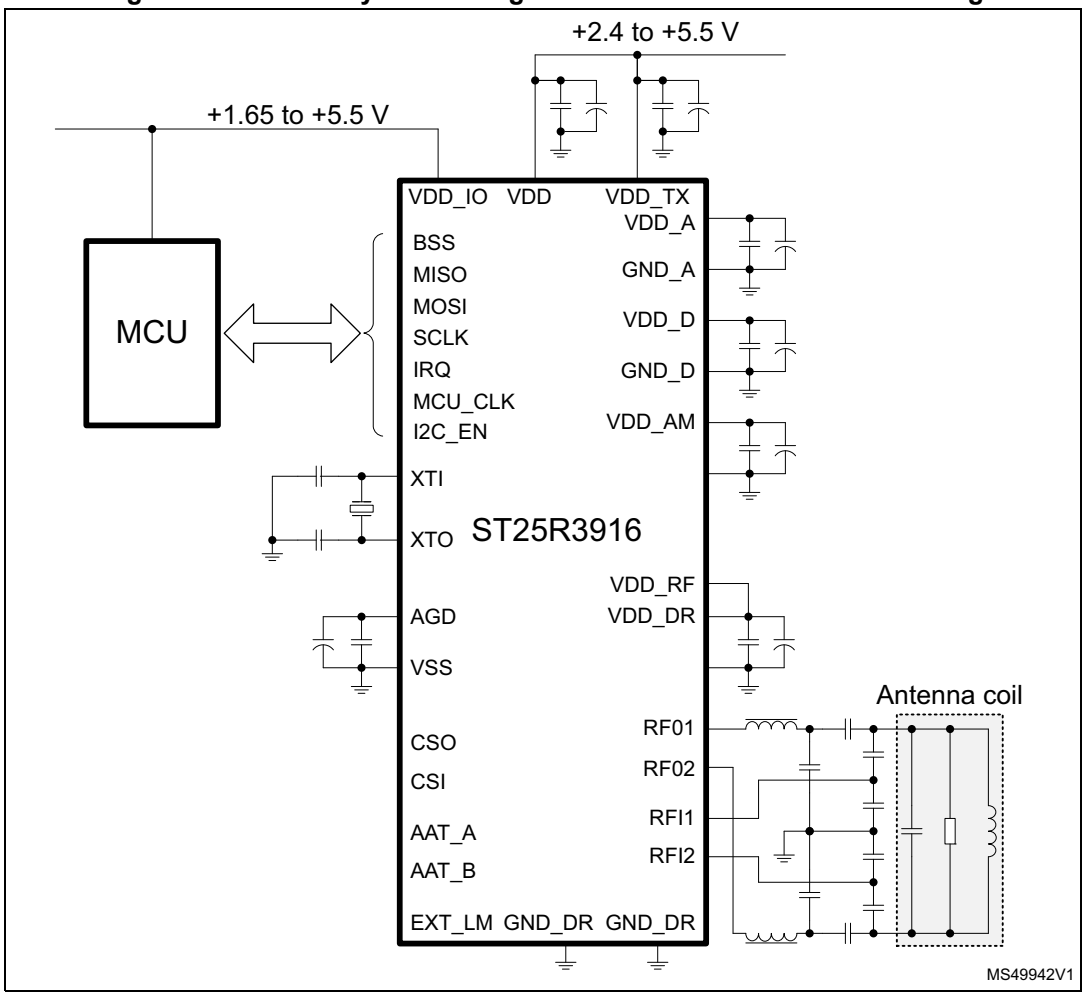


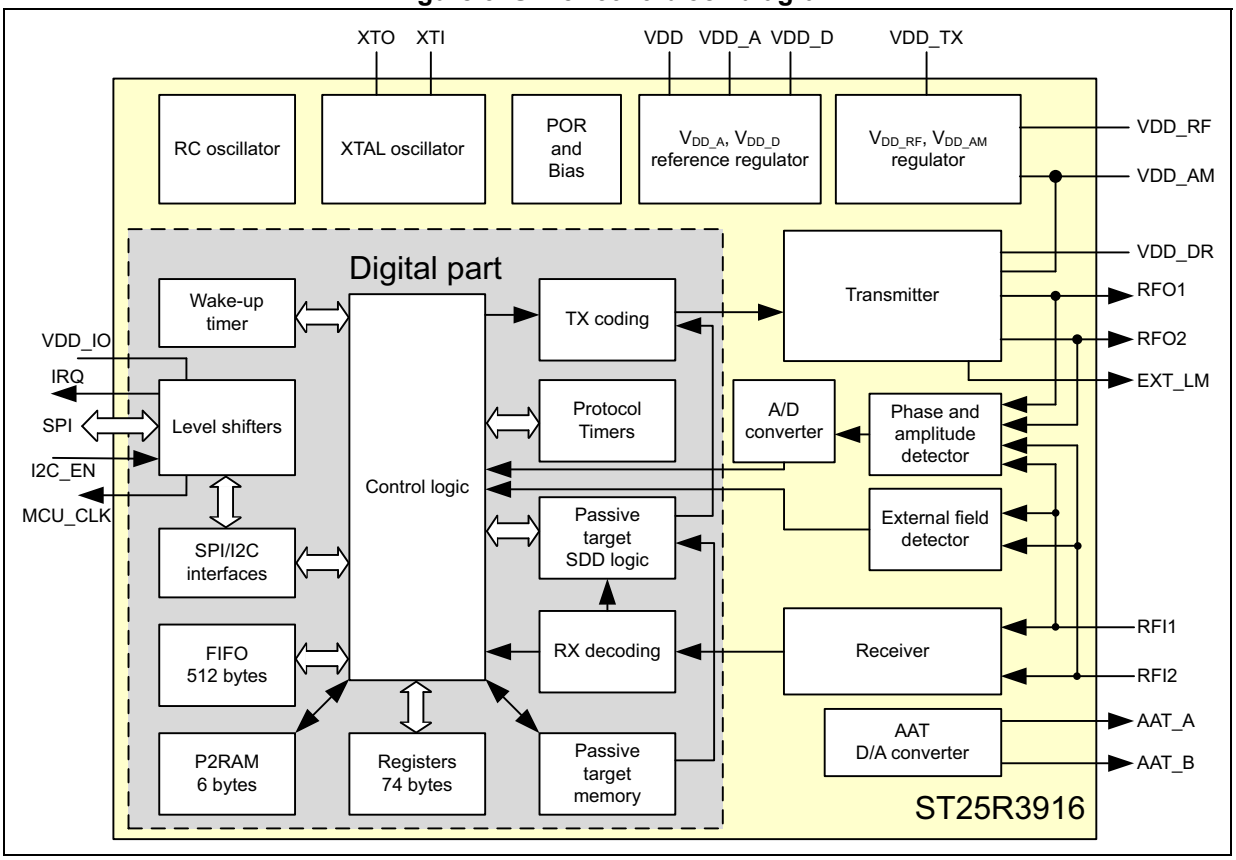
Figure 2. Minimum system configuration - Differential antenna driving



2.2 Block diagram

The ST25R3916 block diagram is shown in *Figure 3*, the main functions are described in the following subsections.

Figure 3. ST25R3916 block diagram



2.2.1 Transmitter

In reader mode the transmitter drives an external antenna through pins RFO1 and RFO2 to generate the RF field. Single sided and differential antenna configurations are supported. The transmitter block also generates the OOK or AM modulation of the transmitted RF signal.

The transmitter can either operate RFO1 and RFO2 independently to drive up to two antennas in single ended configuration or operate RFO1 and RFO2 combined to drive one antenna in differential configuration. The drivers are designed to directly drive antenna(s) integrated on the PCB as well as antennas connected with 50 Ω cables. Some of the advanced features of the ST25R3916 (such as antenna diagnostics) will not be fully usable if the antenna is connected with a 50 Ω cable.

In card emulation mode the transmitter generates the load modulation signal by changing the resistance of the internal antenna driver connected to the antenna via RFO1 and RFO2. Additionally, the transmitter can also drive an external MOS transistor via the EXT_LM pin to generate the load modulation signal.

2.2.2 Receiver

The receiver detects card modulation superimposed on the 13.56 MHz carrier signal. The receiver consists of two receive chains that are built from a set of demodulators, followed by two gain and filtering stages and a final digitizer stage. The demodulators can operate as AM/PM demodulator or as I/Q demodulator. The filter characteristics can be adjusted to match the selected RF mode and bit rate to optimize performance (subcarrier frequencies from 212 to 848 kHz are supported). Apart from the filter stage the receiver incorporates several other features (AGC, squelch) which enable reliable operation in noisy conditions.

The receiver is connected to the antenna via the pins RFI1 and RFI2. The output of the receiver is connected to the framing block that decodes the demodulated and digitized subcarrier signal.

2.2.3 Phase and amplitude detector

The phase detector measures the phase difference between the transmitter output signals (RFO1 and RFO2) and the receiver input signals (RFI1 and RFI2).

The amplitude detector measures the amplitude of the differential RF carrier signal between the receiver inputs RFI1 and RFI2. This differential amplitude signal is directly proportional to the amplitude of the RF signal on the antenna LC tank.

The phase- and amplitude detectors are used for several purposes:

- PM demodulation, by observing RFI1 and RFI2 phase variations (LF signal is fed to the receiver)
- Average phase difference between RFOx pins and RFIx pins, to check antenna tuning
- Measure amplitude of signal present on pins RFI1 and RFI2, proportional to the antenna voltage

2.2.4 Automatic antenna tuning (AAT)

The AAT block consists of two independent 8-bit D/A converters. These converters generate a programmable voltage (from 0 to 3.3 V) to control external variable capacitors.

Note: Using hardware based wake-up in combination with the automatic antenna tuning feature is not recommended. Contact your nearest ST office for further support.

2.2.5 A/D converter

The ST25R3916 features a built in A/D converter. Its input can be multiplexed from different sources and it is used for the diagnostic functions and the low power card detection. The result of the A/D conversion is stored in a register that can be read through the host interface.

2.2.6 Capacitive sensor

The capacitive sensor is used to implement low power detection of card presence. It measures the capacitance between two copper patches connected to the CSI and CSO pins. This capacitance changes with the presence of an object like a card, or a hand.

During calibration the reference capacitance (representing parasitic capacitance of the environment) is stored. In the capacitive low power card detection mode, the ST25R3916 periodically measures the capacitance and compares the measured value to the stored

reference value. If the measured capacitance differs from the stored reference value by more than a register defined threshold, then an interrupt is sent to the external controller.

2.2.7 External field detector

The External field detector is a low power block used in the active or passive target mode to detect the presence of an external RF field. It supports two different external field detection thresholds, namely Peer detection and Collision avoidance.

The Peer detection threshold is used in the active and passive peer to peer modes to detect when the peer device turns on its RF field.

The Collision avoidance threshold is used to detect the presence of an external RF field during the RF collision avoidance procedure.

2.2.8 Quartz crystal oscillator

The quartz crystal oscillator operates with 27.12 MHz crystals. At start-up the transconductance of the oscillator is increased to achieve a fast start-up. Since the start-up time varies with crystal type, temperature and other parameters, the oscillator amplitude is observed and an interrupt is sent when stable oscillator operation is reached.

The oscillator block also provides a clock signal to the external microcontroller (MCU_CLK), according to the settings in the *IO configuration register 1*.

2.2.9 Power supply regulators

The integrated power supply regulators ensures a high power supply rejection ratio (PSRR) for the complete reader system.

Three voltage regulators, one for the analog block, one for the digital block, and one for the RF output drivers, are available to decouple noise sources from the ST25R3916. A fourth voltage regulator generates the reference voltage for the analog receivers (AGDC, analog ground).

The RF output driver voltage regulator can be configured automatically by the ST25R3916 based on the systems power supply stability and RF output power (see *Section 4.2.10: Adjust Regulators* for more details).

2.2.10 POR and bias

This block provides bias currents and reference voltages to all other blocks. It also incorporates a Power on Reset (POR) circuit which provides a reset at power-up and at low supply levels.

2.2.11 RC oscillator and Wake-up timer

The ST25R3916 includes several possibilities for low power detection of a card presence (capacitive sensor, phase measurement, amplitude measurement). The RC oscillator and the register configurable Wake-Up timer are used to periodically trigger the card presence detection in the low power card detection modes.

Note: Using hardware based wake-up in combination with the automatic antenna tuning feature is not recommended. Contact your nearest ST office for further support.

2.2.12 TX coding

This block encodes the transmit frames according to the selected RF mode and bit rate. The SOF (start of frame), EOF (end of frame), CRC and parity bits are generated automatically. The data to transmit are taken from the FIFO.

In Stream mode the framing is bypassed. The FIFO data directly defines the modulation data sent to the transmitter.

In Transparent mode, the framing and FIFO are bypassed, and the MOSI pin directly drives the modulation of the transmitter.

2.2.13 RX decoding

This block decodes received frames according to the selected RF mode and bitrate. The SOF (start of frame), EOF (end of frame), CRC and parity bits are automatically checked and removed by this block. The received data is written to the FIFO.

In Stream mode the framing is bypassed. The digitized subcarrier signal is directly stored in the FIFO.

In Transparent mode, the framing and FIFO are bypassed, the digitized subcarrier signal is directly output on the MISO pin.

2.2.14 FIFO

The ST25R3916 contains a 512-byte FIFO. Depending on the direction of the data transfer, it contains either data which has been received or data which is to be transmitted.

In reader mode the ST25R3916 allows to transmit frames of up to 8191 bytes length and receive frames of arbitrary length. In card emulation mode the FIFO operates like a buffer and the overall length of a single transmit or receive frame is limited to 512 bytes.

2.2.15 Control logic

The control logic contains I/O registers that define the operation of device.

2.2.16 Host interface

A 4-wire Serial peripheral interface (SPI) and a 2-wire I2C interface are available to communicate with an external microcontroller. The pins for the SPI and the I2C interface are shared, and pin I2C_EN is used to select the active interface.

2.2.17 Passive target memory

The ST25R3916 contains a 48-byte RAM to store configuration data for the passive target and card emulation mode.

2.2.18 P2RAM

The P2RAM stores information on wafer number, die position, device subversion, and I2C address. The P2RAM is programmed during production.

3 Pin and signal description

Figure 4. ST25R3916 QFN32 pinout

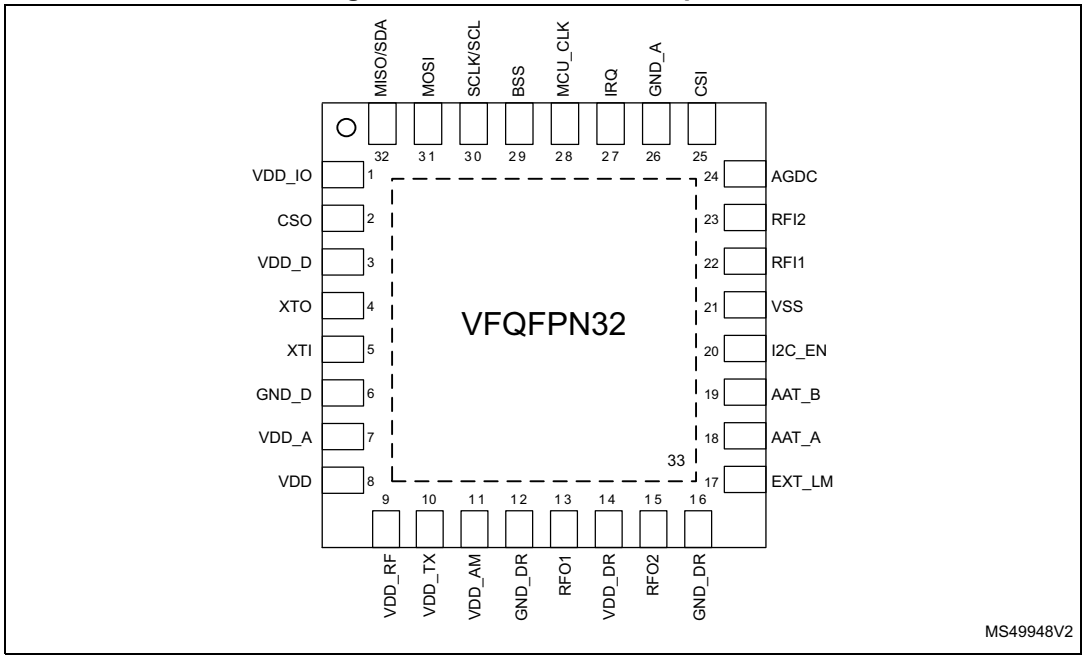


Table 1. VFQFPN32 pin assignment

VFQFPN32	Name	Type(1)	Description
1	VDD_IO	P	Positive supply for peripheral communication
2	CSO	AO	Capacitor sensor output / Analog/Digital test pin
3	VDD_D	AO	Digital supply regulator output
4	XTO	AO	X'tal oscillator output
5	XTI	AI/DI	X'tal oscillator input, in test mode used as digital input (clock)
6	GND_D	P	Digital ground
7	VDD_A	AO	Analog supply regulator output
8	VDD	P	External positive supply
9	VDD_RF	AO	Regulated driver supply for antenna drivers
10	VDD_TX	P	External positive supply for the TX part
11	VDD_AM	AO	Regulated driver supply for AM modulation
12	GND_DR	P	Antenna driver ground, including driver V_{SS}
13	RFO1	AO	Antenna driver output
14	VDD_DR	P	Antenna driver positive supply input
15	RFO2	AO	Antenna driver output
16	GND_DR	P	Antenna driver ground, including driver V_{SS}
17	EXT_LM	AO	External load modulation MOS gate driver

Table 1. VFQFPN32 pin assignment (continued)

VFQFPN32	Name	Type[1]	Description
18	AAT_A	AO	AAT tune voltage for variable capacitor AAT_A
19	AAT_B	AO	AAT tune voltage for variable capacitor AAT_B
20	I2C_EN	DI	I2C interface enable
21	VSS	P	Ground, die substrate potential
22	RFI1	AI	Receiver input
23	RFI2	AI	Receiver input
24	AGDC	AIO	Analog reference voltage
25	CSI	AIO	Capacitor sensor input / Analog/Digital Test pin
26	GND_A	P	Analog ground
27	IRQ	DO	Interrupt request output
28	MCU_CLK	DO	Clock output for MCU
29	BSS	DI	Serial peripheral interface enable (active low)
30	SCLK/SCL	DI	Serial peripheral interface clock / I2C clock
31	MOSI	DI	Serial peripheral interface data input
32	MISO/SDA	DO_T	Serial peripheral interface data output / I2C data line
33	NA	P	Thermal pad

1. P: Power supply pin
AIO: analog I/O, AI: analog input, AO: analog output
DI: digital input, DIPD: digital input with pull-down, DO: digital output, DO_T: digital output/tri-state, DIO: digital bidirectional.

4 Application information

4.1 Communication with an external microcontroller

The ST25R3916 communicates with a microcontroller either via an SPI interface or via an I2C interface. On both interfaces the ST25R3916 acts as a slave device and relies on the microcontroller to initiate all communication. To notify the microcontroller of completed commands or external events (e.g. peer device field on) the ST25R3916 signals an interrupt on the IRQ pin. Additionally, the ST25R3916 can provide a configurable clock signal to the microcontroller on the MCU_CLK pin.

4.1.1 Communication interface selection

The active communication interface is selected via the I2C_EN pin. If this pin is pulled to GND, the ST25R3916 operates in SPI mode. If this pin is pulled to V_{DD_D}, the ST25R3916 operates in I2C mode.

4.1.2 Serial peripheral interface (SPI)

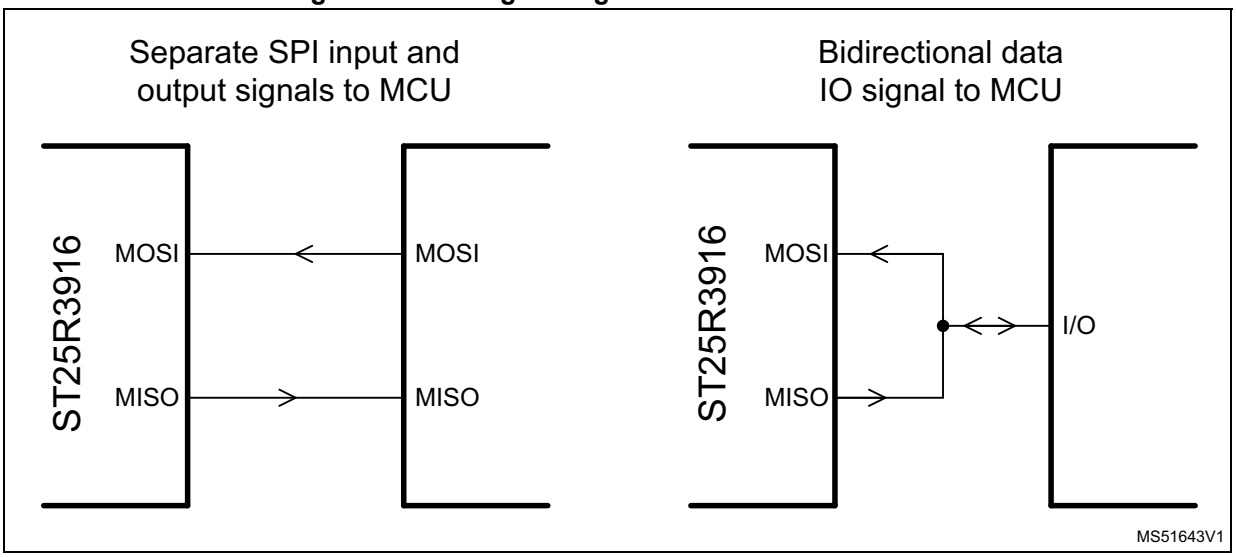
The ST25R3916 has a standard serial peripheral interface with clock polarity of 0, a clock phase of 1, and an active low slave select signal. Communication starts with the MCU pulling BSS low. The MOSI pin is samples on the falling edge of SCLK, and the state of the MISO pin is updated on the rising edge of the SCLK signal. Data is transferred byte-wise, most significant bit first. Read and Write commands support an address auto increment to reduce communication time. *Table 2* provides an overview of the SPI signals.

Table 2. Serial data interface (4-wire interface) signal lines

Name	Signal	Signal level	Description
I2C_EN	Digital input	CMOS	Pull to GND for SPI operation
BSS	Digital input with pull-up		Active low - Slave select
MOSI	Digital input		Master out - Slave in (MCU → ST25R3916)
MISO	Digital output with tristate		Master in - Slave out (ST25R3916 → MCU)
SCLK	Digital input		Serial clock
IRQ	Digital output		Active high - Interrupt output pin

The MISO output is in tristate as long as no output data is available. Due to this the MOSI and the MISO can be externally shorted to create a three-wire SPI. During the time the MISO output is in tristate, it is also possible to switch on a 10 kΩ pull down by activating option bits miso_pd1 and miso_pd2 in the *IO configuration register 2*.

Figure 5. Exchange of signals with a microcontroller



The first two bits of the first byte transmitted after the BSS high to low transition define the SPI operation mode. All Read and Write modes support address auto incrementing, which means that if, after the address and first data byte some additional data bytes are sent (or read), they are written to (or read from) addresses incremented by 1.

Table 3 shows available SPI operation modes. Register read and write operations are possible in all ST25R3916 operation mode. FIFO and PT_memory operations are possible in case en (bit 7 of the *Operation control register*) is set and the crystal oscillator is stable.

Some direct commands are accepted in all operation modes, others require en (bit 7 of the *Operation control register*) to be set and the crystal oscillator to be stable (see *Table 5*).

Table 3. SPI operation modes

Mode	Pattern (communication bits)								Related data
	Mode		Trailer						
	M1	M0	C5	C4	C3	C2	C1	C0	
Register Write	0	0	A5	A4	A3	A2	A1	A0	Data byte (or more bytes in case of auto-incrementing)
Register Read	0	1	A5	A4	A3	A2	A1	A0	
FIFO Load	1	0	0	0	0	0	0	0	One or more bytes of FIFO data
PT_memory load A-config	1	0	1	0	0	0	0	0	Passive target memory, locations from 0 on.
PT_memory load F-config	1	0	1	0	1	0	0	0	Passive target memory, locations from 15 on.
PT_memory load TSN data	1	0	1	0	1	1	0	0	Passive target memory, locations from 36 on. The additional address allows reload of the TSN random numbers without rewriting the whole PT_memory

Table 3. SPI operation modes (continued)

Mode	Pattern (communication bits)								Related data
	Mode		Trailer						
	M1	M0	C5	C4	C3	C2	C1	C0	
PT_memory Read	1	0	1	1	1	1	1	1	Passive target memory, locations from 0 on. A 0 byte is presented to the passive target memory to support reading at all SPI speeds.
FIFO Read	1	0	1	1	1	1	1	1	One or more bytes of FIFO data
Direct Command	1	1	C5	C4	C3	C2	C1	C0	-

Writing data to addressable registers (Write mode)

Figure 6 and *Figure 7* show cases of writing, respectively, a single byte and multiple bytes with auto-incrementing address. After the SPI operation mode bits, the address of register to be written is provided. Then one or more data bytes are transferred from the SPI, always MSB to LSB. The data byte is written in register on falling edge of its last clock. If the register on the defined address does not exist or it is a read only register no write is performed.

Figure 6. SPI communication: writing a single byte

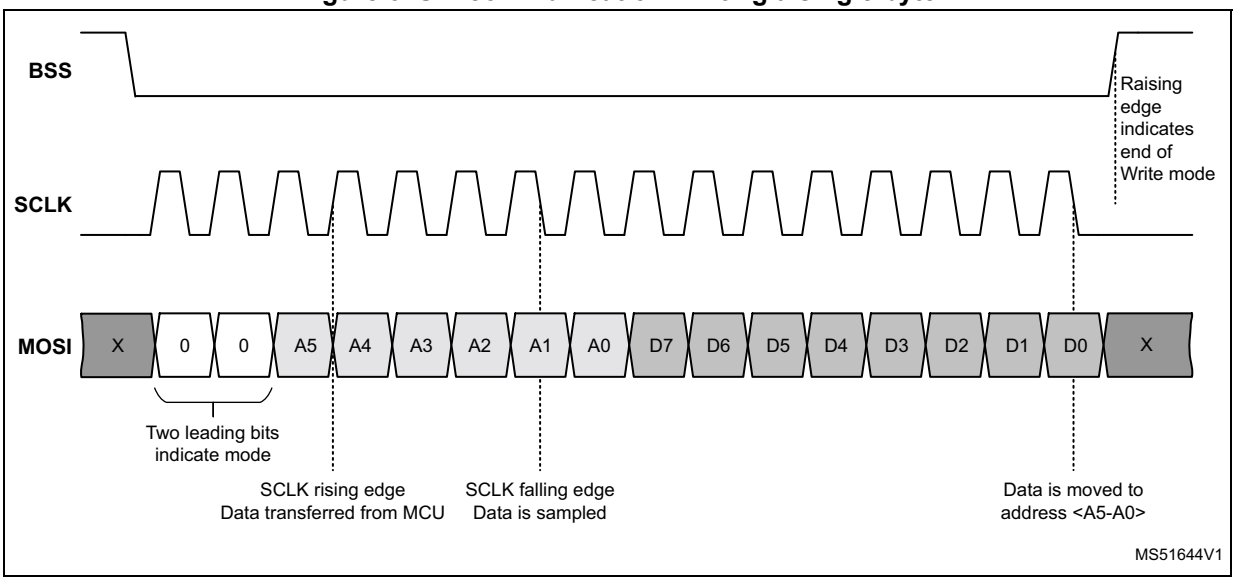
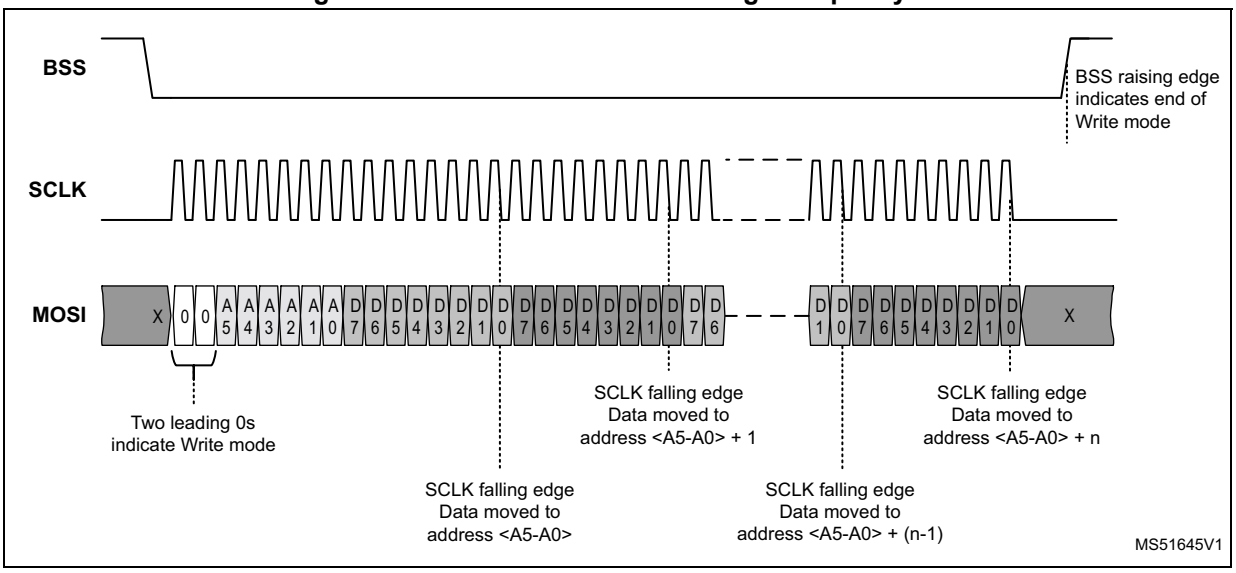


Figure 7. SPI communication: writing multiple bytes

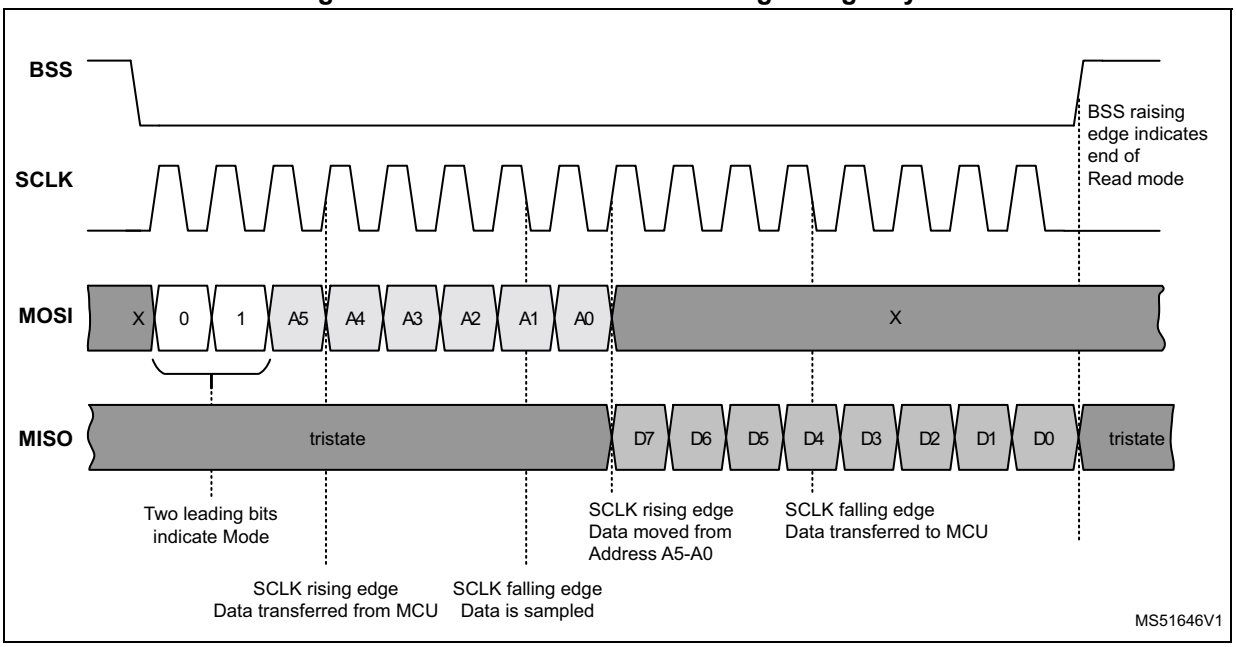


Reading data from addressable registers (Read register mode)

The SPI operation mode bits are followed by the address of the register to be read. Then one or more data bytes are transferred to MISO output (MSB first) for as long as SCLK is present. This mode also supports address auto-incrementing. If there is no register at a certain address, then all 0 data is sent to MISO.

Figure 8 is an example of reading a single byte.

Figure 8. SPI communication: reading a single byte



Read or write access to register space-B

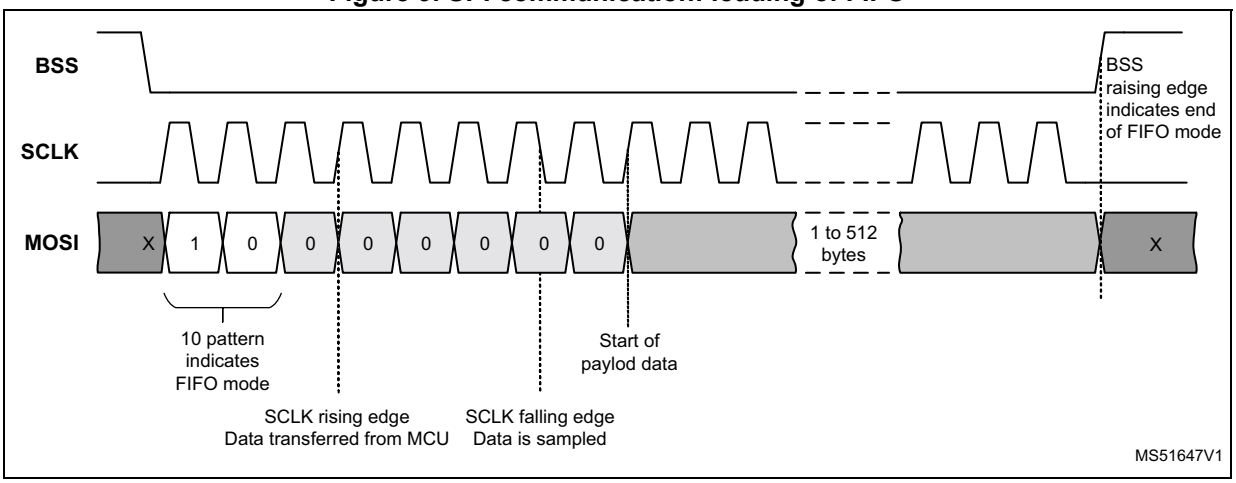
To access the register space-B the register read or write SPI sequence has to be prefixed with the byte FBh. Access to register space-B remains active until the rising edge of BSS.

Loading transmitting data into FIFO

Loading the transmitting data into the FIFO is similar to writing data into an addressable registers. The SPI sequence starts with SPI operation mode bits ‘10’ to indicate a FIFO operation followed by bits <C5:C0> set to 000000b. After the FIFO mode byte at least one and up to 512 data bytes must be sent.

Figure 9 shows how to load the transmitting data into the FIFO.

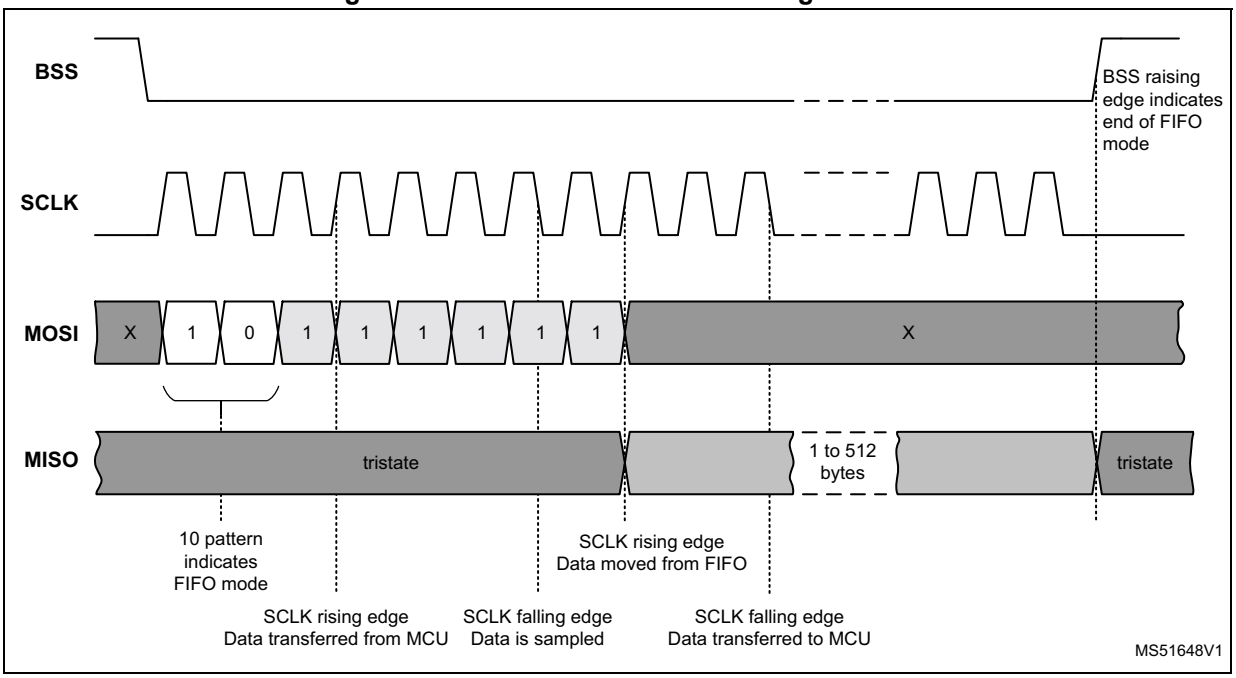
Figure 9. SPI communication: loading of FIFO



Reading received data from FIFO

Reading received data from the FIFO is similar to reading data from an addressable registers. The SPI sequence starts with SPI operation mode bits ‘10’ to indicate a FIFO operation followed by <C5:C0> set to 011111b. After the mode byte the ST25R3916 will output the data from the FIFO as long as SCLK is present and BSS is kept low.

Figure 10. SPI communication: reading of FIFO

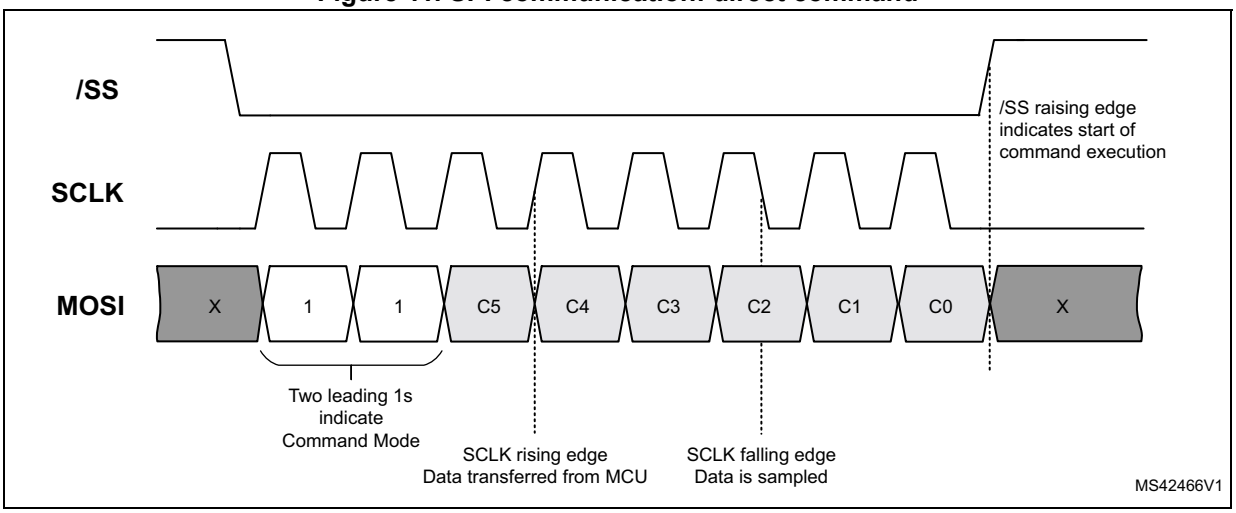


Direct Command mode

Direct Command mode has no arguments, so a single byte is sent. The byte starts with the SPI operation mode bits ‘11’ to indicate Direct Command Mode followed by the direct command code (see *Table 5*) in <C5:C0>, MSB first. Execution of the direct command starts with the rising edge of BSS (see *Figure 11*).

While the execution of some direct commands is immediate, there are others that start a process of certain duration (e.g. calibration, measurements). During the execution of such commands it is not allowed to start another activity over the SPI interface, an IRQ is sent. when the execution is terminated.

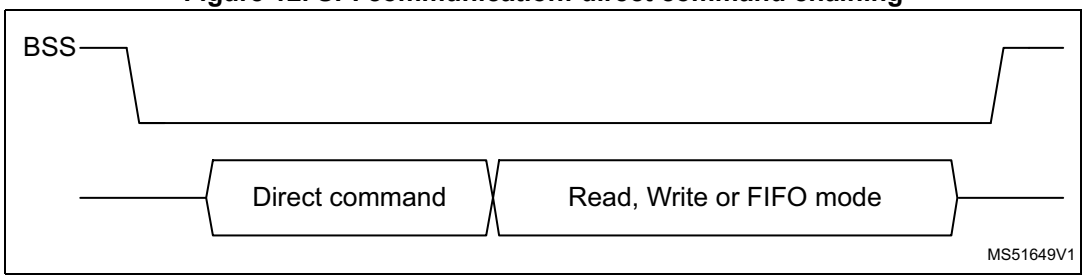
Figure 11. SPI communication: direct command



Direct command chaining

As shown in *Figure 12*, direct commands with immediate execution can be followed by another SPI mode (Read, Write or FIFO) without deactivating the BSS signal in between.

Figure 12. SPI communication: direct command chaining



Loading data in the PT_Memory (PT_Memory Load)

Loading data into the PT_Memory is similar to loading data into the FIFO. There are three mode patterns available to load data into three different parts of the PT_memory, as indicated in *Table 3*. The first byte following the mode/address pattern is stored in the location detailed in *Table 3*, for consecutive bytes the address is automatically incremented and data are stored to consecutive addresses.

The user must take care that the number of loaded bytes fits the size of the selected PT_memory area, not to overwrite data in the following PT_memory areas.

I2C interface

This interface supports:

- Standard-mode (100 kHz)
- Fast-mode (400 kHz)
- Fast-mode Plus (1 MHz)
- High speed mode (3.4 MHz).

Table 4 summarizes the I2C interface signals.

Table 4. I2C interface and interrupt signal lines

Name	Signal	Signal level	Description
I2C_EN	Digital input	CMOS	Pull to V_{DD} for I2C operation
MISO (SDA)	Digital output		I2C data line
SCLK (SCL)	Digital input		I2C clock
IRQ	Digital output		Active high - Interrupt output pin

Writing data to addressable registers (Register Write mode)

After the I2C slave address the address of the register to be written is sent using the same Register Write mode byte as for SPI register write access. The Register Write mode byte is then followed by one or more data bytes. If more than one data byte is sent, the data is stored in subsequent registers starting form the initial register address by incrementing the target address by one for each new data byte.

Figure 13 and *Figure 14* show, respectively, how to write a single byte into a register and how to write multiple bytes into subsequent registers using address auto-incrementing.

Figure 13. Writing a single register

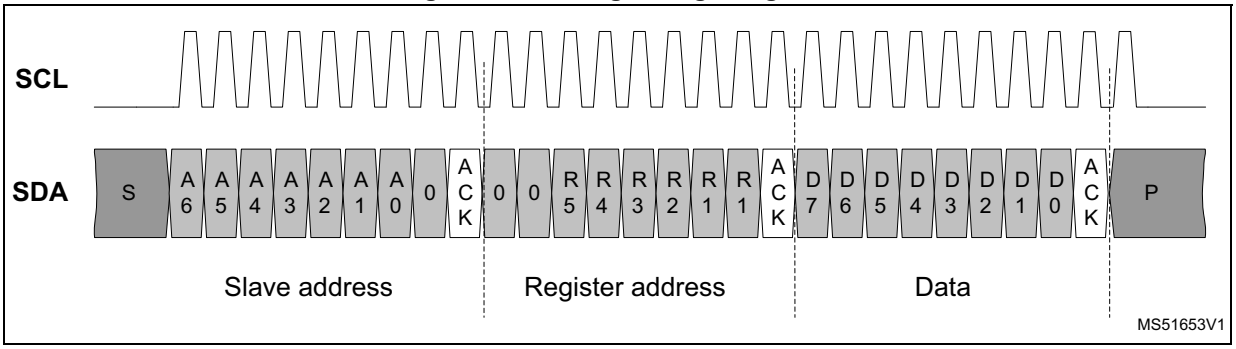
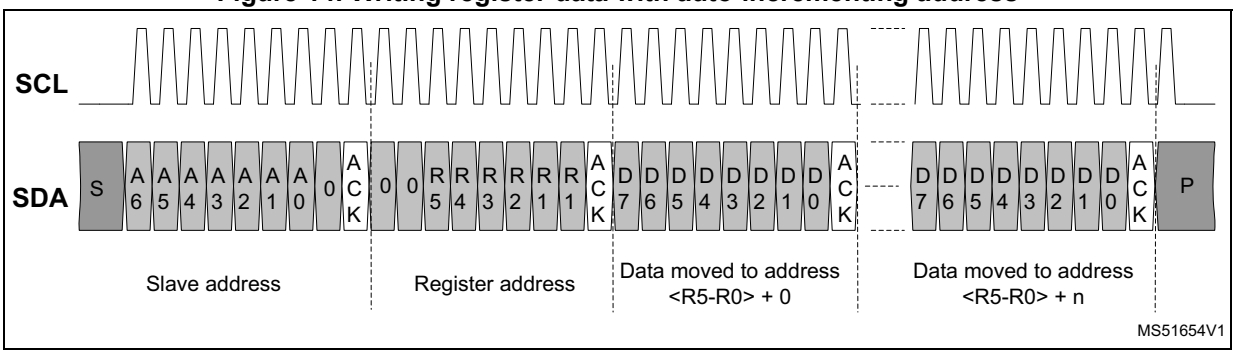


Figure 14. Writing register data with auto-incrementing address

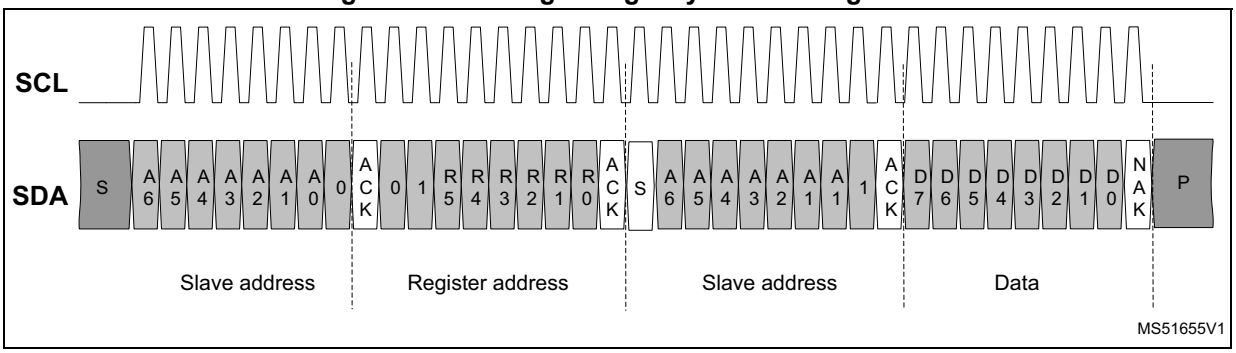


Reading data from addressable registers (Register Read mode)

After the I2C slave address the address of the register to be read is sent using the same Register Read mode byte of the SPI register read access. After the Register Read mode byte the ST25R3916 sends data bytes to the SDA output as long as the MCU keeps SCL. The Register Read mode also supports address auto-incrementing. If the addressed register does not exist, all 0 data is sent to SDA.

Figure 15 shows how to read a single byte from a register.

Figure 15. Reading a single byte from a register

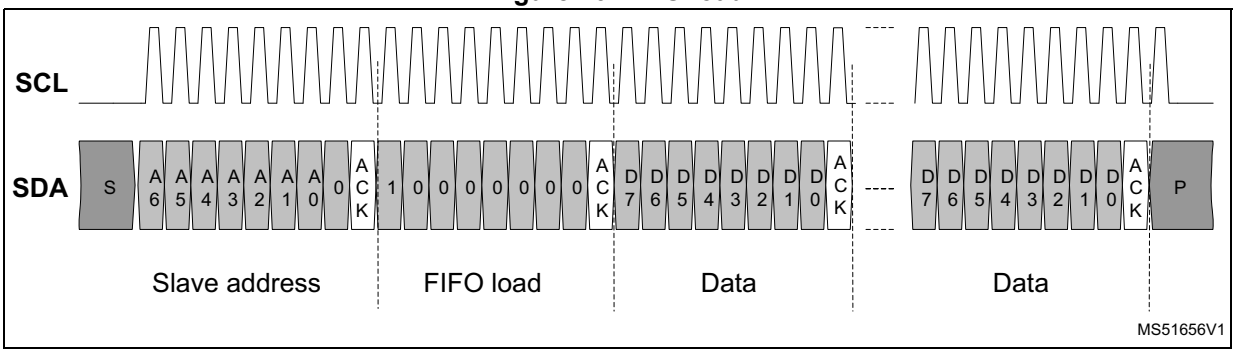


Loading data into FIFO or PT_Memory (FIFO/T_Memory load)

Loading data into FIFO or PT_Memory is similar to writing data into addressable registers. After the I2C slave address the mode byte to trigger a load of the FIFO or selected PT_Memory area is sent (see *Table 3*) followed by the data bytes to be loaded.

Figure 16 shows how to load data into the FIFO.

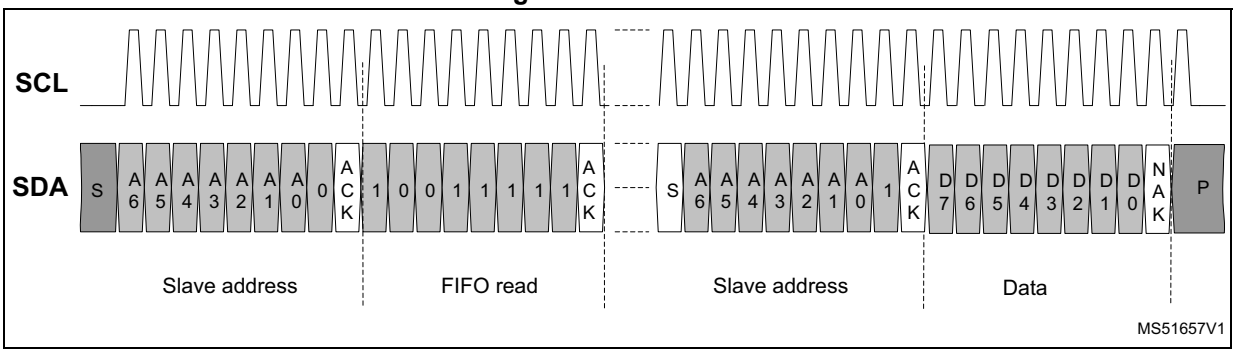
Figure 16. FIFO load



Reading data from the FIFO

Reading data from the FIFO is similar to reading data from addressable registers. After the I2C slave address the mode byte to trigger a read of the FIFO is sent. After receiving the FIFO read mode byte the ST25R3916 sends data bytes from the FIFO for as long as the MCU keeps reading the bus.

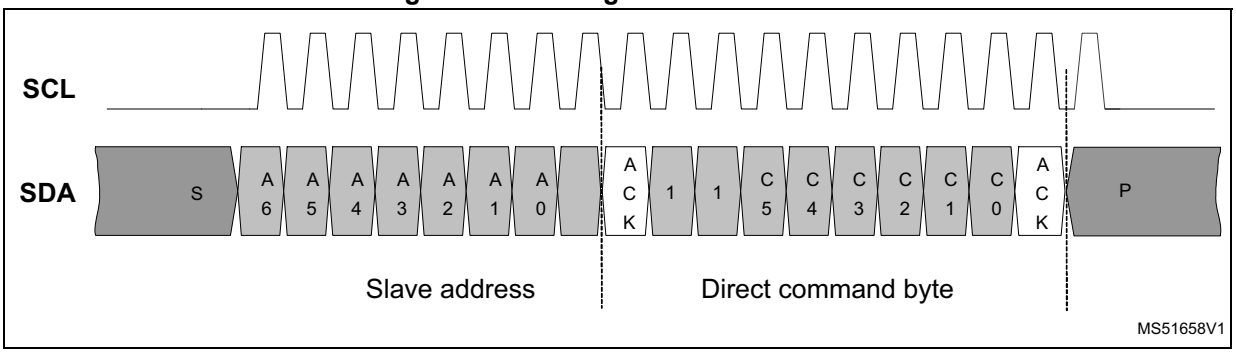
Figure 17. FIFO read



Direct Command mode

After the I2C slave address the mode byte to trigger a direct command is sent. As for SPI some direct commands take some time to execute and no I2C access to the ST25R3916 must be performed until the execution of the direct command is completed. All such direct commands send in interrupt upon completion to notify the MCU that the I2C bus can be used again.

Figure 18. Sending a direct command



I2C access to register space-B

To access the register space-B, byte FBh has to be inserted between the I2C slave address and the register read or write mode byte. Access to register space-B remains active until an I2C Stop Condition is received.

Figure 19. Read and Write mode for register space-B access - Examples

Write to register space B

S	Slave address W	A	FBh	Register address	A	Data 0	A	Data 1	A	...	Data N	A	P

Read from register space B

S	Slave address W	A	FBh	Register address	A	Sr	Slave address R	A	Data 0	A	Data 1	A	...	Data N	N	P

Legend: S: Start, Sr: repeated Start, A: ACK, N: NAK, P: Stop.

I2C: transition to and termination of the Transparent mode

When the transparent mode command is received via I2C, the chip interface lines are switched to the Analogue front end as described in *Section 4.2.13: Transparent Mode*.

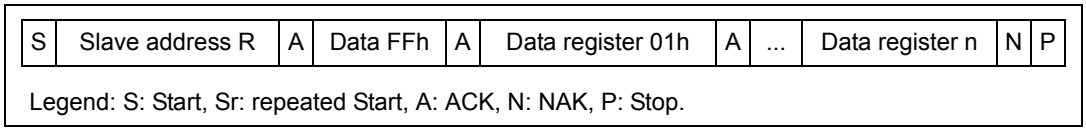
Once in transparent mode the BSS signal is used to distinguish between I2C communication and transparent mode data as follows:

1. the BSS line must be set high before entering the transparent mode, and then kept high during the Transparent mode
2. the Transparent mode is terminated when the BSS line is set to low, followed by at least one SCL clock pulse
3. after the termination of the transparent mode the I2C interface can be used again.

I2C: master reads slave immediately after the first byte

If the I2C master omits the mode byte and reads the ST25R3916 immediately after the slave address, then, as shown in *Figure 20*, it will first output the byte FFh, followed by a register dump starting at addres 01h.

Figure 20. I2C master reads slave immediately after the first byte



This mode is incorporated for an easier the detection of I2C devices, but is not intended to be used in normal operation.

4.2 Direct commands

Table 5. List of direct commands

Code (hex)	Name	Comments	Chaining	Interrupt after termination	Operation mode(1)
C0, C1	Set Default	Puts the ST25R3916 into power-up state	No	No	All
C2, C3	Stop All Activities	Stops all activities: transmission, reception, direct command execution, timers	Yes	No	en
C4	Transmit With CRC	Starts a transmit sequence with automatic CRC generation	Yes	No	en
C5	Transmit Without CRC	Starts a transmit sequence without automatic CRC generation	Yes	No	en
C6	Transmit REQA	Transmits REQA command (ISO14443A mode only)	Yes	No	en, tx_en
C7	Transmit WUPA	Transmits WUPA command (ISO14443A mode only)	Yes	No	en, tx_en
C8	NFC Initial Field ON	Performs Initial RF Collision avoidance and switches on the field	Yes	Yes	en
C9	NFC Response Field ON	Performs Response RF Collision avoidance and switches on the field	Yes	Yes	en
CD	Go to Sense (Idle)	Puts the passive target logic into Sense (Idle) state	Yes	No	en, rx_en
CE	Go to Sleep (Halt)	Puts the passive target logic into Sleep (Halt) state	Yes	No	en, rx_en
D0	Mask Receive Data	Stops receivers and RX decoders	Yes	No	All
D1	Unmask Receive Data	Starts receivers and RX decoders	Yes	No	All
D2	Change AM Modulation state	Changes AM modulation state	Yes	No	en, tx_en
D3	Measure Amplitude	Measures the amplitude of the signal present on RFI inputs and stores the result in the *A/D converter output register*	No	Yes	All(2)
D5	Reset RX Gain	Resets receiver gain to the value in the *Receiver configuration register 4*	No	No	en
D6	Adjust Regulators	Adjusts supply regulators according to the current supply voltage level	No	Yes	en
D8	Calibrate Driver Timing	Starts the driver timing calibration according to the setting in the *TX driver timing display register*	No	No	en
D9	Measure Phase	Measures the phase difference between the signal on RFO and RFI	No	Yes	All(2)

Table 5. List of direct commands (continued)

Code (hex)	Name	Comments	Chaining	Interrupt after termination	Operation mode(1)
DA	Clear RSSI	Clears the RSSI bits in the *RSSI display register* and restarts the measurement	Yes	No	en
DB	Clear FIFO	Clears FIFO, collision and IRQ status	Yes	No	en
DC	Enter Transparent Mode	Enters in Transparent mode	No	No	en
DD	Calibrate Capacitive Sensor	Calibrates capacitive sensor	No	Yes	All
DE	Measure Capacitance	Measures capacitance between CSO and CSI pin	No	Yes	All
DF	Measure Power Supply	-	No	Yes	en
E0	Start General Purpose Timer	-	Yes	No	en
E1	Start Wake-up Timer	-	Yes	No	All except wu
E2	Start Mask-receive Timer	Starts the mask-receive timer and squelch operation	Yes	No	en
E3	Start No-response Timer	-	Yes	No	en
E4	Start PP_{ON2} Timer	-	Yes	No	en
E8	Stop No-response Timer	-	Yes	No	en
FA	RFU	Not used	-	-	-
FB	Register Space-B Access	Enables R/W access to register Space-B	Yes	No	all
Other codes	RFU	Not used	-	-	-

1. Defines which *Operation control register* bits have to be set in order to accept a particular command.
2. Measure amplitude and Measure phase can be used directly from power down mode. In this case the command temporarily enables the oscillator.

4.2.1 Set Default

This direct command puts the ST25R3916 in the same state as power-up initialization:

- performs *Stop All Activities* command
- resets all registers to their default state
- clears all collision bits

Results of previous calibration and adjust commands are lost. No IRQ due to termination of direct command is produced.

4.2.2 Stop All Activities

This direct command stops any ongoing activites:

- performs *Clear FIFO* command
- stops data transmission and reception
- stops all timers, including FDT timer
- clears IRQ line an IRQ status bits
- stops Field ON commands

If Stop All Activities is received during RF collision avoidance the field detection is terminated and field is not set, consequently no interrupts are sent

- stops automatic field ON (same as above)
- stops automatic field OFF

If Stop All Activities is received during waiting for automatic field off via GPT, the field remains on

- nfc_ar is set to 01b, then it clears the awareness that there was a previous reception
- stops Temporary Enable

This command does not update any register apart from the FIFO status registers. Therefore it does not disable the field detector in CE mode (if it was enabled), and it does not switch off the field (if it was enabled).

4.2.3 Clear FIFO

This direct command clears the FIFO and the FIFO status registers. It does not clear the IRQ line or IRQ status bits.

To prepare a transmission send this command first before writing data into the FIFO. If a Clear FIFO command is sent during an ongoing data transmission, then the data transmission is aborted and FIFO and FIFO status registers are cleared.

4.2.4 Transmit commands

The transmit direct commands are used to start a data transmission from the ST25R3916. They switch the device to reception mode after the transmission is completed.

Before sending commands Transmit with CRC and Transmit without CRC, direct command Clear FIFO has to be sent, followed by the definition of the number of transmitted bytes and writing data to be transmitted in FIFO.

Use the direct commands Transmit REQA and Transmit WUPA to transmit ISO14443A short frame commands REQA and WUPA respectively. It is not necessary to send the direct command Clear FIFO before these two commands.

If the antcl bit is set, then the number of valid bits in the last byte must be set to zero (nbtx<2:0> in the *Number of transmitted bytes register 2*) prior to the direct command Transmit REQA or Transmit WUPA.

The direct commands Transmit REQA and Transmit WUPA automatically disable the CRC check of the response frame. The CRC check is enabled again after any of the below conditions:

- Transmit with CRC direct command
- Mask Receive Data direct command
- No Response timer expires

If the direct command Transmit without CRC is used in Felica™ mode the Length and CRC bytes are skipped. After the preamble and Sync bytes the raw FIFO content is transmitted. A transmit length nbtx ≥1 must be used.

4.2.5 NFC Field ON commands

The NFC Field On direct commands are used to perform RF Collision Avoidance. The external field detector must be enabled for these commands to work correctly.

To determine whether an external field is present the ST25R3916 compares the RF voltage level on the RFI1 pin with the collision avoidance threshold defined in the *External field detector activation threshold register*.

If no external field is detected, then the ST25R3916 transmitter is switched on automatically (bit tx_en in the *Operation control register* is set) and an I_apon IRQ is signaled. After the RF guard time defined in the *NFC field on guard timer register* has passed an I_cat IRQ is signaled. At this point the controller can initiate a data transmission using a transmit command.

If an external field is detected, then a I_cac IRQ is signaled, and the ST25R3916 transmitter stays off.

The direct command NFC Initial Field ON performs an Initial Collision Avoidance according to NFCIP-1 standard, and the direct command NFC Response Field ON performs a Response Collision Avoidance according to NFCIP-1 standard. See *Figure 21*, *Figure 22* and *Table 6* for details on the timing of these commands.

Figure 21. Direct command NFC Initial Field ON

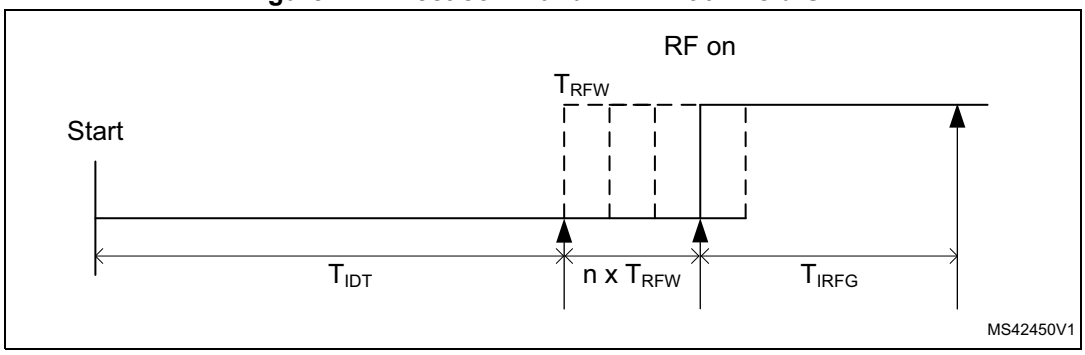


Figure 22. Direct command NFC Response Field ON

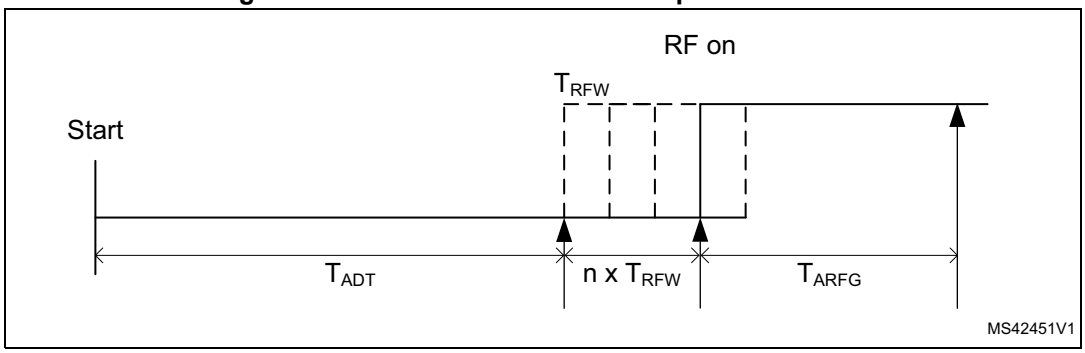


Table 6. Timing parameters of NFC Field ON commands

Parameter	Symbol	Value	Unit	Notes
Initial delay time	T_{IDT}	4096	/ fc	NFC Initial Field ON
RF waiting time	T_{RFW}	512	/ fc	n = 0…3 based on nfc_n<1:0>
Initial guard time	T_{IRFG}	75 µs + NFC Field on guard time	s	NFC Field on guard time defined in the *NFC field on guard timer register*. NFCIP-1 T_{IRFG} requirement: 5 …35 ms
Active delay time	T_{ADT}	768	/ fc	NFC Response Field ON
RF waiting time	T_{RFW}	512	/ fc	n = 0…3 based on nfc_n<1:0> in *Auxiliary definition register*
Active guard time	T_{ARFG}	75 µs + NFC Field on guard time	s	NFC Field on guard time defined in the *NFC field on guard timer register*. NFCPIP-1 T_{ARFG} requirement: > 75 µs + NFC Field on guard times (1024 / fc)

4.2.6 Mask Receive Data and Unmask Receive Data

The direct command Mask Receive Data disables processing of the receiver output by the RX decoders, RSSI measurement, and AGC operation.

The direct command Unmask Receive Data enables processing of the received data by the RX decoders, RSSI measurement and AGC operation. A common use of this command is to re-enable the receiver operation after it was masked by the command Mask Receive Data. If the Mask Receive Timer is still running while the direct command Unmask Receive Data is received, reception is enabled, and the Mask Receive Timer is reset.

In passive target (card emulation) mode, the Unmask Receive Data command prepares the RX decoders for a new data reception and clears the internal FDT timer. In passive target mode, the direct command Unmask Receive Data has to be used only if no further transmission from he ST25R3916 is planned and the device has to wait for the next command to be received.

4.2.7 Change AM Modulation state

This command changes the AM modulation state from unmodulated to modulated, and vice versa. This can be used to measure the AM modulation index with the direct command *Measure Amplitude*.

4.2.8 Measure Amplitude

This command measures the amplitude of the RF signal on the RFI inputs and stores the result in the *A/D converter output register*.

This command enables the transmitter and amplitude detector. The transmitter drives the antenna, and the amplitude detector converts the differential RF signal received back between RFI1 and RFI2 into a proportional DC voltage. This DC voltage is converted with the A/D converter in absolute conversion mode into an 8-bit value and stored in the *A/D converter output register*.

The amplitude detector conversion gain is 0.6 V_{inPP} / V_{out} referenced to the RF signal on a single RFI pin. Thus, one LSB of the A/D converter output represents 13.02 mV_{PP} on either of the RFI inputs.

Note: The maximum allowed voltage level on an RFI pin is 3 V_{PP}. This results in 1.8 V output DC voltage of the amplitude detector and produces a value of E6h after A/D conversion.

Duration time: 25 µs max.

4.2.9 Reset RX Gain

This command initializes the AGC, Squelch and RSSI block and resets the gain reduction to the value set in *Receiver configuration register 4*. Sending this command also stops any ongoing squelch process.

4.2.10 Adjust Regulators

When this command is sent, then the transmitter and receiver are enabled to ensure a high current draw and the regulated voltage V_{DD_RF} is set 250 mV below the power supply level of V_{DD_TX}. Before sending the adjust regulator command it is required to toggle the bit reg_s by setting it first to 1 and then reset it to 0. After the adjustment is completed the state of the transmitter and receiver prior to the command execution is restored (either enabled or disabled).

Duration time: 5 ms max.

This command is not accepted if external definition of the regulated voltage is selected in the *Regulator voltage control register* (bit reg_s is set to 1).

4.2.11 Measure Phase

This command measures the phase difference between the signals on the RFO outputs and the signals on the RFI inputs and stores the result in the *A/D converter output register*.

This command enables the transmitter and phase detector, and performs an A/D conversion of the output of the phase detector with the A/D converter in relative mode. The phase measurement results can be calculated using the following formulas:

- $0 \le \Phi \le 17^o$: result = 255
- $17 < \Phi < 163^o$: angle [º] = 17 + (1 -result / 255) * 146
- $163 \ge \Phi \ge 180^o$: result = 0

Duration time: 25 µs max.

4.2.12 Clear RSSI

The receiver automatically clears the RSSI bits in the *RSSI display register* and starts a new measurement of the RSSI when a new reception is started (e.g. after a Transmit direct command). Since the RSSI bits store the peak value (peak-hold type) eventual variation of the receiver input signal will not be followed (this may happen in case of a long message or test procedure).

The direct command Clear RSSI clears the RSSI bits in the *RSSI display register*, and restarts the RSSI measurement. This allows to obtain multiple RSSI measurements during a single reception.

4.2.13 Transparent Mode

This command sets the receiver and transmitter into the transparent mode. The ST25R3916 enters the transparent mode on the rising edge of the BSS signal of the SPI frame used to send the direct command. The transparent mode is maintained as long as signal BSS is kept high, that is, the following SPI command sent from the microcontroller will automatically stop the transparent mode.

4.2.14 Calibrate Capacitive Sensor

This command calibrates the capacitive sensor.

It is strongly recommended to use this command in power-down mode only to avoid interference with the crystal oscillator or reader magnetic field. Interrupt I_dct is only generated in Ready mode. The measurement status is indicated by status bits in the *Capacitive sensor display register*.

Duration time: 3 ms max.

This command is executed only if the capacitive sensor automatic calibration mode is set (all bits cs_mcal in the *Capacitive sensor control register* are set to 0).

4.2.15 Measure Capacitance

This command performs the capacitance measurement.

It is strongly recommended to use this command in power-down mode only to avoid interference with the crystal oscillator or reader magnetic field.

Duration time: 250 µs max.

4.2.16 Measure Power Supply

This command measures the power supply. The bits mpsv<2:0> in the *Regulator voltage control register* select which signal is measured. The result of the measurement is stored in the *A/D converter output register*.

For power supply measurements the selected supply input voltage is divided by three and measured with the A/D converter in absolute mode. This leads to a resolution of 23.4 mV per LSB for all power supply measurements.

Duration time: 25 µs max.

4.3 Registers

The ST25R3916 has two register spaces, each of them consists of up to 64 registers with address ranging from 00h to 3Fh:

1. register space A (Rs-A), see *Table 7*
2. register space B (Rs-B), see *Table 8*.

There are two types of registers implemented in the ST25R3916:

1. configuration registers: used to configure the device, can be written and read through the SPI or I2C interfaces
2. display registers: read only (RO), contain information about the state of the device.

Registers are set to their default value at power-up and after sending the direct command *Set Default*.

Table 7. List of registers - Space A

Type	Address (hex)	Register space A (Rs-A)
IO configuration	00	*IO configuration register 1*
	01	*IO configuration register 2*
Operation control and mode definition	02	*Operation control register*
	03	*Mode definition register*
	04	*Bit rate definition register*
Protocol configuration	05	*ISO14443A and NFC 106kb/s settings register*
	06	*ISO14443B settings register 1*
	07	*ISO14443B and FeliCa settings register*
	08	*NFCIP-1 passive target definition register*
	09	*Stream mode definition register*
	0A	*Auxiliary definition register*
Receiver configuration	0B	*Receiver configuration register 1*
	0C	*Receiver configuration register 2*
	0D	*Receiver configuration register 3*
	0E	*Receiver configuration register 4*
Timer definition	0F	*Mask receive timer register*
	10	*No-response timer register 1*
	11	*No-response timer register 2*
	12	*Timer and EMV control register*
	13	*General purpose timer register 1*
	14	*General purpose timer register 2*
	15	*PPON2 field waiting register*

Table 7. List of registers - Space A (continued)

Type	Address (hex)	Register space A (Rs-A)
Interrupt and associated reporting	16	*Mask main interrupt register*
	17	*Mask timer and NFC interrupt register*
	18	*Mask error and wake-up interrupt register*
	19	*Mask passive target interrupt register*
	1A	*Main interrupt register*
	1B	*Timer and NFC interrupt register*
	1C	*Error and wake-up interrupt register*
	1D	*Passive target interrupt register*
	1E	*FIFO status register 1*
	1F	*FIFO status register 2*
	20	*Collision display register*
	21	*Passive target display register*
Definition of number of transmitted bytes	22	*Number of transmitted bytes register 1*
	23	*Number of transmitted bytes register 2*
	24	*Bit rate detection display register*
A/D converter output	25	*A/D converter output register*
Antenna calibration	26	*Antenna tuning control register 1*
	27	*Antenna tuning control register 2*
Antenna driver and modulation	28	*TX driver register*
	29	*Passive target modulation register*
External field detector threshold	2A	*External field detector activation threshold register*
	2B	*External field detector deactivation threshold register*
Regulator	2C	*Regulator voltage control register*
Receiver state display	2D	*RSSI display register*
	2E	*Gain reduction state register*
Capacitive sensor	2F	*Capacitive sensor control register*
	30	*Capacitive sensor display register*
Auxiliary display	31	*Auxiliary display register*

Table 7. List of registers - Space A (continued)

Type	Address (hex)	Register space A (Rs-A)
Wake-up	32	*Wake-up timer control register*
	33	*Amplitude measurement configuration register*
	34	*Amplitude measurement reference register*
	35	*Amplitude measurement auto-averaging display register*
	36	*Amplitude measurement display register*
	37	*Phase measurement configuration register*
	38	*Phase measurement reference register*
	39	*Phase measurement auto-averaging display register*
	3A	*Phase measurement display register*
	3B	*Capacitance measurement configuration register*
	3C	*Capacitance measurement reference register*
	3D	*Capacitance measurement auto-averaging display register*
	3E	*Capacitance measurement display register*
IC identity	3F	*IC identity register*

Table 8. List of registers - Space B

Type	Address (hex)	Register space B (Rs-B)
Protocol configuration	05	*EMD suppression configuration register*
	06	*Subcarrier start timer register*
Receiver configuration	0B	*P2P receiver configuration register 1*
	0C	*Correlator configuration register 1*
	0D	*Correlator configuration register 2*
Timer definition	0F	*Squelch timer register*
	15	*NFC field on guard timer register*
Antenna driver and modulation	28	*Auxiliary modulation setting register*
	29	*TX driver timing register*
External field detector threshold	2A	*Resistive AM modulation register*
	2B	*TX driver timing display register*
Regulator	2C	*Regulator display register*
Protection	30	*Overshoot protection configuration register 1*
	31	*Overshoot protection configuration register 1*
	32	*Undershoot protection configuration register 1*
	33	*Undershoot protection configuration register 1*

4.3.1 IO configuration register 1

Register space: A

Address: 00h

Type: RW

Table 9. IO configuration register 1

<table>
<tr><th>Bit</th><th>Name</th><th>Default</th><th colspan="3">Function</th><th>Comments</th></tr>
<tr><td>7</td><td>single</td><td>0</td><td colspan="3">0: Differential antenna driving
1: Only one RFO driver will be used</td><td>Chooses between single and differential antenna driving.</td></tr>
<tr><td>6</td><td>rfo2</td><td>0</td><td colspan="3">0: RFO1, RFI1
1: RFO2, RFI2</td><td>Chooses which output driver and which input will be used in case of single driving.</td></tr>
<tr><td>5</td><td>i2c_thd1</td><td>0</td><td colspan="3" rowspan="2">I2C t_{HD}: non hs-modes / hs-modes
00: 380 ns / 160 ns
01: 180 ns / 160 ns
10: 180 ns / 70 ns
11: 100 ns / 70 ns</td><td>-</td></tr>
<tr><td>4</td><td>i2c_thd0</td><td>0</td><td>-</td></tr>
<tr><td>3</td><td>RFU</td><td>0</td><td colspan="3">-</td><td>-</td></tr>
<tr><td rowspan="4">2</td><td rowspan="4">out_cl1</td><td rowspan="4">0</td><td>out_cl1</td><td>out_cl0</td><td>MCU_CLK</td><td rowspan="4">Selection of clock frequency on MCU_CLK output in case Xtal oscillator is running. With “11” MCU_CLK output is permanently low.</td></tr>
<tr><td>0</td><td>0</td><td>3.39 MHz</td></tr>
<tr><td>0</td><td>1</td><td>6.78 MHz</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">out_cl0</td><td rowspan="2">0</td><td>1</td><td>0</td><td>13.56 MHz</td></tr>
<tr><td>1</td><td>1</td><td>Disabled</td></tr>
<tr><td>0</td><td>lf_clk_off</td><td>0</td><td colspan="3">0: LF clock on MCU_CLK
1: No LF clock on MCU_CLK</td><td>By default the 32 kHz LF clock is present on MCU_CLK output when Xtal oscillator is not running and the MCU_CLK output is not disabled.</td></tr>
</table>

4.3.2 IO configuration register 2

Register space: A

Address: 01h

Type: RW

Table 10. IO configuration register 2

Bit	Name	Default	Function	Comments
7	sup3V	0	0: 5 V supply 1: 3.3 V supply	5 V supply, range: 4.1 V to 5.5 V 3.3 V supply, range: 2.4 V to 3.6 V
6	vspd_off	0	0: Enable V_{DD_D} regulator 1: Disable V_{DD_D} regulator	Used for low cost applications. When this bit is set: – at 3 V or 5 V supply VSP_D and VSP_A must be shorted externally – for 3.3 V applications V_{DD_D} can alternatively be supplied from V_{DD} if V_{DD_A} is not more than 300 mV lower then V_{DD}.
5	aat_en	0	0: disable AAT D/A 1: enable AAT D/A	The AAT D/A converters are enabled if both aat_en and en are set. If only aat_en is set and en is cleared, then the AAT outputs are set to a fixed value. Note that for the fixed value to operate, en must have been set to 1 at least once, prior to having en = 0.
4	miso_pd2	0	1: Pull-down on MISO, when BSS is low and MISO is not driven by the ST25R3916.	Valid only in SPI mode.
3	miso_pd1	0	1: Pull-down on MISO when BSS is high	
2	io_drv_lvl	0	0: Normal IO driver level 1: Increase IO driving level	Increases IO driver strength of MISO, MCU_CLK an IRQ. Recommended to set to 1 for all I2C operation, and for SPI operation if V_{DD_IO} < 3 V.
1	am_ref_rf	0	0: V_{DD_AM} regulator reference from V_{DD_DR} 1: V_{DD_AM} regulator reference from V_{DD_RF}	Selects non modulated RF voltage level reference of the V_{DD_AM} voltage regulator.
0	slow_up	0	1: Slow ramp at Tx on	≥ 10 µs, 10% to 90%, for B

4.3.3 Operation control register

Address: 02h

Type: RW

Table 11. Operation control register(1)

Bit	Name	Default	Function	Comments
7	en	0	1: Enables oscillator and regulator (Ready mode)	-
6	rx_en	0	1: Enables Rx operation	-
5	rx_chn	0	0: Both, AM and PM, channels enabled 1: One channel enabled	If only one Rx channel is enabled, selection is done by the *Receiver configuration register 1* bit ch_sel.
4	rx_man	0	0: Automatic channel selection 1: Manual channel selection	If both Rx channels are enabled, chooses the method of channel selection, manual selection is done by the *Receiver configuration register 1* bit ch_sel.
3	tx_en	0	1: Enables Tx operation	This bit is automatically set by NFC Field ON commands and reset in NFC active communication modes after transmission is finished.
2	wu	0	1: Enables Wake-up mode	According to settings in *Wake-up timer control register*.
1	-	-	Not used	-
0	-	-		-

1. Default setting takes place at power-up only.

4.3.4 Mode definition register

Register space: A

Address: 03h

Type: RW

Table 12. Mode definition register(1)

Bit	Name	Default	Function	Comments
7	targ	0	0: Initiator 1: Target	-
6	om3	0	Refer to *Table 13* and *Table 14*	Selection of operation mode. Different for initiator and target modes.
5	om2	0		
4	om1	0		
3	om0	1		
2	tr_am	0	0: OOK 1: AM	Selects RF modulation mode.
1	nfc_ar1	0	00: Off 01: Automatic field on after any reception (including errors) 10: Always after peer field-off 11: RFU	Automatically starts the Response RF collision avoidance.
0	nfc_ar0	0		

1. Register can be written only in case crystal clock is present and stable (oscok = 1).

Table 13. Initiator operation modes(1)

om3	om2	om1	om0	Comments
0	0	0	0	NFCIP-1 active communication
0	0	0	1	ISO14443A
0	0	1	0	ISO14443B
0	0	1	1	FeliCa™
0	1	0	0	NFC Forum Type 1 tag (Topaz)
1	1	1	0	Sub-carrier stream mode
1	1	1	1	BPSK stream mode
Other combinations				RFU

1. If a non supported operation mode is selected the Tx/Rx operation is disabled.

Table 14. Target operation modes(1)

om3	om2	om1	om0	Comments
0	0	0	1	ISO14443A passive target mode
0	1	0	0	FeliCa™ passive target mode
0	1	1	1	NFCIP-1 active communication mode

Table 14. Target operation modes[1] (continued)

om3	om2	om1	om0	Comments
1	x	x	x	Bit Rate Detection mode, – om2: 0 selected enabled protocols – om2: enable FeliCa™ bit rate detection mode – om0: enable ISO14443A bit rate detection mode
Other combinations				Not allowed

1. The nfc_f0 = 1 must not be set in Bit Rate detection mode (see *Table 16*).

4.3.5 Bit rate definition register

Register space: A

Address: 04h

Type: RW

Table 15. Bit rate definition register

Bit	Name	Default	Function	Comments
7	RFU	0	Refer to *Table 16*	-
6	RFU	0		-
5	tx_rate1	0		Selects bit rate for Tx.
4	tx_rate0	0		
3	RFU	0		-
2	RFU	0		-
1	rx_rate1	0		Selects bit rate for Rx.
0	rx_rate0	0		

Table 16. Bit rate coding(1)

rate3	rate2	rate1	rate0	Bit rate (kbit/s)	Comments
0	0	0	0	fc/128 (~106)	-
0	0	0	1	fc/64 (~212)	-
0	0	1	0	fc/32 (~424)	-
0	0	1	1	fc/16 (~848)	-
Other combinations				-	Not used

1. If a non supported bit rate is selected the Tx/Rx operation is disabled.

4.3.6 ISO14443A and NFC 106kb/s settings register

Register space: A

Address: 05h

Type: RW

Table 17. ISO14443A and NFC 106kb/s settings register

Bit	Name	Default	Function	Comments
7	no_tx_par	0	1: No parity bit is generated during Tx	Data stream is taken from FIFO, transmit to be done using command Transmit Without CRC(1).
6	no_rx_par	0	1: Receive and put in FIFO also the parity and CRC bits	When set to 1 received bit stream is put in the FIFO, no parity and CRC detection is done(1). Supported only for 106 kbit/s data rate.
5	nfc_f0	0	1: Support of NFCIP-1 Transport Frame format	Adds SB (F0) and LEN bytes during Tx and skip SB (F0) byte during Rx. Must not be set in bit rate detection mode.
4	p_len3	0	Refer to *Table 18*	Modulation pulse width, defined in number of 13.56 MHz clock periods.
3	p_len2	0		
2	p_len1	0		
1	p_len0	0		
0	antcl	0	0: Standard frame 1: ISO14443 anticollision frame	Must be set to 1 for reception of ISO14443A bit oriented anticollision frames in reader mode. Must be set to 0 for all other frames and modes.

1. Supported in reader modes only, not supported in card emulation modes.

Table 18. ISO14443A modulation pulse width

p_len3	p_len2	p_len1	p_len0	Pulse width in number of 1 / fc for different bit rates			
				fc/128	fc/64	fc/32	fc/16
0	1	1	1	42	-	-	-
0	1	1	0	41	24	-	-
0	1	0	1	40	23	-	-
0	1	0	0	39	22	13	-
0	0	1	1	38	21	12	8
0	0	1	0	37	20	11	7
0	0	0	1	36	19	10	6
0	0	0	0	35	18	9	5
1	1	1	1	34	17	8	4
1	1	1	0	33	16	7	3
1	1	0	1	32	15	6	2
1	1	0	0	31	14	5	-

Table 18. ISO14443A modulation pulse width (continued)

p_len3	p_len2	p_len1	p_len0	Pulse width in number of 1 / fc for different bit rates			
				fc/128	fc/64	fc/32	fc/16
1	0	1	1	30	13	-	-
1	0	1	0	29	12	-	-
1	0	0	1	28	-	-	-
1	0	0	0	27	-	-	-

4.3.7 ISO14443B settings register 1

Register space: A

Address: 06h

Type: RW

Table 19. ISO14443B settings register 1

Bit	Name	Default	Function				Comments
7	egt2	0	egt2	egt1	egt0	Number of etu	EGT defined in number of etu
			0	0	0	0	
6	egt1	0	0	0	1	1	
			⋮	⋮	⋮	⋮	
5	egt0	0	1	1	0	6	
			1	1	1	6	
4	sof_0	0	0: 10 etu 1: 11 etu				SOF, number of etu with logic 0
3	sof_1	0	0: 2 etu 1: 3 etu				SOF, number of etu with logic 1
2	eof	0	0: 10 etu 1: 11 etu				EOF, number of etu with logic 0
1	half	0	0: SOF and EOF defined by sof_0, sof_1, and eof bit 1: SOF 10.5 etu logic 0, 2.5 etu logic 1, EOF: 10.5 etu logic 0				Sets SOF and EOF settings in middle of specification.
0	rx_st_om	0	0: Start/stop bit must be present for Rx 1: Start/stop bit omission for Rx				SOF fixed to 10 low and 2 etu high, EOF not defined, put in FIFO last full byte. CRC is not checked in this mode. Supported only in a coherent reception mode.

4.3.8 ISO14443B and FeliCa settings register

Register space: A

Address: 07h

Type: RW

Table 20. ISO14443B and FeliCa settings register

Bit	Name	Default	Function	Comments
7	tr1_1	0	Refer to *Table 21*	-
6	tr1_0	0		
5	no_sof	0	1: No SOF PICC to PCD	According to ISO14443-3 chapter 7.10.3.3. Support of B'.
4	no_eof	0	1: No EOF PICC to PCD	According to ISO14443-3 chapter 7.10.3.3. Supported only in coherent reception mode.
3	RFU	0	-	-
2	RFU	0	-	-
1	f_p1	0	00: 48 01: 64 10: 80 11: 96	FeliCa™ preamble length (valid also for NFCIP-1 active communication bit rates 212 and 424 kb/s)
0	f_p0	0		

Table 21. Minimum TR1 codings

tr1_1	tr1_0	Minimum TR1 for a PICC to PCD bit rate	
		fc/128	>fc/128
0	0	80 / fs	
0	1	64 / fs	32 / fs
1	0	Not used	
1	1	Not used	

4.3.9 NFCIP-1 passive target definition register

Register space: A

Address: 08h

Type: RW

Table 22. NFCIP-1 passive target definition register

Bit	Name	Default	Function	Comments
7	fdel3	0	PCD to PICC FDT compensation. Frame compensation defined as fdel<3:0>*1 / fc	Valid for NFC-A CE mode – fdel = 0: Nominal FDT time in produced in logic. – fdel > 0: Shortens the FDT provided by logic. Due to signal processing delays fdel<3:0> = 2 is expected to be a good setting (best value dependents also on filter and antenna).
6	fdel2	0		
5	fdel1	0		
4	fdel0	0		
3	d_ac_ap2p	0	0: Enable AP2P frame recognition 1: Disable AP2P frame recognition	-
2	d_212/424_1r	0	0: Enable automatic SENSF_RES 1: Disable automatic SENSF_RES	Disables the automatic responses in passive target mode, and completely operates via FIFO.
1	RFU	0	RFU	
0	d_106_ac_a	0	0: Enable automatic anti-collision in NFC-A 1: Disable automatic anti-collision in NFC-A	

4.3.10 Stream mode definition register

Register space: A

Address: 09h

Type: RW

Table 23. Stream mode definition register

<table>
<tr><th>Bit</th><th>Name</th><th>Default</th><th colspan="3">Function</th><th>Comments</th></tr>
<tr><td>7</td><td></td><td>0</td><td colspan="3">-</td><td>-</td></tr>
<tr><td>6</td><td>scf1</td><td>0</td><td colspan="3" rowspan="2">Refer to Table 24</td><td rowspan="2">Sub-carrier frequency definition for Sub-carrier and BPSK stream mode.</td></tr>
<tr><td>5</td><td>scf0</td><td>0</td></tr>
<tr><td rowspan="4">4</td><td rowspan="4">scp1</td><td rowspan="4">0</td><td>scp1</td><td>scp0</td><td>Number of pulses</td><td rowspan="4">Number of sub-carrier pulses in report period for Sub-carrier and BPSK stream mode.</td></tr>
<tr><td>0</td><td>0</td><td>1 (BPSK only)</td></tr>
<tr><td>0</td><td>1</td><td>2</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">scp0</td><td rowspan="2">0</td><td>1</td><td>0</td><td>4</td></tr>
<tr><td>1</td><td>1</td><td>8</td></tr>
<tr><td>2</td><td>stx2</td><td>0</td><td colspan="3" rowspan="3">Refer to Table 25</td><td rowspan="3">Definition of time period for Tx modulator control (for Sub-carrier and BPSK stream mode).</td></tr>
<tr><td>1</td><td>stx1</td><td>0</td></tr>
<tr><td>0</td><td>stx0</td><td></td></tr>
</table>

Table 24. Sub-carrier frequency definition for Sub-Carrier stream mode

scf1	scf0	Sub-Carrier mode	BPSK mode
0	0	fc/64 (212 kHz)	fc/16 (848 kHz)
0	1	fc/32 (424 kHz)	RFU
1	0	fc/16 (848 kHz)	
1	1	fc/8 (1695 kHz)	

Table 25. Definition of time period for Stream mode Tx modulator control

stx2	stx1	stx0	Time period
0	0	0	fc/128 (106 kHz)
0	0	1	fc/64 (212 kHz)
0	1	0	fc/32 (424 kHz)
0	1	1	fc/16 (848 kHz)
1	X	X	RFU

4.3.11 Auxiliary definition register

Register space: A

Address: 0Ah

Type: RW

Table 26. Auxiliary definition register

Bit	Name	Default	Function	Comments
7	no_crc_rx	0	0: Receive with CRC check 1: Receive without CRC check	Valid for all protocols, for ISO14443A REQA, WUPA and anticollision receive without CRC is done automatically(1).
6	RFU	0	-	-
5	nfc_id1	0	00: 4 bytes NFCID1 01: 7 bytes NFCID1 1x: RFU	Selects NFCID1 size.
4	nfc_id0	0		
3	mfaz_cl90	0	0: 0° shifted clock for phase measurement 1: 90° shifted clock for phase measurement	Affects also PM demodulation. Should be set to 0 for PM demodulation.
2	dis_corr	0	Refer to *Table 27*	Selects RW receiver operation.
1	nfc_n1	0	-	Value of n for direct commands NFC Initial Field ON and NFC Response Field ON (0…3).
0	nfc_n0	0		

1. Receive without CRC is done automatically when REQA and WUPA commands are sent using direct commands Transmit REQA and Transmit WUPA, respectively, and in case anticollision is performed setting bit antcl.

Table 27. RW receiver operation

Mode	dis_corr = 0	dis_corr = 1
ISO-A (106 to 848 kHz)	Correlator reception	NA
ISO-B (106 to 848 kHz)		Pulse reception (coherent)
Felica™ (212 to 424 kHz)		Pulse reception
NFC Forum Type 1 Tag (Topaz)		NA
Stream modes (scf<1:0> = 01, scp<1:0> = 11)		Pulse reception
Stream modes - Others	NA	Pulse reception

4.3.12 EMD suppression configuration register

Register space: B

Address: 05h

Type: RW

Table 28. EMD suppression configuration register

Bit	Name	Default	Function	Comments
7	emd_emv	0	0: Disable EMD suppression 1: Enable EMD suppression according to EMVCo	Bits no_rx_par and no_crc_rx must be set to 0, and bit nrt_emv must be set to 1 when emd_emv is enabled
6	rx_start_emv	0	0: Reception is enabled (l_rxs) only if the first 4 bits of the frame are error free 1: Reception is enabled (l_rxs) also if there is an error in the first four bits of the frame	Applies to ISO-A 106k only. Must be set to 1 for EMVCo compliance.
5	RFU	0	-	-
4	RFU	0	-	-
3	emd_thld3	0	If the received frame is less than emd_thld<3:0> bytes long then EMD suppression will trigger on reception errors	Must be set to 4 for EMVCo compliance.
2	emd_thld2	0		
1	emd_thld1	0		
0	emd_thld0	0		

4.3.13 Subcarrier start timer register

Register space: B

Address: 06h

Type: RW

Table 29. Subcarrier start timer register

Bit	Name	Default	Function	Comments
7:5	RFU	0	-	-
4:0	sst<4:0>	0	Subcarrier start time Step: 0.25 etu Range: 0 etu to 7.75 etu	Applies to ISO-B, 106 kb/s. If the time from the end of the MRT timer to the detection of a subcarrier is shorter than sst<4:0>, then a soft error interrupt is generated. If emd_emv = 1 the frame will be suppressed as EMD and a restart interrupt will be generated. Note that corr_s3 defines the length of subcarrier start detection and affects the correct sst<4:0> setting.

4.3.14 Receiver configuration register 1

Register space: A

Address: 0Bh

Type: RW

Table 30. Receiver configuration register 1

Bit	Name	Default	Function	Comments
7	ch_sel	0	0: Enable AM channel 1: Enable PM channel	If only one Rx channel is enabled in the *Operation control register* defines which channel is enabled. If both channels are enabled and manual channel selection is active defines which channel is used for receive framing.
6	lp2	0	Low pass control (see *Table 2*)	For recommended filter settings refer to *Table 3*.
5	lp1	0		
4	lp0	0		
3	z600k	0	First and third stage zero setting (see *Table 1*)	
2	h200	0		
1	h80	0		
0	z12k	0		

4.3.15 Receiver configuration register 2

Register space: A

Address: 0Ch

Type: RW

Table 31. Receiver configuration register 2

Bit	Name	Default	Function	Comments
7	demod_mode	0	0: AM/PM demodulation 1: I/Q demodulation	Selects demodulator operation mode. I/Q demodulation requires amd_sel = 1.
6	amd_sel	0	0: peak detector 1: mixer	Selects AM demodulator.
5	sqm_dyn	1	0: Squelch disabled 1: Automatic squelch activation after end of TX	Squelch is activated 18.88 µs after end of TX, and stops when the Mask Receive Timer reaches the sqt<7:0> setting.
4	pulz_61	0	0: Squelch ratio 1 1: Squelch ratio 6/3	Select squelch trigger level. Squelch triggers on signals that are 1 or 6/3 times larger than the digitizing threshold. – Ratio 1: recommended for ISO-A 106k correlator, ISO-A HBR/ISO-B pulse decoder, ISO-15693, and FeliCa™ – Ratio 6/3: recommended for ISO-A HBR/ISO-B correlator
3	agc_en	1	0: AGC disabled 1: AGC enabled	-
2	agc_m	1	0: AGC operates on first eight sub-carrier pulses 1: AGC operates during complete receive period	-
1	agc_alg	0	0: Algorithm with preset is used 1: Algorithm with reset is used	Algorithm with preset is recommended for protocols with short SOF (like ISO14443A fc / 128).
0	agc6_3	0	0: AGC ratio 3 1: AGC ratio 6	Select AGC trigger level. AGC triggers on signals 3 or 6 times above the minimum detectable signal level.

4.3.16 Receiver configuration register 3

Register space: A

Address: 0Dh

Type: RW

Table 32. Receiver configuration register 3

Bit	Name	Default	Function	Comments
7	rg1_am2	1	Gain reduction/boost in first gain stage of AM channel.	0: Full gain 1-6: Gain reduction 2.5 dB per step (15 dB total) 7: Boost +5.5 dB
6	rg1_am1	1		
5	rg1_am0	0		
4	rg1_pm2	1	Gain reduction/boost in first gain stage of PM channel.	0: Full gain 1-6: Gain reduction 2.5 dB per step (15 dB total) 7: Boost +5.5 dB
3	rg1_pm1	1		
2	rg1_pm0	0		
1	lf_en	0	0: HF signal on receiver input 1: LF signal on receiver input	-
0	lf_op	0	0: differential LF operation 1: LF input split (RFI1 to AM channel, RFI2 to PM channel)	-

4.3.17 Receiver configuration register 4

Register space: A

Address: 0Eh

Type: RW

Table 33. Receiver configuration register 4(1)

Bit	Name	Default	Function	Comments
7	rg2_am3	0	AM channel: Gain reduction in second and third stage and digitizer	Only values from 0h to Ah are used: – settings 1h to 4h reduce gain by increasing the digitizer window in 3 dB steps – values from 5h to Ah additionally reduce the gain in second and third gain stage, always in 3 dB steps.
6	rg2_am2	0		
5	rg2_am1	0		
4	rg2_am0	0		
3	rg2_pm3	0	PM channel: Gain reduction in second and third stage and digitizer	Only values from 0h to Ah are used: – settings 1h to 4h reduce gain by increasing the digitizer window in 3 dB steps – values from 5h to Ah additionally reduce the gain in second and third gain stage, always in 3 dB steps.
2	rg2_pm2	0		
1	rg2_pm1	0		
0	rg2_pm0	0		

1. Direct command *Reset RX Gain* is necessary to load the value of this register into AGC, Squelch, and RSSI block.

4.3.18 P2P receiver configuration register 1

Register space: B

Address: 0Bh

Type: RW

Table 34. P2P receiver configuration register 1

Bit	Name	Default	Function	Comments
7	ook_fd	0	OOK fast decay	-
6	ook_rc1	0	00 = 1.4 µs 01 = 1.0 µs 10 = 0.6 µs 11 = 0.2 µs	OOK RC time constant
5	ook_rc0	0		
4	ook_thd1	0	Refer to *Table 35*	OOK threshold level, depends on ook_rc<1:0> configuration.
3	ook_thd0	1		
2	ask_rc1	1	00 = 8.4 µs 01 = 6.8 µs 10 = 4.4 µs 11 = 2.4 µs	ASK RC time constant
1	ask_rc0	0		
0	ask_thd	0	0: 97% 1: 95%	ASK threshold level

Table 35. OOK threshold level settings

ook_thd<1:0>	ook_rc<1:0> = 0	ook_rc<1:0> > 0
00	55%	80%
01	45%	75%
10	35%	70%
11	25%	65%

4.3.19 Correlator configuration register 1

Register space: B

Address: 0Ch

Type: RW

Table 36. Correlator configuration register 1

Bit	Name	Default	Function		Comments
7	corr_s7	1	AGC = max |AM, PM|		-
6	corr_s6	0	ISO-A 106k	0: Collision detection level defined by corr_s<1:0> 1: Collision detection level equal to data slicer level	Selecting the collision detection level with corr_s<1:0> gives better detection of weak collisions. Setting the collision detection level equal to the data slicer gives better noise immunity.
			BPSK (1)	0: Correlator phase correction applied during the complete reception 1: No correlator phase correction after the first data bytes	No phase correction after start recommended for ISO-B 424 kb/s and 848 kb/s operation.
5	corr_s5	0	0: V_{ref} -50 mV setting, 1st squelch step -100 mV 1: V_{ref} -100 mV setting, 1st squelch step -200 mV		-
4	corr_s4	1	0: AM and PM correlation signals digitized separately 1: AM and PM correlation signals summed before digitizing (summation mode)		Summation mode is recommended for all correlator operations
3	corr_s3	0	0: RX bit rate 106kb/s = 17, RX bit rates 212 to 848 kb/s = 9 1: RX bit rate 106kb/s = 33, RX bit rates 212 to 848 kb/s = 17		BPSK start length setting (delay from the start of a tags subcarrier signal to the moment when a subcarrier start is detected). Then circuit starts observing for the first phase transition (9/17/33 ± 2 pilot pulses). At this moment the sst<4:0> check for TR0 is done.
2	corr_s2	0	ISO-A 106k	0: Normal data slicer 1: Fast data slicer	-
			BPSK (1)	0: Normal ref. time constant 1: Long ref. time const. (1.5x normal)	
1	corr_s1	1	ISO-A 106k	Collision level setting MSB	Collision detection level, compared to data detection level: – 00: 16% – 01: 28% – 10: 41% – 11: 53%
			BPSK (1)	Subcarrier end detection level 0: 100% 1: 66%	
0	corr_s0	1	ISO-A 106k	Collision level setting LSB	
			BPSK (1)	0: Subcarrier end detector disabled 1: Subcarrier end detector enabled	

1. BPSK options apply to ISO-A HBR and ISO-B (all bit rates).

4.3.20 Correlator configuration register 2

Register space: B

Address: 0Dh

Type: RW

Table 37. Correlator configuration register 2

Bit	Name	Default	Function	Comments
7	RFU	0	-	-
6	RFU	0		
5	RFU	0		
4	RFU	0		
3	RFU	0		
2	RFU	0		
1	corr_s9	0	0: Sleep mode disable set by timer 1: Sleep mode disable only on rx_on = 1	Correlator sleep mode option. Sleep start: 18 µs no output pulse. Stop with timer: – takes 18 µs (ISO-A/B, F424) – takes 42 µs (stream 15693, F212)
0	corr_s8	0	0: All other standards 1: 424 kHz subcarrier stream mode	Must be set to 1 for 424 kHz subcarrier stream mode.

4.3.21 Mask receive timer register

Register space: A

Address: 0Fh

Type: RW

Table 38. Mask receive timer register

Bit	Name	Default	Function	Comments
7	mrt7	0	mrt_step = 0: Step: 64 / fc (4.72 µs) Range: 256 / fc (~18.88 µs) to 16320 / fc (~1.2 ms) mrt_step = 1: Step: 512 / fc (37.78 µs) Range: 2048 / fc (151 µs) to 130560 / fc (9.62 ms)	Set time after end of TX during which the receiver output is ignored (masked). The minimum mask receive time of 18.88 µs covers the transients in receiver after end of transmission.
6	mrt6	0		
5	mrt5	0		
4	mrt4	0		
3	mrt3	1		
2	mrt2	0		
1	mrt1	0		
0	mrt0	0		

4.3.22 No-response timer register 1

Register space: A

Address: 10h

Type: RW

Table 39. No-response timer register 1

Bit	Name	Default	Function	Comments
7	nrt15	0	No-Response timer definition MSB bits nrt_step = 0: Step: 64 / fc (4.72 µs), Range: 309 ms nrt_step = 1: Step: 4096 / fc (302 µs) Range: 19.8 s.	Defines timeout after end of Tx. In case this timeout expires without detecting a response a No-Response interrupt is sent. In NFC mode the No-Response timer is started only when external field is detected. In the NFCIP-1 active communication mode the No-Response timer is automatically started when the transmitter is turned off after the message has been sent. All 0: No-Response timer is not started. No-Response timer is reset and restarted with Start No-Response Timer direct command.
6	nrt14	0		
5	nrt13	0		
4	nrt12	0		
3	nrt11	0		
2	nrt10	0		
1	nrt9	0		
0	nrt8	0		

4.3.23 No-response timer register 2

Address: 11h

Type: RW

Table 40. No-response timer register 2

Bit	Name	Default	Function	Comments
7	nrt7	0	No-Response timer definition LSB bits	-
6	nrt6	0		
5	nrt5	0		
4	nrt4	0		
3	nrt3	0		
2	nrt2	0		
1	nrt1	0		
0	nrt0	0		

4.3.24 Timer and EMV control register

Register space: A

Address: 12h

Type: RW

Table 41. Timer and EMV control register

Bit	Name	Default	Function	Comments
7	gptc2	0	General purpose timer trigger source. Refer to *Table 42*	-
6	gptc1	0		
5	gptc0	0		
4	RFU	0	-	-
3	mrt_step	0	0: 64 / fc 1: 512 / fc	Mask Receive Timer step size
2	nrt_nfc	0	0: NRT starts at end of TX (own field off) 1: NRT starts at peer field-on event	No-response timer start condition in AP2P initiator and target mode.
1	nrt_emv	0	1: No-response timer EMV mode	-
0	nrt_step	0	0: 64 / fc 1: 4096 / fc	No-response timer step size.

Table 42. Trigger sources

gptc2	gptc1	gptc0	Trigger source
X	X	X	The timer starts always with direct command Start General Purpose Timer.
0	0	0	No additional trigger source.
0	0	1	Additionally starts at End of RX (after EOF).
0	1	0	Additionally starts at Start of RX.
0	1	1	Additionally starts at End of TX In AP2P modes the timer is used to switch the field off. In AP2P modes enables NRT start according to nrt_nfc description.
1	0	0	RFU
1	0	1	
1	1	0	
1	1	1	

4.3.25 General purpose timer register 1

Register space: A

Address: 13h

Type: RW

Table 43. General purpose timer register 1

Bit	Name	Default	Function	Comments
7	gpt15	-	General purpose timeout definition MSB bits Defined in steps of 8 / fc (590 ns) Range from 590 ns to 38,7 ms	-
6	gpt14	-		
5	gpt13	-		
4	gpt12	-		
3	gpt11	-		
2	gpt10	-		
1	gpt9	-		
0	gpt8	-		

4.3.26 General purpose timer register 2

Register space: A

Address: 14h

Type: RW

Table 44. General purpose timer register 2

Bit	Name	Default	Function	Comments
7	gpt7	-	General purpose timeout definition LSB bits Defined in steps of 8 / fc (590 ns) Range from 590 ns to 38,7 ms	-
6	gpt6	-		
5	gpt5	-		
4	gpt4	-		
3	gpt3	-		
2	gpt2	-		
1	gpt1	-		
0	gpt0	-		

4.3.27 PPON2 field waiting register

Register space: A

Address: 15h

Type: RW

Table 45. PP_{ON2} field waiting register

Bit	Name	Default	Function	Comments
7	ppt7	1	PP_{ON2} timer Step: 64 / fc (4.72 µs) Range: 1.204 ms	Maximum time the system waits for the peer device field on in AP2P mode.
6	ppt6	0		
5	ppt5	0		
4	ppt4	0		
3	ppt3	0		
2	ppt2	0		
1	ppt1	0		
0	ppt0	0		

4.3.28 Squelch timer register

Register space: B

Address: 0Fh

Type: RW

Table 46. Squelch timer register

Bit	Name	Default	Function	Comments
7	sqt7	0	Squelch Timer Step, Range: same as *Mask receive timer register*, including mrt_step selection	Squelch is enabled ~20 µs after the end of reader data transmission – sqt<7:0> > 5: Squelch stops after the time defined by sqt<7:0>. Gain reduction due to squelch is locked and used as a starting point for AGC. – Sqt<7:0> ≤ 5 or sqt<7:0> ≥ mrt<7:0>: Squelch is enabled until the MRT expires.
6	sqt6	0		
5	sqt5	0		
4	sqt4	0		
3	sqt3	0		
2	sqt2	0		
1	sqt1	0		
0	sqt0	0		

4.3.29 NFC field on guard timer register

Register space: B

Address: 15h

Type: RW

Table 47. NFC field on guard timer register

Bit	Name	Default	Function	Comments
7	nfc_gt7	0	NFC field on guard timer Step: 2048 / fc (151 µs) Range: 38.66 ms	Used by NFC field on commands. The value nfc_gt<7:0> is added to the initial 75 µs in T_{IRFG} and T_{ARFG}. Set to 33 for T_{IRFG} (75 µs + 4.984 ms= 5.06 ms) Set to 0 for T_{ARFG} (75 µs + 0 ms = 75 µs)
6	nfc_gt6	0		
5	nfc_gt5	1		
4	nfc_gt4	1		
3	nfc_gt3	0		
2	nfc_gt2	0		
1	nfc_gt1	1		
0	nfc_gt0	1		

4.3.30 Mask main interrupt register

Register space: A

Address: 16h

Type: RW

Table 48. Mask main interrupt register

Bit	Name	Default	Function	Comments
7	M_osc	0	1: Mask IRQ when oscillator frequency is stable	-
6	M_wl	0	1: Mask IRQ due to FIFO water level	-
5	M_rxs	0	1: Mask IRQ due to start of receive	-
4	M_rxe	0	1: Mask IRQ due to end of receive	-
3	M_txe	0	1: Mask IRQ due to end of transmission	-
2	M_col	0	1: Mask IRQ due to bit collision	-
1	M_rx_rest	0	1: Mask IRQ due to automatic reception restart	-
0	RFU	0	Not used	-

4.3.31 Mask timer and NFC interrupt register

Register space: A

Address: 17h

Type: RW

Table 49. Mask timer and NFC interrupt register

Bit	Name	Default	Function	Comments
7	M_dct	0	1: Mask IRQ due to termination of direct command	-
6	M_nre	0	1: Mask IRQ due to No-Response Timer expire	-
5	M_gpe	0	1: Mask IRQ due to general purpose timer expire	-
4	M_eon	0	1: Mask IRQ due to detection of external field higher than Target activation level	-
3	M_eof	0	1: Mask IRQ due to detection of external field drop below Target activation level	-
2	M_cac	0	1: Mask IRQ due to detection of collision during RF Collision Avoidance	-
1	M_cat	0	1: Mask IRQ after minimum guard time expire	-
0	M_nfct	0	1: Mask IRQ when in target mode the initiator bit rate has been recognized	-

4.3.32 Mask error and wake-up interrupt register

Register space: A

Address: 18h

Type: RW

Table 50. Mask error and wake-up interrupt register

Bit	Name	Default	Function	Comments
7	M_crc	0	1: Mask IRQ due to CRC error	-
6	M_par	0	1: Mask IRQ due to parity error	-
5	M_err2	0	1: Mask IRQ due to soft framing error	-
4	M_err1	0	1: Mask IRQ due to hard framing error	-
3	M_wt	0	1: Mask IRQ due to wake-up timer interrupt	-
2	M_wam	0	1: Mask Wake-up IRQ due to amplitude measurement	-
1	M_wph	0	1: Mask Wake-up IRQ due to phase measurement.	-
0	M_wcap	0	1: Mask Wake-up IRQ due to capacitance measurement	-

4.3.33 Mask passive target interrupt register

Register space: A

Address: 19h

Type: RW

Table 51. Mask error and wake-up interrupt register

Bit	Name	Default	Function	Comments
7	M_ppon2	0	1: Mask IRQ from PPON2 field on waiting timer	-
6	M_sl_wl	0	1: Mask IRQ for Passive target slot number water level	-
5	M_apon	0	1: Mask IRQ due to Active PP Field on event	-
4	M_rxe_pta	0	1: Mask IRQ due to end of receive when the device is handling the response	-
3	M_wu_f	0	1: Mask IRQ NFC 212/424 kb/s passive target active	-
2	RFU	0	-	-
1	M_wu_a*	0	1: Mask IRQ NFC 106 kb/s passive target Active*	-
0	M_wu_a	0	1: Mask IRQ NFC 106 kb/s passive target Active	-

4.3.34 Main interrupt register

Register space: A

Address: 1Ah

Type: R

Table 52. Main interrupt register

Bit	Name	Default	Function	Comments
7	I_osc	-	IRQ when oscillator frequency is stable	Set after oscillator is started by setting *Operation control register* bit en.
6	I_wl	-	IRQ due to FIFO water level	Set during receive, if more than 300 bytes are in the FIFO. Set during transmit, if less than 200 bytes are in the FIFO.
5	I_rxs	-	IRQ due to start of receive	-
4	I_rxe	-	IRQ due to end of receive	-
3	I_txe	-	IRQ due to end of transmission	-
2	I_col	-	IRQ due to bit collision	-
1	I_rx_rest	-	IRQ due to automatic reception restart	Set when a frame is suppressed as EMD
0	RFU	-	-	-

4.3.35 Timer and NFC interrupt register

Register space: A

Address: 1Bh

Type: R

Table 53. Timer and NFC interrupt register(1)

Bit	Name	Default	Function	Comments
7	I_dct	-	IRQ due to termination of direct command	-
6	I_nre	-	IRQ due to No-response timer expire	-
5	I_gpe	-	IRQ due to general purpose timer expire	-
4	I_eon	-	IRQ due to detection of external field higher than Target activation level	-
3	I_eof	-	IRQ due to detection of external field drop below Target activation level	-
2	I_cac	-	IRQ due to detection of collision during RF Collision Avoidance	-
1	I_cat	-	IRQ after minimum guard time expire	An external field was not detected during RF collision avoidance, field was switched on, IRQ sent after minimum guard time according to NFCIP-1.
0	I_nfct	-	IRQ when in target mode the initiator bit rate was recognized	-

1. After register has been read, its content is set to 0.

4.3.36 Error and wake-up interrupt register

Register space: A

Address: 1Ch

Type: R

Table 54. Error and wake-up interrupt register(1)

Bit	Name	Default	Function	Comments
7	I_crc	-	CRC error	-
6	I_par	-	Parity error	-
5	I_err2	-	Soft framing error	Framing error that does not result in corrupted Rx data.
4	I_err1	-	Hard framing error	Framing error that results in corrupted Rx data.
3	I_wt	-	Wake-up timer interrupt	Timeout after execution of Start Wake-Up Timer command in case option with IRQ at every timeout is selected.
2	I_wam	-	Wake-up interrupt due to amplitude measurement	Result of amplitude measurement Δam larger than reference.
1	I_wph	-	Wake-up interrupt due to phase measurement.	Result of phase measurement Δpm larger than reference.
0	I_wcap	-	Wake-up interrupt due to capacitance measurement	Result of capacitance measurement Δcm larger than reference.

1. After Main Interrupt Register has been read, its content is set to 0.

4.3.37 Passive target interrupt register

Register space: A

Address: 1Dh

Type: R

Table 55. Passive target interrupt register(1)

Bit	Name	Default	Function	Comments
7	I_ppon2	-	PPON2 field on waiting timer interrupt	-
6	I_sl_wl	-	IRQ for passive target slot number water level	Sent if four unused slot numbers (TSN) remain in PT_memory.
5	I_apon	-	IRQ due to active P2P field on event	Sent after RF collision avoidance, if there was no collision and field was turned on.
4	I_rxe_pta	-	IRQ due to end of receive, 3916 is handling the response	Sent in passive target mode when NFC-A anti-collision or NFC-F SENSF_RES is automatically sent (MCU action required).
3	I_wu_f	-	NFC 212/424kb/s Passive target ‘Active’ interrupt	Sent after NFC 212/424 kb/s automatic response to SENSF_REQ was sent.
2	RFU	-	RFU	-
1	I_wu_a*	-	Passive target Active* interrupt	Sent when Active* state is reached.
0	I_wu_a	-	Passive target Active interrupt	Sent when Active state is reached.

1. After register has been read, its content is set to 0.

4.3.38 FIFO status register 1

Register space: A

Address: 1Eh

Type: R

Table 56. FIFO status register 1

Bit	Name	Default	Function	Comments
7	fifo_b7	-	Number of bytes in the FIFO (LSB)	Valid range is from 0 to 512.
6	fifo_b6	-		
5	fifo_b5	-		
4	fifo_b4	-		
3	fifo_b3	-		
2	fifo_b2	-		
1	fifo_b1	-		
0	fifo_b0	-		

4.3.39 FIFO status register 2

Register space: A

Address: 1Fh

Type: R

Table 57. FIFO status register 2

Bit	Name	Default	Function	Comments
7	fifo_b9	-	Number of bytes in the FIFO (MSB)	-
6	fifo_b8	-		-
5	fifo_unf	-	1: FIFO underflow	-
4	fifo_ovr	-	1: FIFO overflow	-
3	fifo_lb2	-	Number of bits in the last FIFO byte if it was not complete	The received bits are stored in the LSB part of the last byte in the FIFO. If I_err1 is set then fifo_lb<2:0> dos not contain valid data.
2	fifo_lb1	-		
1	fifo_lb0	-		
0	np_lb	-	1: Parity bit is missing in the last byte	The bit is set if the last received byte is complete with 8 data bits but he parity bit is missing. If I_err1 is set then np_lb does not contain valid data.

4.3.40 Collision display register

Register space: A

Address: 20h

Type: R

Table 58. Collision display register

Bit	Name	Default	Function	Comments
7	c_byte3	-	Number of full bytes before the bit collision happened.	The *Collision display register* range covers ISO14443A anticollision command. If collision (or framing error interpreted as collision) happens in a longer message, the *Collision display register* is not set. If I_err1 is set then c_byte<3:0> and c_bit<2:0> do not contain valid data.
6	c_byte2	-		
5	c_byte1	-		
4	c_byte0	-		
3	c_bit2	-	Number of bits before the collision in the byte where the collision happened	
2	c_bit1	-		
1	c_bit0	-		
0	c_pb	-	1: Collision in parity bit	This error is reported if the first detected collision is in a parity bit. If I_err1 is set then c_pb dos not contain valid data.

4.3.41 Passive target display register

Register space: A

Address: 21h

Type: R

Table 59. Passive target display register

Bit	Name	Default	Function	Comments
7	RFU	-	-	-
6	RFU	-	-	-
5	RFU	-	-	-
4	RFU	-	-	-
3	pta_state3	-	0000: POWER OFF 0001: IDLE 0010: READY_L1 0011: READY_L2 0100: RFU 0101:ACTIVE 0110: RFU 1001: HALT 1010: READY_L1* 1011: READY_L2* 1100: RFU 1101: ACTIVE*	ISO-A passive target states. In ACTIVE or ACTIVE* state, the MCU must handle all commands, including SENSE/IDLE and SLEEP/HALT.
2	pta_state2	-		
1	pta_state1	-		
0	pta_state0	-		

4.3.42 Number of transmitted bytes register 1

Register space: A

Address: 22h

Type: RW

Table 60. Number of transmitted bytes register 1

Bit	Name	Default	Function	Comments
7	ntx12	0	Number of full bytes to be transmitted, MSB bits	Maximum supported number of bytes is 8191.
6	ntx11	0		
5	ntx10	0		
4	ntx9	0		
3	ntx8	0		
2	ntx7	0		
1	ntx6	0		
0	ntx5	0		

4.3.43 Number of transmitted bytes register 2

Register space: A

Address: 23h

Type: RW

Table 61. Number of transmitted bytes register 2(1) (2)

Bit	Name	Default	Function	Comments
7	ntx4	0	Number of full bytes to be transmitted, MSB bits	Maximum supported number of bytes is 8191.
6	ntx3	0		
5	ntx2	0		
4	ntx1	0		
3	ntx0	0		
2	nbtx2	0	Number of bits to transmit after the last full byte. Set to 000 to transmit only full bytes.	Bit transmission starts from LSB. Applicable for ISO14443A: – bit oriented anticollision frame in case last byte is a split byte – Tx is done without parity bit generation – passive target: 4-bit ACK, NACK
1	nbtx1	0		
0	nbtx0	0		

1. If anctl bit is set while card is in idle state and nbtx is not 000, then i_par will be triggered during REQA and WUPA direct command is issued.
2. Transmission of short or incomplete messages only works for ISO-A/B using the command Transmit without CRC.

4.3.44 Bit rate detection display register

Register space: A

Address: 24h

Type: R

Table 62. Bit rate detection display register

Bit	Name	Default	Function	Comments
7	RFU	-	-	-
6	RFU	-	-	-
5	nfc_rate1	-	Refer to *Table 16*	Result of automatic bit rate detection in the bit rate detection target mode.
4	nfc_rate0	-		
3	ppt2_on	-	1: PP_{ON2} timer is running	State of internal timers.
2	gpt_on	-	1: General purpose timer is running	
1	nrt_on	-	1: No-response timer is running	
0	mrt_on	-	1: Mask receive timer is running	

4.3.45 A/D converter output register

Register space: A

Address: 25h

Type: R

Table 63. A/D converter output register

Bit	Name	Default	Function	Comments
7	ad7	-	Displays result of last A/D conversion.	-
6	ad6	-		
5	ad5	-		
4	ad4	-		
3	ad3	-		
2	ad2	-		
1	ad1	-		
0	ad0	-		

4.3.46 Antenna tuning control register 1

Register space: A

Address: 26h

Type: R

Table 64. Antenna tuning control register 1

Bit	Name	Default	Function	Comments
7	aat_A_7	1	AAT-A D/A converter input.	AAT-A voltage (in V) = (0.044 + 0.868 * aat_A<7:0> / 255) * V_{DD_A}
6	aat_A_6	0		
5	aat_A_5	0		
4	aat_A_4	0		
3	aat_A_3	0		
2	aat_A_2	0		
1	aat_A_1	0		
0	aat_A_0	0		

4.3.47 Antenna tuning control register 2

Register space: A

Address: 27h

Type: R

Table 65. Antenna tuning control register 2

Bit	Name	Default	Function	Comments
7	aat_B_7	1	AAT-B D/A converter input.	AAT-B voltage (in V) = (0.044 + 0.868 * aat_B<7:0> / 255) * V_{DD_A}
6	aat_B_6	0		
5	aat_B_5	0		
4	aat_B_4	0		
3	aat_B_3	0		
2	aat_B_2	0		
1	aat_B_1	0		
0	aat_B_0	0		

4.3.48 TX driver register

Register space: A

Address: 28h

Type: RW

Table 66. TX driver register

Bit	Name	Default	Function	Comments
7	am_mod3	0	AM modulation index (see *Table 67*)	-
6	am_mod2	1		
5	am_mod1	1		
4	am_mod0	1		
3	d_res3	0	RFO driver resistance (see *Table 68*)	-
2	d_res2	0		
1	d_res1	0		
0	d_res0	0		

Table 67. AM modulation index

am_mod<3:0>	Modulation (%)
0	5
1	6
2	7
3	8
4	9
5	10
6	11
7	12
8	13
9	14
10	15
11	17
12	19
13	22
14	26
15	40

Table 68. RFO driver resistance

d_res<3:0>	Driver output resistance (Ω)
0	1.0
1	2.0
2	4.1
3-4	8.3
5-14	17.1
15	High Z

4.3.49 Passive target modulation register

Register space: A

Address: 29h

Type: RW

Table 69. AM Modulation Depth display register

Bit	Name	Default	Function	Comments
7	ptm_res3	0	Refer to *Table 70*	RFO resistance during passive load modulation, modulated state. ptm_res<3:0> must be set before the *Mode definition register* is set to passive target mode.
6	ptm_res2	1		
5	ptm_res1	1		
4	ptm_res0	1		
3	pt_res3	0		RFO resistance during passive load modulation, unmodulated state. pt_res<3:0> must be set before the *Mode definition register* is set to passive target mode.
2	pt_res2	0		
1	pt_res1	0		
0	pt_res0	0		

Table 70. Passive target modulated and unmodulated state driver output resistance

ptm_res<3:0> pt_res<3:0>	Driver output resistance R_{RFO} (Ω)
0	1.0
1	2.0
2	4.1
3	8.3
4	12.2
5	17.1
6	25.6
7	32.0
8	36.6
9	42.7
10	51.2
11	64.0
12	85.3
13	128.0
14	256.0
15	High Z

4.3.50 Auxiliary modulation setting register

Register space: B

Address: 28h

Type: RW

Table 71. Auxiliary modulation setting register

Bit	Name	Default	Function	Comments
7	dis_reg_am	0	0: Regulator AM enabeld 1: Regulator AM disabled	Uses am_mod<3:0> to set the modulation index for regulator based AM modulation. Logic of this bit is inverted. Set to 0 to enable regulator AM.
6	lm_ext_pol	0	0: Normal polarity 1: Inverse polarity	Normal polarity: LM_EXT pin load modulation signal is active high. Inverse polarity: LM_EXT pin load modulation signal is active low.
5	lm_ext	0	0: External load modulation disabled 1: External load modulation enabled	Enables output of load modulation signal on LM_EXT pin.
4	lm_dri	1	0: Driver load modulation disabled 1: Driver load modulation enabled	Uses *Passive target modulation register* to set driver load modulation resistance.
3	res_am	0	0: Resistive AM modulation disabled 1: Resistive AM modulation enabled	Uses md_res<6:0> to configure resistive AM modulated driver resistance.
2	RFU	0	-	-
1	RFU	0	-	-
0	RFU	0	-	-

4.3.51 TX driver timing register

Register space: B

Address: 29h

Type: RW

Table 72. TX driver timing register

Bit	Name	Default	Function	Comments
7	d_rat_t3	0	Driver transient ratio target (in number of non-overlap times in one RF period)	The value presents the target ratio between one RF period and whole non-overlap time (both sides L to H and H to L). The system starts with the slowest available transient and measures the ratio. If this is lower than targeted the system switches to faster transient. The procedure is repeated until the target ratio is reached (or exceeded for the first time). There are five steps available, procedure can take up to ten RF periods.
6	d_rat_t2	1		
5	d_rat_t1	1		
4	d_rat_t0	1		
3	d_tim_man	1	0: Use automatically acquired timing setting 1: Use manual timing setting	-
2	d_tim_m2	1	000: Slow 001: Medium slow 010: Nominal 011: Medium fast 1xx: Fast	Manual driver timing, used if d_tim_man is set to 1.
1	d_tim_m1	0		
0	d_tim_m0	0		

4.3.52 Resistive AM modulation register

Register space: B

Address: 2Ah

Type: RW

Table 73. Resistive AM modulation register

Bit	Name	Default	Function	Comments
7	fa3_f	0	0: Use normal non-overlap 1: Use minimum non-overlap	-
6	md_res6	0	Refer to *Table 74*.	Resistive AM modulated state driver output resistance.
5	md_res5	0		
4	md_res4	0		
3	md_res3	0		
2	md_res2	0		
1	md_res1	0		
0	md_res0	0		

Table 74. Resistive AM modulated state driver output resistance

md_res<6:0>	Driver output resistance R_{RFO} (Ω)	md_res<6:0>	Driver output resistance R_{RFO} (Ω)
0	4.063	32	8.258
1	4.129	33	8.533
2	4.197	34	8.828
3	4.267	35	9.143
4	4.339	36	9.481
5	4.414	37	9.846
6	4.491	38	10.240
7	4.571	39	10.667
8	4.655	40	11.130
9	4.741	41	11.636
10	4.830	42	12.190
11	4.923	43	12.800
12	5.020	44	13.474
13	5.120	45	14.222
14	5.224	46	15.059
15	5.333	47	16.000
16	5.447	48	17.067
17	5.565	49	18.286

Table 74. Resistive AM modulated state driver output resistance (continued)

md_res<6:0>	Driver output resistance R_{RFO} (Ω)	md_res<6:0>	Driver output resistance R_{RFO} (Ω)
18	5.689	50	19.692
19	5.818	51	21.333
20	5.953	52	23.273
21	6.095	53	25.600
22	6.244	54	28.444
23	6.400	55	32.000
24	6.564	56	36.571
25	6.737	57	42.667
26	6.919	58	51.200
27	7.111	59	64.000
28	7.314	60	85.333
29	7.529	61	128.000
30	7.758	62	256.000
31	8.000	63	High Z

4.3.53 TX driver timing display register

Register space: B

Address: 2Bh

Type: R

Table 75. TX driver timing display register

Bit	Name	Default	Function	Comments
7	d_rat_r3	-	Driver Transient ratio readout (in number of non-overlap times in one RF period)	Driver transient ratio readout
6	d_rat_r2	-		
5	d_rat_r1	-		
4	d_rat_r0	-		
3	RFU	-	-	-
2	d_tim_r2	-	000: Slow 001: Medium slow 010: Nominal 011: Medium fast 1xx: Fast	Driver timing readout
1	d_tim_1	-		
0	d_tim_0	-		

4.3.54 External field detector activation threshold register

Register space: A

Address: 2Ah

Type: RW

Table 76. External field detector activation threshold register

Bit	Name	Default	Function	Comments
7	RFU	0	Not used	-
6	trg_l2	0	Peer detection threshold. Refer to *Table 78*.	-
5	trg_l1	1		
4	trg_l0	1		
3	rfe_t3	0	Collision avoidance threshold. Refer to *Table 79*.	-
2	rfe_t2	0		
1	rfe_t1	1		
0	rfe_t0	1		

4.3.55 External field detector deactivation threshold register

Register space: A

Address: 2Bh

Type: RW

Table 77. External field detector deactivation threshold register

Bit	Name	Default	Function	Comments
7	RFU	0	Not used	-
6	trg_ld2	0	Deactivation peer detection threshold (see *Table 78*).	-
5	trg_ld1	1		
4	trg_ld0	1		
3	rfe_td3	0	Deactivation collision avoidance threshold (see *Table 79*).	-
2	rfe_td2	0		
1	rfe_td1	1		
0	rfe_td0	1		

Table 78. Peer detection threshold as seen on RFI1 input

trg_l2	trg_l1	trg_l0	Peer detection threshold voltage (mV_{pp}) on RFI1
0	0	0	75
0	0	1	105
0	1	0	150
0	1	1	205
1	0	0	290
1	0	1	400
1	1	0	560
1	1	1	800

Table 79. Collision avoidance threshold as seen on RFI1 input

rfe_3	rfe_2	rfe_1	rfe_0	Collision avoidance threshold voltage (mV_{pp}) on RFI1
0	0	0	0	75
0	0	0	1	105
0	0	1	0	150
0	0	1	1	205
0	1	0	0	290
0	1	0	1	400
0	1	1	0	560
0	1	1	1	800
1	0	0	0	25
1	0	0	1	33
1	0	1	0	47
1	0	1	1	64
1	1	0	0	90
1	1	0	1	125
1	1	1	0	175
1	1	1	1	250

4.3.56 Regulator voltage control register

Register space: A

Address: 2Ch

Type: RW

Table 80. Regulator voltage control register

Bit	Name	Default	Function	Comments
7	reg_s	0	0: Regulated voltages are defined by result of Adjust Regulators command 1: Regulated voltages are defined by rege_x bits written in this register	Defines mode of regulator voltage setting.
6	rege_3	0	External definition of regulated voltage (see *Table 82*). In 5 V mode V_{SP_D} and V_{SP_A} regulators are set to 3.4 V	In 5 V mode V_{DD_D} and V_{DD_A} regulators are set to 3.4 V. In 3.3 V mode V_{DD_D} and V_{DD_A} regulators are set to the same value as V_{DD_RF}.
5	rege_2	0		
4	rege_1	0		
3	rege_0	0		
2	mpsv2	0	000: V_{DD} 001: V_{DD_A} 010: V_{DD_D} 011: V_{DD_RF} 100: V_{DD_AM} 101: RFU 110: RFU 111: RFU	Defines source of direct command *Measure Power Supply*.
1	mpsv1	0		
0	mpsv0	0		

4.3.57 Regulator display register

Register space: B

Address: 2Ch

Type: R

Table 81. Regulator display register

Bit	Name	Default	Function	Comments
7	reg_3	-	Voltage regulator setting after *Adjust Regulators* command. Refer to *Table 82* for definition.	-
6	reg_2	-		
5	reg_1	-		
4	reg_0	-		
3	RFU	-	-	-
2	RFU	-	-	-
1	RFU	-	-	-
0	i_lim	-	1: V_{DD_RF} regulator in current limit mode	-

Table 82. Regulated voltages

reg_3	reg_2	reg_1	reg_0	Typical regulated voltage (V)	
rege_3	rege_2	rege_1	rege_0	5 V mode	3.3 V mode
1	1	1	1	5.1	3.4
1	1	1	0	5.0	3.3
1	1	0	1	4.9	3.2
1	1	0	0	4.8	3.1
1	0	1	1	4.7	3.0
1	0	1	0	4.6	2.9
1	0	0	1	4.5	2.8
1	0	0	0	4.4	2.7
0	1	1	1	4.3	2.6
0	1	1	0	4.2	2.5
0	1	0	1	4.1	2.4
0	1	0	0	4.0	-
0	0	1	1	3.9	-
0	0	1	0	3.8	-
0	0	0	1	3.7	-
0	0	0	0	3.6	-

4.3.58 RSSI display register

Register space: A

Address: 2Dh

Type: R

Table 83. RSSI display register

Bit	Name	Default	Function	Comments
7	rssi_am_3	-	AM channel RSSI peak value. Refer to *Table 84* for definition.	Stores the AM channel RSSI peak value until the start of the next reception, or until the *Clear RSSI* command is sent.
6	rssi_am_2	-		
5	rssi_am_1	-		
4	rssi_am_0	-		
3	rssi_pm_3	-	PM channel RSSI peak value. Refer to *Table 84* for definition.	Stores the PM channel RSSI peak value until the start of the next reception, or until the *Clear RSSI* command is sent.
2	rssi_pm_2	-		
1	rssi_pm_1	-		
0	rssi_pm_0	-		

Table 84. RSSI

rssi_3	rssi_2	rssi_1	rssi_0	Typical signal on RFI1 (mV_{rms})
0	0	0	0	≤20
0	0	0	1	>20
0	0	1	0	>27
0	0	1	1	>37
0	1	0	0	>52
0	1	0	1	>72
0	1	1	0	>99
0	1	1	1	>136
1	0	0	0	>190
1	0	0	1	>262
1	0	1	0	>357
1	0	1	1	>500
1	1	0	0	>686
1	1	0	1	>950
1	1	1	0	>1150
1	1	1	1	

4.3.59 Gain reduction state register

Register space: A

Address: 2Eh

Type: R

Table 85. Gain reduction state register

Bit	Name	Default	Function	Comments
7	gs_am_3	-	Refer to rg2_am<3:0> for value explanation.	Overall AM channel second and third stage gain reduction (includes register gain reduction, squelch and AGC).
6	gs_am_2	-		
5	gs_am_1	-		
4	gs_am_0	-		
3	gs_pm_3	-	Refer to rg2_pm<3:0> for value explanation.	Overall PM channel second and third stage gain reduction (includes register gain reduction, squelch and AGC).
2	gs_pm_2	-		
1	gs_pm_1	-		
0	gs_pm_0	-		

4.3.60 Capacitive sensor control register

Register space: A

Address: 2Fh

Type: RW

Table 86. Capacitive sensor control register

Bit	Name	Default	Function	Comments
7	cs_mcal4	0	1.6 pF	Manual capacitive sensor calibration value (binary weighted). Sets cs_mcal<4:0> to 0 to enable automatic calibration mode.
6	cs_mcal3	0	0.8 pF	
5	cs_mcal2	0	0.4 pF	
4	cs_mcal1	0	0.2 pF	
3	cs_mcal0	0	0.1 pF	
2	cs_g2	0	000: 2.8 V / pF 001: 6.5 V / pF 010: 1.1 V / pF 100: 0.5 V / pF 110: 0.35 V / pF Others: Not used	Capacitor sensor gain.
1	cs_g1	0		
0	cs_g0	0		

4.3.61 Capacitive sensor display register

Register space: A

Address: 30h

Type: R

Table 87. Capacitive sensor display register

Bit	Name	Default	Function	Comments
7	cs_cal4	-	1.6 pF	Capacitive sensor calibration value (binary weighted).
6	cs_cal3	-	0.8 pF	
5	cs_cal2	-	0.4 pF	
4	cs_cal1	-	0.2 pF	
3	cs_cal0	-	0.1 pF	
2	cs_cal_end	-	1: Calibration ended	-
1	cs_cal_err	-	1: Calibration error	-
0	RFU	-	-	-

4.3.62 Auxiliary display register

Register space: A

Address: 31h

Type: R

Table 88. Auxiliary display register

Bit	Name	Default	Function	Comments
7	a_cha	-	0: AM 1: PM	Receiver channel used in ongoing/last reception.
6	efd_o	-	1: External field detected	External field detector output.
5	tx_on	-	1: Transmission is active	Data transmission due to automatic handling of CE mode collision avoidance are not indicated.
4	osc_ok	-	1: Xtal oscillation is stable	Indication that Xtal oscillator is active and its output is stable.
3	rx_on	-	1: Receive decoder is enabled	-
2	rx_act	-	1: Receive decoder is receiving a message	-
1	en_peer	-	1: External Field Detector is active in Peer detection mode	-
0	en_ac	-	1: External Field Detector is active in RF Collision Avoidance mode	-

4.3.63 Overshoot protection configuration register 1

Register space: B

Address: 30h

Type: RW

Table 89. Overshoot protection configuration register 1

Bit	Name	Default	Function	Comments
7	ov_tx_mode1	0	00: Drive with V_{DD_DR} 01: Drive with V_{DD_AM} 10: Driver stop (at GND / V_{DD_DR}) 11: RFU	Selects RF drive level to apply when ov_patternX is set to 1.
6	ov_tx_mode0	0		
5	ov_pattern13	0	-	-
4	ov_pattern12	0	-	-
3	ov_pattern11	0	-	-
2	ov_pattern10	0	-	-
1	ov_pattern9	0	-	-
0	ov_pattern8	0	-	-

4.3.64 Overshoot protection configuration register 2

Register space: B

Address: 31h

Type: RW

Table 90. Overshoot protection configuration register 2

Bit	Name	Default	Function	Comments
7	ov_pattern7	0	-	-
6	ov_pattern6	0	-	-
5	ov_pattern5	0	-	-
4	ov_pattern4	0	-	-
3	ov_pattern3	0	-	-
2	ov_pattern2	0	-	-
1	ov_pattern1	0	-	-
0	ov_pattern0	0	-	-

4.3.65 Undershoot protection configuration register 1

Register space: B

Address: 32h

Type: RW

Table 91. Undershoot protection configuration register 1

Bit	Name	Default	Function	Comments
7	un_tx_mode1	0	00: Drive with V_{DD_DR} 01: Drive with V_{DD_AM} 10: Driver stop (at GND / V_{DD_DR}) 11: RFU	Selects RF drive level to apply when un_patternX is set to 1.
6	un_tx_mode0	0		
5	un_pattern13	0	-	-
4	un_pattern12	0	-	-
3	un_pattern11	0	-	-
2	un_pattern10	0	-	-
1	un_pattern9	0	-	-
0	un_pattern8	0	-	-

4.3.66 Undershoot protection configuration register 2

Register space: B

Address: 33h

Type: RW

Table 92. Overshoot protection configuration register 2

Bit	Name	Default	Function	Comments
7	un_pattern7	0	-	-
6	un_pattern6	0	-	-
5	un_pattern5	0	-	-
4	un_pattern4	0	-	-
3	un_pattern3	0	-	-
2	un_pattern2	0	-	-
1	un_pattern1	0	-	-
0	un_pattern0	0	-	-

4.3.67 Wake-up timer control register

Register space: A

Address: 32h

Type: RW

Table 93. Wake-up timer control register

Bit	Name	Default	Function	Comments
7	wur	0	0: 100 ms 1: 10 ms	Wake-up timer range
6	wut2	0	Refer to *Table 94*	Wake-up timer timeout value
5	wut1	0		
4	wut0	0		
3	wto	0	1: IRQ at every timeout	-
2	wam	0	1: At timeout perform amplitude measurement	Generates I_wam interrupt if amplitude difference is larger than Δam.
1	wph	0	1: At timeout perform phase measurement	Generates I_wph interrupt if phase difference islarger than Δpm.
0	wcap	0	1: At timeout perform capacitance measurement	Generates I_wcap interrupt if capacitance difference is larger than Δcm.

Table 94. Typical wake-up time

wut2	wut1	wut0	100 ms range (wur = 0)	10 ms range (wur = 1)
0	0	0	100 ms	10 ms
0	0	1	200 ms	20 ms
0	1	0	300 ms	30 ms
0	1	1	400 ms	40 ms
1	0	0	500 ms	50 ms
1	0	1	600 ms	60 ms
1	1	0	700 ms	70 ms
1	1	1	800 ms	80 ms

4.3.68 Amplitude measurement configuration register

Register space: A

Address: 33h

Type: RW

Table 95. Amplitude measurement configuration register

Bit	Name	Default	Function	Comments
7	am_d3	0	Definition of Δam (difference vs. reference that triggers interrupt)	-
6	am_d2	0		
5	am_d1	0		
4	am_d0	0		
3	am_aam	0	0: Exclude the IRQ measurement 1: Include the IRQ measurement	Includes/excludes the measurement that causes IRQ (having difference > Δam to reference) in auto-averaging.
2	am_aew1	0	00: 4 01: 8 10: 16 11: 32	Weight of last measurement result for auto-averaging.
1	am_aew2	0		
0	am_ae	0	0: Use *Amplitude measurement reference register*	Selects reference value for amplitude measurement Wake-Up mode.

4.3.69 Amplitude measurement reference register

Register space: A

Address: 34h

Type: RW

Table 96. Amplitude measurement reference register

Bit	Name	Default	Function	Comments
7	am_ref7	0	-	-
6	am_ref6	0	-	-
5	am_ref5	0	-	-
4	am_ref4	0	-	-
3	am_ref3	0	-	-
2	am_ref2	0	-	-
1	am_ref1	0	-	-
0	am_ref0	0	-	-

4.3.70 Amplitude measurement auto-averaging display register

Register space: A

Address: 35h

Type: R

Table 97. Amplitude measurement auto-averaging display register

Bit	Name	Default	Function	Comments
7	amd_aad7	0	-	-
6	amd_aad6	0	-	-
5	amd_aad5	0	-	-
4	amd_aad4	0	-	-
3	amd_aad3	0	-	-
2	amd_aad2	0	-	-
1	amd_aad1	0	-	-
0	amd_aad0	0	-	-

4.3.71 Amplitude measurement display register

Register space: A

Address: 36h

Type: R

Table 98. Amplitude measurement display register

Bit	Name	Default	Function	Comments
7	am_amd7	0	-	-
6	am_amd6	0	-	-
5	am_amd5	0	-	-
4	am_amd4	0	-	-
3	am_amd3	0	-	-
2	am_amd2	0	-	-
1	am_amd1	0	-	-
0	am_amd0	0	-	-

4.3.72 Phase measurement configuration register

Register space: A

Address: 37h

Type: RW

Table 99. Phase measurement configuration register

Bit	Name	Default	Function	Comments
7	pm_d3	0	Definition of Δpm (difference to reference that triggers interrupt)	-
6	pm_d2	0		
5	pm_d1	0		
4	pm_d0	0		
3	pm_aam	0	0: Exclude the IRQ measurement 1: Include the IRQ measurement	Includes/excludes the measurement value that triggered the I_wph interrupt in the auto-averaging.
2	pm_aew1	0	00: 4 01: 8 10: 16 11: 32	Weight of last measurement result for auto-averaging.
1	pm_aew0	0		
0	pm_ae	0	0: Use *Phase measurement reference register* 1: Use phase measurement auto-averaging as reference	Selects reference value for phase measurement Wake-Up mode.

4.3.73 Phase measurement reference register

Register space: A

Address: 38h

Type: RW

Table 100. Phase measurement reference register

Bit	Name	Default	Function	Comments
7	pm_ref7	0	-	-
6	pm_ref6	0	-	-
5	pm_ref5	0	-	-
4	pm_ref4	0	-	-
3	pm_ref3	0	-	-
2	pm_ref2	0	-	-
1	pm_ref1	0	-	-
0	pm_ref0	0	-	-

4.3.74 Phase measurement auto-averaging display register

Register space: A

Address: 39h

Type: R

Table 101. Phase measurement auto-averaging display register

Bit	Name	Default	Function	Comments
7	pm_aad7	0	-	-
6	pm_aad6	0	-	-
5	pm_aad5	0	-	-
4	pm_aad4	0	-	-
3	pm_aad3	0	-	-
2	pm_aad2	0	-	-
1	pm_aad1	0	-	-
0	pm_aad0	0	-	-

4.3.75 Phase measurement display register

Register space: A

Address: 3Ah

Type: R

Table 102. Phase measurement display register

Bit	Name	Default	Function	Comments
7	pm_amd7	0	0	-
6	pm_amd6	0	0	-
5	pm_amd5	0	0	-
4	pm_amd4	0	0	-
3	pm_amd3	0	0	-
2	pm_amd2	0	0	-
1	pm_amd1	0	0	-
0	pm_amd0	0	0	-

4.3.76 Capacitance measurement configuration register

Register space: A

Address: 3Bh

Type: RW

Table 103. Capacitance measurement configuration register

Bit	Name	Default	Function	Comments
7	cm_d3	0	Definition of Δcm (difference to reference that triggers interrupt)	-
6	cm_d2	0		
5	cm_d1	0		
4	cm_d0	0		
3	cm_aam	0	0: Exclude the IRQ measurement 1: Include the IRQ measurement	Includes/excludes the measurement that causes IRQ (having difference > Δcm to reference) in auto-averaging.
2	cm_aew1	0	00: 4 01: 8 10: 16 11: 32	Weight of last measurement result for auto-averaging.
1	cm_aew0	0		
0	cm_ae	0	0: Use *Capacitance measurement reference register* 1: Use capacitance measurement auto-averaging as reference	Selects reference value for capacitance measurement Wake-Up mode.

4.3.77 Capacitance measurement reference register

Register space: A

Address: 3Ch

Type: RW

Table 104. Capacitance measurement reference register

Bit	Name	Default	Function	Comments
7	cm_ref7	0	-	-
6	cm_ref6	0	-	-
5	cm_ref5	0	-	-
4	cm_ref4	0	-	-
3	cm_ref3	0	-	-
2	cm_ref2	0	-	-
1	cm_ref1	0	-	-
0	cm_ref0	0	-	-

4.3.78 Capacitance measurement auto-averaging display register

Register space: A

Address: 3Dh

Type: R

Table 105. Capacitance measurement auto-averaging display register

Bit	Name	Default	Function	Comments
7	cm_aad7	0	-	-
6	cm_aad6	0	-	-
5	cm_aad5	0	-	-
4	cm_aad4	0	-	-
3	cm_aad3	0	-	-
2	cm_aad2	0	-	-
1	cm_aad1	0	-	-
0	cm_aad0	0	-	-

4.3.79 Capacitance measurement display register

Register space: A

Address: 3Eh

Type: R

Table 106. Capacitance measurement display register

Bit	Name	Default	Function	Comments
7	cm_amd7	0	-	-
6	cm_amd6	0	-	-
5	cm_amd_	0	-	-
4	cm_amd_	0	-	-
3	cm_amd3	0	-	-
2	cm_amd2	0	-	-
1	cm_amd1	0	-	-
0	cm_amd0	0	-	-

4.3.80 IC identity register

Register space: A

Address: 3Fh

Type: R

Table 107. IC identity register

Bit	Name	Default	Function	Comments
7	ic_type4	0	IC type code 00101: ST25R3916	5-bit IC type code
6	ic_type3	0		
5	ic_type2	1		
4	ic_type1	0		
3	ic_type0	1		
2	ic_rev2	0	IC revision code 010: rev 3.1	3-bit IC revision code
1	ic_rev1	1		
0	ic_rev0	0		

5 Electrical characteristics

5.1 Absolute maximum ratings

Stresses beyond the limits listed in *Table 108* may cause permanent damage to the device. These are stress ratings only.

Functional operation of the device at these or any other conditions beyond those indicated in *Table 108* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 108. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}, V_{DD_TX}(1)	Positive supply voltage	-0.3	6.0	V
V_{DDs3v}, V_{DD_TXs3v}(1)	Positive supply voltage in case option bit sup3V is set	-0.3	5	
$\Delta_{VDD-VDD\_TX}$(1)	Difference between V_{DD} and V_{DD_TX}	-0.3	0.3	
V_{DD_IO}(1)	Peripheral communication supply voltage	-0.3	6	
V_{GND}(1)	Negative supply voltage	-0.3	0.3	
V_{pIO} (1)	Voltage for peripheral IO communication pins (27 to 32)	-0.3	6	
V_{p5V} (1)	Voltage for other pins (9, 11, 13, 14, 15, 17 and 20) in the 5 V domain	-0.3	6	
V_{p3V} (1)	Voltage for other pins (2 to 5, 7, 18, 19 and 22 to 25) in the 3 V domain	-0.3	5	
I_{scr}	Input current (latch-up immunity) according to JESD78D	-100	100	mA
ESD voltage	Electrostatic discharge voltage according to JS-001-2014, human body model	-	2000	V
P_t	Total power dissipation (all supplies and outputs)	-	300	mW
T_{strg}	Storage temperature	-55	125	°C
T_{body}	Package body temperature according to IPC/JEDEC J-STD-020C(2)	-	260	
-	Humidity non-condensing	5	85	%

1. Referenced to V_{SS}.
2. The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020C “Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices”.

5.2 Operating conditions

All defined tolerances for external components in this specification need to be ensured over the whole operation conditions range and also over lifetime.

Table 109. Operating conditions

Symbol	Parameter	Min	Max	Unit
V_{DD}, V_{DD_TX}[1] [2]	Positive supply voltage (pins 8 and 10)	2.4	5.5	V
V_{DD_DR}[1]	Driver positive supply voltage when driver is directly supplied (pin 14) Mandatory condition: $V_{DD\_DR} \leq V_{DD}$, V_{DD_TX}	2.4	5.5	
V_{DDs3v}, V_{DD_TXs3v}[1]	Positive supply voltage when option bit sup3V is set	2.4	3.6	
$\Delta_{VDD\text{-}VDD\_TX}$[1]	Difference between V_{DD} and V_{DD_TX}	-0.2	0.2	
V_{DD_IO}[1]	Peripheral communication supply voltage (pin 1)	1.65	5.5	
V_{GND}[1]	Negative supply voltage (pins 6, 12, 16 and 26)	0	0	
V_{pIO}[1]	Voltage for peripheral IO communication pins (27 to 32)	0	5.5	
V_{p5V}[1]	Voltage for other pins (9, 11, 13, 14, 15, 17, and 20) in the 5 V domain	0	5.5	
V_{p3V}[1]	Voltage for other pins (2 to 5, 7, 18, 19 and 22 to 25) in the 3 V domain	0	5.5	
T_{Jun}	Junction temperature	-40	125	°C
V_{RFI_A}	RFI input amplitude[3]	0.15	3	V_{PP}

1. Referenced to V_{SS}.
2. If power supply is lower than 2.6 V, PSSR cannot be improved using internal regulators (minimum regulated voltage is 2.4 V).
3. The minimum RFI input signal definition is meant for NFC active P2P reception and NFC passive target reception. In HF reader mode and NFC transmit mode recommended signal level is 2.5 V_{PP}.

5.3 DC/AC characteristics for digital inputs and outputs

Table 110. Characteristics of CMOS I/Os (V_{DD} = 3.3 V)

Type	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Inputs(1)	V_{IH}	High level input voltage	-	0.8 * V_{DD_IO}	-	-	V
	V_{IL}	Low level input voltage	-	-	-	0.2 * V_{DD_IO}	
	I_{LEAK}	Input leakage current	V_{DD_IO} = 5.5 V	-1	-	1	µA
Output(2)	V_{OH}	High level output voltage	I_{source} = 1 mA V_{DD_IO} = 3.3 V	0.9 * V_{DD_IO}	-	-	V
			I_{source} = 0.5 mA V_{DD_IO} = 1.8 V io_drv_lvl = 1		-	-	
	V_{OL}	Low level output voltage	V_{DD_IO} = 3.3 V	-	-	0.1 * V_{DD_IO}	
			V_{DD_IO} = 1.8 V	-	-	0.1 * V_{DD_IO}	
	C_L	Capacitive load	-	-	-	50	pF
	R_O	Output resistance	V_{DD_IO} = 3.3 V	-	250	500	Ω
	R_{PD}	Pull-down resistance pin MISO(3)	V_{DD_IO} = 3.3 V	-	10	-	kΩ

1. Pins BSS, MOSI and SCLK.
2. Pins MISO, IRQ and MCU_CLK, io_drv_lvl = 0 (see *IO configuration register 2*).
3. Use bits miso_pd1 and miso_pd2 in the *IO configuration register 2* to control the optional pull down on the MISO pin.

Table 111. Characteristics of CMOS I/Os (V_{DD} = 2.4 to 5.5 V, characterized only)

Type	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Inputs(1)	V_{IH}	High level input voltage	-	0.8 * V_{DD_IO}	-	-	V
	V_{IL}	Low level input voltage	-	-	-	0.2 * V_{DD_IO}	
	I_{LEAK}	Input leakage current	V_{DD_IO} = 5.5 V	-1	-	1	µA
Output(2)	V_{OH}	High level output voltage	I_{source} = 1 mA V_{DD_IO} = 3.3 V	0.9 * V_{DD_IO}	-	-	V
			I_{source} = 0.5 mA V_{DD_IO} = 1.8 V io_drv_lvl = 1		-	1.8 V	
	V_{OL}	Low level output voltage	V_{DD_IO} = 3.3 V	-	-	0.1 * V_{DD_IO}	
			V_{DD_IO} = 1.8 V	-	-	0.1 * V_{DD_IO}	
	C_L	Capacitive load	-	-	-	50	pF
	R_O	Output resistance	V_{DD_IO} = 3.3 V	-	250	500	Ω
	R_{PD}	Pull-down resistance pin MISO(3)	V_{DD_IO} = 3.3 V	-	10	-	kΩ

1. Pins BSS, MOSI and SCLK.
2. Pins MISO, IRQ and MCU_CLK, io_drv_lvl = 0 (see *IO configuration register 2*).
3. Use bits miso_pd1 and miso_pd2 in the *IO configuration register 2* to control the optional pull down on the MISO pin.

5.4 Electrical characteristics

Table 112. ST25R3916 electrical characteristics[1] (V_{DD} = 3.3 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{PD}	Supply current in Power-down mode	T_{Jun} = -40 °C to 25 °C [2]	-	0.8	2.5	µA
		T_{Jun} = 85 °C [2]	-	2	20	
		T_{Jun} = 125 °C [2]	-	12	60	
I_{NFCT}	Supply current in Initial NFC target mode	T_{Jun} = -40 °C to 25 °C [3]	-	3.5	7.0	µA
		T_{Jun} = 85 °C [3]	-	5	20	
		T_{Jun} = 125 °C [3]	-	14	60	
I_{WU}	Supply current in Wake-up mode (logic and RC oscillator)	T_{Jun} = -40 °C to 25 °C [4]	-	3.0	6.3	µA
		T_{Jun} = 85 °C [4]		2.8	20	
		T_{Jun} = 125 °C [4]		15	60	
I_{CS}	Capacitive sensor supply current	[5]	-	1.1	2.0	mA
I_{RD}	Supply current in Ready mode	[6]	-	4.5	7.5	
I_{AL}	Supply current all active	[7]	-	16	23	
I_{AL-AM}	Supply current all active, AM	[8]	-	17	26	
I_{AL1}	Supply current all active single RX channel	[9]	-	11	16	
R_{RFO}	RFO1 and RFO2 driver output resistance	I_{RFO} = 10 mA	-	1.7	4	Ω
V_{RFI}	RFI input sensitivity	[10]	-	0.5	-	mV_{rms}
R_{RFI}	RFI input resistance	-	-	12	16	kΩ
V_{POR}	Power on reset voltage	-	1.0	1.45	2.0	V
V_{AGDC}	AGDC voltage	[6]	1.4	1.5	1.6	
V_{REG}	Regulated voltage	[11]	2.65	3.00	3.20	

1. 3.3 V supply mode with VDD = 3.3 V, unless noted otherwise. Regulated voltages are set at 3.0 V, 27.12 MHz Xtal connected to XTO and XTI.
2. Registers 00h to 07h (no clock on MCU_CLK), 01h to 80h (3 V supply mode), other registers in default state.
3. Registers 00h to 07h (no clock on MCU_CLK), 01h to 80h (3 V supply mode), 02h to 03h (external field detector enable), 03h to E8h (enable NFC Target mode), other registers in default state.
4. Registers 00h to 07h (no clock on MCU_CLK), 01h to 80h (3 V supply mode), 02h to 04h (enable Wake-up mode), 32h to 08h (100 ms timeout, IRQ at every timeout), other registers in default state.
5. Registers 00h to 07h (no clock on MCU_CLK), 01h to 80h (3 V supply mode), Test register 02h to 0Eh (tdana<3:0>=0Eh; CS analog test mode 14), other registers in default state.
6. Registers 00h to 07h (no clock on MCU_CLK), 01h to C0h (3 V supply mode, disable VDD_D), 02h to 80h (en=1), 2Ch to D8h (3.0 V regulator), other registers in default state, short VDD_A and VDD_D.
7. Registers 00h to 07h (no clock on MCU_CLK), 01h to C0h (3 V supply mode, disable VDD_D), 02h to C8h (enable RX, enable TX), 28h to 7Fh (RFO segments disabled), 2Ch to D8h (3.0 V regulator), other registers in default state, short VDD_A and VDD_D.
8. Registers 00h to 07h (no clock on MCU_CLK), 01h to C0h (3 V supply mode, disable VDD_D), 02h to C8h (enable RX, enable TX), 03h to 14h (AM modulation), 28h to 7Fh (RFO segments disabled), 2Ch to D8h (3.0 V regulator), other registers in default state, short VDD_A and VDD_D.
9. Registers 00h to 07h (no clock on MCU_CLK), 01h to C0h (3 V supply mode, disable VDD_D), 02h to E8h (enable RX, 1 RX channel, enable TX), 28h to 7Fh (RFO segments disabled), 2Ch to D8h (3.0 V regulator), other registers in default state, short VDD_A and VDD_D.
10. f_{SUB} = 848 kHz, AM channel with peak detector input stage selected.

11. Manual regulator mode, regulated voltage set to 3.0 V, measured on pin VDD_RF: register 00h set to 0Fh, register 01h set to 80h (3 V supply mode), register 02h set to E8h (one channel RX, enable TX), 2Ch to D8h (3.0 V regulator), other registers in default state.

Table 113. ST25R3916 electrical characteristics (V_{DD} = 5.5 V)(1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{PD}	Supply current in Power-down mode	T_{Jun} = -40 to 25 °C (3)	-	1	-	µA
		T_{Jun} = 125 °C (3)	-	26	-	
I_{NFCT}	Supply current in initial NFC target mode	T_{Jun} = -40 to 25 °C (4)	-	4	-	
		T_{Jun} = 125 °C (4)	-	35	-	
I_{WU}	Supply current in Wake-up mode (logic and RC oscillator)	T_{Jun} = -40 to 25 °C (5)	-	3	-	
		T_{Jun} = 125 °C (5)	-	35	-	
I_{CS}	Capacitive sensor supply current	T_{Jun} = -40 to 25 °C (6)	-	1.30	-	mA
		T_{Jun} = 125 °C (6)	-	1.25	-	
I_{RD}	Supply current in Ready mode	T_{Jun} = -40 to 25 °C (7)	-	5.0	-	
		T_{Jun} = 125 °C (7)	-	5.6	-	
I_{AL}	Supply current all active	T_{Jun} = -40 to 25 °C (8)	-	16.0	-	
		T_{Jun} = 125 °C (8)	-	17.5	-	
I_{AL-AM}	Supply current all active, AM	T_{Jun} = -40 to 25 °C (9)	-	17.5	-	
		T_{Jun} = 125 °C (9)	-	20.0	-	
I_{AL1}	Supply current all active single RX channel	T_{Jun} = -40 to 25 °C (10)	-	12.0	-	
		T_{Jun} = 125 °C (10)	-	12.2	-	
R_{RFO}	RFO1 and RFO2 driver output resistance	I_{RFO} = 10 mA T_{Jun} = -40 to 25 °C	-	1.4	-	Ω
		I_{RFO} = 10 mA T_{Jun} = 125 °C	-	2.4	-	
R_{RFI}	RFI input resistance	T_{Jun} = -40 to 25 °C	-	13.5	-	kΩ
		T_{Jun} = 125 °C	-	12.5	-	
V_{POR}	Power on reset voltage, 25°C	T_{Jun} = -40 to 25 °C	-	1.7	-	V
		T_{Jun} = 125 °C	-	1.2	-	
V_{AGDC}	AGDC voltage	T_{Jun} = -40 to 25 °C(8)	-	1.5	-	
		T_{Jun} = 125 °C(8)	-	1.5	-	

1. Characterized only.
2. 5.0 V supply mode with V_{DD} = 5.5 V unless noted otherwise. Regulated voltages set to 5.1 V, 27.12 MHz Xtal connected to XTO and XTI.
3. Registers 00h to 07h (no clock on MCU_CLK), 01h to 00h (5 V supply mode), other registers in default state.
4. Registers 00h to 07h (no clock on MCU_CLK), 01h to 00h (5 V supply mode), 02h to 03h (external field detector enable), 03h to E8h (enable NFC Target mode), other registers in default state.
5. Registers 00h to 07h (no clock on MCU_CLK), 01h to 00h (5 V supply mode), 02h to 04h (enable Wake-up mode), 32h to 08h (100 ms timeout, IRQ at every timeout), other registers in default state.
6. Registers 00h to 07h (no clock on MCU_CLK), 01h to 00h (5 V supply mode), Test register 02h to 0Eh (tdana<3:0>=0Eh; CS analog test mode 14), other registers in default state.

7. Registers 00h to 07h (no clock on MCU_CLK), 01h to 40h (5 V supply mode, disable VDD_D), 02h to 80h (en=1), 2Ch to F8h (5.1 V regulator), other registers in default state, short VDD_A and VDD_D.
8. Registers 00h to 07h (no clock on MCU_CLK), 01h to 40h (5 V supply mode, disable VDD_D), 02h to C8h (enable RX, enable TX), 28h to 7Fh (RFO segments disabled), 2Ch to F8h (5.1 V regulator), other registers in default state, short VDD_A and VDD_D.
9. Registers 00h to 07h (no clock on MCU_CLK), 01h to 40h (5 V supply mode, disable VDD_D), 02h to C8h (enable RX, enable TX), 03h to 14h (AM modulation), 28h to 7Fh (RFO segments disabled), 2Ch to F8h (5.1 V regulator), other registers in default state, short VDD_A and VDD_D.
10. Registers 00h to 07h (no clock on MCU_CLK), 01h to 40h (5 V supply mode, disable VDD_D), 02h to E8h (enable RX, 1 RX channel, enable TX), 28h to 7Fh (RFO segments disabled), 2Ch to F8h (5.1 V regulator), other registers in default state, short VDD_A and VDD_D.

Table 114. ST25R3916 electrical characteristics (V_{DD} = 2.4 V)(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{PD}	Supply current in Power-down mode	T_{Jun} = -40 to 25 °C (3)	-	0.5	-	µA
		T_{Jun} = 125 °C (3)	-	17	-	
I_{NFCT}	Supply current in initial NFC target mode	T_{Jun} = -40 to 25 °C (4)	-	3	-	
		T_{Jun} = 125 °C (4)	-	22	-	
I_{WU}	Supply current in Wake-up mode (logic and RC oscillator)	T_{Jun} = -40 to 25 °C (5)	-	1.8	-	
		T_{Jun} = 125 °C (5)	-	22	-	
I_{CS}	Capacitive sensor supply current	T_{Jun} = -40 to 25 °C (6)	-	0.65	-	mA
		T_{Jun} = 125 °C (6)	-	1.0	-	
I_{RD}	Supply current in Ready mode	T_{Jun} = -40 to 25 °C (7)	-	3.0	-	
		T_{Jun} = 125 °C (7)	-	3.8	-	
I_{AL}	Supply current all active	T_{Jun} = -40 to 25 °C (8)	-	13.0	-	
		T_{Jun} = 125 °C (8)	-	14.8	-	
I_{AL-AM}	Supply current all active, AM	T_{Jun} = -40 to 25 °C (9)	-	16.0	-	
		T_{Jun} = 125 °C (9)	-	16.0	-	
I_{AL1}	Supply current all active single RX channel	T_{Jun} = -40 to 25 °C (10)	-	8.5	-	
		T_{Jun} = 125 °C (10)	-	9.5	-	
R_{RFO}	RFO1 and RFO2 driver output resistance	I_{RFO} = 10 mA T_{Jun} = -40 to 25 °C	-	1.8	-	Ω
		I_{RFO} = 10 mA T_{Jun} = 125 °C	-	2.5	-	
R_{RFI}	RFI input resistance	T_{Jun} = -40 to 25 °C	-	13.5	-	kΩ
		T_{Jun} = 125 °C	-	12.6	-	
V_{POR}	Power on reset voltage, 25°C	T_{Jun} = -40 to 25 °C	-	1.7	-	V
		T_{Jun} = 125 °C	-	1.2	-	
V_{AGDC}	AGDC voltage	T_{Jun} = -40 to 25 °C	-	1.5	-	
		T_{Jun} = 125 °C	-	1.5	-	

1. Characterized only.
2. 3.3 V supply mode with V_{DD} = 2.4 V unless noted otherwise. Regulated voltages set to 2.4 V, 27.12 MHz Xtal connected to XTO and XTI.

3. Registers 00h to 07h (no clock on MCU_CLK), 01h to 80h (3 V supply mode), other registers in default state.
4. Registers 00h to 07h (no clock on MCU_CLK), 01h to 80h (3 V supply mode), 02h to 03h (external field detector enable), 03h to E8h (enable NFC Target mode), other registers in default state.
5. Registers 00h to 07h (no clock on MCU_CLK), 01h to 80h (3 V supply mode), 02h to 04h (enable Wake-up mode), 32h to 08h (100 ms timeout, IRQ at every timeout), other registers in default state.
6. Registers 00h to 07h (no clock on MCU_CLK), 01h to 80h (3 V supply mode), Test register 02h to 0Eh (tdana<3:0>=0Eh; CS analog test mode 14), other registers in default state.
7. Registers 00h to 07h (no clock on MCU_CLK), 01h to C0h (3 V supply mode, disable VDD_D), 02h to 80h (en=1), 2Ch to A8h (2.4 V regulator), other registers in default state, short VDD_A and VDD_D.
8. Registers 00h to 07h (no clock on MCU_CLK), 01h to C0h (3 V supply mode, disable VDD_D), 02h to C8h (enable RX, enable TX), 28h to 7Fh (RFO segments disabled), 2Ch to A8h (2.4 V regulator), other registers in default state, short VDD_A and VDD_D.
9. Registers 00h to 07h (no clock on MCU_CLK), 01h to C0h (3 V supply mode, disable VDD_D), 02h to C8h (enable RX, enable TX), 03h to 14h (AM modulation), 28h to 7Fh (RFO segments disabled), 2Ch to A8h (2.4 V regulator), other registers in default state, short VDD_A and VDD_D.
10. Registers 00h to 07h (no clock on MCU_CLK), 01h to C0h (3 V supply mode, disable VDD_D), 02h to E8h (enable RX, 1 RX channel, enable TX), 28h to 7Fh (RFO segments disabled), 2Ch to A8h (2.4 V regulator), other registers in default state, short VDD_A and VDD_D.

5.5 SPI interface characteristics

Table 115. SPI characteristics (V_{DD} = V_{DD_IO} = 3.3 V)

Operation	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
General	T_{SCLK}	SCLK period	$T_{SCLK} = T_{SCLKL} + T_{SCLKH}$	100	-	-	ns
	T_{SCLKL}	SCLK low	-	40	-	-	
	T_{SCLKH}	SCLK high	-	40	-	-	
	T_{SSH}	SPI reset (BSS high)	-	100	-	-	
	T_{NCSL}	BSS falling to SCLK rising	First SCLK pulse	25	-	-	
	T_{NCSH}	SCLK falling to BSS rising	Last SCLK pulse	25	-	-	
	T_{DIS}(1)	Data in setup time	-	10	-	-	
	T_{DIH}(1)	Data in hold time	-	10	-	-	
Read	T_{DOD}(1)	Data out delay	$C_{load} \leq 50$ pF	-	20	-	
	T_{DOHZ}(1)	Data out to high impedance delay	$C_{load} \leq 50$ pF	-	20	-	

1. Characterized only.

Table 116. SPI characteristics (V_{DD} = 2.4 to 5.5 V, V_{DD_IO} = 3.3 V)

Operation	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
General	T_{SCLK}	SCLK period	$T_{SCLK} = T_{SCLKL} + T_{SCLKH}$	100	-	-	ns
	T_{SCLKL}	SCLK low	-	40	-	-	
	T_{SCLKH}	SCLK high	-	40	-	-	
	T_{SSH}	SPI reset (BSS high)	-	100	-	-	
	T_{NCSL}	BSS falling to SCLK rising	First SCLK pulse	25	-	-	
	T_{NCSH}	SCLK falling to BSS rising	Last SCLK pulse	25	-	-	
	T_{DIS}(1)	Data in setup time	-	10	-	-	
	T_{DIH}(1)	Data in hold time	-	10	-	-	
Read	T_{DOD}(1)	Data out delay	$C_{load} \leq 50$ pF	-	20	-	
	T_{DOHZ}(1)	Data out to high impedance delay	$C_{load} \leq 50$ pF	-	20	-	

1. Characterized only.

Figure 23. SPI timing diagram - General operation

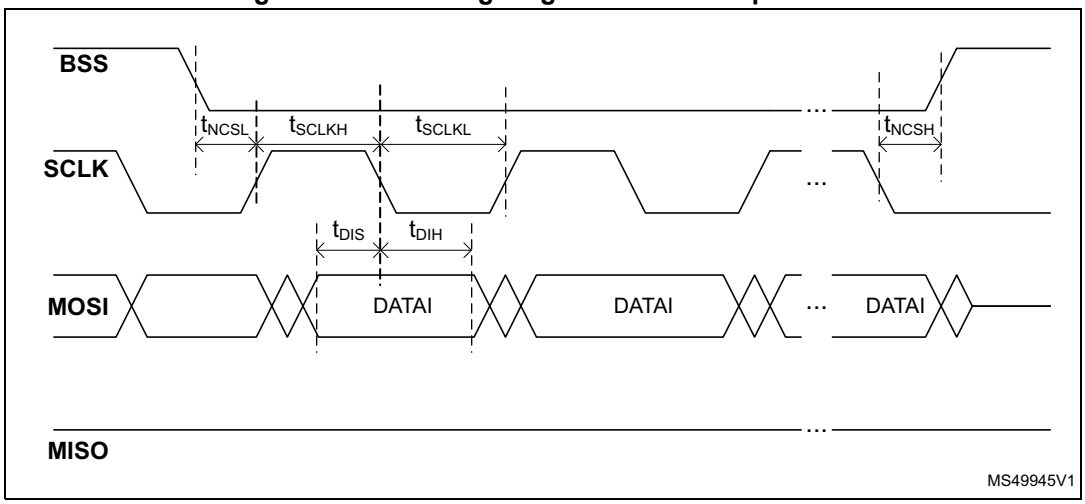
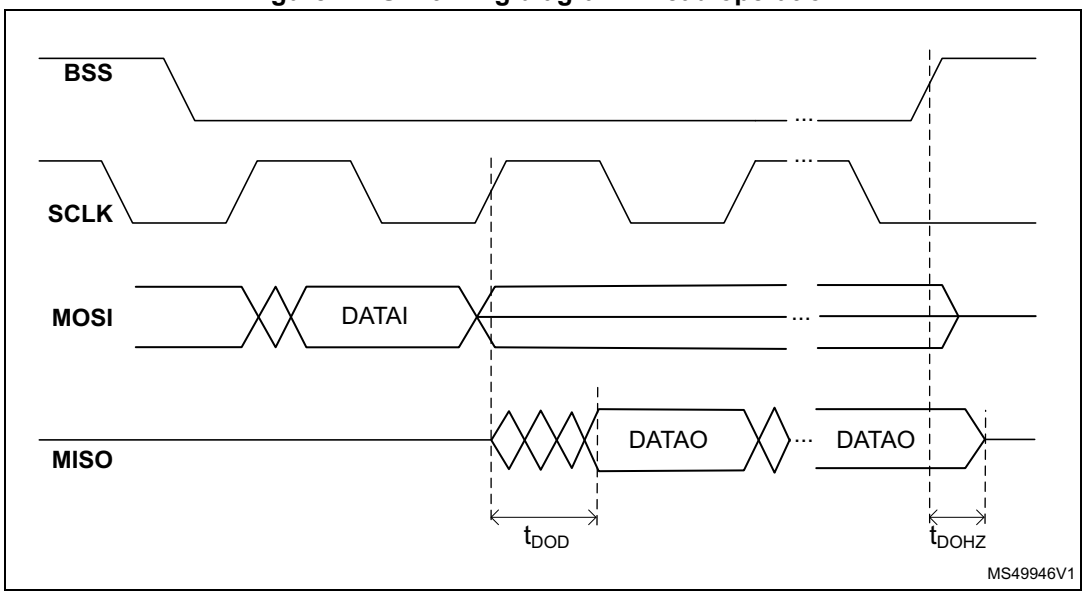


Figure 24. SPI timing diagram - Read operation



5.6 I2C interface characteristics

Timing according to I2C protocol. Drivers for up to 3.4 MHz operation.

Transition from 100 kHz / 400 kHz /1 MHz mode to 3.4 MHz mode (High Speed mode) is done via Master code 00001XXX, as described in the I2C specification.

Table 117. AC measurement conditions

Symbol	Parameter	Min	Max	Unit
C_{BUS}	Load capacitance	100		pF
-	SCL input rise/fall time, SDA input fall time	-	50	ns

Table 118. AC measurement conditions - I2C configuration

Mode	Rate	Setting
S	100 kHz	i2c_thd = 00b, io_drv_lvl = 1b
F	400 kHz	i2c_thd = 01b, io_drvl_lvl = 1b
F+	1000 kHz	i2c_thd = 11b, Io_drv_lvl = 1b
HS	3400 kHz	i2c_thd = 11b, io_drv_lvl = 1b

Table 119. Input parameters

Symbol	Parameter(1)	Conditions	Min	Max	Unit
C_{IN}	Input capacitance (SDA)	-	-	15	pF
	Input capacitance (SCL)	-	-	15	

1. Characterized only.

Table 120. DC characteristics

Symbol	Parameter(1)	Conditions (in addition to those in *Table 117* and *Table 118*)	Min	Max	Unit
I_{LI}	Input leakage current (SCL, SDA)	V_{IN} = V_{SS} or V_{CC}, device in Standby mode	-	± 10	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}	-	± 10	
V_{IL}	Input low voltage (SCL, SDA)	-	-0.4	0.2 V_{DD_IO}	V
V_{IH}	Input high voltage (SCL, SDA)	-	0.8 V_{DD_IO}	V_{DD_IO} + 0.4	
V_{OL}	Output low voltage	V_{DD_IO} = 1.8 V, I_{OL} = 1.0 mA	-	0.1 V_{DD_IO}	
		V_{DD_IO} = 2.5 V, I_{OL} = 2.1 mA	-	0.1 V_{DD_IO}	
		V_{DD_IO} = 3.3 V, I_{OL} = 8mA	-	0.1 V_{DD_IO}	

1. Characterized only.

Table 121. 400 kHz AC characteristics (V_{DD} = 3.3 V, V_{DD_IO} = 1.65 V)(1)

Symbol	Alt.	Parameter	Min	Max	Unit
f_C	f_{SCL}	Clock frequency	-	400	kHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	600	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	1300	-	
t_{QL1QL2}	t_F	SDA (out) fall time	-	300	
t_{DXCH}	$t_{SU:DAT}$	Data in set up time	100	-	
$t_{CLDX}X$	$t_{HD:DAT}$	Data in hold time	0	-	
t_{CLQX}	t_{DH}	Data out hold time	50	-	
t_{CLQV}	t_{AA}	Clock low to next data valid (access time)	-	900	
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	600	-	
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	600	-	
t_{CHDH}	$t_{SU:STO}$	Stop condition set up time	600	-	
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	1300	-	
t_{NS}(2)	-	Pulse width ignored (input filter on SCL and SDA), single glitch	-	40	

1. Conditions in addition to those specified in *Table 117* and *Table 118*.
2. Characterized only.

Table 122. 400 kHz AC characteristics (V_{DD} = 2.4 to 5.5 V, V_{DD_IO} = 1.65 V)(1) (2)

Symbol	Alt.	Parameter	Min	Max	Unit
f_C	f_{SCL}	Clock frequency	-	400	kHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	600	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	1300	-	
t_{QL1QL2}	t_F	SDA (out) fall time	-	300	
t_{DXCH}	$t_{SU:DAT}$	Data in set up time	100	-	
$t_{CLDX}X$	$t_{HD:DAT}$	Data in hold time	0	-	
t_{CLQX}	t_{DH}	Data out hold time	50	-	
t_{CLQV}	t_{AA}	Clock low to next data valid (access time)	-	900	
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	600	-	
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	600	-	
t_{CHDH}	$t_{SU:STO}$	Stop condition set up time	600	-	
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	1300	-	
t_{NS}	-	Pulse width ignored (input filter on SCL and SDA), single glitch	-	40	

1. Conditions in addition to those specified in *Table 117* and *Table 118*.
2. Characterized only.

Table 123. 1 MHz AC characteristics (V_{DD} = 3.3 V, V_{DD_IO} = 1.65 V)(1)

Symbol	Alt.	Parameter	Min	Max	Unit
f_C	f_{SCL}	Clock frequency	-	1	MHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	260	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	500	-	
t_{QL1QL2}	t_F	SDA (out) fall time	-	120	
t_{DXCH}	$t_{SU:DAT}$	Data in set up time	50	-	
$t_{CLDX}X$	$t_{HD:DAT}$	Data in hold time	0	-	
t_{CLQX}	t_{DH}	Data out hold time	50	-	
t_{CLQV}	t_{AA}	Clock low to next data valid (access time)	-	450	
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	250	-	
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	250	-	
t_{CHDH}	$t_{SU:STO}$	Stop condition set up time	250	-	
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	500	-	
t_{NS}(2)	-	Pulse width ignored (input filter on SCL and SDA), single glitch	-	40	

1. Conditions in addition to those specified in *Table 117* and *Table 118*.
2. Characterized only.

Table 124. 1 MHz AC characteristics (V_{DD} = 2.4 to 5.5 V, V_{DD_IO} = 1.65 V)(1) (2)

Symbol	Alt.	Parameter	Min	Max	Unit
f_C	f_{SCL}	Clock frequency	-	1	MHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	260	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	500	-	
t_{QL1QL2}	t_F	SDA (out) fall time	-	120	
t_{DXCH}	$t_{SU:DAT}$	Data in set up time	50	-	
$t_{CLDX}X$	$t_{HD:DAT}$	Data in hold time	0	-	
t_{CLQX}	t_{DH}	Data out hold time	50	-	
t_{CLQV}	t_{AA}	Clock low to next data valid (access time)	-	450	
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	250	-	
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	250	-	
t_{CHDH}	$t_{SU:STO}$	Stop condition set up time	250	-	
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	500	-	
t_{NS}	-	Pulse width ignored (input filter on SCL and SDA), single glitch	-	40	

1. Conditions in addition to those specified in *Table 117* and *Table 118*.
2. Characterized only.

Table 125. 3.4 MHz AC characteristics (V_{DD} = 3.3 V, V_{DD_IO} = 1.65 V)(1)

Symbol	Alt.	Parameter	Min	Max	Unit
f_C	f_{SCL}	Clock frequency	-	3.4	MHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	80	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	160	-	
t_{QL1QL2}	t_F	SDA (out) fall time (10-100 pF)	-	100	
t_{DXCH}	$t_{SU:DAT}$	Data in set up time	25	-	
$t_{CLDX}X$	$t_{HD:DAT}$	Data in hold time	0	-	
t_{CLQX}	t_{DH}	Data out hold time	20	-	
t_{CLQV}	t_{AA}	Clock low to next data valid (access time), $V_{DD} \geq 3.3$ V	-	110	
		Clock low to next data valid (access time), $V_{DD} < 3.3$ V	-	160	
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	160	-	
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	160	-	
t_{CHDH}	$t_{SU:STO}$	Stop condition set up time	160	-	
t_{NS}(2)	-	Pulse width ignored (input filter on SCL and SDA), single glitch	-	10	

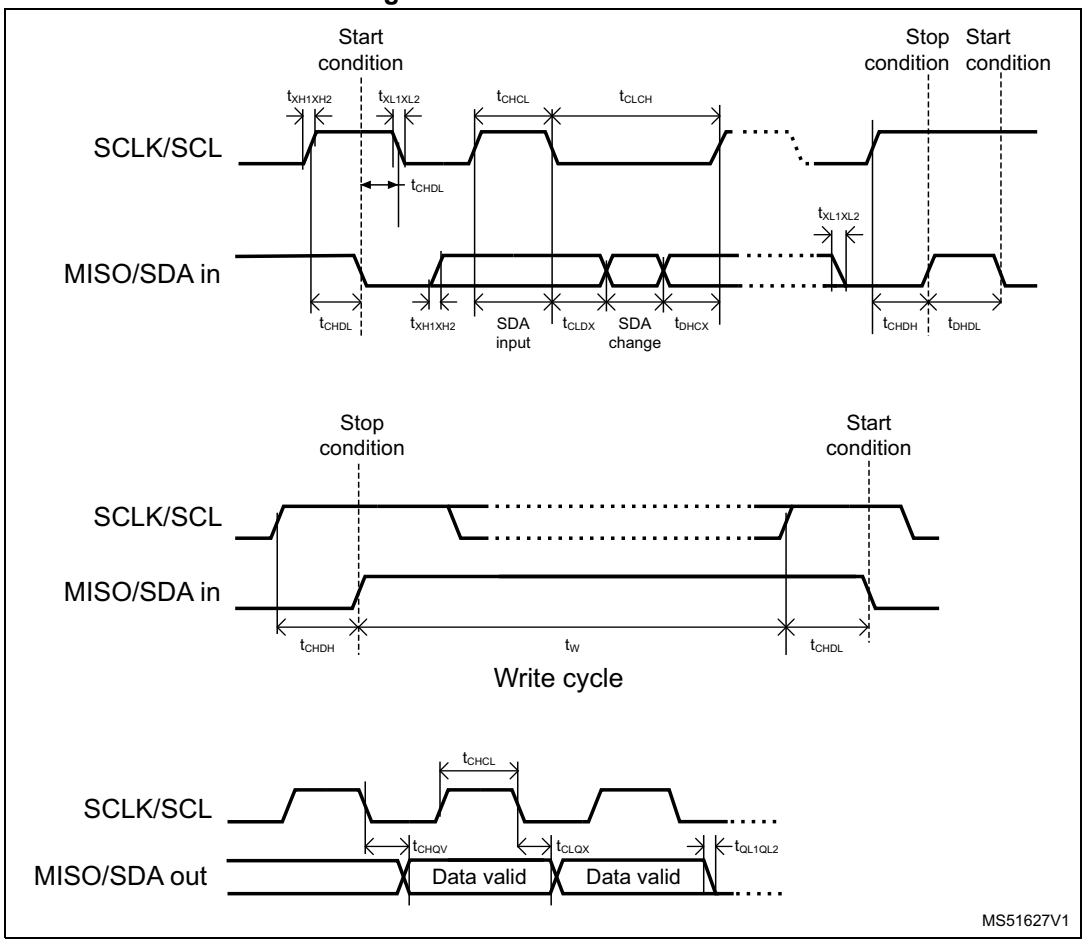
1. Conditions in addition to those specified in *Table 117* and *Table 118*.
2. Characterized only.

Table 126. 3.4 MHz AC characteristics (V_{DD} = 2.4 to 5.5 V, V_{DD_IO} = 1.65 V)(1) (2)

Symbol	Alt.	Parameter	Min	Max	Unit
f_C	f_{SCL}	Clock frequency	-	3.4	MHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	80	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	160	-	
t_{QL1QL2}	t_F	SDA (out) fall time (10-100 pF)	-	100	
t_{DXCH}	$t_{SU:DAT}$	Data in set up time	25	-	
$t_{CLDX}X$	$t_{HD:DAT}$	Data in hold time	0	-	
t_{CLQX}	t_{DH}	Data out hold time	20	-	
t_{CLQV}	t_{AA}	Clock low to next data valid (access time), $V_{DD} \geq 3.3$ V	-	110	
		Clock low to next data valid (access time), $V_{DD} < 3.3$ V	-	160	
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	160	-	
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	160	-	
t_{CHDH}	$t_{SU:STO}$	Stop condition set up time	160	-	
t_{NS}	-	Pulse width ignored (input filter on SCL and SDA), single glitch	-	10	

1. Conditions in addition to those specified in *Table 117* and *Table 118*.
2. Characterized only.

Figure 25. I2C AC waveforms



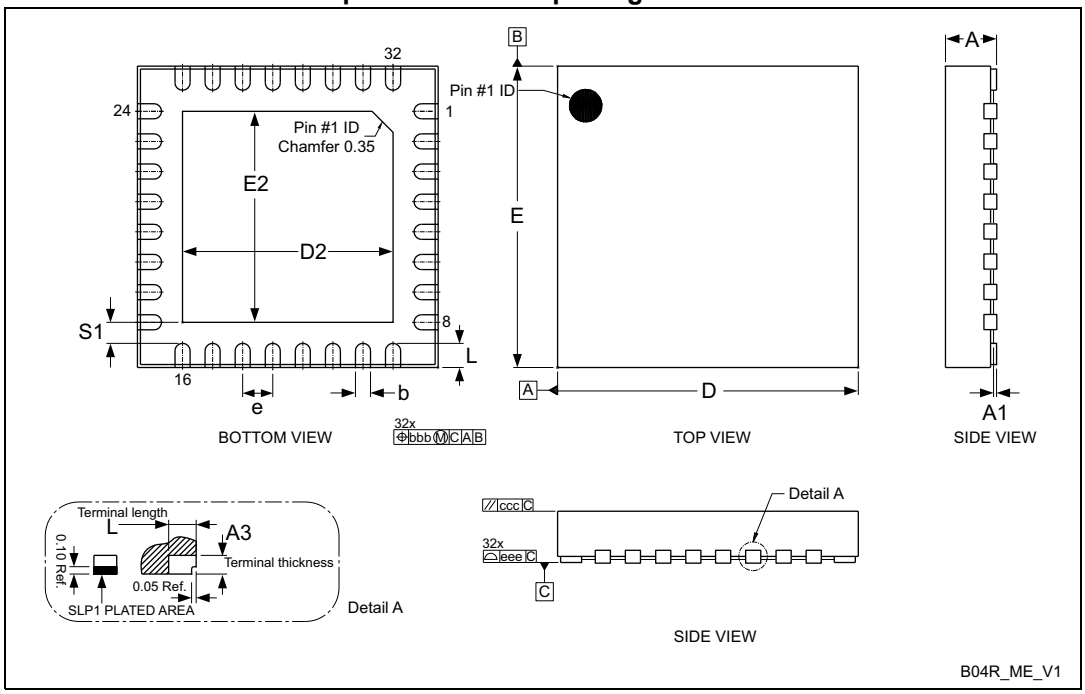
6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at *www.st.com*.

ECOPACK® is an ST trademark.

6.1 VFQFPN32 package information

Figure 26. VFQFPN - 32 pins, 5x5 mm, 0.5 mm pitch, very thin fine pitch quad flat no lead package outline



1. Drawing is not to scale.
2. Coplanarity applies to the exposed pad as well as the terminal.

Table 127. VFQFPN - 32 pins, 5x5 mm, 0.5 mm pitch, very thin fine pitch quad flat no lead mechanical data

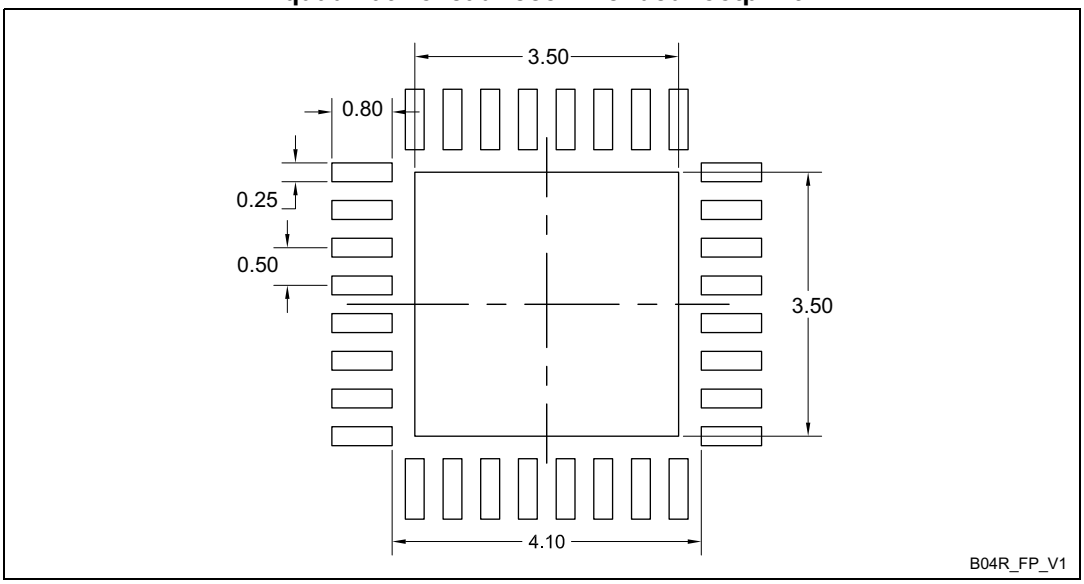
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.800	0.900	1.000	0.0315	0.0354	0.0394
A1	0	-	0.050	0	-	0.0020
A3		0.200			0.0079	
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
b	0.180	0.250	0.300	0.0071	0.0098	0.0118

Table 127. VFQFPN - 32 pins, 5x5 mm, 0.5 mm pitch, very thin fine pitch quad flat no lead mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
D		5.000			0.1969	
D2	3.400	3.500	3.600	0.1339	0.1378	0.1417
E		5.000			0.1969	
E2	3.400	3.500	3.600	0.1339	0.1378	0.1417
e		0.500			0.0197	
S1		0.350			0.0138	
bbb	-	0.100	-	-	0.0039	-
ccc	-	0.100	-	-	0.0039	-
eee	-	0.080	-	-	0.0031	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 27. VFQFPN - 32 pins, 5x5 mm, 0.5 mm pitch, very thin fine pitch quad flat no lead recommended footprint



1. Dimensions are expressed in millimeters.

7 Ordering information

Example: ST25 R 3916 -A QW T

Device type

ST25 = NFC/RFID tags and readers

Product type

R = NFC/HF reader

Product feature

3916 = High performance NFC universal device and EMVCo reader

Temperature range

A = -40 °C to 125 °C

Package/Packaging

QW = 32-pin VFQFPN (5 x 5 mm) with wettable flanks

Tape and reel

T = 4000 pcs/reel

Note: Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

8 Revision history

Table 128. Document revision history

Date	Revision	Changes
30-Jan-2019	1	Initial release.