

## Phase Control Thyristors (Hockey PUK Version), 720 A



TO-200AB (E-PUK)

### FEATURES

- Center amplifying gate
- Metal case with ceramic insulator
- International standard case TO-200AB (E-PUK)
- Lead (Pb)-free
- Designed and qualified for industrial level



**RoHS**  
COMPLIANT

### TYPICAL APPLICATIONS

- DC motor controls
- Controlled DC power supplies
- AC controllers

### PRODUCT SUMMARY

$I_{T(AV)}$	720 A
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### MAJOR RATINGS AND CHARACTERISTICS

PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$		720	A
	$T_{hs}$	55	°C
$I_{T(RMS)}$		1420	A
	$T_{hs}$	25	°C
$I_{TSM}$	50 Hz	9000	A
	60 Hz	9420	
$I^2t$	50 Hz	405	kA <sup>2</sup> s
	60 Hz	370	
$V_{DRM}/V_{RRM}$		400 to 1600	V
$t_q$	Typical	100	μs
$T_j$		- 40 to 125	°C

### ELECTRICAL SPECIFICATIONS

#### VOLTAGE RATINGS

TYPE NUMBER	VOLTAGE CODE	$V_{DRM}/V_{RRM}$ , MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE V	$V_{RSM}$ , MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	$I_{DRM}/I_{RRM}$ MAXIMUM AT $T_J = T_J$ MAXIMUM mA
ST330C..C	04	400	500	50
	08	800	900	
	12	1200	1300	
	14	1400	1500	
	16	1600	1700	

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ABSOLUTE MAXIMUM RATINGS						
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS	
Maximum average on-state current at heatsink temperature	$I_{T(AV)}$	180° conduction, half sine wave double side (single side) cooled		720 (350)	A	
				55 (75)	°C	
Maximum RMS on-state current	$I_{T(RMS)}$	DC at 25 °C heatsink temperature double side cooled		1420		
Maximum peak, one-cycle non-repetitive surge current	$I_{TSM}$	t = 10 ms	No voltage reapplied	9000	A	
		t = 8.3 ms		Sinusoidal half wave, initial $T_J = T_J$ maximum		9420
		t = 10 ms	100 % $V_{RRM}$ reapplied			7570
		t = 8.3 ms				7920
Maximum $I^2t$ for fusing	$I^2t$	t = 10 ms	No voltage reapplied		405	kA <sup>2</sup> s
		t = 8.3 ms		370		
		t = 10 ms	100 % $V_{RRM}$ reapplied	287		
		t = 8.3 ms		262		
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 to 10 ms, no voltage reapplied		4050	kA <sup>2</sup> /s	
Low level value of threshold voltage	$V_{T(TO)1}$	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$ , $T_J = T_J$ maximum		0.91	V	
High level value of threshold voltage	$V_{T(TO)2}$	$(I > \pi \times I_{T(AV)})$ , $T_J = T_J$ maximum		0.92		
Low level value of on-state slope resistance	$r_{t1}$	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$ , $T_J = T_J$ maximum		0.58	mΩ	
High level value of on-state slope resistance	$r_{t2}$	$(I > \pi \times I_{T(AV)})$ , $T_J = T_J$ maximum		0.57		
Maximum on-state voltage	$V_{TM}$	$I_{pk} = 1810$ A, $T_J = T_J$ maximum, $t_p = 10$ ms sine pulse		1.96	V	
Maximum holding current	$I_H$	$T_J = 25$ °C, anode supply 12 V resistive load		600	mA	
Typical latching current	$I_L$			1000		

SWITCHING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum non-repetitive rate of rise of turned-on current	di/dt	Gate drive 20 V, 20 Ω, $t_r \leq 1$ μs $T_J = T_J$ maximum, anode voltage $\leq 80\%$ $V_{DRM}$		1000	A/μs
Typical delay time	$t_d$	Gate current 1 A, $di_g/dt = 1$ A/μs $V_d = 0.67\%$ $V_{DRM}$ , $T_J = 25$ °C		1.0	μs
Typical turn-off time	$t_q$	$I_{TM} = 550$ A, $T_J = T_J$ maximum, $di/dt = 40$ A/μs, $V_R = 50$ V, $dV/dt = 20$ V/μs, gate 0 V 100 Ω, $t_p = 500$ μs		100	

BLOCKING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum linear to 80 % rated $V_{DRM}$		500	V/μs
Maximum peak reverse and off-state leakage current	$I_{RRM}$ , $I_{DRM}$	$T_J = T_J$ maximum, rated $V_{DRM}/V_{RRM}$ applied		50	mA



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TRIGGERING						
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES		UNITS	
			TYP.	MAX.		
Maximum peak gate power	$P_{GM}$	$T_J = T_J$ maximum, $t_p \leq 5$ ms	10.0		W	
Maximum average gate power	$P_{G(AV)}$	$T_J = T_J$ maximum, $f = 50$ Hz, $d\% = 50$	2.0			
Maximum peak positive gate current	$I_{GM}$	$T_J = T_J$ maximum, $t_p \leq 5$ ms	3.0		A	
Maximum peak positive gate voltage	$+V_{GM}$	$T_J = T_J$ maximum, $t_p \leq 5$ ms	20		V	
Maximum peak negative gate voltage	$-V_{GM}$		5.0			
DC gate current required to trigger	$I_{GT}$	Maximum required gate trigger/ current/voltage are the lowest value which will trigger all units 12 V anode to cathode applied	$T_J = -40$ °C	200	-	mA
			$T_J = 25$ °C	100	200	
			$T_J = 125$ °C	50	-	
DC gate voltage required to trigger	$V_{GT}$	Maximum required gate trigger/ current/voltage are the lowest value which will trigger all units 12 V anode to cathode applied	$T_J = -40$ °C	2.5	-	V
			$T_J = 25$ °C	1.8	3.0	
			$T_J = 125$ °C	1.1	-	
DC gate current not to trigger	$I_{GD}$	$T_J = T_J$ maximum	10		mA	
DC gate voltage not to trigger	$V_{GD}$		0.25		V	

THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum operating junction temperature range	$T_J$		- 40 to 125	°C
Maximum storage temperature range	$T_{Stg}$		- 40 to 150	
Maximum thermal resistance, junction to heatsink	$R_{thJ-hs}$	DC operation single side cooled	0.09	K/W
		DC operation double side cooled	0.04	
Maximum thermal resistance, case to heatsink	$R_{thC-hs}$	DC operation single side cooled	0.02	
		DC operation double side cooled	0.01	
Mounting force, $\pm 10$ %			9800 (1000)	N (kg)
Approximate weight			83	g
Case style		See dimensions - link at the end of datasheet	TO-200AB (E-PUK)	

$\Delta R_{thJ-hs}$ CONDUCTION						
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION		RECTANGULAR CONDUCTION		TEST CONDITIONS	UNITS
	SINGLE SIDE	DOUBLE SIDE	SINGLE SIDE	DOUBLE SIDE		
180°	0.012	0.011	0.008	0.007	$T_J = T_J$ maximum	K/W
120°	0.014	0.012	0.014	0.013		
90°	0.017	0.015	0.019	0.017		
60°	0.025	0.022	0.026	0.023		
30°	0.043	0.036	0.043	0.037		

**Note**

- The table above shows the increment of thermal resistance  $R_{thJ-hs}$  when devices operate at different conduction angles than DC

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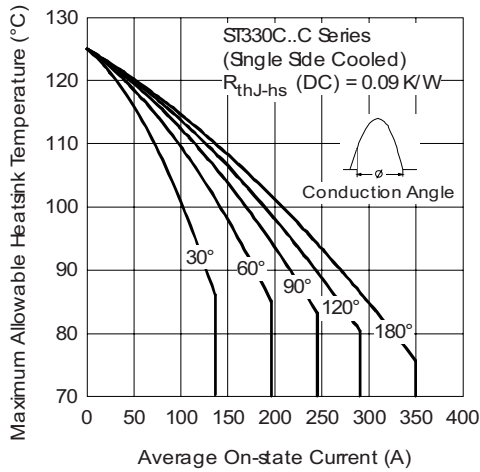


Fig. 1 - Current Ratings Characteristics

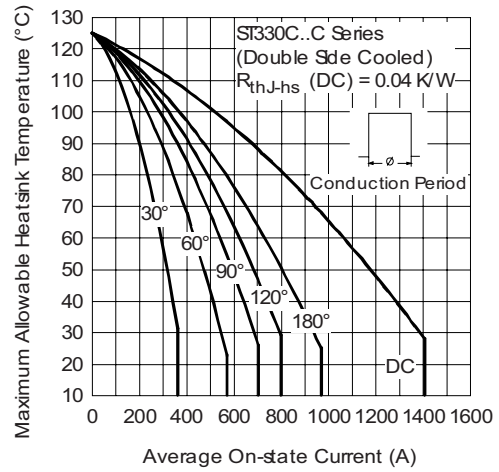


Fig. 4 - Current Ratings Characteristics

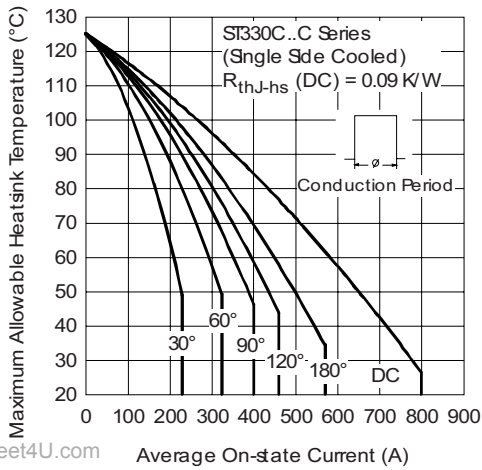


Fig. 2 - Current Ratings Characteristics

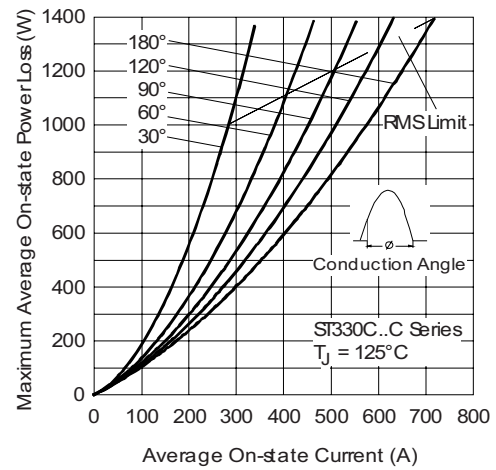


Fig. 5 - On-State Power Loss Characteristics

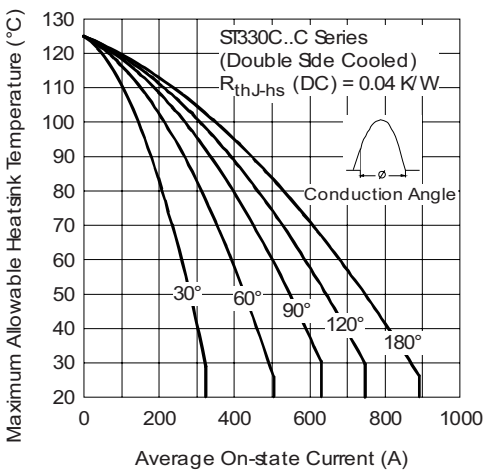


Fig. 3 - Current Ratings Characteristics

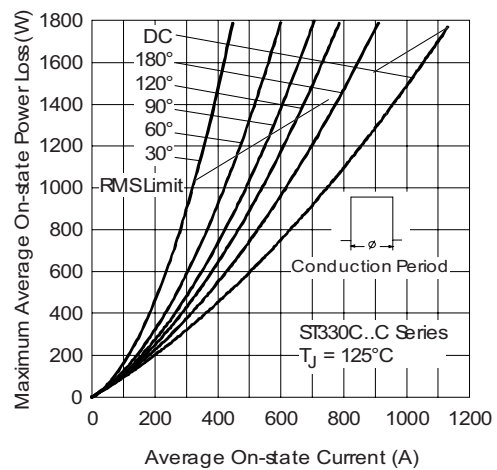


Fig. 6 - On-State Power Loss Characteristics

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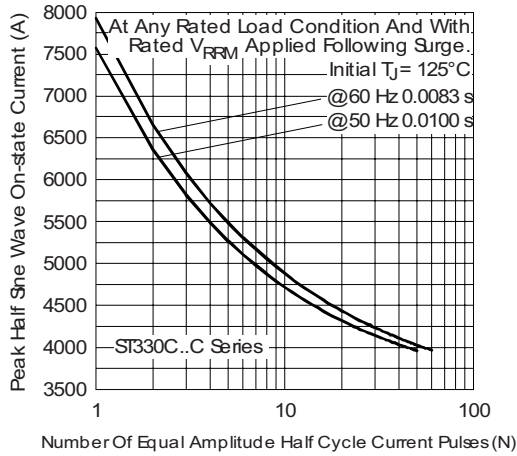


Fig. 7 - Maximum Non-Repetitive Surge Current Single and Double Side Cooled

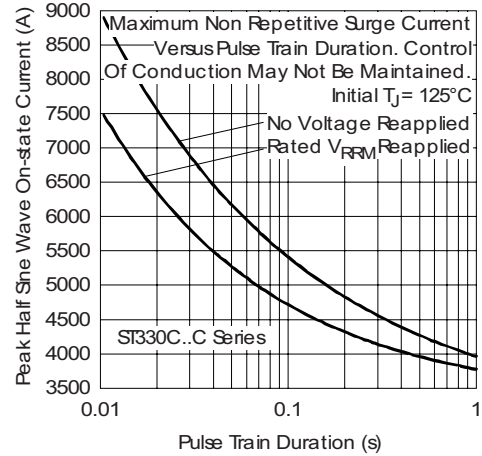


Fig. 8 - Maximum Non-Repetitive Surge Current Single and Double Side Cooled

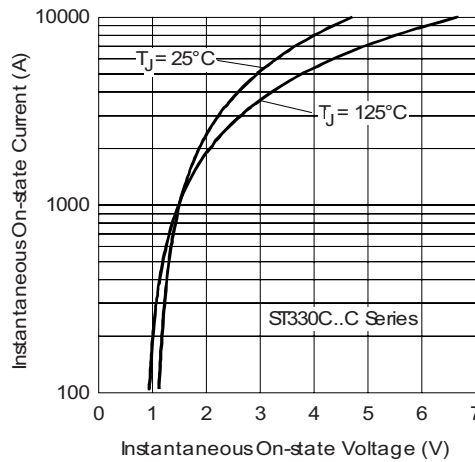


Fig. 9 - On-State Voltage Drop Characteristics

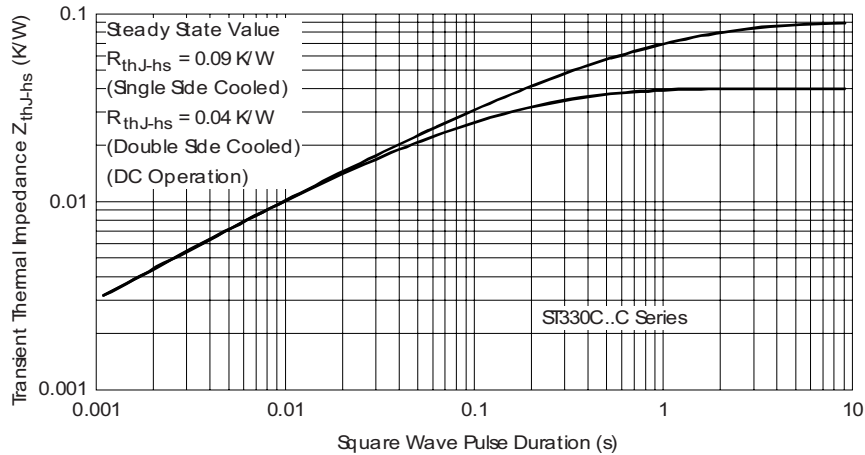


Fig. 10 - Thermal Impedance  $Z_{thJ-hs}$  Characteristics

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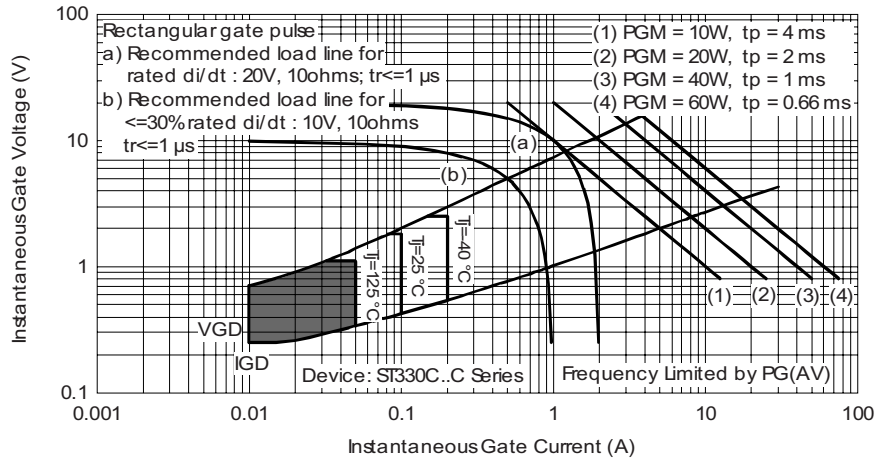


Fig. 11 - Gate Characteristics

### ORDERING INFORMATION TABLE

Device code	<b>ST</b>	<b>33</b>	<b>0</b>	<b>C</b>	<b>16</b>	<b>C</b>	<b>1</b>	<b>-</b>	<b>PbF</b>
	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)

- 1** - Thyristor
- 2** - Essential part number
- 3** - 0 = Converter grade
- 4** - C = Ceramic PUK
- 5** - Voltage code x 100 =  $V_{RRM}$  (see Voltage Ratings table)
- 6** - C = PUK case TO-200AB (E-PUK)
- 7** - 0 = Eyelet terminals (gate and auxiliary cathode unsoldered leads)  
 1 = Fast-on terminals (gate and auxiliary cathode unsoldered leads)  
 2 = Eyelet terminals (gate and auxiliary cathode soldered leads)  
 3 = Fast-on terminals (gate and auxiliary cathode soldered leads)
- 8** - Critical dV/dt: • None = 500 V/μs (standard selection)  
 • L = 1000 V/μs (special selection)
- 9** - Lead (Pb)-free

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#### LINKS TO RELATED DOCUMENTS

Dimensions	<a href="http://www.vishay.com/doc?95075">http://www.vishay.com/doc?95075</a>
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