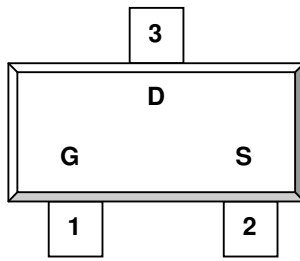


**DESCRIPTION**

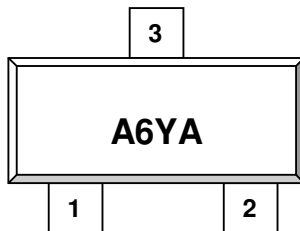
ST3406SRG is the N-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management, other battery powered circuits, and low in-line power loss are required. The product is in a very small outline surface mount package.

**PIN CONFIGURATION  
SOT-23**


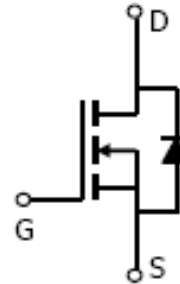
1.Gate 2.Source 3.Drain

**FEATURE**

- 30V/5.4A,  $R_{DS(ON)} = 26m\Omega$  (Typ.) @  $V_{GS} = 10V$
- 30V/4.6A,  $R_{DS(ON)} = 38m\Omega$  @  $V_{GS} = 4.5V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23 package design

**PART MARKING  
SOT-23**


Y: Year Code A: Week Code



**ST3406SRG**

N Channel Enhancement Mode MOSFET

5.4A

**ABSOLUTE MAXIMUM RATINGS** (Ta = 25°C Unless otherwise noted )

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V <sub>DSS</sub>	30	V
Gate-Source Voltage	V <sub>GSS</sub>	±20	V
Continuous Drain Current (T <sub>J</sub> =150°C)	I <sub>D</sub>	T <sub>A</sub> =25°C 5.4	A
		T <sub>A</sub> =70°C 3.2	
Pulsed Drain Current	I <sub>DM</sub>	25	A
Continuous Source Current (Diode Conduction)	I <sub>S</sub>	1.7	A
Power Dissipation	P <sub>D</sub>	T <sub>A</sub> =25°C 2.0	W
		T <sub>A</sub> =70°C 1.3	
Operation Junction Temperature	T <sub>J</sub>	150	°C
Storage Temperature Range	T <sub>STG</sub>	-55/150	°C
Thermal Resistance-Junction to Ambient	R <sub>θJA</sub>	90	°C/W



**ST3406SRG**

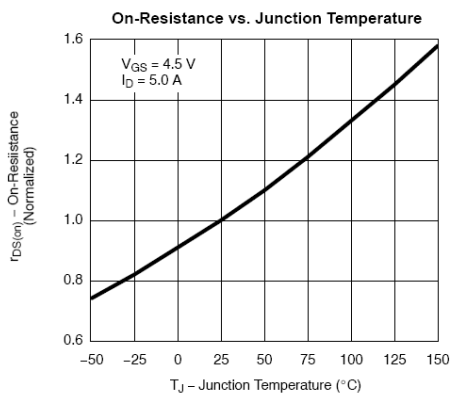
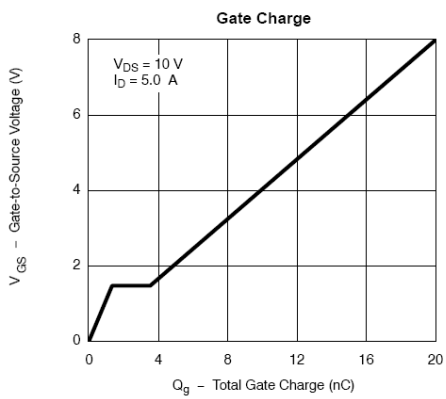
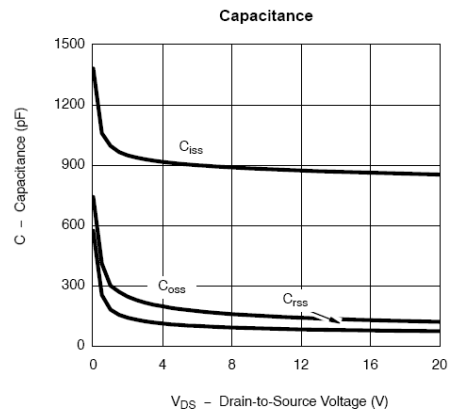
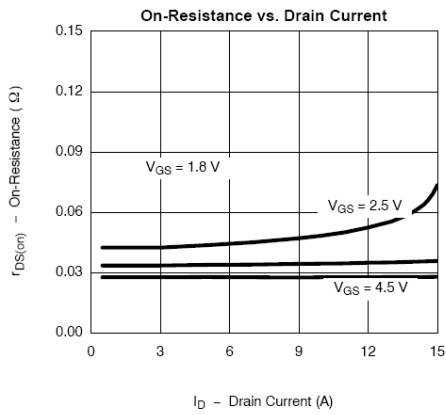
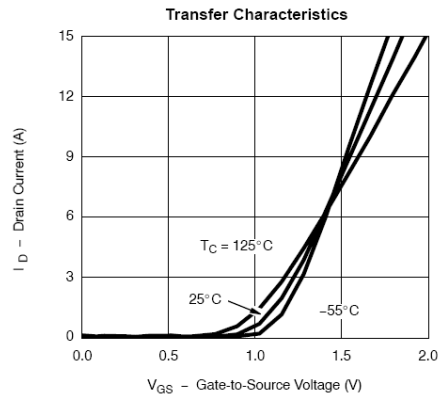
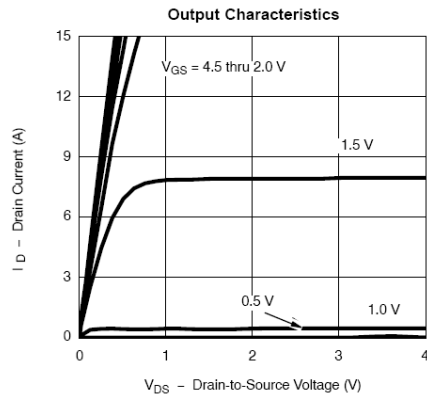


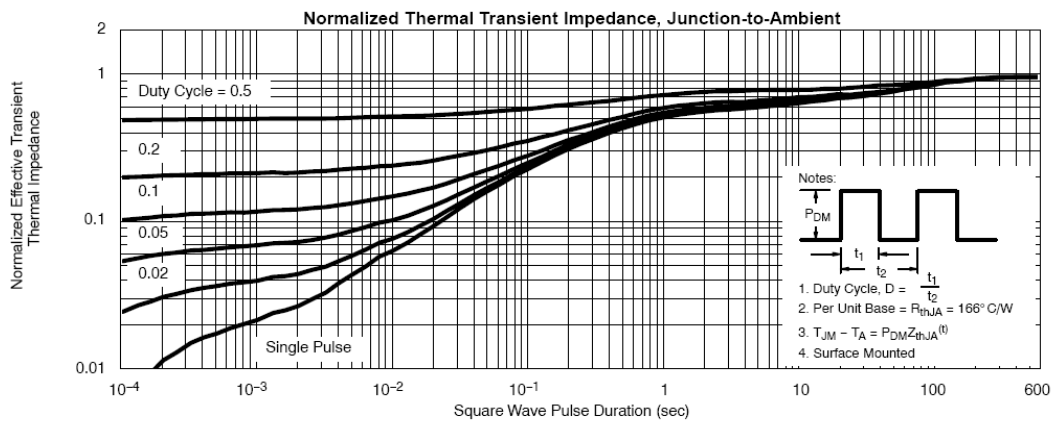
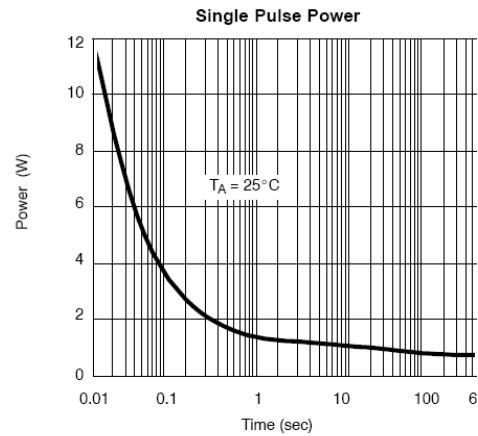
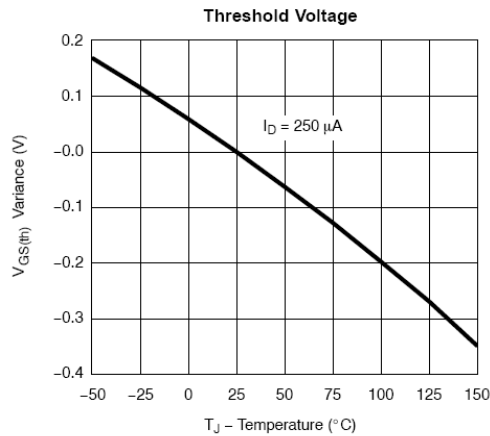
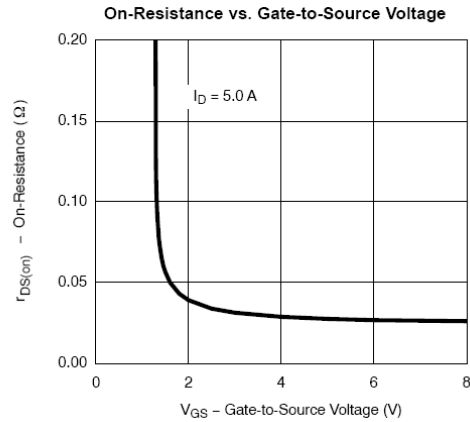
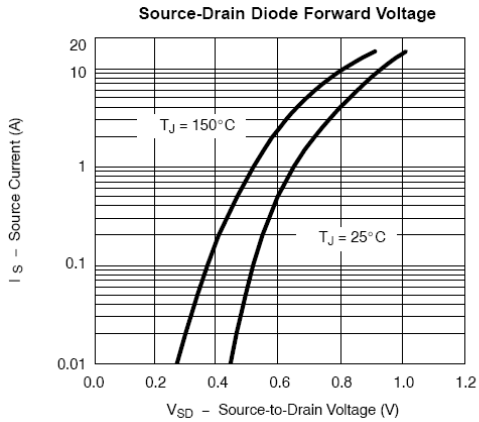
N Channel Enhancement Mode MOSFET

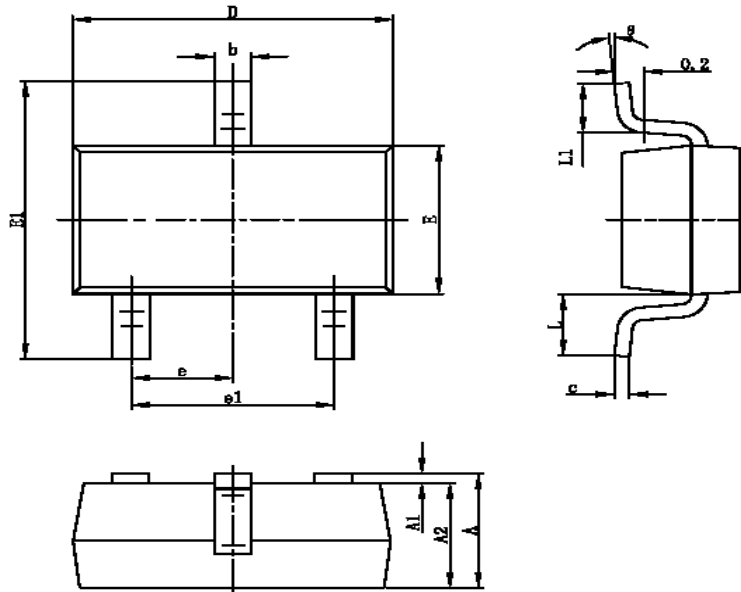
5.4A

**ELECTRICAL CHARACTERISTICS** ( Ta = 25°C Unless otherwise noted )

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0		3.0	V
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=24V, V_{GS}=0V$			1	uA
		$V_{DS}=24V, V_{GS}=0V$ $T_J=55^\circ C$			10	
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=4.0A$ $V_{GS}=4.5V, I_D=3.6A$		26 38		m $\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS}=4.5V, I_D=5.4A$		12		S
Diode Forward Voltage	$V_{SD}$	$I_S=1.7A, V_{GS}=0V$		0.8	1.2	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=15V$ $V_{GS}=10V$ $I_D=6.7A$		10	18	nC
Gate-Source Charge	$Q_{gs}$			1.6		
Gate-Drain Charge	$Q_{gd}$			3.1		
Input Capacitance	$C_{iss}$	$V_{DS}=15V$ $V_{GS}=0V$ $F=1MHz$		450		pF
Output Capacitance	$C_{oss}$			240		
Reverse Transfer Capacitance	$C_{rss}$			38		
Turn-On Time	$t_{d(on)}$ $t_r$	$V_{DD}=15V$ $R_L=15\Omega$ $I_D=1.0A$ $V_{GEN}=10V$ $R_G=6\Omega$		7	15	nS
Turn-Off Time	$t_{d(off)}$ $t_f$			10	20	
				20	40	
				11	20	

**TYPICAL CHARACTERISTICS (25°C unless otherwise noted)**


**TYPICAL CHARACTERISTICS (25°C unless otherwise noted)**


**SOT-23 PACKAGE OUTLINE**


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°