MODEL: ST4761B01-3

Ver. 0.1
Date: 08.Mar.2013

Customer's Approval	CSOT
Signature Date	Approved By Product Director Date Name:Richard Lung Signature:
	Reviewed By PM Manager Date Name:Aaron Tu Signature:
	Reviewed ByProject Leader Date Name:Guanzheng lee Signature:
	Reviewed ByPM Date Name:Yingnan Zou Signature:

Contents

Revision History

Version	Date	Page (New)	Section	Description	Revision by
Ver. 0.1	08.Mar..2013	All	All	Tentative Specification was First Issued.	Yingnan Zou

1. General Description

1.1 Product Features

- **FHD Resolution (1920 x 1080)**
- **VeryHigh Contrast Ratio:4000:1**
- **Fast Response Time**
- **Ultra Wide Viewing Angle: 178° (H)/178° (V)(CR≥10)**
- **DE (Data Enable) Mode**
- **LVDS (Low Voltage Differential Signaling) Interface**

1.2Overview

ST4761B01-3 is a diagonal47.6"color active matrix LCDopen cellwith2ch-LVDS interface. This open cellis a transmissive type display operating in the normally black mode. It supports 1920x1080FHD resolution and can display up to16.7M colors (8bit). Each pixel is divided into Red, Green and Blue sub-pixels which are arranged in vertical stripe.

This open celldedicates for LCD TV products and provides excellent performance which includes high transparency, ultra wide viewing angleand high color depth. CSOT open cell comply with RoHS for identification.

1.3 General Information

Item	Specification	Unit	Note
Active Area	1054.08(H)x592.92(V)	mm	
Cell Size	1068.750(H) x 607.610 (V) x 1.750 (D)	mm	
Weight	1.9	kg	Max.
Driving Scheme	a-Si TFT Active Matrix	-	
Number of Pixels	1920x1080	pixel	
Pixel Pitch (Sub Pixel)	0.183 (H) x 0.549 (V)	mm	
Pixel Arrangement	RGB Vertical Stripe	-	
Display Colors	16.7 M	color	8bit
Display Mode	Transmissive Mode, Normally Black	-	
Glass Thickness (Array/CF)	0.5/0.5	mm	
Color Chromaticity	R=(0.639,0.335) G=(0.319,0.626) B=(0.155,0.052) W=(0.280,0.290)		Typical value measured at CSOT's module: MT4761B01-1
Contrast Ratio	4000:1(Typ.)		
Cell Transmittance	5.65% (Typ.)	%	
View Angle(CR>10)	+89/-89(H),+89/-89(V) (Typ.)		
Polarizer(CF side)	Anti-glare, Haze2%, Hard Coating(3H)		
Polarizer(TFT side)	Hard Coating(3H)		

2.Absolute Maximum Ratings

2.1 AbsoluteMaximum Ratings ($T_A = 25 \pm 2$ °C)

The followings are maximum values which, if exceeded, may cause damage to the unit.

Item	Symbol	Value		Unit
		Min.	Max.	
Power Supply Voltage	V_{CC}	-0.3	13.8	V
Input Signal Voltage	V_{IN}	-0.3	4.0	V

2.2 Environment Requirement (BasedonCSOT ModuleMT4761B01-1)

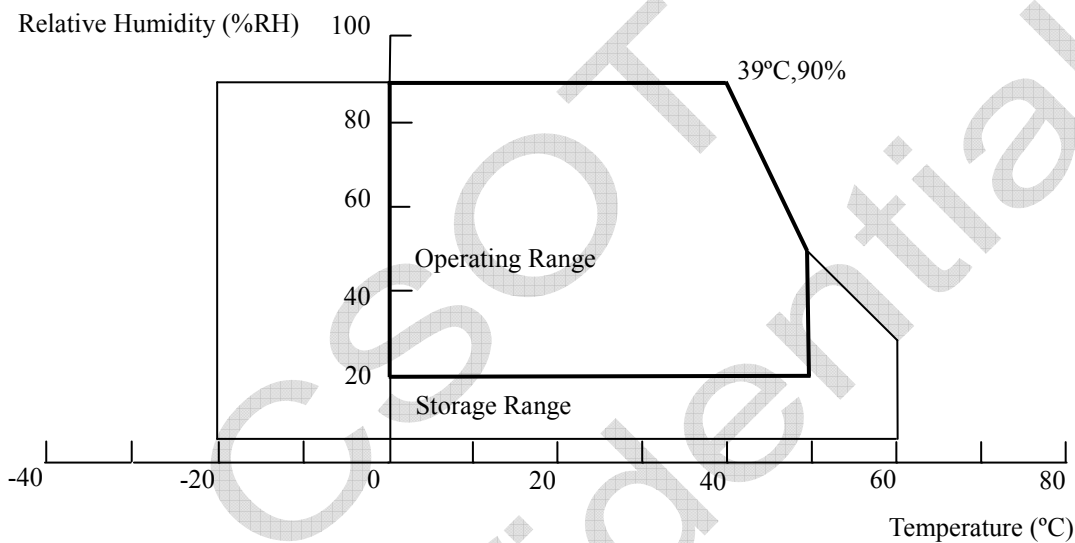(1) Temperature and relative humidity range are shown as below.

Fig. 2.1Operating and storage environment

(a) 90%RH maximum ($T_A \leq 39$ °C).

(b) Wet-bulb temperature should be 39ºCmaximum ($T_A > 39$ °C).

(c) No condensation.

(2) The storage temperature is between - 20 ºCto 60 ºC,and the operating ambient temperature is between 0 ºC to 50 ºC.

The maximum operating temperature is based on the testcondition that the surface temperature of display area is less than or equalto 65ºC with LCD module in a temperature controlled chamber alone. Thermalmanagement should be considered in final product design to prevent the surfacetemperature of display area from being over 65ºC. The range of operating temperature may degrade in case of improper thermal management in the end product design.

(3) The rating of environment is based on LCD module. Leave LCD cell alone, this environment conditioncan't be guaranteed. Except LCD cell, the customer has to consider the ability of other parts of LCDmodule and LCD module process.

2.3 AbsoluteRatings of Environment (Open Cell)

When storing open cell as spares for a long time,please follow the precaution instructions:

(1) Do not store the module in high temperatureand high humidity for a long time. It is highly recommended to store the module with temperature from20ºC to 30ºCin normal humidity (50±10%RH) with shipping package.

(2)The open cell should be keep within one month shelf life

3.Electrical Specification

3.1 Open Cell Power Consumption (TA = 25 ± 2 °C)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12.0	13.2	V	(1)
Rush Current		I_{RUSH}	-	-	2.0	A	(2)
Power Supply Current	White Pattern	I_{CC}	-	0.38	0.49	A	(3)
	Horizontal Stripe	I_{CC}	-	0.78	1.01	A	
	Black Pattern	I_{CC}	-	0.34	0.44	A	

Note:

(1)The ripple voltage should be controlled less than10%ofV_{CC}.

(2)Measurement condition: $V_{CC=12V}$ rising time=470μs.

Fig. 3.1 V_{CC} rising time condition
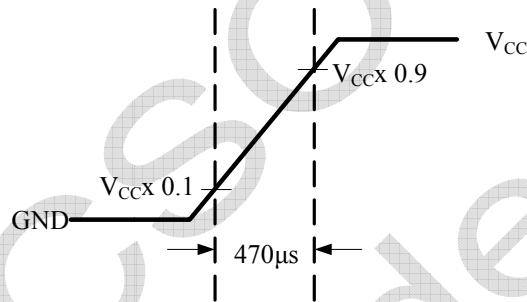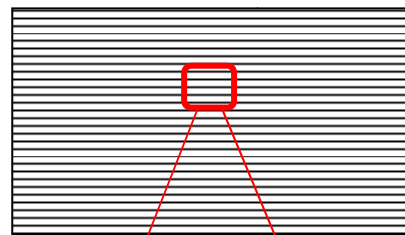
(3)Measurement condition:V_{CC}=12V, Ta = 25 ± 2ºC, F = 60 Hz. The test patterns are shown as below.

A. White Pattern

B. Horizontal Pattern

C. Black Pattern
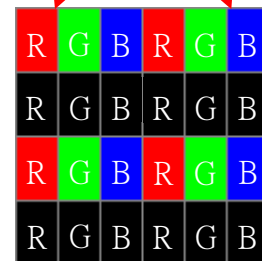
Fig. 3.2 Test patterns

3.2 LVDS Characteristics

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
LVDS Interface	Differential Input High Threshold Voltage	V_{TH}	+100	-	-	mV	(1)
	Differential Input Low Threshold Voltage	V_{TL}	-	-	-100	mV	
	Common InputVoltage	V_{CM}	1.0	1.2	1.4	V	
	Differential Input Voltage	$|V_{ID}|$	200	400	600	mV	
	Terminating Resistor	R_T	87.5	100	112.5	ohm	
CMOSInterface	Input High ThresholdVoltage	V_{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	-	0.7	V	

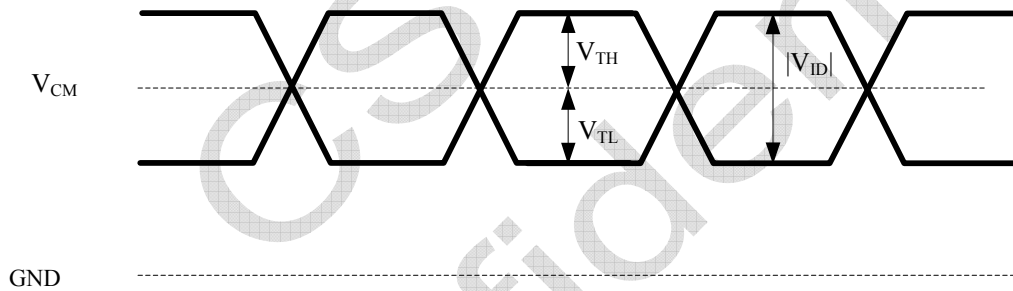Note:

(1) The LVDS input signal has been defined as follows:

Fig. 3.3 LVDS input signal

4.Input Terminal Pin Assignment

4.1 Interface Pin Assignment

CN1: CT000041-513C (FCN)or equivalent(see Note (1))

Pin No.	Symbol	Description	Note
1	N.C	No Connection	(1)
2	SCL	I2C Serial Clock (for 3D Format Selection Function)	
3	SDA	I2C Serial Data (for 3D Format Selection Function)	
4	N.C	No Connection	(1)
5	L/R_O	Output Signal for Left Right Glasses Control (High: Left Glass turn onLow:Right glass turn on)	
6	N.C.	No Connection	
7	SELLVDS	Input Signal for LVDS Data Format Selection (High:VESA Format,Low or Open JEIDA Format)	(2)
8	N.C.	No Connection	(1)
9	N.C.	No Connection	(1)
10	N.C.	No Connection	(1)
11	GND	Ground	
12	ORX0-	Odd Pixel Negative LVDS Differential Data Input. Channel 0	
13	ORX0+	Odd Pixel Positive LVDS Differential Data Input. Channel 0	
14	ORX1-	Odd Pixel Negative LVDS Differential Data Input. Channel 1	
15	ORX1+	Odd Pixel Positive LVDS Differential Data Input. Channel 1	
16	ORX2-	Odd Pixel Negative LVDS Differential Data Input. Channel 2	
17	ORX2+	Odd Pixel Positive LVDS Differential Data Input. Channel 2	
18	GND	Ground	
19	OCLK-	Odd Pixel Negative LVDS Differential Clock Input	
20	OCLK+	Odd Pixel Positive LVDS Differential Clock Input	
21	GND	Ground	
22	ORX3-	Odd Pixel Negative LVDS Differential Data Input. Channel 3	
23	ORX3+	Odd Pixel Positive LVDS Differential Data Input. Channel 3	
24	N.C.	No Connection	(1)
25	N.C.	No Connection	(1)
26	2D/3D	Input Signal for 2D/3D Mode Selection (High:3D Enable,LOW:3D Disable)	
27	N.C.	No Connection	(1)
28	ERX0-	Even Pixel Negative LVDS Differential Data Input. Channel 0	
29	ERX0+	Even pixel Positive LVDS Differential Data Input. Channel 0	
30	ERX1-	Even Pixel Negative LVDS Differential Data Input. Channel 1	

31	ERX1+	Even Pixel Positive LVDS Differential Data Input. Channel 1	
32	ERX2-	Even Pixel Negative LVDS Differential Data Input. Channel 2	
33	ERX2+	Even Pixel Positive LVDS Differential Data Input. Channel 2	
34	GND	Ground	
35	ECLK-	Even Pixel Negative LVDS Differential Clock Input	
36	ECLK+	Even Pixel Negative LVDS Differential Clock Input	
37	GND	Ground	
38	ERX3-	Even Pixel Negative LVDS Differential Data Input. Channel 3	
39	ERX3+	Even Pixel Positive LVDS Differential Data Input. Channel 3	
40	N.C.	No Connection	
41	N.C.	No Connection	
42	N.C.	No Connection	(1)
43	N.C.	No Connection	(1)
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	N.C.	No Connection	(1)
48	VCC	+12V Power Supply	
49	VCC	+12V Power Supply	
50	VCC	+12V Power Supply	
51	VCC	+12V Power Supply	

Note:

(1)For CSOT internal only,please let it open.

(2) High: connect to +3.3V→VESA Format;Low: connect to GND or Open→JEIDA format.

(3)The first LVDS data is ODD LVDS data
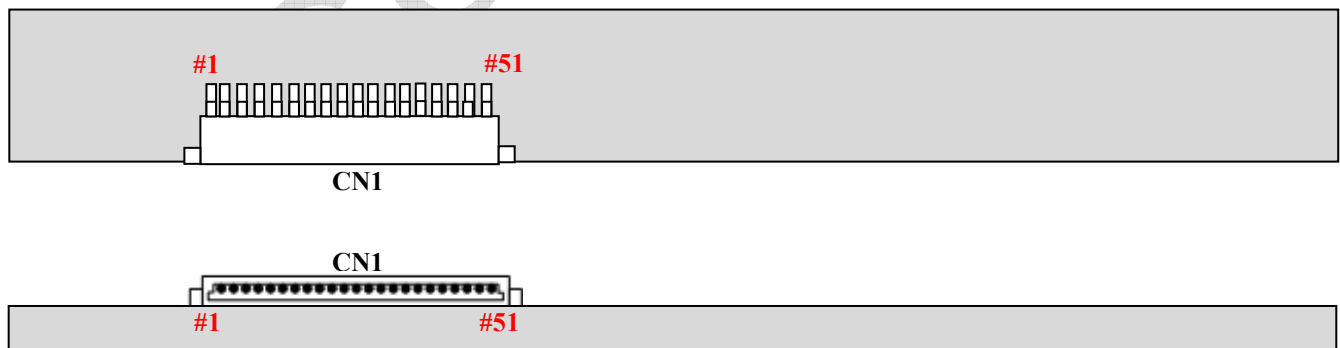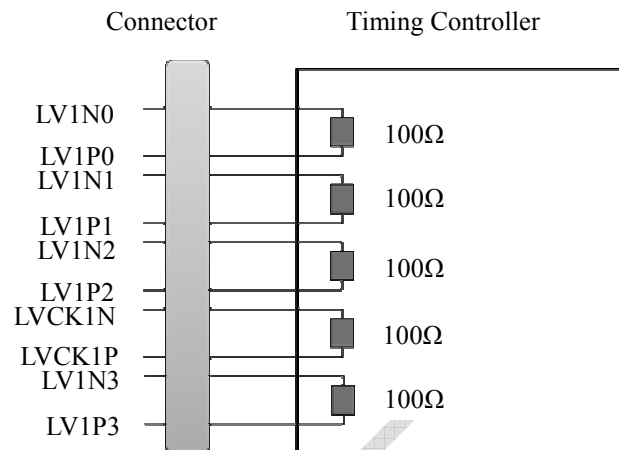
(4)The direction of pin assignment is shown as below:

Fig. 4.1 LVDS connector direction sketch map

4.2 Block Diagram of Interface

Connector   Timing Controller

LV1N0 — 100Ω
LV1P0
LV1N1 — 100Ω
LV1P1
LV1N2 — 100Ω
LV1P2
LVCK1N — 100Ω
LVCK1P
LV1N3 — 100Ω
LV1P3

Attention:

(1) Thisopen cell uses a 100 ohms (Ω) resistor between positive and negative lines of each receiver input.

(2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line respectively.

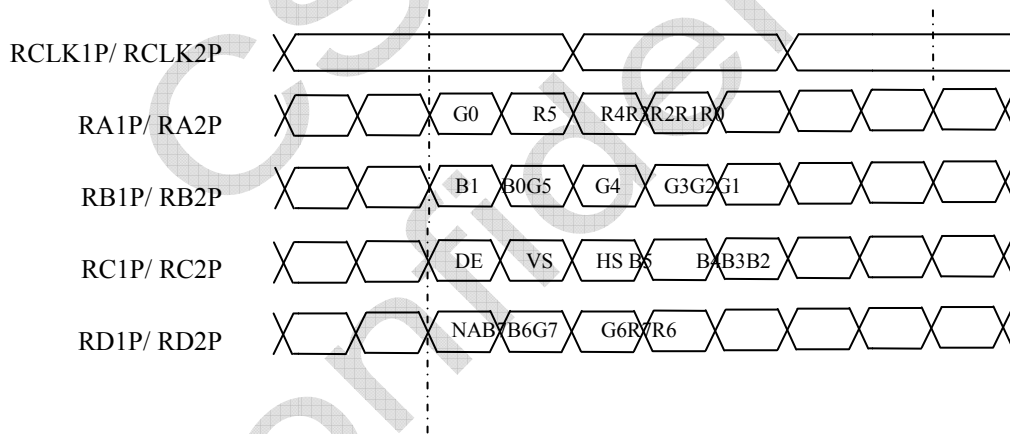## 4.3 LVDS Interface

4.3.1 VESA Format (SELLVDS = H)

RCLK1P/ RCLK2P

RA1P/ RA2P   G0 R5 R4R3R2R1R0

RB1P/ RB2P   B1 B0G5 G4 G3G2G1

RC1P/ RC2P   DE VS HS B5 B4B3B2

RD1P/ RD2P   NAB7B6G7 G6R7R6

Fig. 4.2VESAformat

4.3.2 JEIDA Format (SELLVDS = L or Open)

RCLK1P / RCLK2P

RA1P/ RA2P   G2   R7   R6R5R4R3R2

RB1P/ RB2P   B3   B2G7   G6   G5G4G3

RC1P/ RC2P   DE   VS   HS B7   B6B5B4

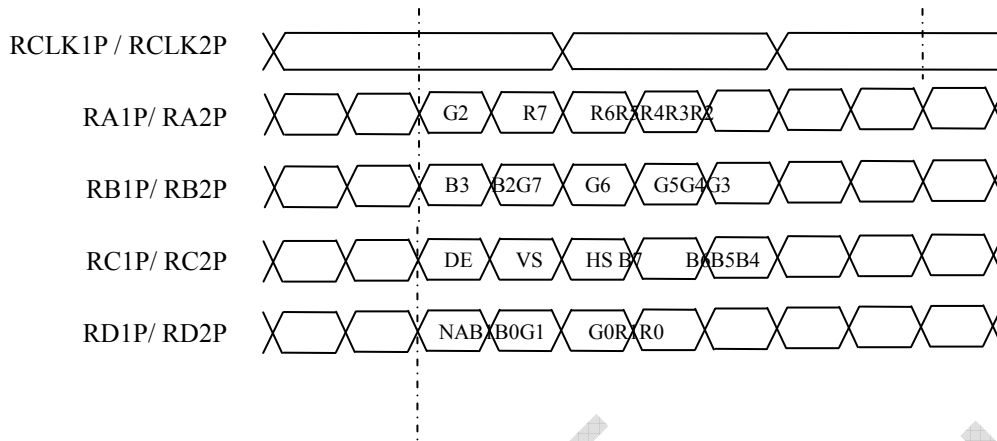RD1P/ RD2P   NAB   B0G1   G0R1   R0
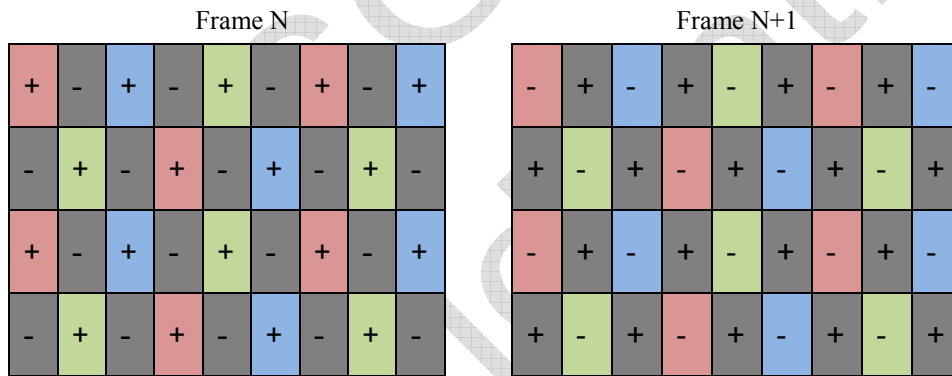
Fig. 4.3 JEIDA format

4.4 Pattern FOR Vcom Adjustment

Dot - inversion pattern

Frame N   Frame N+1

5.Interface Timing

5.1 TimingTable (DE Only Mode)

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDSClock	Frequency	F_{CLK} $(=1/T_{CLK})$	55.2	74.25	77.8	MHz	
Vertical Term	Frame Rate	F	57	60	62.5	Hz	
	Total	T_V	1115	1125	1380	T_H	$T_V=T_{VD}+T_{VB}$
	Display	T_{VD}		1080			
	Blank	T_{VB}	35	45	300	T_H	
Horizontal Term	Total	T_H	1050	1100	1150	T_{CLK}	$T_H=T_{HD}+T_{HB}$
	Display	T_{HD}		960			
	Blank	T_{HB}	90	140	190	T_{CLK}	

Attention:

(1)The module is operated in DE only mode, Hsync and Vsync input signal have no effect on normal operation.
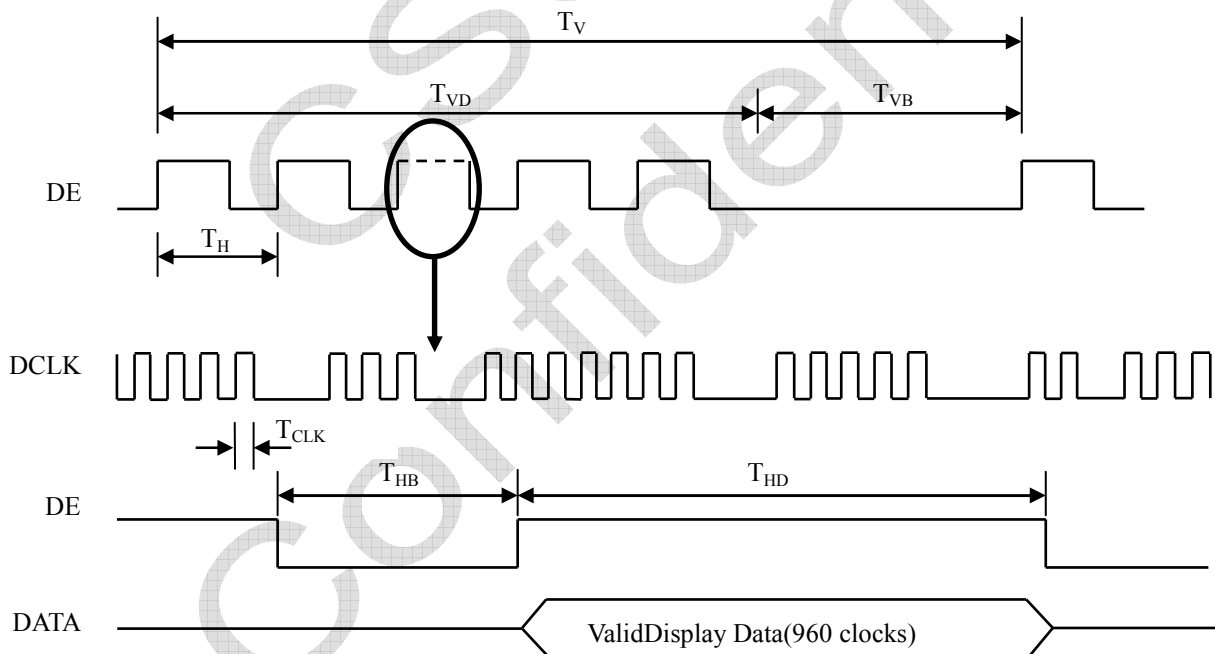

Fig. 5.1 Interface signal timingdiagram

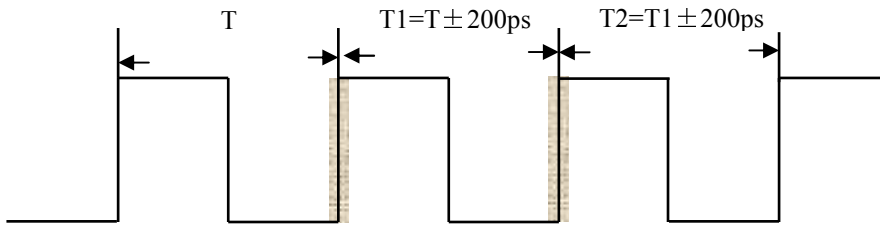(2) The input clock cycle-to-cycle is defined as below figures.

Fig. 5.2 jitter

6. Optical Characteristics

6.1 Measurement Conditions

The tablebelow is the test condition of optical measurement.

Item	Symbol	Value	Unit
Ambient Temperature	T_A	25±2	ºC
Ambient Humidity	H_A	50±10	%RH
Supply Voltage	V_{CC}	12	V
Driving Signal	Refer to the typical value inChapter 3: Electrical Specification		
Vertical Refresh Rate	F_R	120	Hz

To avoid abrupt temperature change during optical measurement, it's suggested to warm up the LCD module more than 60 minutes after lighting the backlight and in the windless environment.

To measure the LCD cell, it is suggested to set up the standard measurement system as Fig. 6.1. The measuring area S should contain at least 500 pixels ofthe LCD cell as illustrated in Fig.6.2(A means the area allocated to one pixel).In this model, for example, the minimum measuring distance Z is 370mm when θ is 2 degree. Hence, 500mm is the typical measuring distance. This measuring condition is referred to 301-2H of VESA FPDM 2.0 about viewing distance, angle, and angular field of view definition.
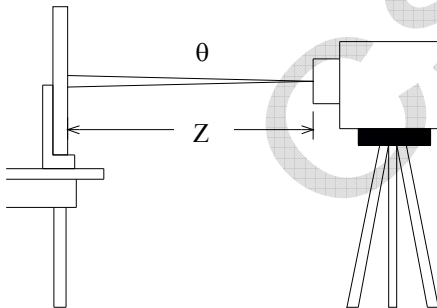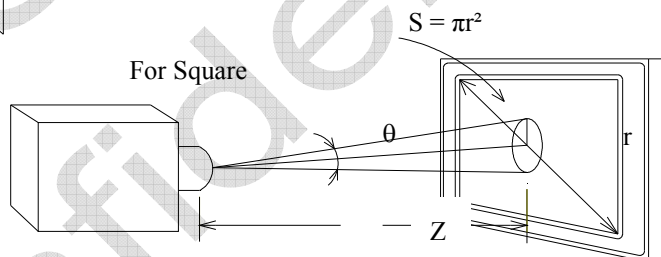
Fig. 6.1The standard set-up system of measurement   Fig. 6.2The area S contains at least 500 pixels to be measured

$$N = \frac{S}{A} \geqslant 500\text{pixels}$$

N means the actual number of the pixels in the area S.

6.2 Optical Specifications

The table below of optical characteristics is measured by MINOLTA CS2000,MINOLTA CA310, ELDIM OPTIScope-SAand ELDIM EZContrast in dark room.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Static Contrast Ratio		CR		-	4000	-	-	(1) (2)
Response Time		T_L		-	6.5	12	ms	(3)
Center Transmittance		T%		-	5.65		%	(2)(4)
Color Chromaticity (CIE1931)	Red	R_X	$\theta_H=0°$, $\theta_V=0°$ Normal direction at center point withCSOT's module: MT4761B01-1	Typ. - 0.03	0.639	Typ. +0.03	-	(2) (5)
		R_Y			0.335		-	
	Green	G_X			0.319		-	
		G_Y			0.626		-	
	Blue	B_X			0.155		-	
		B_Y			0.052		-	
	White	W_X			0.280		-	
		W_Y			0.290		-	
	Color Gamut	CG		-	72	-	% NTSC	
Viewing Angle	Horizontal	θ_{H+}	CR≥10	-	89	-	Deg.	(6)
		θ_{H-}		-	89	-		
	Vertical	θ_{V+}		-	89	-		
		θ_{V-}		-	89	-		

Note:

(1)Definition of static contrast ratio (CR):

It's necessary to switch off all the dynamic and dimming function when measuring the static contrast ratio.

$$\text{Static Contrast Ratio (CR)} = \frac{\text{CR-W}}{\text{CR-D}}$$

CR-W is the luminancemeasured by LMD (light-measuring device) at the center point of the LCD module with full-screen displaying white. The standard setup of measurement is illustrated in Fig. 6.3; CR-D is the luminance measured by LMD at the center point of the LCD module with full-screen displaying black. The LMD in this item is CS2000.

(2)The LMD in the item could be a spectroradiometer such as (KONICA MINOLTA) CS2000, CS1000(TOPCON), SR-UL2 or the same level spectroradiometer. Other display color analyzer (KONICA MINOLTA) CA210, CA310 or (TOPCON) BM-7 could be involved after being calibrated with a spectroradiometer on each stage of a product.
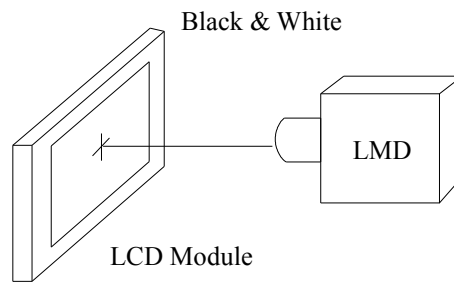
Fig. 6.3 The standard setup of CR measurement

(3) Response time T_L is defined as the average transition time in the response time matrix. The table below is the response time matrix in which each element $t_{X \text{ to } Y}$ is the transition time from luminance ratio X to Y. X and Yare two different luminance ratiosamong0%,25%,50%,75%, and 100%luminance. The transition time $t_{X \text{ to } Y}$ is defined as the time taken from 10% to 90% of the luminance difference between X and Y (X<Y) as illustrated in Fig.6.4. When X>Y, the definition of $t_{X \text{ to } Y}$ is the time taken from 90% to 10% of the luminance difference between X and Y.The response time is optimized on refresh rate F_r=60Hz.

Measured Transition Time		Luminance Ratio of Previous Frame				
		0%	25%	50%	75%	100%
Luminance Ratio of Current Frame	0%		$t_{25\% \text{ to } 0\%}$	$t_{50\% \text{ to } 0\%}$	$t_{75\% \text{ to } 0\%}$	$t_{100\% \text{ to } 0\%}$
	25%	$t_{0\% \text{ to } 25\%}$		$t_{50\% \text{ to } 25\%}$	$t_{75\% \text{ to } 25\%}$	$t_{100\% \text{ to } 25\%}$
	50%	$t_{0\% \text{ to } 50\%}$	$t_{25\% \text{ to } 50\%}$		$t_{75\% \text{ to } 50\%}$	$t_{100\% \text{ to } 50\%}$
	75%	$t_{0\% \text{ to } 75\%}$	$t_{25\% \text{ to } 75\%}$	$t_{50\% \text{ to } 75\%}$		$t_{100\% \text{ to } 75\%}$
	100%	$t_{0\% \text{ to } 100\%}$	$t_{25\% \text{ to } 100\%}$	$t_{50\% \text{ to } 100\%}$	$t_{75\% \text{ to } 100\%}$	

$t_{X \text{ to } Y}$ means the transition time from luminance ratioX to Y.
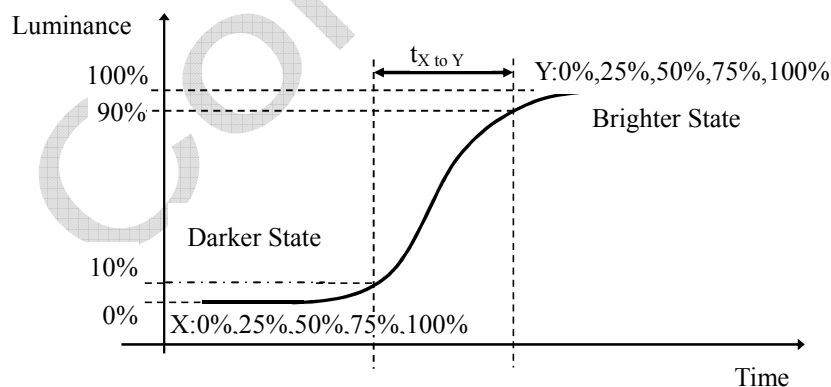
Fig. 6.4The definition of $t_{X \text{ to } Y}$

All the transition time is measured at the center point of the LCD module by ELDIM OPTIScope-SA.

(4) Definition of center Transmittance (T%):

Thetransmittance is measured with full white pattern (Gray 255)

$$\text{Static Contrast Ratio (CR)} = \frac{\text{Luminance of LCD module}}{\text{Luminance of Backlight}}$$

(5) Definition of color chromaticity:

Each chromaticity coordinates (x, y) are measured in CIE1931 color space when full-screen displaying primary color R, G, B and white. The color gamut is defined as the fraction in percent of the area of the triangle bounded by R, G, B coordinates and the area is defined by NTSC 1953 color standard in the CIE color space. Chromaticity coordinates are measured by CS2000 and the standard setup of measurement is shown in Fig. 6.5.
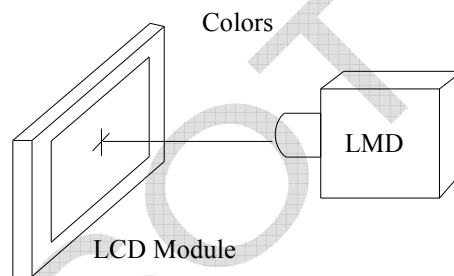

Fig. 6.5 The standard setup of color chromaticity measurement

(6)Definition of viewing angle coordinate system (θ_H,θ_V):

The contrast ratio is measured at the center point of the LCD module. The viewing angles are defined at the angle that the contrast ratio is larger than 10 at four directions relative to the perpendicular direction of the LCD module(two vertical angles:up θ_{V+} and downθ_{V-}; and two horizontal angles:right θ_{H+} and leftθ_{H-}) as illustrated in Fig. 6.6. The contrast ratio is measured by ELDIM EZContrast.
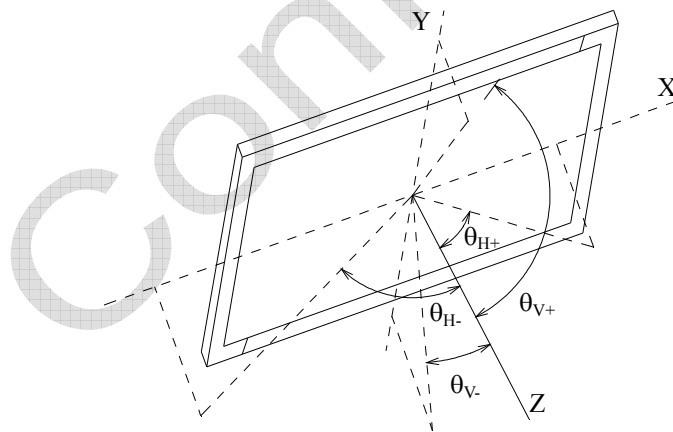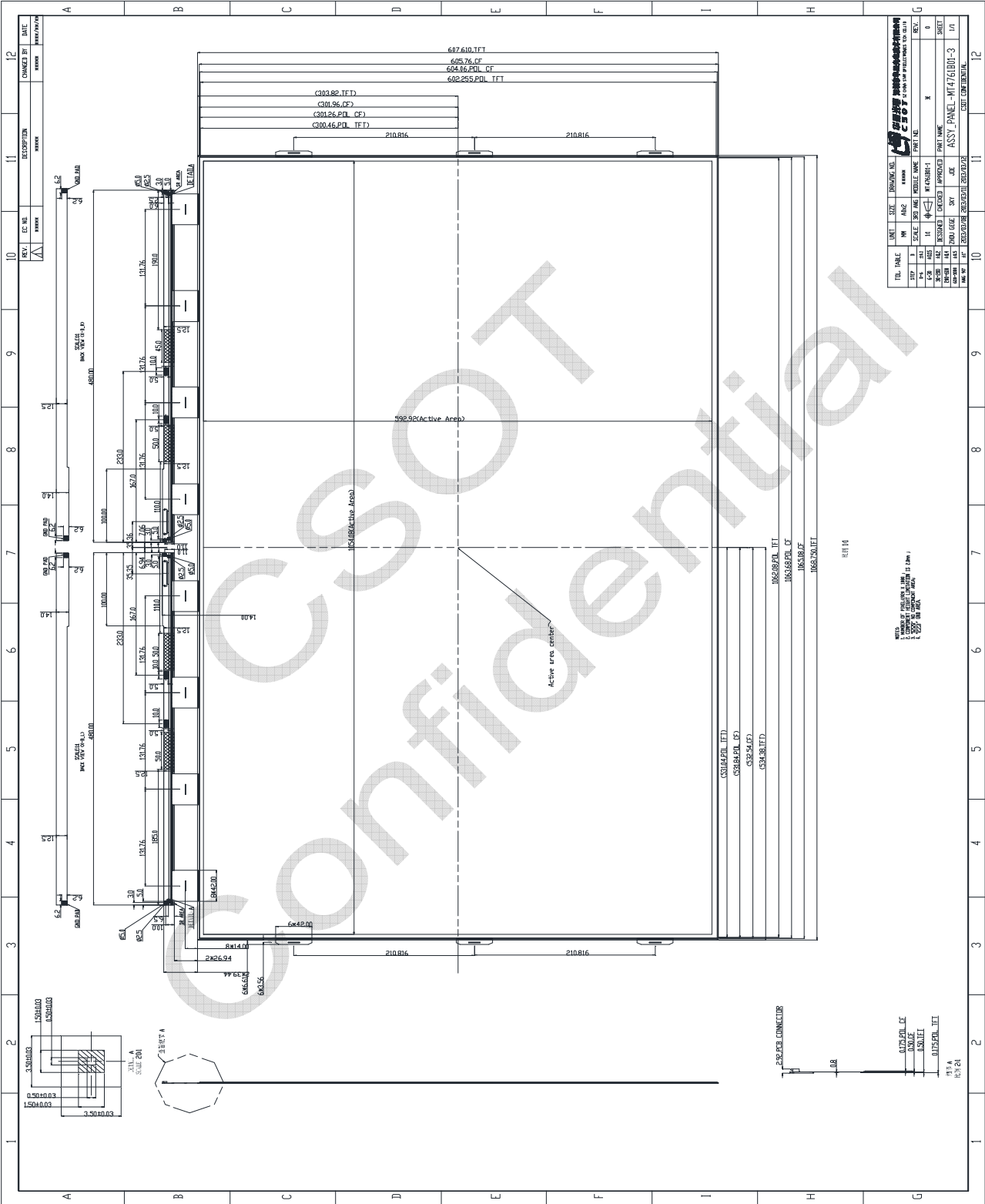

Fig. 6.6Viewing angle coordination system

7. MechanicalCharacteristics
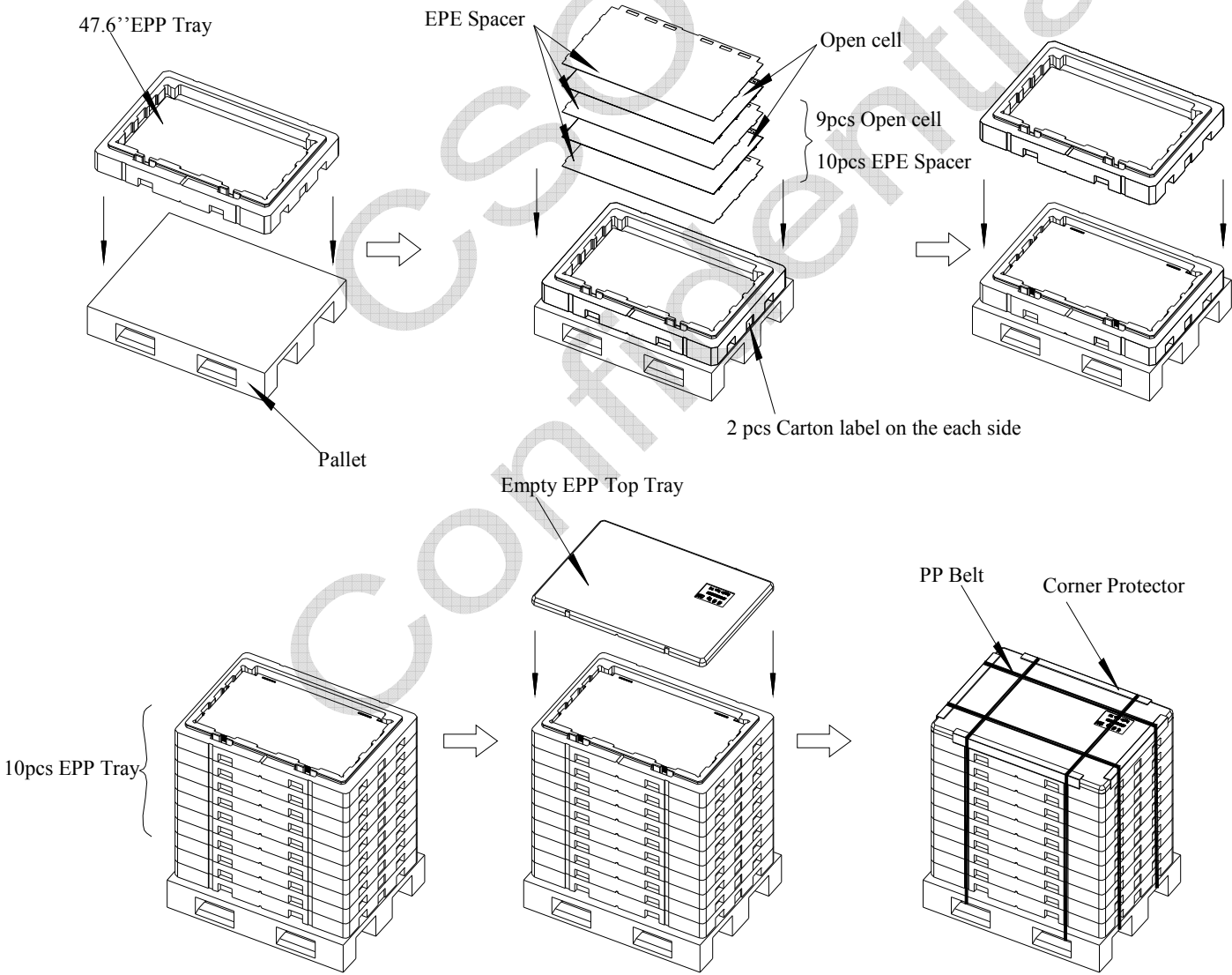
7.1Mechanical Specification

7.2 Packing

7.2.1PackingSpecifications

Item	Specification		
	Quantity	Dimension (mm)	Weight (kg)
Packing Box	9 pcs/box	1235(L) x 883 (W) x95 (H)	Net Weight: 18 (Max.) Gross Weight: 22(Max.)
Pallet	1	1250.00 (L) x 1000.00 (W) x 160.00 (H)	Net Weight:22
Stack Layer	10		
Boxes per Pallet	10boxes/pallet		
Pallet after Packing	90pcs/pallet	1250.0 (L) x 1000.0 (W) x 995.0 (H)	Gross Weight:244kg/pallet

7.2.2 PackingMethod

47.6''EPP Tray

Pallet

EPE Spacer

Open cell

9pcs Open cell

10pcs EPE Spacer

2 pcs Carton label on the each side

Empty EPP Top Tray

PP Belt   Corner Protector

10pcs EPP Tray

PE Sheet

PE Film

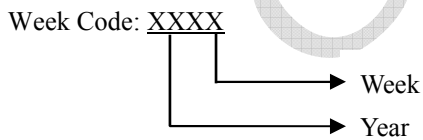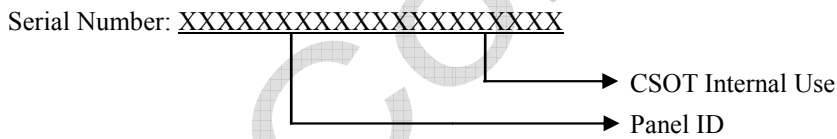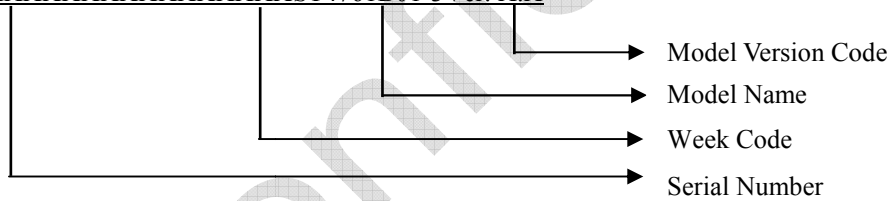2 pcs Carton label on the each side

PP Belt   PP Belt
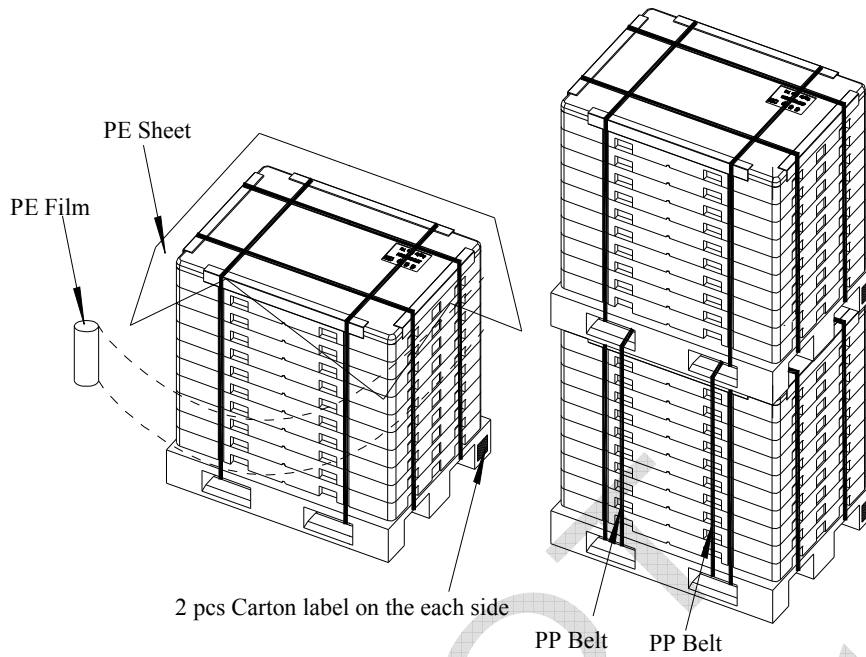
8. Definition of Labels

8.1Open CellLabel

XXXXXXXXXXXXXXXXXXXXXXXXXXST4761B01-3Ver. X.X

→ Model Version Code

→ Model Name

→ Week Code

→ Serial Number

Serial Number: XXXXXXXXXXXXXXXXXXX

→ CSOT Internal Use

→ Panel ID

Week Code: XXXX

→ Week

→ Year
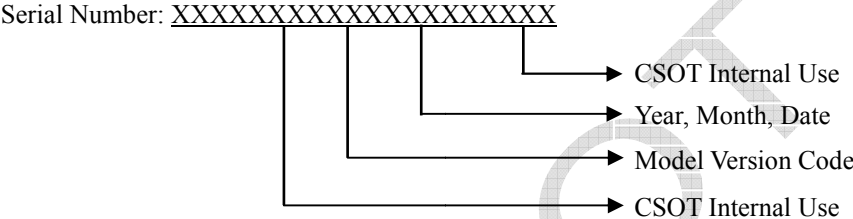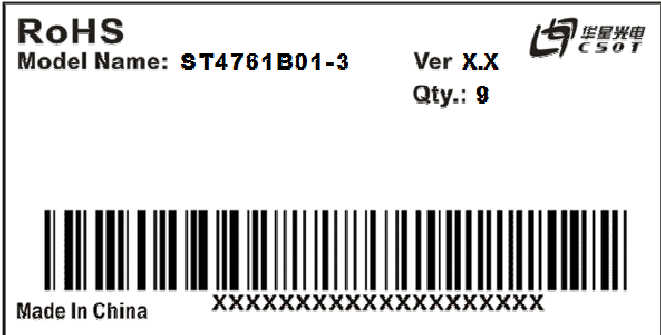
Year: 2010 =10, 2011 = 11 …2020= 20, 2021= 21…

Week: 01, 02, 03 …

Model Name: ST4761B01-3

Ver.X.X: Version, for example: 0.1, 0.2, … , 1.1, 1.2, …, 2.1, 2.2, …

8.2 Carton Label

Serial Number: XXXXXXXXXXXXXXXXXXXX

→ CSOT Internal Use
→ Year, Month, Date
→ Model Version Code
→ CSOT Internal Use

8.3 PalletLabel

Model Name: ST4761B01-3

Serial Number: XXXXXXXXXXXXX

→ CSOT Internal Use
→ Year, Month
→ Model Version Code
→ CSOT Internal Use
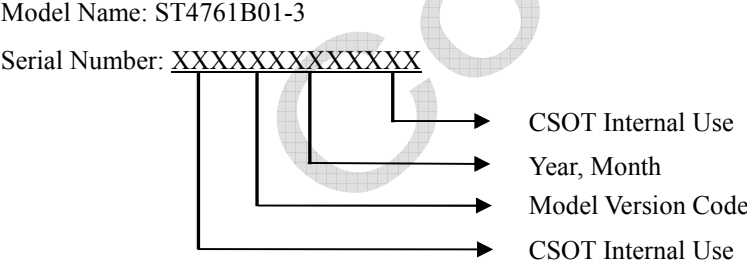
9. Precautions

9.1 Assembly and Handling Precautions

(1) Do not apply rough force such as bending or twisting to the open cell during assembly.

(2) It is recommended to assemble or install a open cell into the user's system in clean working areas. The dust and oil may cause electrical shortor damage the polarizer.

(3) Do not apply pressure or impulse to the open cell to prevent the damage to the open cell.

(4) Always follow the correct power-on sequence. This can prevent the damage and latch-up to the LSI chips.

(5) Do not plug in or pull out the interface connector while the open cell is in operation.

(6)Use soft dry clothwithout chemicals for cleaning because the surface of polarizeris very soft and easily be scratched.

(7) Moisture can easily penetrate into the open cell and may cause the damage during operation.

(8) High temperature or humidity may deteriorate the performance of the open cell. Please store open cell in the specified storageconditions.

(9) When ambient temperature is lower than 10ºC, the display quality might be deteriorated. For example, the response time will become slow.

9.2 Safety Precautions

(1) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(2)After the open cell end of life, it is not harmful in case of normal operation and storage.