

## Features and Benefits

- 3-Axis Electronic Magnetometer
- Cost effective and compact solution
- Factory set full scale range  
Max  $\pm 48$  gauss selectable
- On chip EEPROM trimming
- Operating temp range:-  $40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
- 1.8V compatible IO
- 16 bits ADC
- Fast mode IIC serial interface
- Interrupt supported
- RoHS compliant

## Applications

- Electronic Compass
- Smartphone
- Tablet PC
- Handheld devices

## General Description

The ST480M is an integrated 3-axis magnetometer with signal processing circuitry and integrated IIC interface. It provides excellent temperature stability and high resolution over the whole operating temperature range ( $-40^{\circ}\text{C} \sim 85^{\circ}\text{C}$ ).

The ST480M has  $\pm 48$  gauss Full Scale Range to provide multi-domain application.

The ST480M delivers output signal proportional to magnetic field it measures on each axis. Meanwhile, it provides an IIC digital output. Factory trimmed scale factors eliminate the need for external active components and end-user calibration.

The ST480M is packaged in BGA, QFN, Flip LGA or WL-CSP package.

## Order Information

Model Name	Full Scale Range	Package Description
ST480MC	$\pm 48$ gauss	8pin WL-CSP, $1.28*1.28*0.5\text{mm}^3$
ST480MW	$\pm 48$ gauss	14pin BGA, $1.6*1.6*0.85\text{mm}^3$
ST480MF	$\pm 48$ gauss	14pin Flip-LGA, $1.6*1.6*0.75\text{mm}^3$
ST480MB	$\pm 48$ gauss	14pin BGA, $2*2*0.85\text{mm}^3$
ST480MQ	$\pm 48$ gauss	16pin QFN, $3*3*0.85\text{mm}^3$

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## 1. Functional Diagram

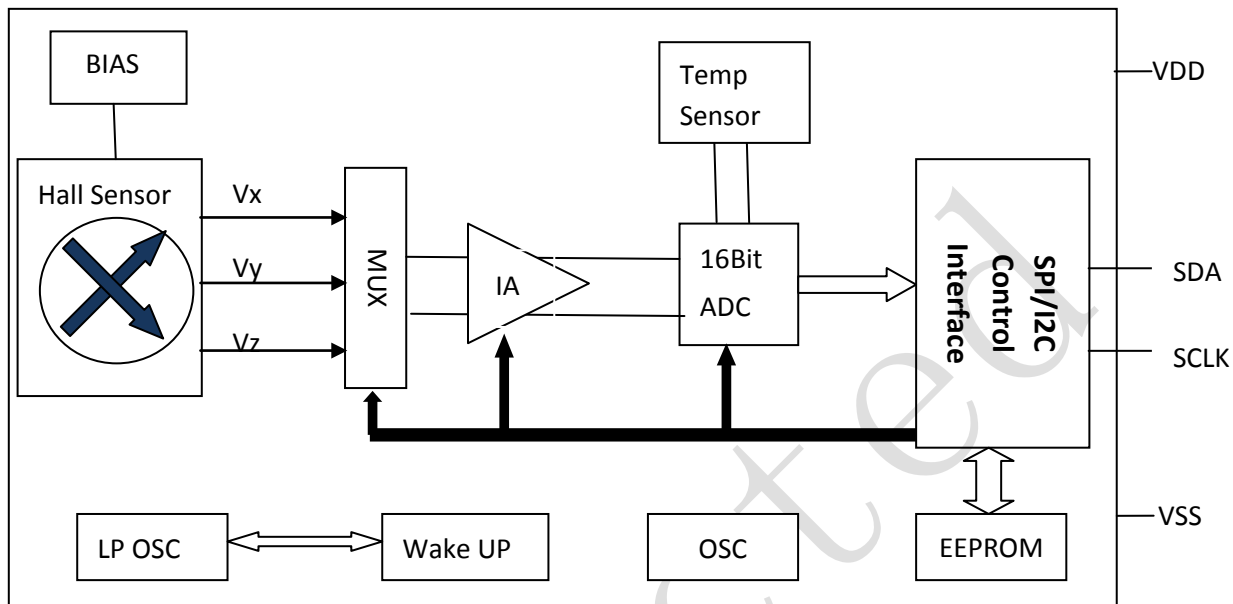


Figure 1: Function block diagram

## 2. Sensor Specifications

DC Operating Parameters T=-40°C to 85°C, Vdd=2.2V to 3.6V (unless otherwise specified)

All parameters are specified @ Vdd=3.0V and T=25°C

Parameter	Conditions	Min.	Typ.	Max.	Unit
Full Range	Each axis		±48		gauss
Non Linearity	±48gauss		0.1		% of FS
Sensitivity	Z axis		400		LSBs/Gauss
	X and Y axis		667		LSBs/Gauss
Magnetic Resolution	Z axis		2.5		mG/LSB
	X and Y axis		1.5		mG/LSB
T <sub>CONV</sub>	From idle to data ready	1		256	mS
T <sub>STBY</sub>	From IDLE to STBY		250		μS
T <sub>ACTIVE</sub>	From STBY to ACTIVE		8		μS
T <sub>INTERVAL</sub>	Time in between 2 conversions(Burst mode or Wake-up on Change)	20		5000	mS
T <sub>POR</sub>	Power-on-reset completion time		0.6	1.5	ms
T <sub>CONVM</sub>	Single Magnetic axis conversion time(1) typical programming range	0.192		66.56	ms
		[(2+2 <sup>DIG_FILT</sup> )*2 <sup>OSR</sup> *0.064]			
T <sub>CONVT</sub>	Temperature conversion time typical programming range	0.192		1.54	ms
		[2 <sup>OSR2</sup> *0.192]			
T <sub>CONV_SMM</sub>	Total conversion time in Single Measurement Mode(1)	T <sub>STBY</sub> + T <sub>ACTIVE</sub> + m*T <sub>CONVM</sub> + T <sub>CONVT</sub>			ms
T <sub>CONV_BURSTWOC</sub>	Total conversion time in BURST or WOC Mode(1)	T <sub>ACTIVE</sub> + m*T <sub>CONVM</sub> + T <sub>CONVT</sub>			ms

(1) This conversion time is defined as the time to acquire a single axis of the magnetic flux density. When measuring multiple axes, they are obtained through time-multiplexing, i.e. X(t), Y(t+T<sub>CONVM</sub>) and Z(t+2\*T<sub>CONVM</sub>). The conversion time is programmable through parameters OSR and DIG\_FILT for magnetic conversion time and OSR<sub>2</sub> for temperature conversion time.

(2) The time T<sub>INTERVAL</sub> is defined as the time between the end of one set of measurements (any combination of TXYZ) and the start of the following same set of measurements in BURST and

WOC mode.

### 3. Electrical Characteristics

Electrical characteristics @ Vdd=3.0V, T=25°C unless otherwise noted

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Power supply		2.2	3	3.6	V
VLOGIC	Digital IO power supply		1.65	1.8	VDD	V
I <sub>DD· CONV</sub>	Conversion Current			2.4	3.5	mA
I <sub>DD· STBY</sub>	Standby Current			80		μA
I <sub>DD· IDLE</sub>	Idle current			1	2	μA
I <sub>DD· NOM</sub>	Nominal Current	Data-rate =10Hz, t <sub>CONV</sub> =16mS		0.4		mA

### 4. Absolute Maximum Ratings

Stress above those listed as “Absolute Maximum Ratings” may cause permanent damage to the device.

Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Parameter	Min	Max	Unit
Operating supply voltage	-0.3	6	V
Operating Temperature	-40	85	°C
Storage Temperature Range	-50	125	°C
ESD( HBM )		2000	V

### 5. Pin Order and Pin Description

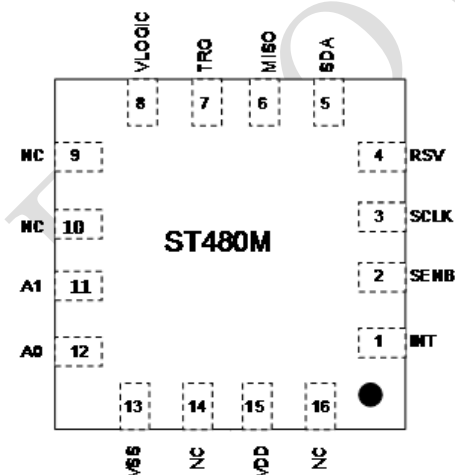


Figure 5.1: PIN Order for ST480MQ Top view  
QFN-16pin 3 x 3 x 0.85mm<sup>3</sup>

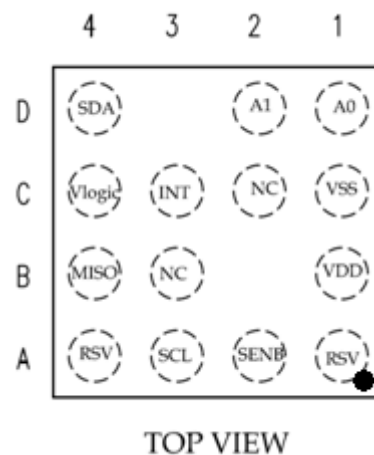
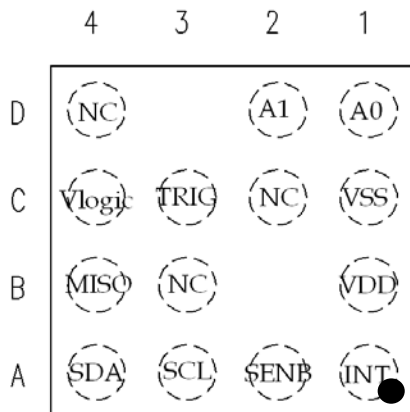
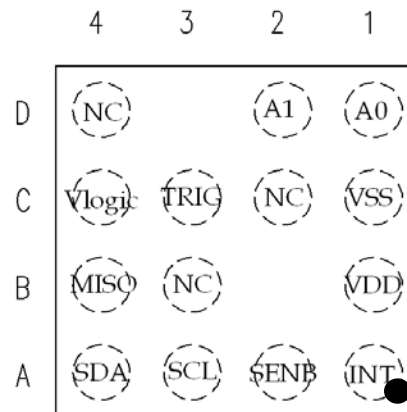


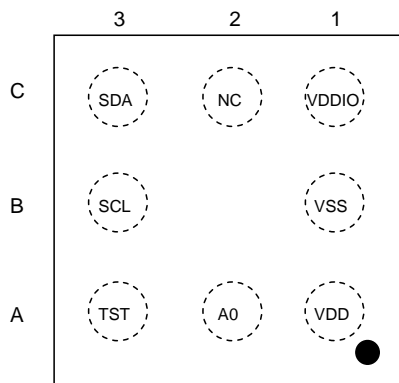
Figure 5.2: PIN Order for ST480MB Top view  
BGA-14pin 2 x 2 x 0.85 mm<sup>3</sup>



**Figure 5.3: PIN order for ST480MF Top view**  
Flip-LGA 14pin 1.6 x 1.6 x 0.75 mm<sup>3</sup>



**Figure 5.4: PIN order for ST480MW Top view**  
BGA 14pin 1.6 x 1.6 x 0.85 mm<sup>3</sup>



**Figure 5.5: PIN order for ST480MC Top view**  
WL-CSP 8pin 1.28 x 1.28 x 0.5 mm<sup>3</sup>

Table PIN Description (may be changed to compliant with 3 types of pin orders, note1)

PIN No. ST480MQ	PIN No. ST480MB	PIN No. ST480MF ST480MW	PIN Name	PIN Function
1	C3	A1	INT	Interrupt output, read data while INT is High
2	A2	A2	SENB	BUS Select; SENB=0 for SPI; SENB=1 for IIC;
3	A3	A3	SCLK	IIC serial clock input when SENB=1; SPI serial clock input when SENB=0;
4	A4,A1		RSV	Reserved, left open
5	D4	A4	SDA	I2C serial data input/output pin when SENB=1; SPI data input pin when SENB=0;
6	B4	B4	MISO	SPI data output pin when SENB=0;
7		C3	TRG	Trig input for data read/Data ready signal output pin, active "H"

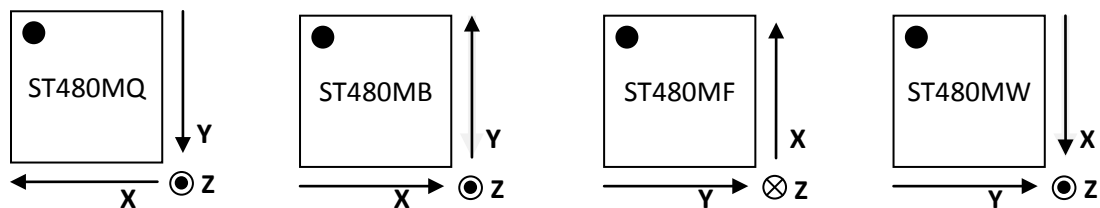
8	C4	C4	VLOGIC	Digital interface positive power supply pin
9, 10, 14,16	B3,C2	B3,C2 D4	NC	No Connected
11	D2	D2	A1	Second LSB of 7bits IIC address; Do not float
12	D1	D1	A0	LSB of 7bits IIC address; Do not float
13	C1	C1	VSS	GND
15	B1	B1	VDD	Power supply

PIN No. ST480MC	PIN Name	PIN Function
A1	VDD	Positive power supply pin.
A2	A0	LSB of 7bits IIC address; Do not float
A3	TST	Test pin Pulled down by 100kΩ internal resistor. Keep this pin electrically non-connected.
B1	VSS	Ground pin.
B3	SCL	Control data clock input pin Input: Schmidt trigger
C1	VDDIO	Digital interface positive power supply pin
C2	NC	No Connected
C3	SDA	I2C serial data input/output pin

## 6. Functional Explanation

### 6.1 Magnetic Sensor

The measurement data increases as the magnetic flux density increases in the arrow directions.



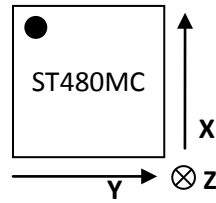


Figure 6.1: Sensor Direction of ST480M

## 6.2 The noise of sensor:

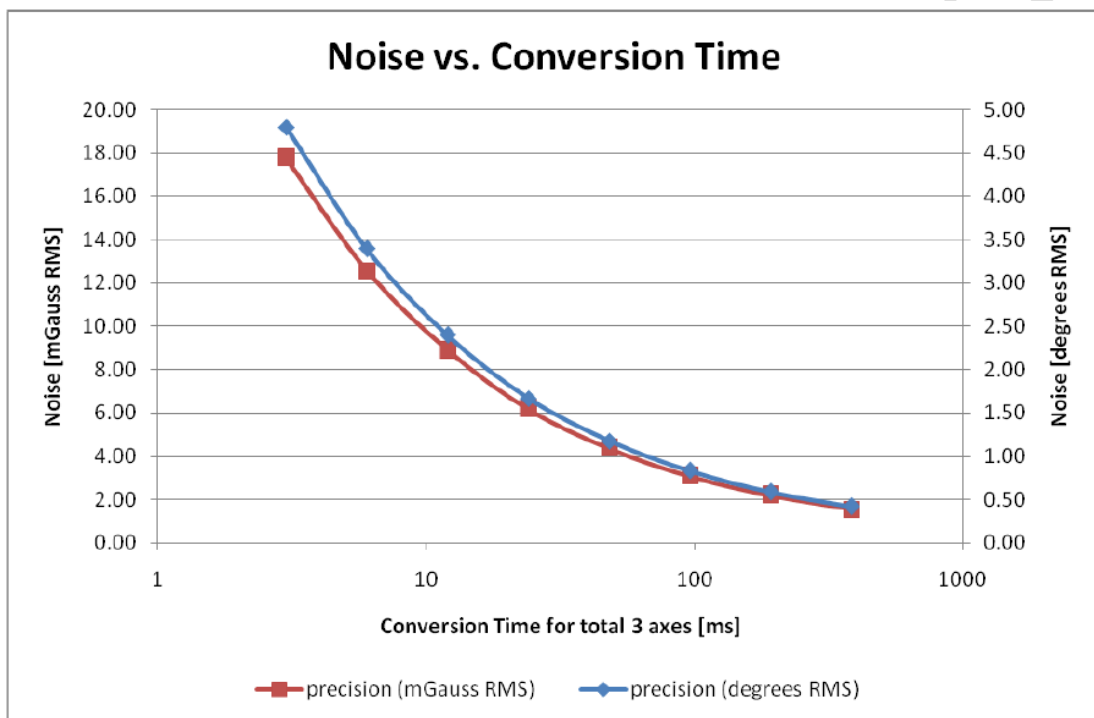
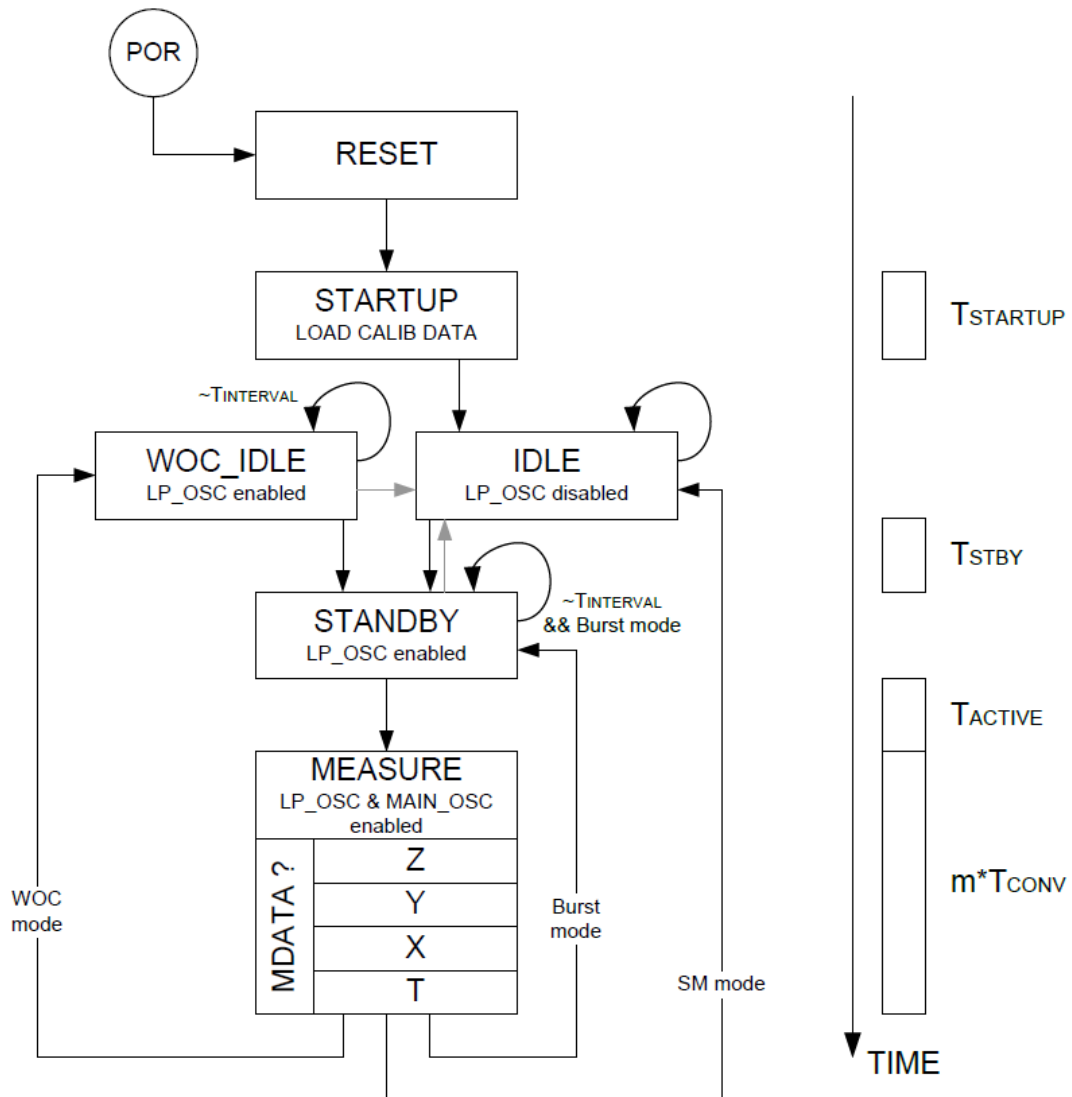


Figure 6.2: Relation between the noise and conversion time

## 6.3 Operation mode

The ST480M can operate in 3 modes: single measurement mode , burst mode , wakeup mode . The statement changed should follow the state diagram





**Figure 6.3: Top-Level State Diagram with indication of timings**

- **Single measurement mode**

The master will ask for data via the corresponding protocol (I<sup>2</sup>C or SPI), waking up the ASIC to make a single conversion, immediately followed by an automatic return to sleep mode (IDLE) until the next polling of the master. This polling can also be done by strobing the TRG pin, which has the same effect as sending a protocol command for a single measurement.

Whenever the sensor is set to this mode (or after startup) the ST480M goes to the IDLE state where it awaits a command from the master to perform a certain acquisition. The duration of the acquisition will be the concatenation of the  $T_{STBY}$ ,  $T_{ACTIVE}$  and  $m \cdot T_{CONV}$  (with  $m$  # of axes). The conversion time will effectively be programmable by the user, but is equally a function of the required axes/temperature to be measured. Upon reception of such a polling command from the master, the sensor will make the necessary acquisitions,

and set the INT/DRDY pin high to signal that the measurement has been performed and the master can read out the data on the bus at his convenience. The INT/DRDY will be cleared either when:

- The master has issued a command to read out at least one of the measured components
- The master issues an Exit (EX) command to cancel the measurement
- The chip is reset, after POR (Power-on reset) or Reset command (RT)

- Burst mode:

The ASIC will have a programmable data rate at which it will operate. This data rate implies auto-wakeup and sequencing of the ASIC, flagging that data is ready on a dedicated pin (INT). The maximum data rate will correspond to  $1/3 \cdot T_{CONV}$  in case of 3 axes magnetic data. The time during which the ASIC has a counter running, but is not doing an actual conversion is called the Standby mode (STBY).

When the sensor is operating in burst mode, it will make conversions at specific time intervals. The programmability of the user is the following:

- Burst speed (TINTERVAL)
- Conversion time (TCONV)
- Axes/Temperature (MDATA)

Whenever the ST480M has made the selected conversions (based on MDATA), the DRDY pin will be set active H to indicate that the data is ready. It will remain high until the master has sent the command to read out at least one of the converted quantities (ZYXT). Should the master have failed to read out any of them by the time the sensor has made a new conversion, the DRDY pin will be strobed low for 10 $\mu$ s, and the next rising edge will indicate a new set of data is ready.

- Wake-Up on Change:

This mode is similar to the burst mode in the sense that the device will be auto-sequencing, with the difference that the measured component(s) is/are compared with a reference and in case the difference is bigger than a user-defined threshold, the INT pin is set. The user can select which axes and/or temperature fall under this cyclic check, and which thresholds are allowed.

User can change the operating mode at all time through a specific command on the bus. The default start-up mode is Single Measurement mode (in IDLE state), but with a proper user command any mode can be set after power-up. Changing to Burst or WOC mode, coming from Single Measure mode is always accompanied by a measurement first. The top-level state diagram indicating the different modes and some relevant timing is shown below in Figure . In the Measure state, the MDATA flag will define which components will be measured (ZYXT). The sequential order cannot be modified by the user.

The Wake-Up on Change (WOC) functionality can be set by the master with as main purpose to only receive an interrupt when a certain threshold is crossed. The WOC mode will

always compare a new burst value with a reference value in order to assess if the difference between both exceeds a user-defined threshold. The reference value is defined as one of the following:

- The first measurement of WOC mode is stored as reference value once, as a result of a measurement. This measurement at “t=0” is then the basis for comparison.
- The reference for acquisition (t) is always acquisition (t-1), in such a way that the INT/DRDY will only be set if the derivative of any component exceeds a threshold.

The in-application programmability is the same as for burst mode, but now the thresholds for setting the interrupt are also programmable by the user, as well as the reference, if the latter is data(t=0) or data(t-1).

## 7. Serial Interface

### 7.1 Data Transfer protocol

The supported protocols are I2C and SPI. The SENB/CS pin (pin #2 in QFN package) is used to define the protocol to be used:

- /CS = 0 for SPI, addressing the ST480M slave in SPI mode (3- and 4-wire)
- /CS = 1 for I2C, addressing the ST480M slave when the correct address is transmitted over the bus

To make sure the activity on the SPI bus can't be accidentally interpreted as I2C protocol, programming bits are available in the EEPROM of the ST480M to select the protocol. It concerns the COMM\_MODE[1:0] bits with the following effect:

COMM_MODE[1]	COMM_MODE[0]	Description
0	X	The mode in which the first valid command is transmitted to the ST480M defines the operating mode (SPI or I2C) for all its future commands, until a reset (hard or soft) is done.
1	0	SPI mode only
1	1	I2C mode only

#### 7.1.1 I2C Protocol

##### Slave Address

The ST480M always work as a slave device. The I2C address is made up of some memory written value and hard-coded bits as follows: I2C\_ADDR[7:0] = {EE\_I2C\_ADDR[4:0],A<sub>1</sub>,A<sub>0</sub>,R/W} with A<sub>i</sub> the user-selectable active-high value of the input pads of the ST480M, referred to the V<sub>DD</sub> supply system and EE\_I2C\_ADDR[4:0] default programmed to 03h. When the R/W bit is set to “1”, READ instruction is executed. When the R/W bit is set to “0”, WRITE instruction is executed.

Table1: for ST480MW/ ST480MF/ ST480MB/ ST480MQ:

MSB						LSB	
0	0	0	1	1	A1	A0	R/W

Table2: for ST480MC (8pin WL-CSP):

MSB						LSB	
0	0	0	1	1	0	A0	R/W

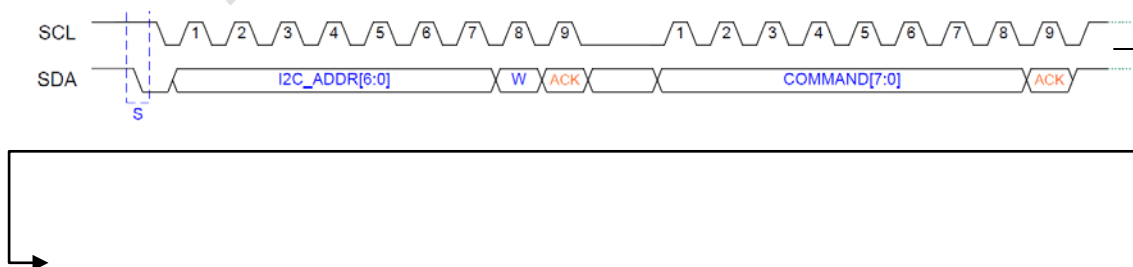
Note: for ST480MC (8pin WL-CSP), A1 please connect to Gnd, for other package type A1 is second LSB of 7bits IIC address.

**I2C Principle**

The ST480M supports I2C communication in both Standard Mode and Fast Mode. Bytes are transmitted MSB first, and in order to reconstruct words, the bytes need to be concatenated MSByte first. The general principle of communication is always the same:

1. Initiating the communication is always done by the Master (Start condition S)
2. Addressing the Slave (ST480M) followed by a cleared bit to indicate the Master intends to write something to the specific addressed Slave
3. Acknowledging by the Slave if the transmitted address corresponds to the Slave’s I2C address. If the latter isn’t the case, any further activity on the bus except a Sr (Start Repeat) and P (Stop) condition will be ignored by the ST480M
4. Sending a Command Byte by the Master, as depicted in Figure 5. The Slave will always acknowledge this, even if it is an unrecognized command.
5. Issuing a Start Repeat (Sr) condition by the Master in order to restart the addressing phase
6. Addressing the Slave (ST480M) followed by a set bit to indicate the Master intends to read something from the specific addressed Slave
7. Acknowledging by the Slave if the transmitted address corresponds to the Slave’s I2C address. If the latter isn’t the case, any further activity on the bus except a Sr (Start Repeat) and P (Stop) condition will be ignored by the ST480M
8. Transmitting the Status Byte by the Slave, who is in control of the bus
9. Acknowledging by the Master if the data is well received
10. Generating a Stop condition (P) by the master

The Master controlled bus activity is shown in blue, the Slave controlled bus activity is shown in orange. In case a command is longer than a single byte, the bytes are transmitted sequentially before generating the Start Repeat (Sr) condition.



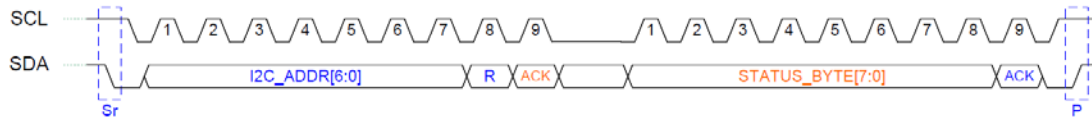


Figure 7.1 I2C slave protocol

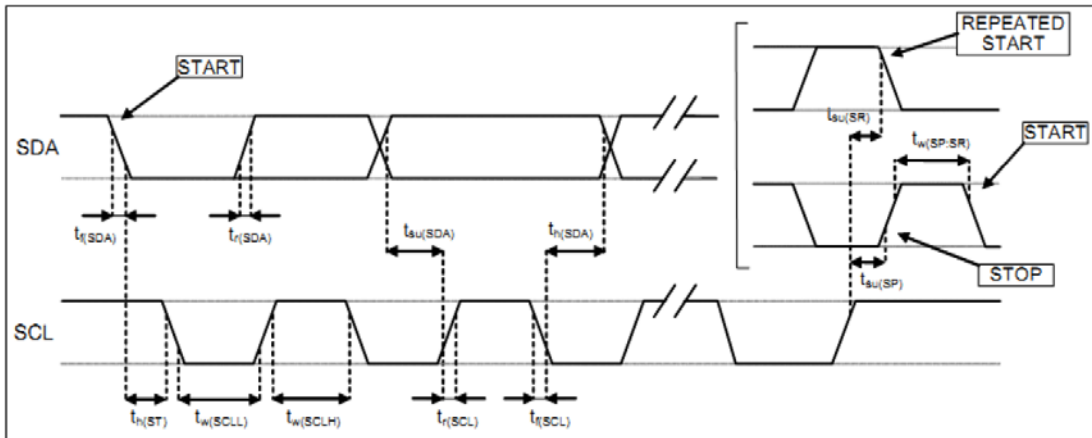


Figure 7.2 I2C slave timing diagram

Symbol	Parameter	I <sup>2</sup> C standard mode <sup>(1)</sup>		I <sup>2</sup> C fast mode <sup>(1)</sup>		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_h(SDA)$	SDA data hold time	0	3.45	0	0.9	$\mu$ s
$t_r(SDA) \ t_r(SCL)$	SDA and SCL rise time		1000	$20 + 0.1C_b^{(2)}$	300	ns
$t_f(SDA) \ t_f(SCL)$	SDA and SCL fall time		300	$20 + 0.1C_b^{(2)}$	300	
$t_h(ST)$	START condition hold time	4		0.6		$\mu$ s
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_w(SP:SR)$	Bus free time between STOP and START condition	4.7		1.3		

Figure 7.3 I2C slave timing value

### 7.1.2 SPI Protocol

The ST480M can handle SPI communication at a bitrate of 10Mhz. The SPI communication is implemented in a half-duplex way, showing high similarities with I2C communication, but addressing through the \CS (Chip Select) pin instead of through bus arbitration. The half-duplex nature is at the basis of the 3-wire SPI support. The implemented SPI mode is mode 3: CPHA=1

(data changed on leading edge and captured on trailing edge, and CPOL=1 (high level is inactive state). The Chip Select line is active-low.

Symbol	Parameter	Value <sup>(1)</sup>		Unit
		Min	Max	
$t_c(\text{SPC})$	SPI clock cycle	100		ns
$f_c(\text{SPC})$	SPI clock frequency		10	MHz
$t_{su}(\text{CS})$	CS setup time	5		ns
$t_h(\text{CS})$	CS hold time	10		
$t_{su}(\text{SI})$	SDI input setup time	5		
$t_h(\text{SI})$	SDI input hold time	15		
$t_v(\text{SO})$	SDO valid output time		50	
$t_h(\text{SO})$	SDO output hold time	5		
$t_{dis}(\text{SO})$	SDO output disable time		50	

Figure 7.4 SPI Timing Value

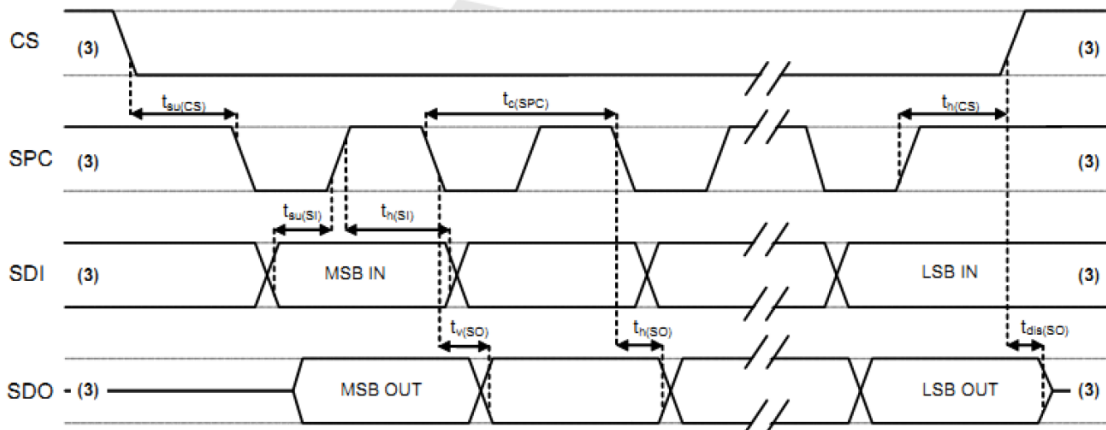
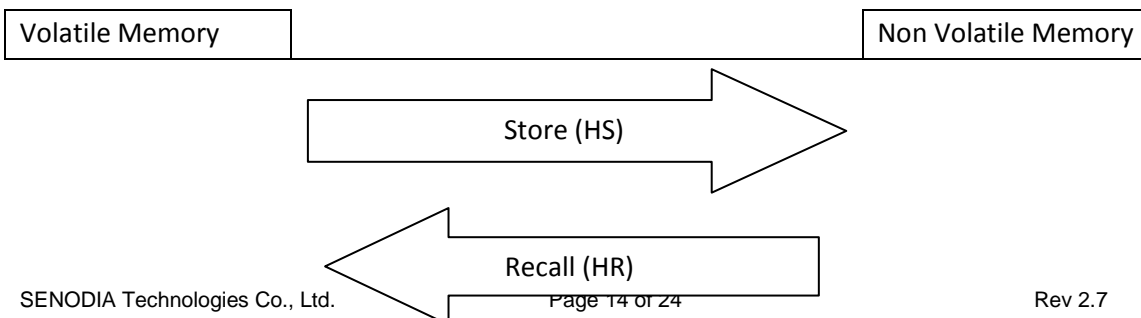
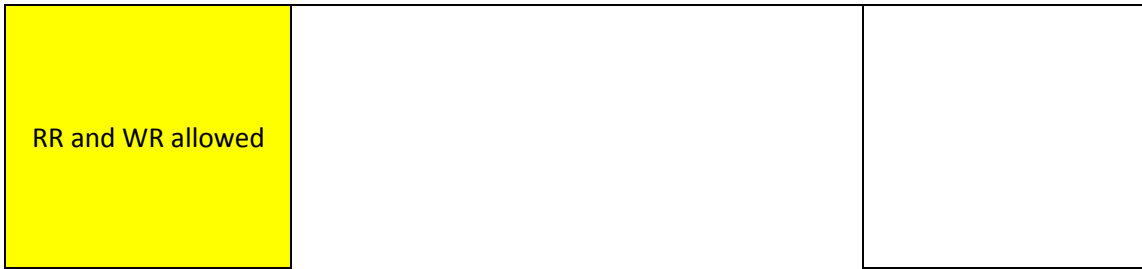


Figure 7.5 SPI Timing diagram

## 7.2 Register map

The ST480M has ten 16bit Registers of non-volatile memory, and the same amount of volatile memory, The RR and WR commands impact the volatile memory only(yellow Area), there no direct access possible to the non-volatile memory.





**Figure 7.6 Memory Relationship**

The Volatile memory map is given:

Address	Bit Number																
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x00	RESERVED_LOW								BIST	Zseries			Gain Sel		HALLCONF		
0x01	INT/TRIG		COMM_MODE		WOC_DIFF		EXT_TRIG		TCMP_EN		BURST_SEL (zyxt)				BURST_DATA_RATE		
0x02					OSR2				RES_XYZ				DIG_FILT		OSR		
0x03	SENS_TC_HT								SENS_TC_LT								
0x04	OFFSET_X																
0x05	OFFSET_Y																
0x06	OFFSET_Z																
0x07	WOXY_THRESHOLD																
0x08	WOZ_THRESHOLD																
0x09	WOT_THRESHOLD																

**Table 7.1 Register Map**

Note: Address[1:0] = 0x00

- RESERVED\_LOW : Reserved IO trimming bits
- BIST : Enabled the on-chip coil, applying a Z-field [Built-In Self Test]
- Z\_SERIES : Enable all plates for Z-measurement
- GAIN\_SEL[2:0] : Analog chain gain setting, factor 5 between min and max code
- HALLCONF[3:0] : Hall plate spinning rate adjustment
- TRIG\_INT\_SEL : Puts TRIG\_INT pin in TRIG mode when cleared, INT mode otherwise
- COMM\_MODE[1:0] : Allow only SPI [10b], only I2C [11b] or both [0xb] according to CS pin
- WOC\_DIFF : Sets the Wake-up On Change based on  $\Delta\{\text{sample}(t), \text{sample}(t-1)\}$
- EXT\_TRIG : Allows external trigger inputs when set, if TRIG\_INT\_SEL = 0
- TCMP\_EN : Enables on-chip sensitivity drift compensation
- BURST\_SEL[3:0] : Defines the MDATA in burst mode if SB command argument = 0
- BURST\_DATARATE[6:0] : Defines  $T_{\text{INTERVAL}}$  as BURST\_DATA\_RATE \* 20ms
- OSR2[1:0] : Temperature sensor ADC oversampling ratio
- RES\_XYZ[5:0] : Selects the desired 16-bit output value from the 19-bit ADC
- DIG\_FILT[1:0] : Digital filter applicable to ADC
- OSR[1:0] : Magnetic sensor ADC oversampling ratio
- SENS\_TC\_HT[7:0] : Sensitivity drift compensation factor for  $T < T_{\text{REF}}$

- SENS\_TC\_LT[7:0] : Sensitivity drift compensation factor for  $T > T_{REF}$
- OFFSET\_i[15:0] : Constant offset correction, independent for  $i = X, Y, Z$
- WO\_i\_THRESHOLD[15:0] : Wake-up On Change threshold, independent for  $i = X, Y, Z$  and T

### 7.3 Command List

The ST480M only listens to a specific set of commands. Apart from the Reset command, all commands generate a status byte that can be read out. The table below indicates the 12 different commands that are (conditionally) accepted by the ST480M.

CommandName	Symbol	CMD Byte	Output Bytes <sup>(2)</sup>		
Start Burst Mode	SB	0001 zyxt <sup>(1)</sup>	N/A		
Start Wake-up on Change Mode	SW	0010 zyxt <sup>(1)</sup>	N/A		
Start Single Measurement Mode	SM	0011 zyxt <sup>(1)</sup>	N/A		
Read Measurement	RM	0100 zyxt <sup>(1)</sup>	N/A		
Read Register	RR	0101 0000	Register Address	High Byte	Low Byte
Write Register	WR	0110 0000	High Byte	Low Byte	Register Address
Exit Mode	EM	1000 0000	N/A		
Memory Recall	HR	1101 0000	N/A		
Memory Store	HS	1110 0000	N/A		
Reset	RT	1111 0000	N/A		

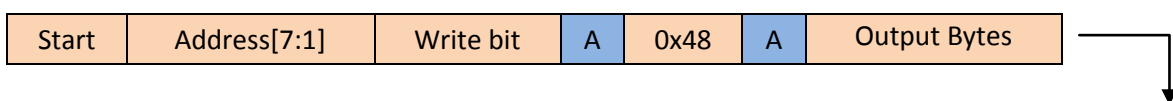
**Table 7.2 Command List**

Note: (1) The argument in all mode-starting commands (SB/SW/SM) is a nibble specifying the conversions to be performed by the sensor in the following order «zyxt». For example, if only Y axis and temperature are to be measured in Single Measurement mode the correct command to be transmitted is 0x35h.

(2) Output Bytes have to been sent before Start repeat

### 7.4 Command Usage:

All of the command usage should follow the sequence ,Each command has its owns input and output bytes , outputs byte can be found in the command list table , only RR and RM has input bytes.





R/S	Address[7:1]	Read bit	A	State Byte	A	Input Bytes	A	P
-----	--------------	----------	---	------------	---	-------------	---	---

**State Byte:**

The status byte is the first byte transmitted by the ST480M in response to a command issued by the master. It is composed of a fixed combination of informative bits:

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
BURST_MODE	WOC_MODE	SM_MODE	ERROR	SED	RS	D1	D0

**MODE bits**

these bits define in which mode the ST480M is currently set. Whenever a mode transition command is rejected, the first status byte after this command will have the expected mode bit cleared, which serves as an indication that the command has been rejected, next to the ERROR bit. The SM\_MODE flag can be the result of an SM command or from raising the TRG pin when TRG mode is enabled in the volatile memory of the ST480M.

**ERROR bit**

this bit is set in case a command has been rejected or in case an uncorrectable error is detected in the memory, a so called ECC\_ERROR. A single error in the memory can be corrected (see SED bit), two errors can be detected and will generate the ECC\_ERROR. In such a case all commands but the RT (Reset) command will be rejected.

**SED bit**

the single error detection bit simply flags that a bit error in the non-volatile memory has been corrected. It is purely informative and has no impact on the operation of the ST480M.

**RS bit**

whenever the ST480M gets out of a reset situation – both hard and soft reset – the RS flag is set to highlight this situation to the master in the first status byte that is read out. As soon as the first status byte is read, the flag is cleared until the next reset occurs.

**D[1:0] bits**

These bits only have a meaning after the RM commands, when data is expected as a response from the ST480M. The number of response bytes correspond to  $2 * D[1:0] + 2$ , so the expected byte counts are either 2, 4, 6 or 8.

**RateByte:**

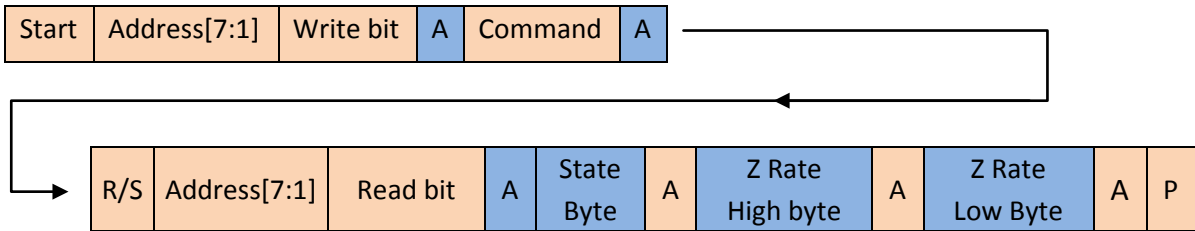
All of the rate byte data is supplied as complement, the bit7 of High Byte is considered to be a sign mark bit

**Example of Command usage:**

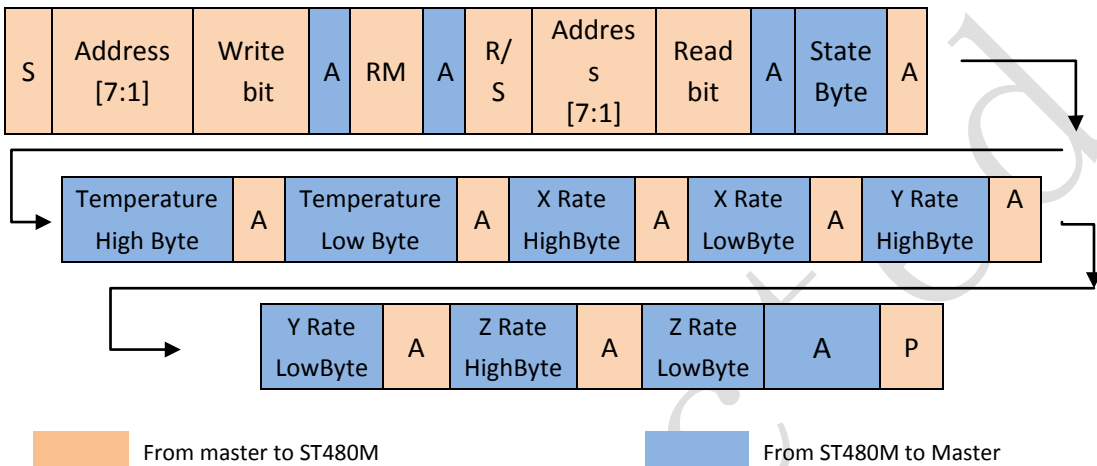
- **Read measurement RM**

The command Read Measurement can get the Sensor Rate while the ST480M set out a int signal, generally speaking, the amounts of input bytes depends on the argument of <zyxt> in mode command , each bit represent two bytes of rate data , the RATA data order is fixed as Temperature Rate, RateX, RateY,RateZ . If we wants RateZ only , the sequence of I2C should

follow the rule:

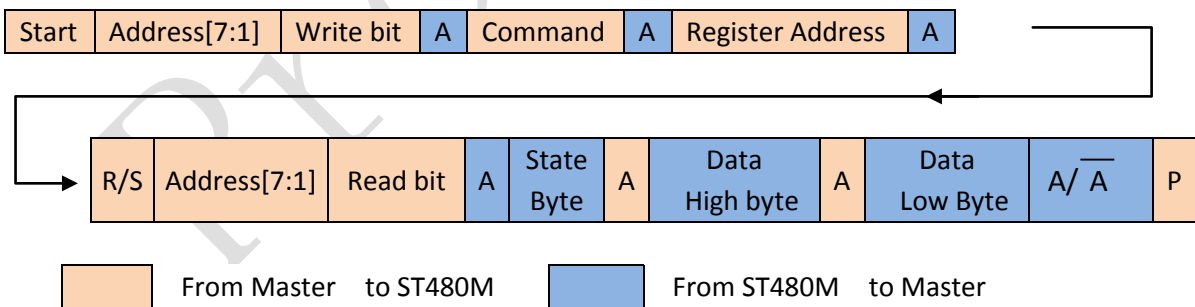


If we want to acquire all of the data, the sequence of I2C should be organized as below:



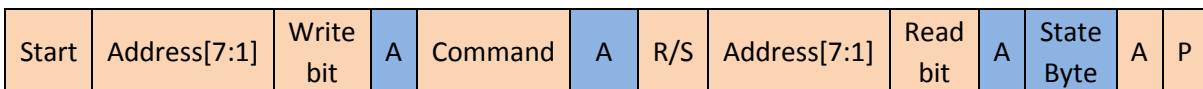
● Read Register(RR)

The Volatile memory data can be read out by the Command of Read Register(RR). The command byte should be followed while the I2C writing address has been sent out. Before a restart of IIC protocol, the register address needed, then the register data will be received following a read IIC address.



● Other commands

The usage of left commands is quite easy for they do not have input or output bytes, just follow the sequence bellow completely.



## 8. Typical Application

### 8.1 Typical Application Circuit

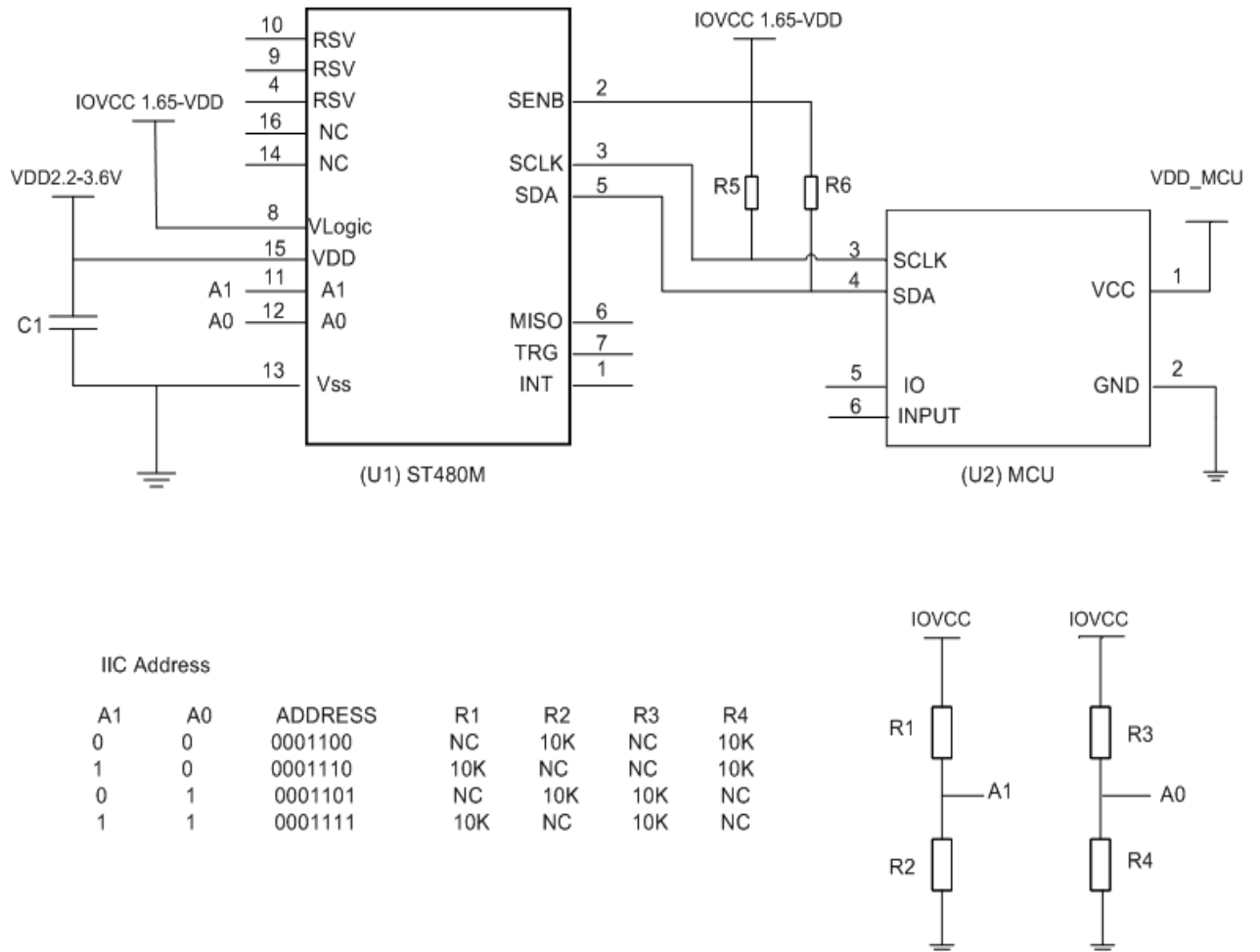


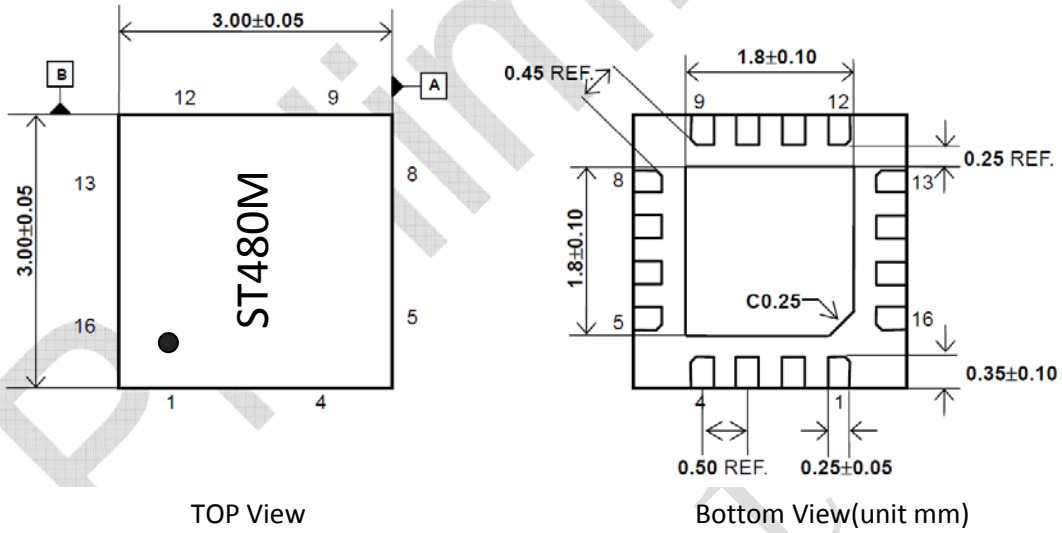
Figure 8.1: Reference Application Circuitry using I2C interface

### 8.2 Bill of Materials for External Components

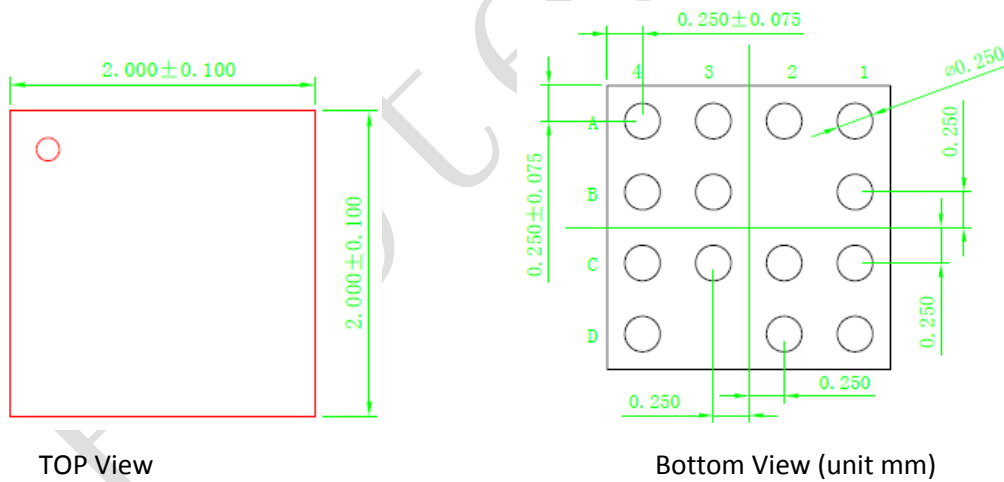
Item	Quantity	Reference	Part	Footprint
1	1	C1	0.1uF	SC0603
2	2	R5,R6	2.2Kohm	SR0603
3	4	R1,R2,R3,R4	10Kohm or NC	SR0603
4	1	U1	ST480MC	WLCSF-8

## 9. Outline Dimensions

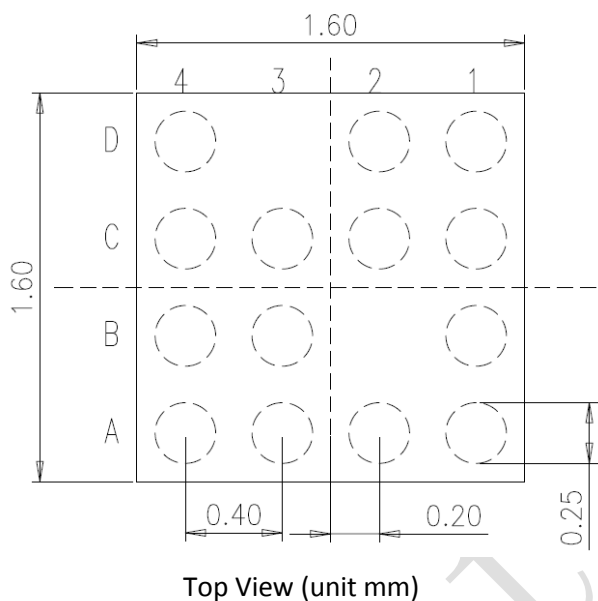
### 9.1 ST480MQ QFN3X3 Package



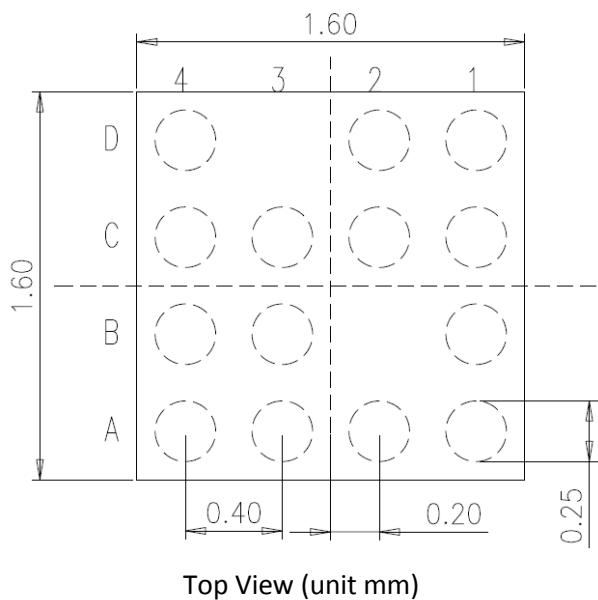
### 9.2 ST480MB BGA2X2 Package



**9.3 ST480MF Flip-LGA1.6X1.6 Package**



**9.4 ST480MW BGA1.6X1.6 Package**



**9.5 ST480MC WL-CSP 1.28X1.28 Package**

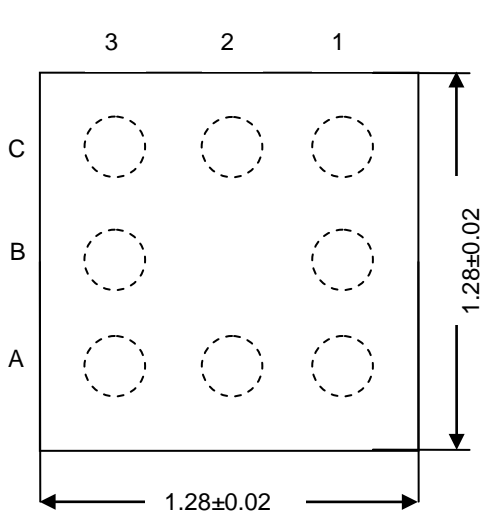


Figure 9.1: Top View (unit mm)

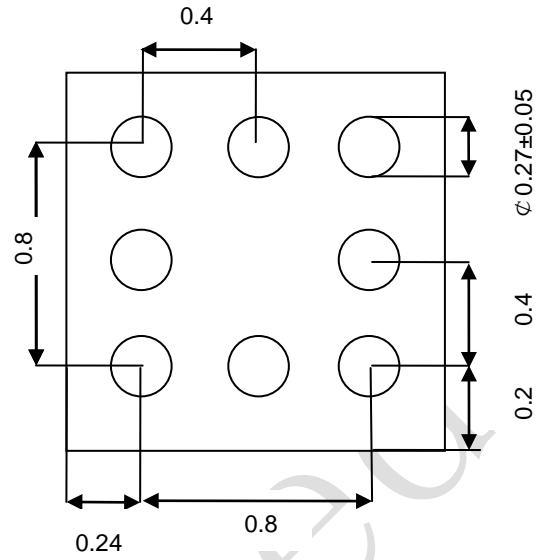


Figure 9.2: Bottom View (unit mm)

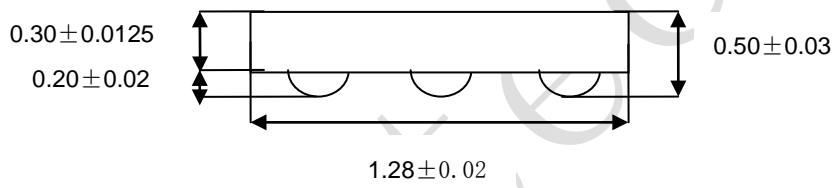


Figure 9.3: Side View (unit mm)

### 9.6 ST480MC Recommended Foot Print Pattern

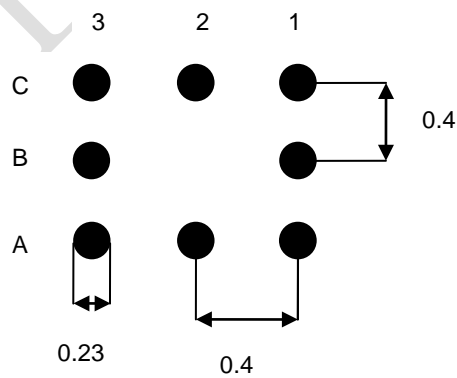
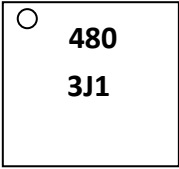


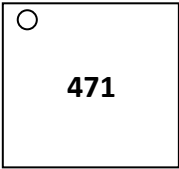
Figure 9.4: Recommended Foot Print Pattern

## 9.7 Package laser Mark

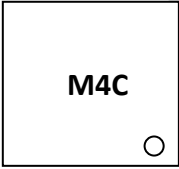
### 9.7.1 ST480MB/ ST480MF marking

Mark	Name	Symbol	Remark
	Pin 1 identifier	○	
	Product Name	<b>480</b>	3 numeric digits, fixed to identify product name
	Trace Code	<b>3J1</b>	3 alphanumeric digits, variable to generate mass production trace code: YWL (year, week, lot number)

### 9.7.2 ST480MW marking

Mark	Name	Symbol	Remark
	Pin 1 identifier	○	
	Trace Code	<b>471</b>	3 alphanumeric digits, variable to generate mass production trace code: YWL (year, week, lot number)

### 9.7.3 ST480MC marking

Mark	Name	Symbol	Remark
	Pin 1 identifier	○	
	Product Name	<b>M</b>	Alphabetic M: fixed to identify product name
	Trace Code	<b>4C</b>	2 alphanumeric digits, variable to generate mass production trace code: YW (year, week)

## 10. Reliability

ST480MC reliability test plan follows JEDEC 47I standards, Stress-Test-Driven Qualification of Integrated Circuits”.

## 11. Environment Compliant

ST480MC is compliant with RoHS2.0 standards and meet HF requirements.

## 12. Revision History

Date	Revision	Changes
2012-12-20	1.0	Preliminary Version Release.
2013-3-8	1.1	Modify part 6.1
2013-9-3	2.0	Modify Order Information, part 5,part 6.1 and part9
2014-6-24	2.1	Add ST480MC
2014-8-1	2.2	Update 7.1.1 I2C Protocol slave address
2014-8-4	2.3	Update 6.1 figure 4: ST480MC
2014-9-30	2.4	Update part 9.6
2014-11-6	2.5	Update part 9.6.3
2014-12-29	2.6	Update part 2,3,8 &9.5
2015-5-12	2.7	Update part 9.5 &9.6

## 13. Disclaimer

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