Preliminary

EXAR ...the analog plus company™

ST49C107A-04

Preprogrammed CPU Mother Board Frequency Generator

June 1997-3

FEATURES

- Provides Reference Clock And Synthesized Clock
- 5 to 32 MHz Input Reference Frequency
- Pin-to-Pin Compatible to Avasem AV9107
- Programmable Analog Phase Locked Loop
- Low Power Single 5V CMOS Technology
- Up to 16 Frequencies Stored Internally
- 8/14 pin DIP or SOIC Package

GENERAL DESCRIPTION

The ST49C107A-04 is a mask programmable monolithic analog CMOS device designed to generate two simultaneous clocks. The output frequency can vary from 2 to 130MHz, with up to 16 single selectable preprogrammed frequencies stored in internal ROM.

The ST49C107A-04 is designed to replace existing CPU mother board clocks generated from individual oscillators in order to reduce board space and number of oscillators. To provide high speed and low jitter clock, the parts utilize a high speed analog CMOS phase locked loop using 14.318 MHz system clock as the reference clock (note that reference clock can be changed to generate optional frequencies from a standard programmed device). The programmed clock outputs are selectable via four address lines.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
ST49C107ACF14-04	14 Lead 150 Mil JEDEC SOIC	0°C to 70°C

BLOCK DIAGRAM

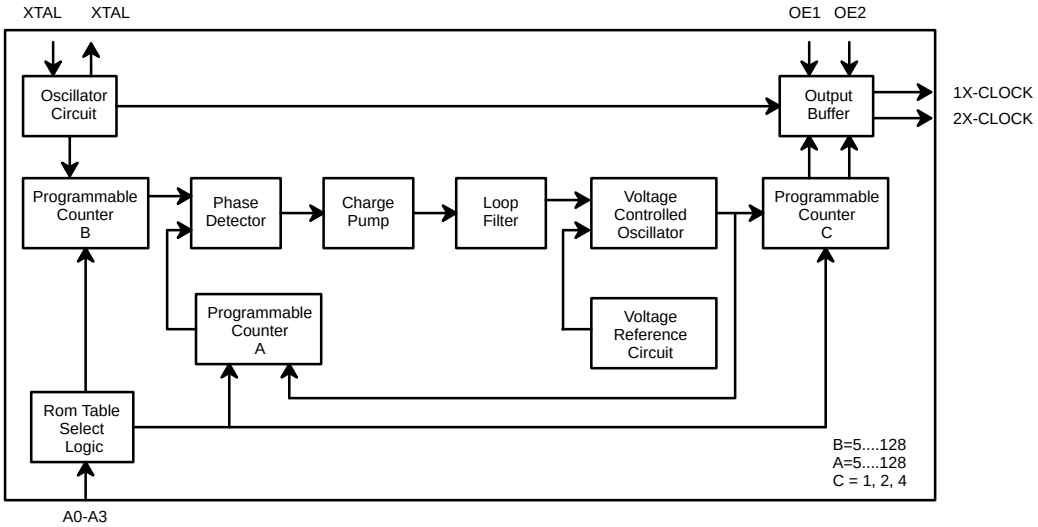

Figure 1. Block Diagram

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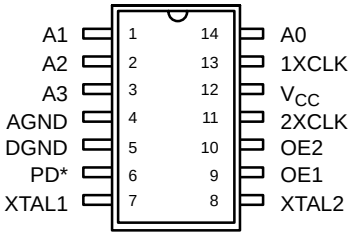
PIN CONFIGURATION



14 Lead SOIC (Jedec, 0.150")

PIN DESCRIPTION

Symbol	Pin #	Type	Description
A1	1	I	**Frequency Select Address Input 2[1].**
A2	2	I	**Frequency Select Address Input 3[1].**
A3	3	I	**Frequency Select Address Input 4[1].**
AGND	4	O	**Analog Ground.**
DGND	5	O	**Digital Ground.**
PD	6	I	**Power-down (Active Low).** Shuts off chip when low[1].
XTAL1	7	I	**Crystal Or External Clock Input.** A crystal can be connected to this pin and XTAL2 pin to generate internal phase locked loop reference clock. For external 14.318 MHz clock, XTAL2 is left open or used as buffered clock output.
XTAL2	8	O	**Crystal Output.**
OE1	9	I	**1X-CLOCK Output Enable (Active High).** 1X-CLOCK output is three stated when this pin is low[1].
OE2	10	I	**2X-CLOCK Output Enable (Active High).** 2X-CLOCK output is three stated when this pin is low[1].
2XCLK	11	O	**Programmed Output Clock.**
V_{CC}	12	I	**Positive Supply Voltage.** Single +5 volts.
1XCLK	13	O	**2X-CLOCK Divide-by-two Output.**
A0	14	I	**Frequency Select Address Input 1[1].**

Notes
[1]Have internal pull-up resistors on inputs.

DC ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10% Unless Otherwise Specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{IL}	Input Low Level			0.8	V	
V_{IH}	Input High Level	2.0			V	
V_{OL}	Output Low Level			0.4	V	I_{OL} = 8.0mA
V_{OH}	Output High Level	2.4			V	I_{OH} = 8.0mA
I_{IL}	Input Low Current			-10	µA	Except Crystal Input
I_{IH}	Input High Current			1	µA	V_{IN}=V_{CC}
I_{CC}	Operating Current		45	55	mA	No Load. CLOCK=100MHz
I_{SB}	Standby Current		25		µA	No Load
R_{IN}	Input Pull-up Resistance	500	900	1300	kΩ	

DC ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10% Unless Otherwise Specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
T_1	1X, 2X-CLOCK Rise Time		1	2	ns	CL=20pF 0.8V - 2.0V
T_2	1X, 2X-CLOCK Fall Time		1	2	ns	CL=20pF 2.0V - 0.8V
T_4	Duty Cycle	40	50	60	%	1.4V Switch Point
T_5	Duty Cycle	45	50	55	%	V_{CC}/2 Switch Point
T_3	Jitter 1 Sigma		±0.5	±2	%	
T_3	Jitter Absolute		±3	±5	%	
T	Input Frequency	2		32	MHz	
T_7	Buffered Clock Rise Time			20	ns	
T_8	Buffered Clock Fall Time			20	ns	

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Supply Range . . . . . 7 Volts
Voltage at Any Pin . . . . . GND-0.3V to V_{CC} +0.3V

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . -40°C to +150°C
Package Dissipation . . . . . 500 mW

EXTERNAL CLOCK CONNECTION

To minimize the noise pickup, it is recommended to connect 0.047 (F capacitor to XTAL1, and keep the lead length of the capacitor to XTAL1 to a minimum to reduce noise susceptibility.

FREQUENCY SELECT CALCULATION

The ST49C107A-04 contains an analog phase locked loop circuit with digital closed loop dividers and a final output multiplexer to achieve the desired dividing ratios for the clock output.

The accuracy of the frequencies produced by the ST49C107A-04 depends on the input frequency and divider ratios. The formula for calculating the exact output frequency is as follows:

CLKOUT = CLKIN * Factor

For proper output frequency, the ST49C107A-04 can accept a reference frequency from 5 - 32MHz with max output frequency of 130MHz (2X – clock).

CLOCK OUTPUT TABLE FOR ST49C107A-04 (using 14.318 MHz input. All frequencies in MHz).

A3	A2	A1	A0	Factor	2X-CLOCK	CLOCK
0	0	0	0	95/17	80.02	40.01
0	0	0	1	107/23	66.62	33.31
0	0	1	0	35/10	50.11	25.06
0	0	1	1	95/34	40.01	20.00
0	1	0	0	56/8	100.23	50.11
0	1	0	1	107/46	33.31	16.66
0	1	1	0	38/17	32.01	16.00
0	1	1	1	35/20	25.06	12.47
1	0	0	0	76/17	64.02	32.01
1	0	0	1	2	2X-Input	1X-Input
1	0	1	0	3	3X-Input	1.5X-Input
1	0	1	1	8	8X-Input	4X-Input
1	1	0	0	1/2	0.5X-Input	0.25X-Input
1	1	0	1	1/4	0.25X-Input	0.125X-Input
1	1	1	0	109/13	120.00	60.00
1	1	1	1	118/13	129.96	64.98

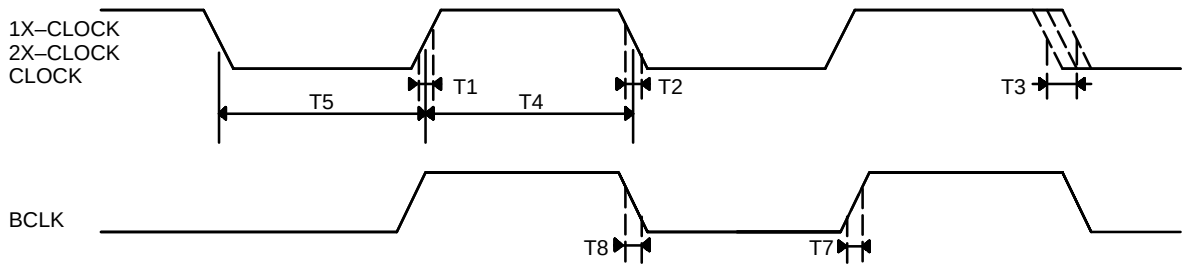
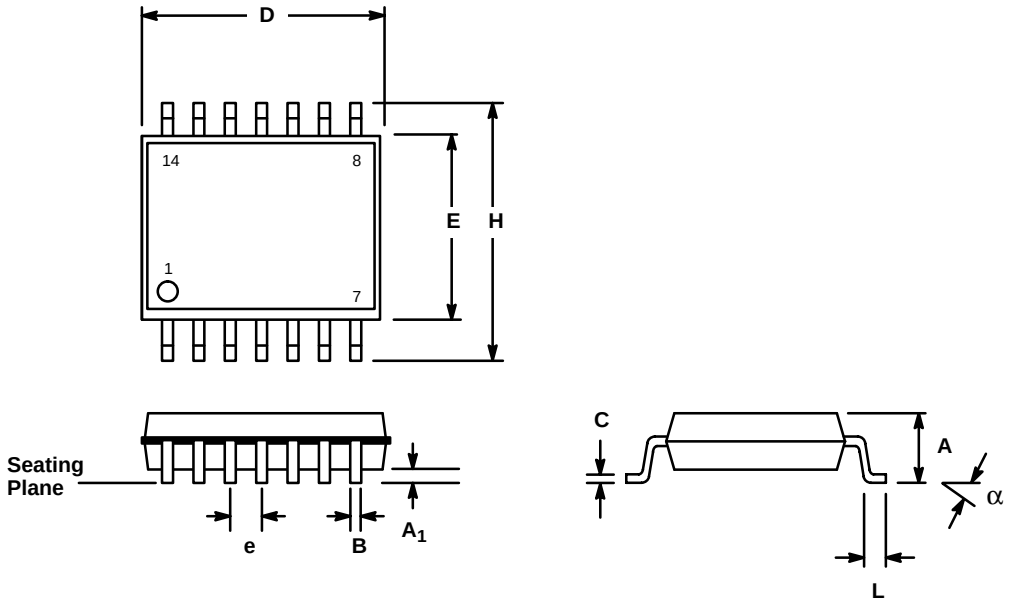


Figure 2. Timing Diagram

14 LEAD SMALL OUTLINE
(150 MIL JEDEC SOIC)

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A_1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.19	0.25
D	0.337	0.344	8.55	8.75
E	0.150	0.157	3.80	4.00
e	0.050 BSC		1.27 BSC	
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

Note: The control dimension is the millimeter column

Notes

Notes

NOTICE

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