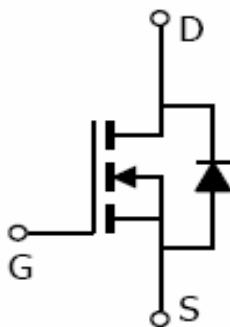
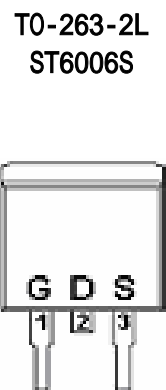
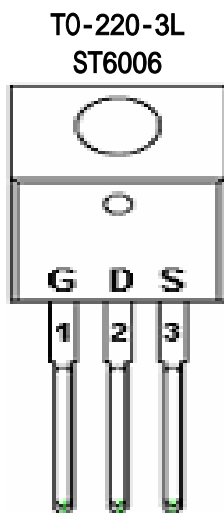


DESCRIPTION

The ST6006 is the N-Channel logic enhancement mode power field effect transistor are produced using high cell density, DMOS trench technology.

This ST6006 is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

PIN CONFIGURATION**APPLICATIONS**

- Power Supplies
- Converters
- Power Motor controls
- Bridge Circuit

FEATURE

- 20V/2.8A, $R_{DS(ON)} = 85\text{m-ohm}$
@ $V_{GS} = 4.5\text{V}$
- 20V/2.4A, $R_{DS(ON)} = 115\text{m-ohm}$
@ $V_{GS} = 2.5\text{V}$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23-3L package design

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ORDERING INFORMATION

Part Number	Package	Part Marking
ST6006T220TG	TO-220-3L	ST6006D
ST6006T220RG	TO-263-2L	ST6006

ABSOLUTE MAXIMUM RATINGS (Ta = 25 Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	VDSS	60	V
Gate-Source Voltage	VGSS	+/-20	V
Continuous Drain Current (TJ=150)	ID	60	A
		TA=25	
	TA=70		
Pulsed Drain Current	IDM	120	A
Continuous Source Current (Diode Conduction)	IS	60	A
Power Dissipation	PD	120	W
		TA=25	
	TA=70		
Operation Junction Temperature	TJ	150	
Storage Temperature Range	TSTG	-55/150	
Thermal Resistance-Junction to Ambient	R JA	40 62.5	/W

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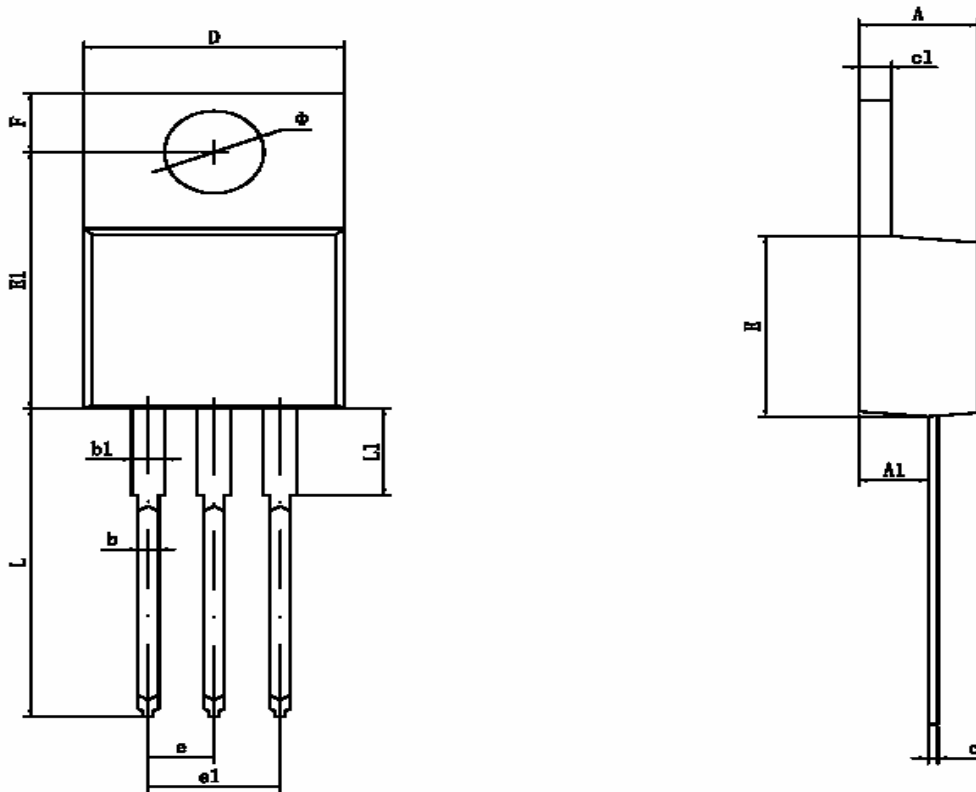
60V/60A

ELECTRICAL CHARACTERISTICS ($T_a = 25$ Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=10\mu A$	60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=50\mu A$	1.0		3.0	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=20V$			100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=60V, V_{GS}=0V$			1	uA
		$V_{DS}=20V, V_{GS}=0V$ $T_J=125$			50	
		$V_{DS}=60V, V_{GS}=0V$ $T_J=175$				
On-State Drain Current	$I_{D(on)}$	$V_{DS}=5V, V_{GS}=10V$	60			A
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=30A$		12	16	m
		$V_{GS}=10V, I_D=30A$ $T_J=125$		24	30	
		$V_{GS}=10V, I_D=30A$ $T_J=175$		31	37	
		$V_{GS}=5V, I_D=30A$		14	19	
Forward Transconductance	g_{fs}	$V_{DS}=15V, I_D=30A$		49		S
Diode Forward Voltage	V_{SD}	$I_F=60A, V_{GS}=0V$			1.6	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=30V, V_{GS}=10V$ $I_D = 60A$		39	60	nC
Gate-Source Charge	Q_{gs}			12		
Gate-Drain Charge	Q_{gd}			10		
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V$ $F=1MHz$		2000		pF
Output Capacitance	C_{oss}			400		
Reverse Transfer Capacitance	C_{rss}			115		
Turn-On Time	$t_{d(on)}$	$V_{DD}=10V, R_L=5.5$ $I_D=3.6A, V_{GEN}=4.5V$ $R_G=6$		12	25	nS
	t_r			36	60	
Turn-Off Time	$t_{d(off)}$			34	60	
	t_f			10	25	

60V/60A

TO-220-3L PACKAGE OUTLINE
ST6006



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.470	4.670	0.176	0.184
A1	2.520	2.820	0.099	0.111
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.310	0.530	0.012	0.021
c1	1.170	1.370	0.046	0.054
D	10.010	10.310	0.394	0.406
E	8.500	8.900	0.335	0.350
E1	12.060	12.460	0.475	0.491
e	2.540TYP		0.100TYP	
e1	4.980	5.180	0.196	0.204
F	2.590	2.890	0.102	0.114
L	13.400	13.800	0.528	0.543
L1	3.560	3.960	0.140	0.156
Φ	3.790	3.890	0.149	0.153



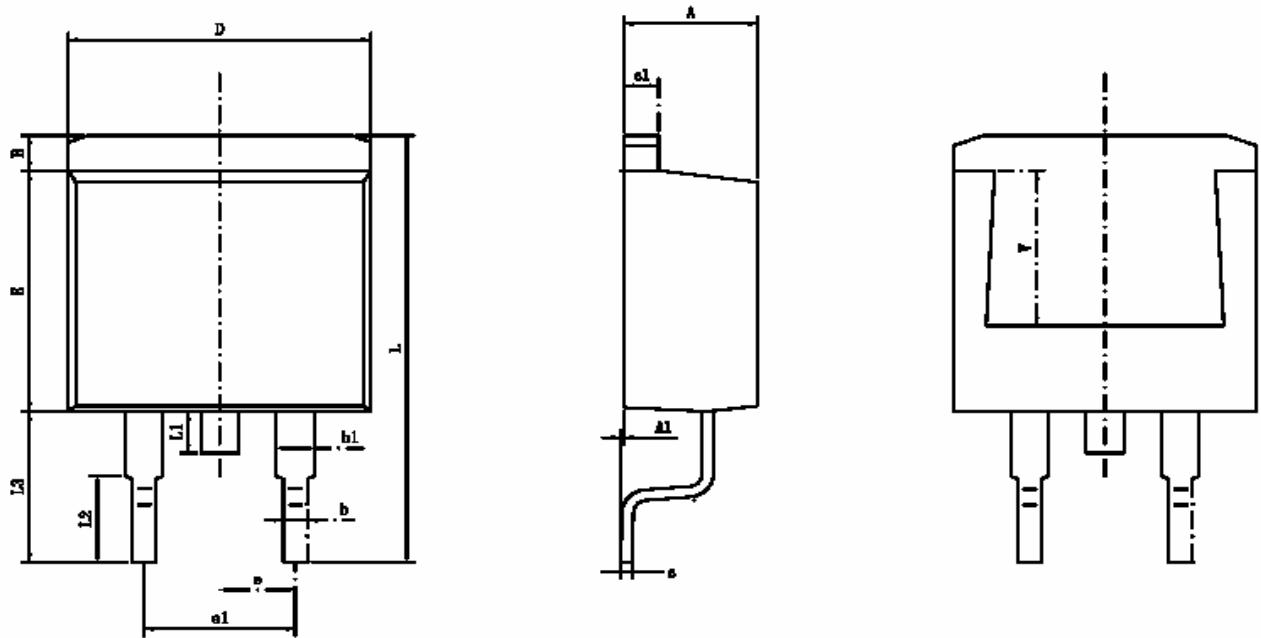
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60V/60

TO-263-2L PACKAGE OUTLINE
ST6006S



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.470	4.670	0.176	0.184
A1	0.000	0.150	0.000	0.006
B	1.170	1.370	0.046	0.054
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.310	0.530	0.012	0.021
c1	1.170	1.370	0.046	0.054
D	10.010	10.310	0.394	0.406
E	8.500	8.900	0.335	0.350
e	2.540TYP		0.100TYP	
e1	4.980	5.180	0.196	0.204
L	15.050	15.450	0.593	0.608
L1	1.300	1.700	0.051	0.067
L2	2.340	2.740	0.092	0.108
L3	5.080	5.480	0.200	0.216
V	5.600REF		0.220REF	



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TYPICAL CHARACTERISTICS

Figure 1. Maximum Effective Thermal Impedance, Junction-to-Case

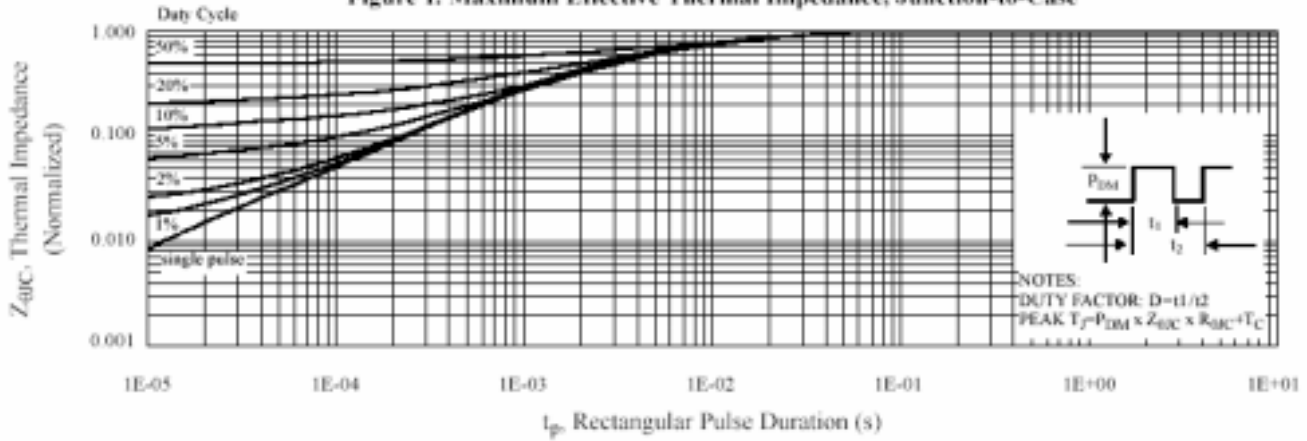


Figure 2. Maximum Power Dissipation vs Case Temperature

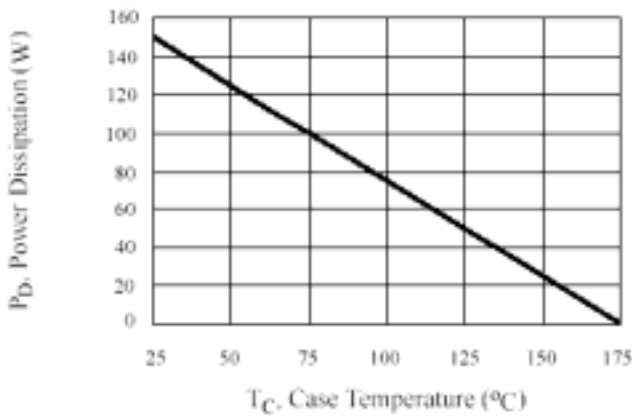


Figure 3. Maximum Continuous Drain Current vs Case Temperature

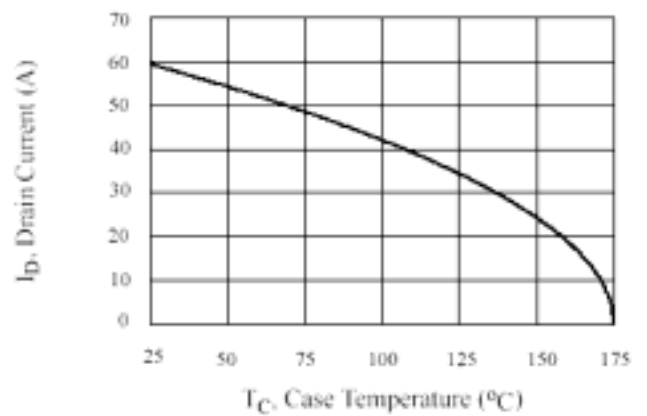


Figure 4. Typical Output Characteristics

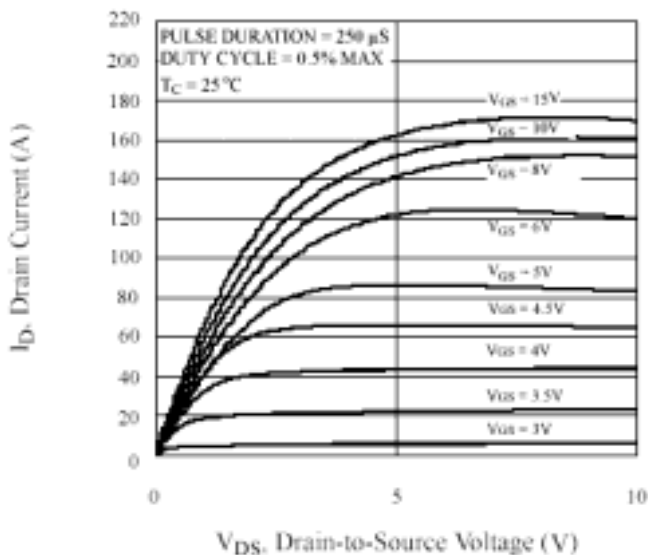
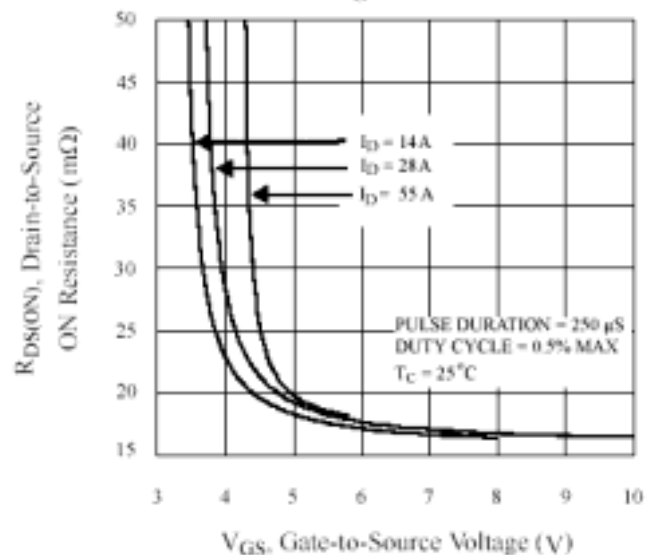


Figure 5. Typical Drain-to-Source ON Resistance vs Gate Voltage and Drain Current



TYPICAL CHARACTERISTICS

Figure 6. Maximum Peak Current Capability

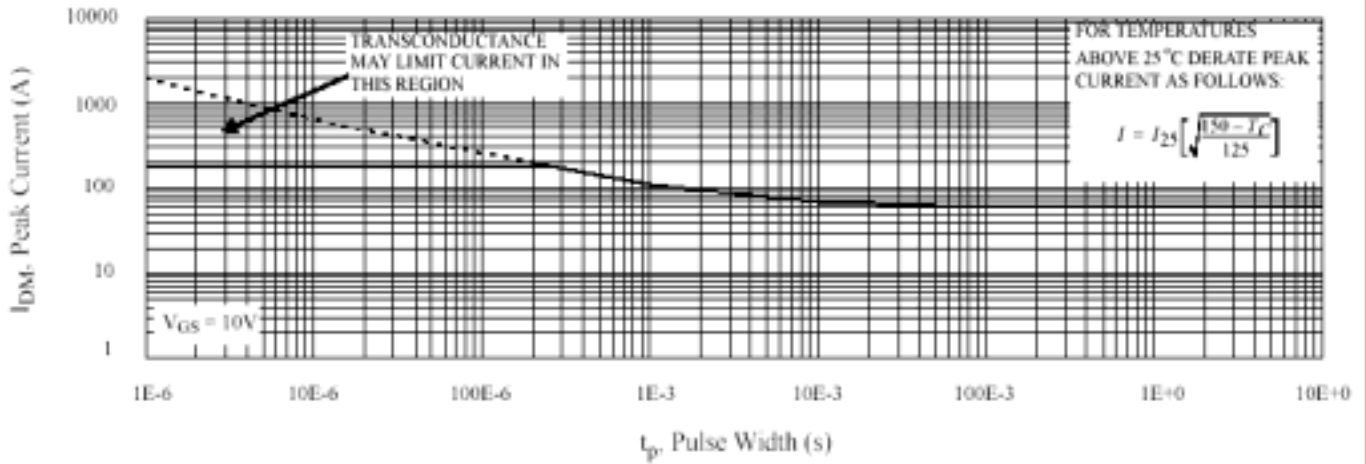


Figure 7. Typical Transfer Characteristics

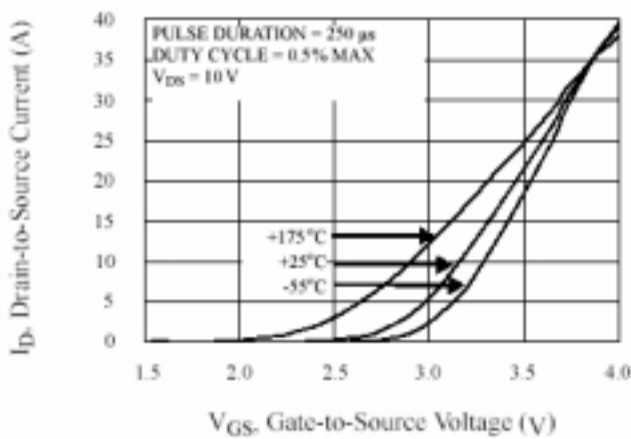


Figure 8. Unclamped Inductive Switching Capability

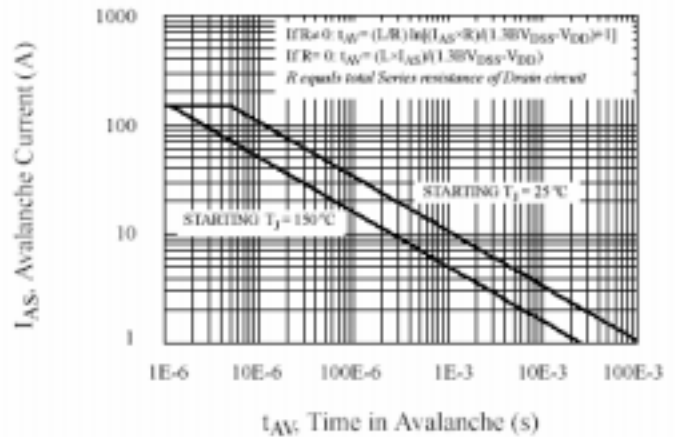


Figure 9. Typical Drain-to-Source ON Resistance vs Drain Current

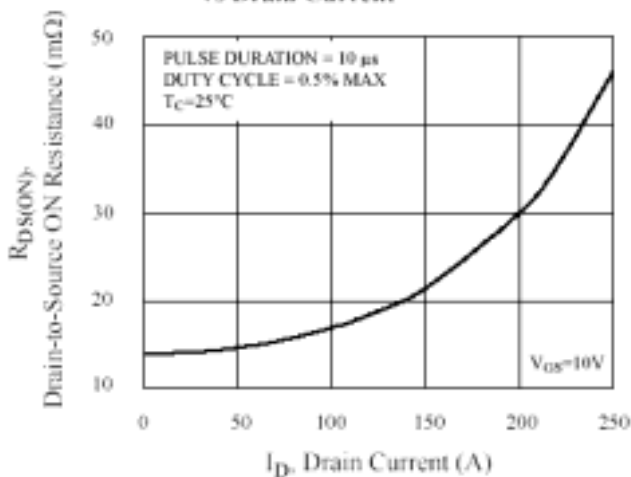
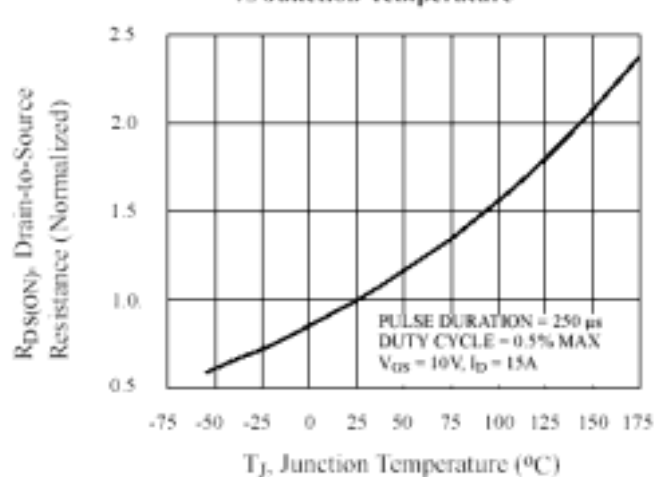


Figure 10. Typical Drain-to-Source ON Resistance vs Junction Temperature



60V60A

TYPICAL CHARACTERISTICS

Figure 11. Typical Breakdown Voltage vs Junction Temperature

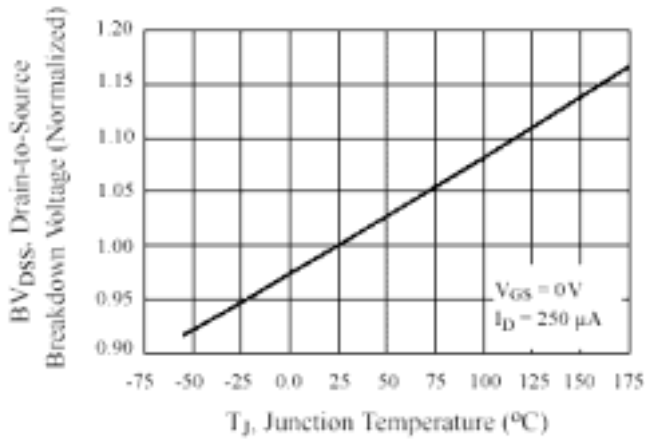


Figure 12. Typical Threshold Voltage vs Junction Temperature

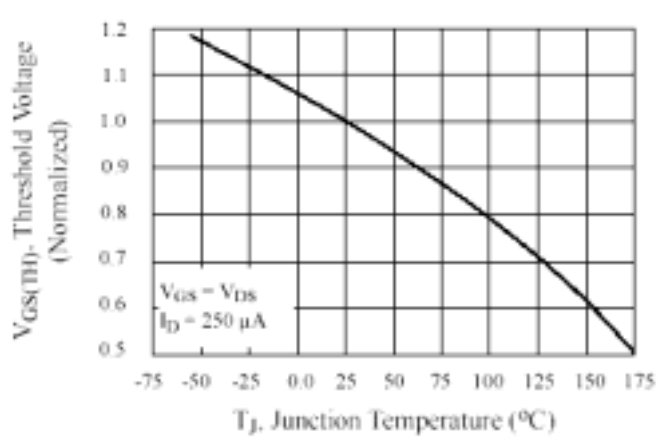


Figure 13. Maximum Forward Bias Safe Operating Area

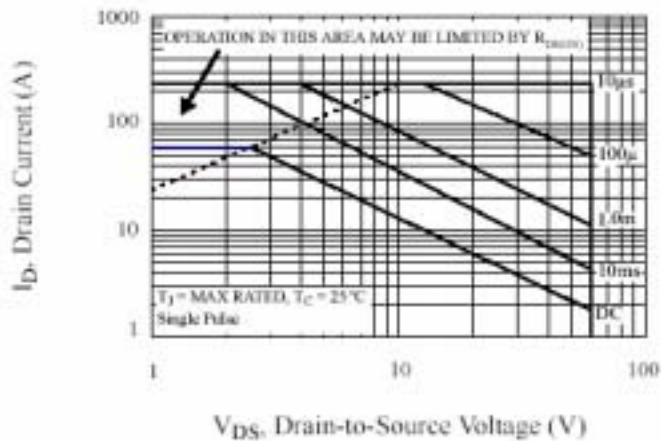


Figure 14. Typical Capacitance vs Drain-to-Source Voltage

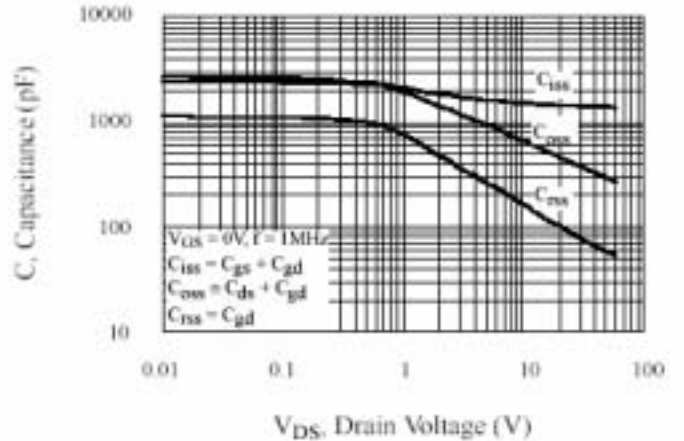


Figure 15. Typical Gate Charge vs Gate-to-Source Voltage

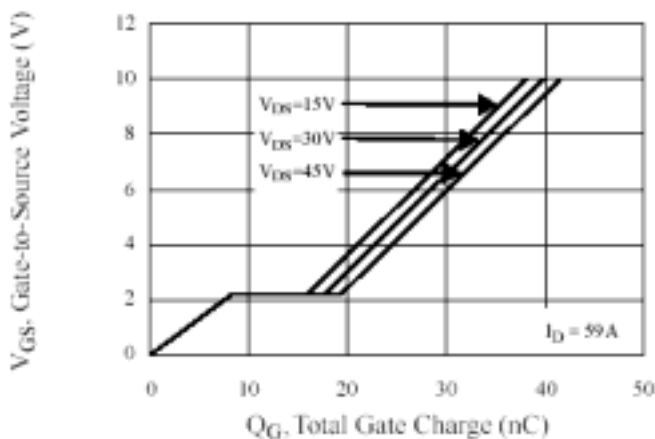


Figure 16. Typical Body Diode Transfer Characteristics

