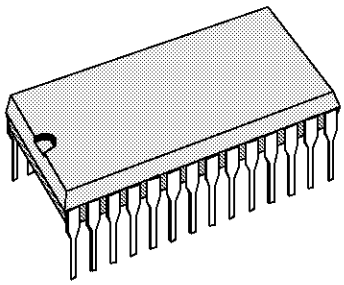
SGS-THOMSON MICROELECTRONICS

ST6294

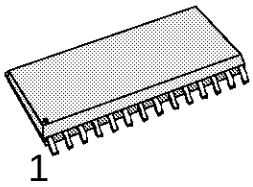
8-BIT HCMOS MCU WITH A/D CONVERTER, EEPROM & AUTO-RELOAD TIMER

PRELIMINARY DATA

- 3 to 6.0V Supply Operating Range
- 8 MHz Maximum Clock Frequency
- -25 to +85°C Operating Temperature Range
- Run, Wait & Stop Modes
- 5 different interrupt vectors
- Look-up table capability in ROM
- User ROM: 3868 bytes
- Data ROM: User selectable size (in program ROM)
- Data RAM: 128 bytes
- EEPROM: 128 bytes
- PDIP28, PSO28 packages
- 21 fully software programmable I/O as:
  - Input with pull-up resistor
  - Input without pull-up resistor
  - Input with interrupt generation
  - Open-drain or push-pull outputs
  - Analog Inputs
- 8 I/O lines can sink up to 20mA for direct LED or TRIAC driving
- 8 bit counter with a 7-bit programmable prescaler (Timer1)
- 8 bit auto-reload timer with 7-bit programmable prescaler (AR Timer)
- Digital Watchdog
- 8 bit A/D Converter with up to 13 analog inputs
- 8 bit Synchronous Peripheral Interface (SPI)
- On-chip clock oscillator (Quartz Crystal or Ceramic)
- Power-on Reset
- Clock output
- 9 powerful addressing modes
- The development tool of the ST6294 microcontrollers consists of the ST626x-EMU emulation and development system connected via a standard RS232 serial line to an MS-DOS Personal Computer



PDIP28



PSO28

(Ordering Information at the end of the datasheet)

Figure 1. ST6294 Pin Configuration

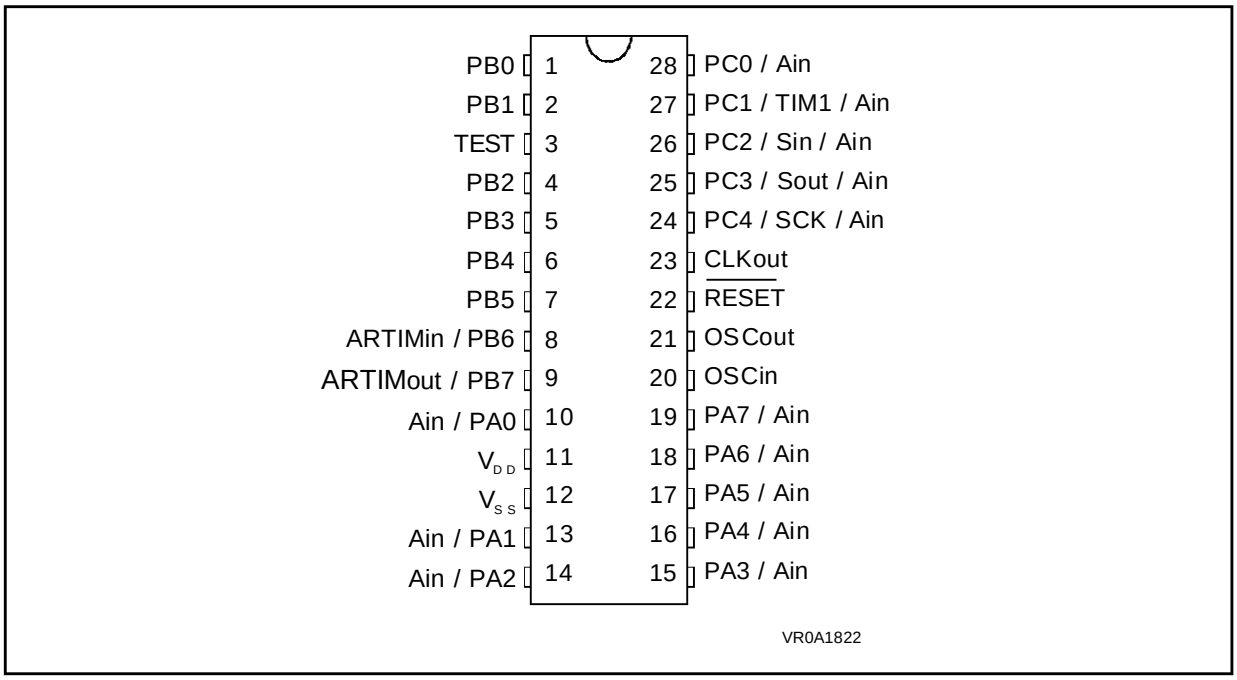
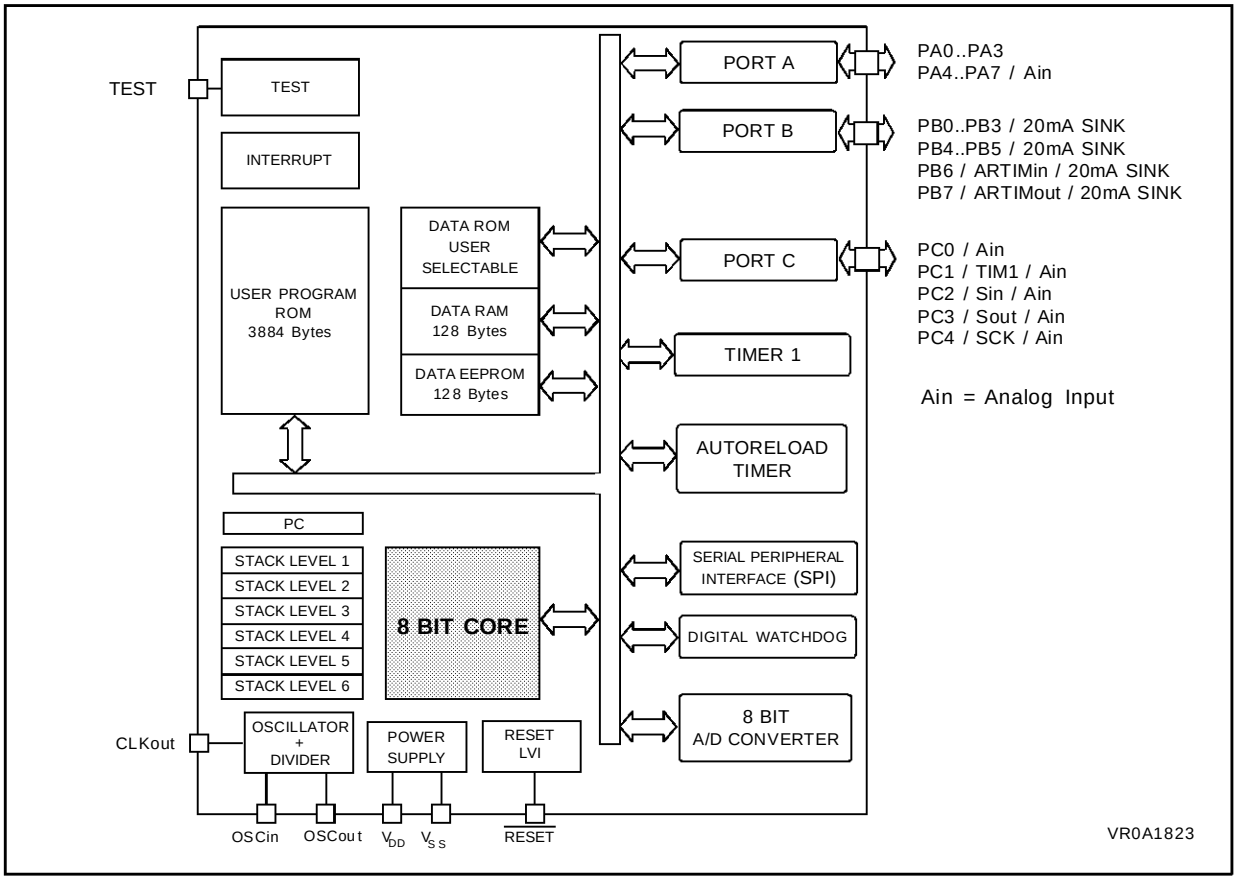


Figure 2. ST6294 Block Diagram



GENERAL DESCRIPTION

The ST6294 microcontroller is member of the 8-bit HCMOS ST62xx family, a series of devices oriented to low-medium complexity applications. All ST62xx members are based on a building block approach: a common core is surrounded by a combination of on-chip peripherals (macrocells).

The macrocells of the ST6294 are: the Timer peripheral that includes an 8-bit counter with a 7-bit software programmable prescaler (Timer1), the 8-bit Auto-reload Timer with 7 bit programmable prescaler (AR Timer), the 8-bit A/D Converter with up to 13 analog inputs (A/D inputs are alternate functions of I/O pins), the Digital Watchdog (DWD) and an 8-bit Serial synchronous Peripheral Interface (SPI). In addition, these devices offer 128 bytes of EEPROM for non volatile data storage.
The ST6294 is a version of the ST6265 specifically tailored to be used in telephone set applications. The only difference is that a CKOUT pin is provided instead of the NMI pin. For this reason this datasheet only contains information relating to the differences to the ST6265, and thus should be read in conjunction with the ST6265 datasheet. The ST62E94 EPROM version is available for prototypes and low-volume production; also OTP version is available.

PIN DESCRIPTION

V_{DD} and V_{SS}. Power is supplied to the MCU using these two pins. V_{DD} is power and V_{SS} is the ground connection.

OSCin and OSCout. These pins are internally connected with the on-chip oscillator circuit. A quartz crystal, a ceramic resonator or an external clock signal can be connected between these two pins in order to allow the correct operation of the MCU with various stability/cost trade-offs. The frequency at OSCin and OSCout is internally divided by 1, 2 or 4 by a software controlled divider.The OSCin pin is the input pin, the OSCout pin is the output pin.

$\overline{\text{RESET}}$. The active low $\overline{\text{RESET}}$ pin is used to restart the microcontroller to the beginning of its program.

TEST. The TEST must be held at V_{SS} for normal operation (an internal pull-down resistor selects normal operating mode if TEST pin is not connected).

CKOUT. This clock pin outputs the oscillator frequency divided by 2 ($f_{OSC}/2$). This function can be disabled by software to reduce power consumption.

PC1/TIM1/Ain. This pin can be used as a Port C I/O bit, as Timer 1 I/O pin or as analog input for the on-chip A/D converter. If programmed to be the Timer 1 pin, in input mode it is connected to the prescaler and acts as external timer clock or as control gate for the internal timer clock. In the output mode the timer pin outputs the data bit when a time out occurs.
To use this pin as Timer 1 output a dedicated bit in the TIMER 1 Status/Control Register must be set. To use this pin as input pin the I/O pin has to be programmed as input. The analog mode should be programmed to use the line as an analog input.

PB6/ARTIMin, PB7/ARTIMout. These pins are either Port B I/O bits or the Input and Output pins of the Auto-reload Timer. To be used as timer input function PB6 has to be programmed as input with or without pull-up. A dedicated bit in the AR TIMER Mode Control Register sets PB7 as timer output function.

PA0-PA7. These 8 lines are organized as one I/O port (A). Each line may be configured under software control as input with or without internal pull-up resistor, interrupt generating input with pull-up resistor, analog input, open-drain or push-pull output.

PB0-PB3, PB4, PB5. These 6 lines are organized as one I/O port (B). Each line may be configured under software control as input with or without internal pull-up resistor, interrupt generating input with pull-up resistor, open-drain or push-pull output. In output mode these lines can also sink 20mA for direct LED and TRIAC driving. The reset configuration of PB0-PB3 can be selected by mask option (pull-up or high impedance).

PC0-PC4. These 5 lines are organized as one I/O port (C). Each line may be configured under software control as input with or without internal pull-up resistor, interrupt generating input with pull-up resistor, analog input for the A/D converter, open-drain or push-pull output. PC2-PC4 can also be used as respectively Data in, Data out and Clock I/O pins for the on-chip SPI to carry the synchronous serial I/O signals.

ST6294 DESCRIPTION

The ST6294 is a version of the ST6265 standard device dedicated to telephone set application.

From a user point of view (with the following exceptions) the ST6294 product has exactly the same software and hardware features as the ST6265.

NMI

There is no external NMI pin in the ST6294. Although the ST6294 uses the standard ST62 core, which includes the NMI function. The user program therefore cannot place the ST62 in NMI mode. However, NMI mode is the default mode at power on or after a system reset generated by the watchdog or through the RESET pin. In these cases, the user software must perform a RETI instruction to exit from NMI mode to enable further interrupts from other sources prior to any other instruction. The ST6265 data sheet must therefore be read in this respect.

CKOUT PIN

The CKOUT pin is a dedicated output pin which enables a stabilized clock output to drive external circuits without any additional components. The clock output can be disabled by software to reduce power cosumption.

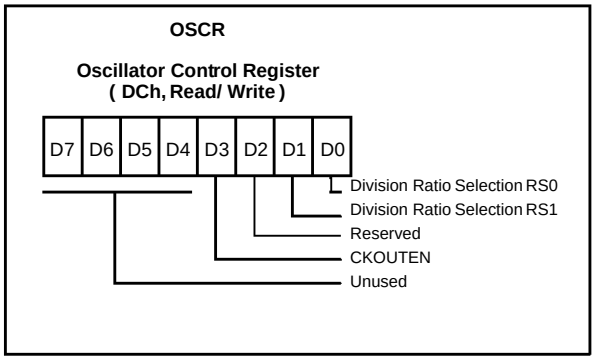
The output frequency is the oscillator frequency (before the Oscillator Divider) divided by 2 (f_{OSC}/ 2). The CKOUT pin is enabled through bit CKOUTEN of the Oscillator Control Register, at address DCh. The CKOUT pin provides high drive current capability.

Note :

When enabled through the CKOUTEN bit, the clock output increases the device overall power consumption by around 200µA. It should therefore be disabled when the lowest power consumption is required.

Oscillator Control Register

Figure 3. Oscillator Control Register



D7-D4. These bits are not used.

CKOUTEN. This bit, when cleared to zero, enables the output of the oscillator frequency divided by 2 at pin CKOUT. When it is set to one, pin CKOUT is held high. CKOUTEN is cleared on reset.

D2. Reserved. Must be kept low.

RS1-RS0. These bits select the division ratio of the Oscillator Divider in order to generate the internal frequency. The following selections are available:

RS1	RS0	Division Ratio
0	0	1
0	1	2
1	0	4
1	1	4

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

This product contains devices to protect the inputs against damage due to high static voltages, however it is advised to take normal precaution to avoid application of any voltage higher than maximum rated voltages.

For proper operation it is recommended that V_I and V_O must be higher than V_{SS} and smaller V_{DD}. Reliability is enhanced if unused inputs are connected to an appropriated logic voltage level (V_{DD} or V_{SS}).

Power Considerations. The average chip-junction temperature, Tj, in Celsius can be obtained from :

$Tj = T_A + PD \times RthJA$

Where : T_A = Ambient Temperature.

RthJA = Package thermal resistance (junction-to ambient).

PD = Pint + Pport.

Pint = $I_{DD} \times V_{DD}$ (chip internal power).

Pport = Port power dissipation (determinated by the user).

Symbol	Parameter Value	Unit	
V_{DD}	Supply Voltage	-0.3 to 7.0	V
V_I	Input Voltage	V_{SS} - 0.3 to V_{DD} + 0.3(1)	V
V_O	Output Voltage	V_{SS} - 0.3 to V_{DD} + 0.3(1)	V
I_O	Current Drain per Pin Excluding V_{DD}, V_{SS}	10	mA
I_{INJ+}	Pin Injection current (positive), All I/O, V_{DD} = 4.5V	+5	mA
I_{INJ-}	Pin Injection current (negative), All I/O, V_{DD} = 4.5V	-5	mA
IV_{DD}	Total Current into V_{DD} (source)	50	mA
IV_{SS}	Total Current out of V_{SS} (sink)	50	mA
Tj	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-60 to 150	°C

Notes :

- Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device . This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

- (1) Within these limits, clamping diodes are guarantee to be not conductive. Voltages outside these limits are authorised as long as injection current is kept within the specification.

THERMAL CHARACTERISTIC

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
RthJA	Thermal Resistance	PDIP28		55		°C/W
		PSO28		75		

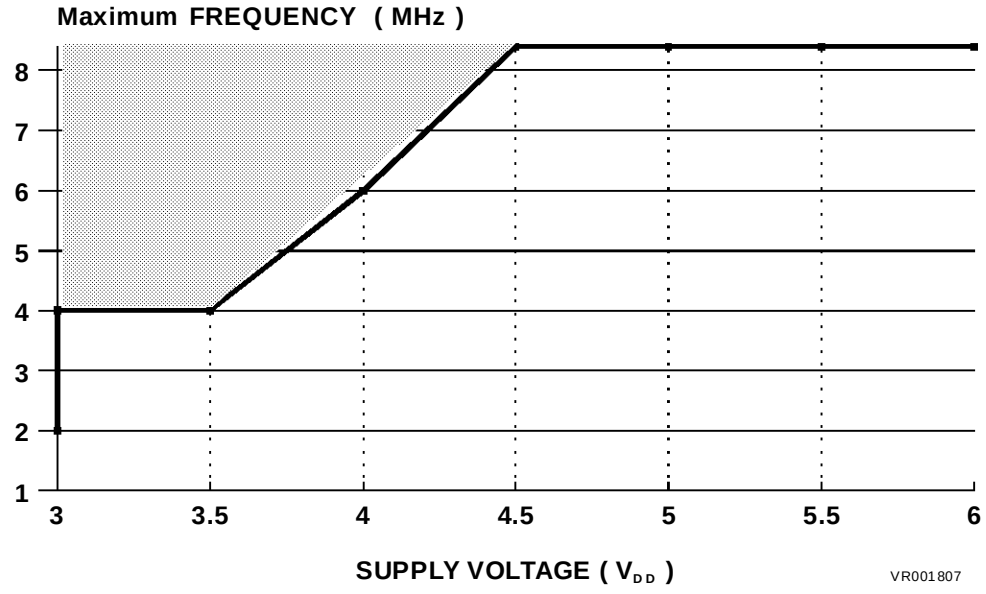
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
T_A	Operating Temperature	8 Suffix Version	-25		85	°C
V_{DD}	Operating Supply Voltage	f_{OSC}= 4MHz f_{INT} = 4MHz	3.0		6.0	V
		f_{OSC} = 8MHz f_{INT} = 8MHz	4.5		6.0	V
f_{INT}	Internal Frequency (3)	V_{DD} = 3V V_{DD} = 4.5V	0 0		4.0 8.0	MHz MHz
I_{INJ+}	Pin Injection Current (positive) Digital Input (1) Analog Inputs (2)	V_{DD} = 4.5 to 5.5V			+5	mA
I_{INJ-}	Pin Injection Current (negative) Digital Input (1) Analog Inputs	V_{DD} = 4.5 to 5.5V			-5	mA

Notes :

1. A current of ± 5mA can be forced on each pin of the digital section without affecting the functional behaviour of the device. For a positive current injected into one pin, a part of this current (~ 10%) can be expected to flow from the neighbouring pins.
2. If a total current of +1 mA is flowing into the single analog channel or if the total current flowing into all the analog inputs is of 1mA, all the resulting conversions are shifted by +1 LSB. If a total positive current is flowing into the single analog channel or if the total current flowing into all the analog inputs is of 5mA, all the resulting conversions are shifted by +2 LSB.
3. An oscillator frequency above 1MHz is recommended for reliable A/D results.

Maximum Operating FREQUENCY (Fmax) Versus SUPPLY VOLTAGE (V_{DD})



The shaded area is outside the ST6294 operating range, device functionality is not guaranteed.

DC ELECTRICAL CHARACTERISTICS

(T_A = -25 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IL}	Input Low Level Voltage All inputs				V_{DD} x 0.3	V
V_{IH}	Input High Level Voltage All inputs		V_{DD} x 0.7		V	
V_{OL}	Low Level Output Voltage	V_{DD}=5V I_{OL} = 10µA, All I/O pins CKOUT I_{OL} = 5mA, Standard I/O CKOUT I_{OL} = 10mA, Port B I_{OL} = 20mA, Port B			0.1 0.8 0.8 1.3	V
V_{OH}	High Level Output Voltage	V_{DD}=5V I_{OH} = -10µA I_{OH} = -5.0mA I_{OH} = -1.5mA, V_{DD}=3V	4.9 3.5 2.0			V
I_{PU}	Input Pull-up Current Input Mode with Pull-up Port A, B, C,	V_{IN} = V_{SS}, V_{DD}=3.0-6V			100	µA
I_{IL} I_{IH}	Input Leakage Current (1)	V_{IN} = V_{SS} V_{IN} = V_{DD}			1.0	µA
I_{DD}	Supply Current in RESET Mode	V_{RESET}=V_{SS}, f_{OSC}=4MHz V_{DD}<3.8V V_{DD}<6.0V			0.70 1.25	mA
	Supply Current in RUN Mode (2)	V_{DD}=6.0V, f_{INT}=8MHz All peripherals on (1)			6.6	mA
		V_{DD}=3.8V, f_{INT}=4MHz All peripherals on (1)			1.5	mA
		V_{DD}=3.8V, f_{INT}=1MHz f_{OSC}=4MHz Peripherals disabled (2)			0.65	mA
	Supply Current in WAIT Mode (3)	V_{DD}=6.0V, f_{INT}=8MHz Peripherals disabled (3) V_{DD}=3.8V, f_{INT}=4MHz Peripherals disabled (3)			1.30 0.35	mA
	Supply Current in STOP Mode	V_{DD}=6.0V			20	µA

Notes :

1. A/D Converter running, EEPROM enabled; Timer 1 and AR Timer running; CKOUTpin enabled. When the EEPROM is in write cycle, an additional 300µA must be added to I_{DD}max
2. A/D Converter in Stand-by; EEPROM in Stand-by; CKOUT pin disabled
3. A/D Converter in Stand-by; EEPROM in Stand-by; CKOUT pin disabled; Timer 1 and AR Timer stopped
4. Hysteresis voltage between switching levels

AC ELECTRICAL CHARACTERISTICS

(T_A = -25to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
f_{OSC}	Oscillator Frequency	V_{DD} = 3.0V V_{DD} = 4.5V			4 8	MHz
t_{OHL}	High to Low Transition Time	Port A, B, C, CKOUT C_L=100pF		40		ns
t_{OLH}	Low to High Transition Time	Port A, B, C, CKOUT C_L=100pF		40		
t_{SU}	Oscillator Start-up Time	$C_{L1} = C_{L2}$ = 22pF V_{DD}=5V		5	10	ms
t_{REC}	Supply Recovery Time (1)		100			
T_{WR}	Minimum Pulse Width (V_{DD} = 5V) RESET pin, NMI pin		100		ns	
T_{WEE}	EEPROM Write Time	T_A = 25°C One Byte		5	10	ms
Endurance	EEPROM WRITE/ERASE Cycle	Q_A L_{OT} Acceptance	300.000			cycles
Retention	EEPROM Data Retention	T_A = 25°C	10		years	
C_{IN}	Input Capacitance	All Inputs Pins			10	pF
C_{OUT}	Output Capacitance	All Outputs Pins			10	pF

Note:

1. Period for which V_{DD} has to be connected at 0V to allow internal Reset function at next power-up.

I/O PORT CHARACTERISTICS

(T_A = -25 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IL}	Input Low Level Voltage	I/O Pins			0.3x V_{DD}	V
V_{IH}	Input High Level Voltage	I/O Pins	0.7x V_{DD}			V
V_{OL}	Low Level Output Voltage	V_{DD}= 5.0V I_{OL}= 10µA , All I/O Pins, CKOUT I_{OL}= 5mA , Standard I/O, CKOUT I_{OL}= 10mA , Port B I_{OL}= 20mA , Port B			0.1 0.8 0.8 1.3	V
V_{OH}	High Level Output Voltage	I_{OH}= – 10µA I_{OH}= – 5mA, V_{DD}= 5.0V I_{OH}= – 1.5mA, V_{DD}= 3.0V	V_{DD}-0.1 3.5 2.0			V
I_{IL} I_{IH}	Input Leakage Current I/O Pins (pull-up resistor off)	Vin= V_{DD} or V_{SS} V_{DD}= 3.0V V_{DD}= 5.5V		0.1 0.1	1.0 1.0	µA

SPI CHARACTERISTICS

(T_A = -25 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
f_{CL}	Clock Frequency at SCK				500	kHz
t_{SV}	Data Set up time on Sin			TBD		
t_H	Data hold time on Sin			TBD		
t_{TS}	Delay Transmission started on Sin	8MHz	0	Note 1		µs

Note 1. Minimum time: 0µs
Maximum time: 1 instruction cycle

TIMER1 CHARACTERISTICS

(T_A = -25 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
t_{RES}	Resolution		$\frac{12}{f_{INT}}$			s
f_{IN}	Input Frequency on TIM1 Pin				$\frac{f_{INT}}{8}$	MHz
t_W	Pulse Width at TIM1 Pin	V_{DD} = 3.0V $V_{DD} \geq$ 4.5V	1 125			µs ns

AR TIMER CHARACTERISTICS

(T_A = -25 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
t_{RES}	Resolution		$\frac{1}{f_{INT}}$			s
f_{ARin}	Input Frequency on ARTIMin pin	STOP Mode RUN and WAIT Modes			2 $\frac{f_{INT}}{4}$	MHz MHz
t_W	Pulse Width at ARTIMin Pin	V_{DD} = 3.0V $V_{DD} \geq$ 4.5V	125 125			ns ns

A/D CONVERTER CHARACTERISTICS

(T_A= -25 to +85°C unless otherwise specified)

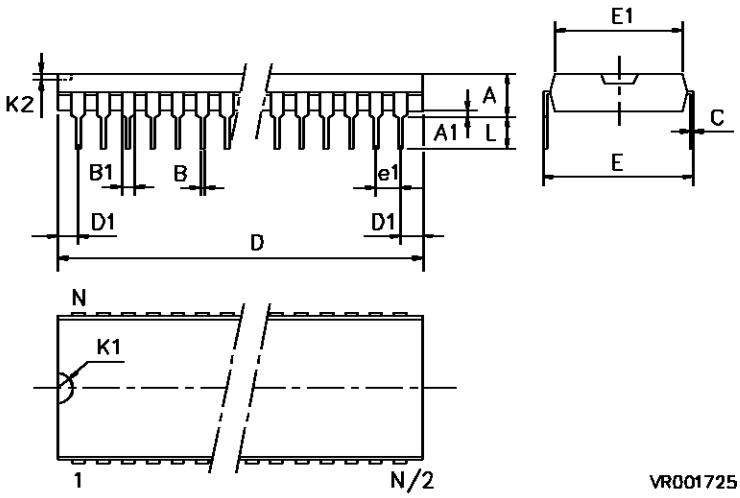
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Res	Resolution			8		Bit
A_{TOT}	Total Accuracy (1) (2)	f_{OSC} > 1.2MHz f_{OSC} > 32kHz			±2 ±4	LSB
t_C	Conversion Time	f_{OSC} = 8MHz		70		µs
V_{AN}	Conversion Range		V_{SS}		V_{DD}	V
ZIR	Zero Input Reading	Conversion result when $V_{IN} = V_{SS}$	00		Hex	
FSR	Full Scale Reading	Conversion result when $V_{IN} = V_{DD}$			FF	Hex
AD_I	Analog Input Current During Conversion	V_{DD}= 4.5V			1.0	µA
AC_{IN} (3)	Analog Input Capacitance			2	5	pF
ASI	Analog Source Impedance	Analog Channel switched just before conversion start (4)			30	kΩ

Notes:

1. Noise at V_{DD}, V_{SS} <10mV
2. With oscillator frequencies less than 1MHz, the A/D Converter accuracy is decreased.
3. Excluding Pad Capacitance.
4. ASI can be increased as long as the load of the A/D Converter input capacitor is ensured before conversion start.

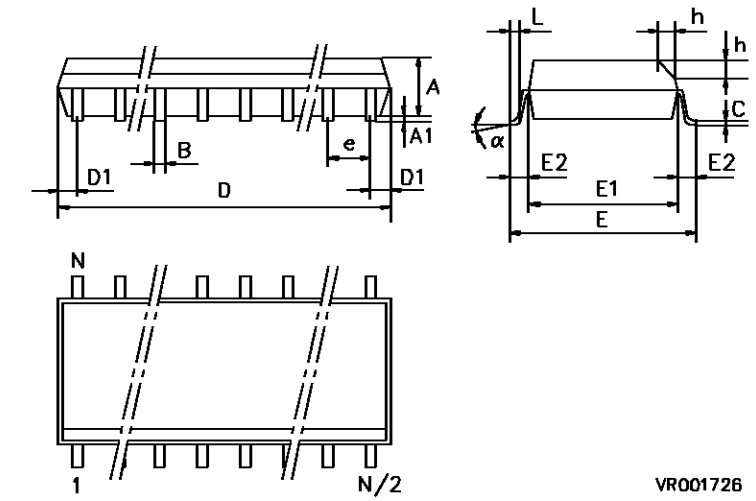
PACKAGE MECHANICAL DATA

Figure 4. 28-Pin Dual in Line Plastic (B), 600-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.2		4.8	0.086		0.189
A1	0.51		1.77	0.010		0.069
B	0.38		0.58	0.015		0.023
B1	0.97		1.52	0.055		0.065
C	0.2		0.3	0.008		0.009
D	35.06		36.22	1.400		1.425
D1	–	–	–	–	–	–
E			16.3			0.641
E1		12.9				0.508
K1	–	–	–	–	–	–
K2	–	–	–	–	–	–
L	3.18		4.44	1.25		0.174
e1		2.54			0.10	
Number of Pins						
N	28					

Figure 5. 28-Lead Small Outline Plastic (M), 300-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.05		2.55	0.081		0.10
A1	0.1		0.3	0.004		.0118
B	0.35		0.49	.0138		.0192
C	0.23		0.32	.0091		.0125
D	17.7		18.1	.6969		.7125
D1	–	–	–	–	–	–
E	10.0		10.65	0.394		0.419
E1	7.40		7.60	.2914		.2992
E2	–	–	–	–	–	–
L	0.40		1.27	0.016		0.050
e		1.27			0.05	
α	–	–	–	–	–	–
Number of Pins						
N	28					

ORDERING INFORMATION

The following chapter deals with the procedure for transfer customer codes to SGS-THOMSON.

Communication of the customer code. Customer code is made up of the ROM contents and the list of the selected mask options. The ROM contents are to be sent on one diskette with the hexadecimal file generated by the development tool. All unused bytes must be set to FFh.

The selected mask options are communicated to SGS-THOMSON using the correctly filled OPTION LIST appended.

Listing Generation & Verification. When SGS-THOMSON receives the diskette, a computer listing is generated from it. This listing refers exactly to the mask that will be used to produce the microcontroller. Then the listing is returned to the customer that must thoroughly check, complete, sign and return it to SGS-THOMSON. The signed listing constitutes a part of the contractual agreement for the creation of the customer mask.

SGS-THOMSON sales organization will provide detailed information on contractual points.

Table 1. ROM Memory Map

ST6294 (4K ROM Devices)

Device Address	Description
0000h-007Fh	Reserved (1)
0080h-0F9Fh	User ROM
0FA0h-0FEFh	Reserved (1)
0FF0h-0FF7h	Interrupt Vectors
0FF8h-0FFBh	Reserved (1)
0FFCh-0FFDh	NMI Interrupt Vector
0FFEh-0FFFh	Reset Vector

Note 1. Reserved Areas should be filled with FFh

ORDERING INFORMATION TABLE

Sales Type	ROM x8	I/O	Temperature Range	Package
ST6294B8/XXX	4K Bytes	21	-25 to + 85°C	PDIP28
ST6294M8/XXX	4K Bytes	21	-25 to +85°C	PSO28

Note: /XXX is a 2-3 alphanumeric character code added to the generic sales type on receipt of a ROM code and valid options.

ST6294 MICROCONTROLLER OPTION LIST

Customer . . . . . .
Address . . . . . .
. . . . . .
Contact . . . . . .
Phone No . . . . . .
Reference . . . . . .

SGS-THOMSON Microelectronics references

Device:
[ ] ST6294

Package: [ ] Dual in Line Plastic [ ] Small Outline Plastic

In this case, select conditioning

[ ] Standard (Stick)
[ ] Tape & Reel

Temperature Range: [ ] -25°C to + 85°C

Special Marking: [ ] No

[ ] Yes "_ _ _ _ _ _ _ _ _ _"

Authorized characters are letters, digits, '.', '–', '/' and spaces only.
Maximum character count is 10 char. for DIP packages
and 8 char. for SO packages.

PB0/PB1 Status during reset

[ ] Input with pull-up [ ] High impedance

PB2/PB3 Status during reset

[ ] Input with pull-up [ ] High impedance

Watchdog Selection:

[ ] Hardware Activation (no STOP mode) [ ] Software Activation (STOP mode available)

Notes . . . . . .
. . . . . .
Signature . . . . . .
Date . . . . . .

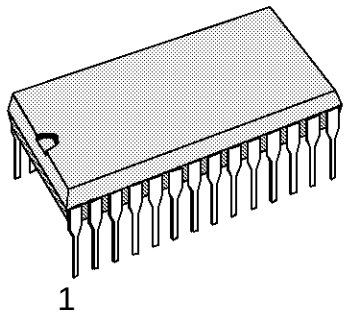
SGS-THOMSON MICROELECTRONICS

ST62E94, T94

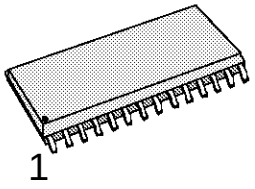
8-BIT EPROM HCMOS MCUs WITH A/D CONVERTER, EEPROM & AUTORELOAD TIMER

PRELIMINARY DATA

- 3.0 to 6.0V Supply Operating Range
- 8 MHz Maximum Clock Frequency
- -25 to +85°C Operating Temperature Range
- Run, Wait & Stop Modes
- 5 different interrupt vectors
- Look-up table capability in ROM
- User EPROM: 3868 bytes
  Data ROM: User selectable size (in program EPROM)
  Data RAM: 128 bytes
  EEPROM: 128 bytes
- PDIP28, PSO28 (ST62T94) packages
- CDIP28W (ST62E94) packages
- 21 fully software programmable I/O as:
  – Input with pull-up resistor
  – Input without Pull-up resistor
  – Input with interrupt generation
  – Open-drain or push-pull outputs
  – Analog Inputs
- 8 I/O lines can sink up to 20mA for direct LED or TRIAC driving
- 8 bit counter with a 7-bit programmable prescaler (Timer1)
- 8 bit Autoreload timer with 7-bit programmable prescaler (AR Timer)
- Digital Watchdog
- 8 bit A/D Converter with up to analog inputs
- 8 bit Synchronous Peripheral Interface (SPI)
- On-chip clock oscillator (Quartz or Ceramic)
- Power-on Reset
- Clock output
- 9 powerful addressing modes



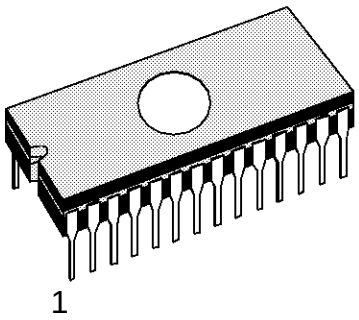
PDIP28



PSO28

(Ordering Information at the end of the datasheet)

EPROM PACKAGES



CDIP28W

The ST62E94 is the EPROM version; ST62T94 is the OTP version; both are fully compatible with ST6294 ROM version.

Figure 6. ST62E94/T94 Pin Configuration

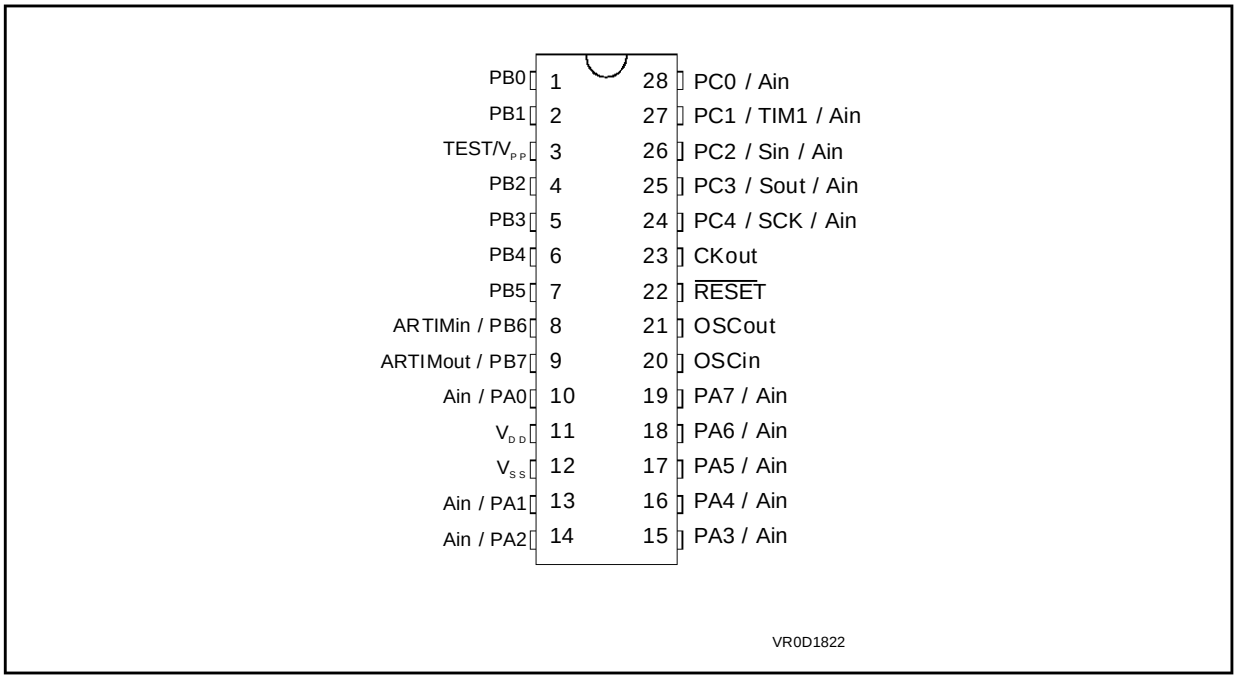
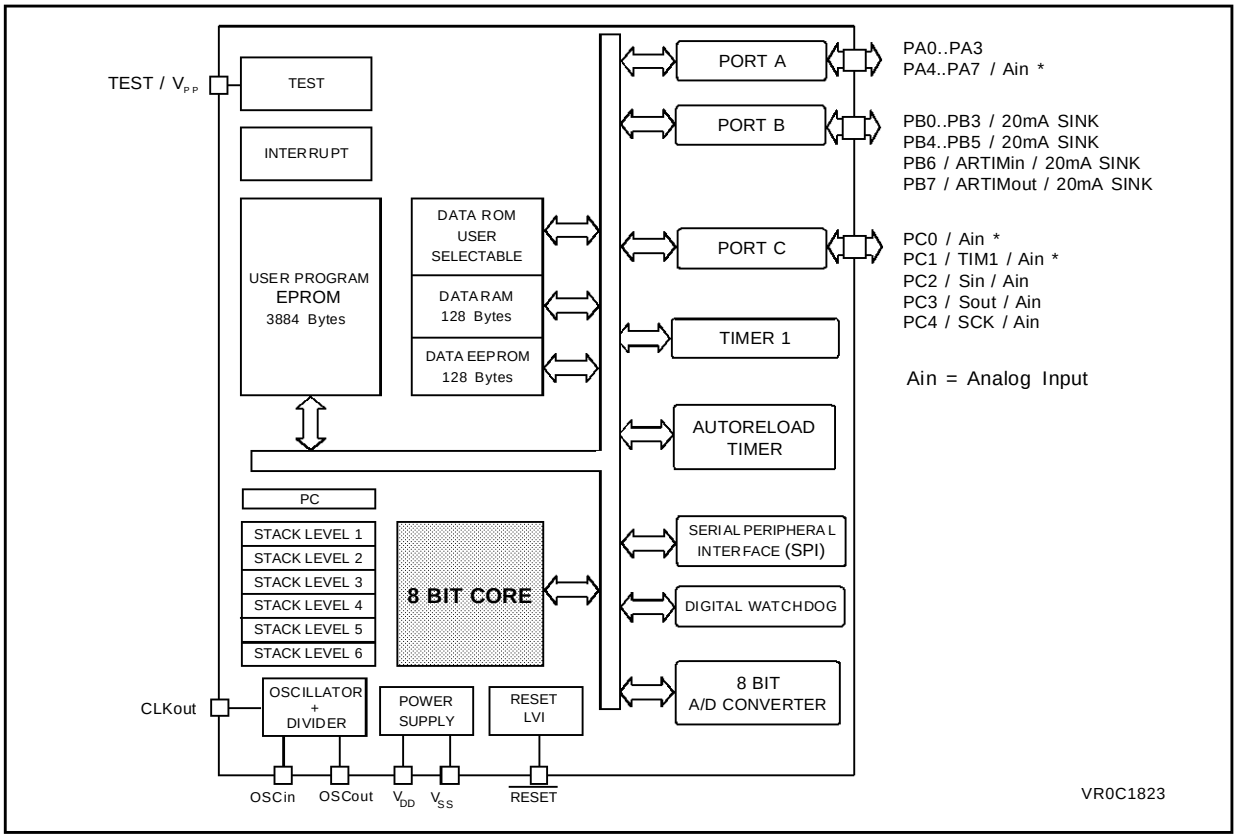


Figure 7. ST62E94 Block Diagram



GENERAL DESCRIPTION

The ST62E94,T94 microcontrollers are members of the 8-bit HCMOS ST62xx family, a series of devices oriented to low-medium complexity applications.

They are the EPROM and OTP versions of the ST6294 device. EPROM are suited for development. OTPs are suited for prototyping, preseries, low to mid volume series and inventory optimization for customer having several applications using the same MCU. All ST62xx members are based on a building block approach: a common core is surrounded by a combination of on-chip peripherals (macrocells).
The macrocells of the ST62E94, T94 are: the timer peripheral that includes an 8-bit counter with a 7-bit software programmable prescaler (Timer1), the 8-bit Auto-reload Timer with 7 bit programmable prescaler (AR Timer), the 8-bit A/D Converter with up to 13 analog inputs (A/D inputs are alternate functions of I/O pins), the Digital Watchdog (DWD) and an 8-bit Serial synchronous Peripheral Interface (SPI). In addition, these devices offer 128 bytes of EEPROM for non volatile data storage.
The ST62E94 ,T94 are a version of the ST62E65, T65 specifically tailored to be used in telephone set applications. The only difference is that a CKOUT pin is provided instead of the NMI input pin.

PIN DESCRIPTION

V_{DD} and V_{SS}. Power is supplied to the MCU using these two pins. V_{DD} is power and V_{SS} is the ground connection.

OSCin and OSCout. These pins are internally connected with the on-chip oscillator circuit. A quartz crystal, a ceramic resonator or an external clock signal can be connected between these two pins in order to allow the correct operation of the MCU with various stability/cost trade-offs. The frequency at OSCin and OSCout is internally divided by 1, 2 or 4 by a software controlled divider.The OSCin pin is the input pin, the OSCout pin is the output pin.

$\overline{\text{RESET}}$. The active low $\overline{\text{RESET}}$ pin is used to restart the microcontroller to the beginning of its program.

TEST. The TEST must be held at VSS for normal operation (an internal pull-down resistor selects normal operating mode if TEST pin is not connected).

CKOUT. This clock pin outputs the oscillator frequency divided by 2 ($f_{OSC}/2$). This function can be disabled by software to reduce power consumption.

PC1/TIM1/Ain. This pin can be used as a Port C I/O bit, as Timer 1 I/O pin or as analog input for the on-chip A/D converter. If programmed to be the Timer 1 pin, in input mode it is connected to the prescaler and acts as external timer clock or as control gate for the internal timer clock. In the output mode the timer pin outputs the data bit when a time out occurs.
To use this pin as Timer 1 output a dedicated bit in the TIMER 1 Status/Control Register must be set. To use this pin as input pin the I/O pin has to be programmed as input. The analog mode should be programmed to use the line as an analog input.

PB6/ARTIMin, PB7/ARTIMout. These pins are either Port B I/O bits or the Input and Output pins of the Auto-reload Timer. To be used as timer input function PB6 has to be programmed as input with or without pull-up. A dedicated bit in the AR TIMER Mode Control Register sets PB7 as timer output function.

PA0-PA7. These 8 lines are organized as one I/O port (A). Each line may be configured under software control as input with or without internal pull-up resistor, interrupt generating input with pull-up resistor, analog input, open-drain or push-pull output.

PB0-PB3, PB4, PB5. These 6 lines are organized as one I/O port (B). Each line may be configured under software control as input with or without internal pull-up resistor, interrupt generating input with pull-up resistor, open-drain or push-pull output. In output mode these lines can also sink 20mA for direct LED and TRIAC driving.

PC0-PC4. These 5 lines are organized as one I/O port (C). Each line may be configured under software control as input with or without internal pull-up resistor, interrupt generating input with pull-up resistor, analog input for the A/D converter, open-drain or push-pull output. PC2-PC4 can also be used as respectively Data in, Data out and Clock I/O pins for the on-chip SPI to carry the synchronous serial I/O signals.

THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST6294 DEVICE FOR FURTHER DETAILS.

EPROM/OTP DESCRIPTION

The ST62E94 is the EPROM version of the ST6294 product. It is intended for use during the development of an application and for pre-production and small volume production. ST62T94 OTP has the same characteristics. It includes EPROM memory instead of the ROM memory and so the program can be easily modified by the user with the ST62E6x EPROM programming tools from SGS-THOMSON.

From a user point of view (with the following exceptions) the ST62E94, T94 products have exactly the same software and hardware features as the ROM version. An additional mode is used to configure the part for programming of the EPROM, this is set by a +12.5V voltage applied to the TEST/V_{PP} pin. The programming of the ST62E94, T94 is described in the User Manual of the EPROM Programming Board.
Note also the Low Voltage option of ROM devices can not be emulated on EPROM or OTP devices

ROM Option Emulation

The ROM mask options that can be selected by the user in the ROM devices can be selected on the EPROM/OTP devices by an EPROM CODE byte that can be programmed with the ST62E6x EPROM programming tools available from SGS-THOMSON. This EPROM CODE byte is automatically read, and the selected options enabled, when the chip reset is activated.
The Option byte is written during programming either by using the PC menu (PC driven Mode) or automatically (stand-alone mode).

EPROM Programming Mode

An additional mode is used to configure the part for programming of the EPROM, this is set by a 12.5V voltage applied to the TEST/V_{PP} pin. The programming of the ST62E94, T94 is described in the User Manual of the EPROM Programming board.

EPROM ERASING

The EPROM of the windowed package of the ST62E94 may be erased by exposure to Ultra Violet light.
The erasure characteristic of the ST62E94 is such that erasure begins when the memory is exposed to light with a wave lengths shorter than approximately 4000Å. It should be noted that sunlights and some types of fluorescent lamps have wavelengths in the range 3000-4000Å. It is thus recommended that the window of the ST62E94 packages be covered by an opaque label to prevent unintentional erasure problems when testing the application in such an environment.

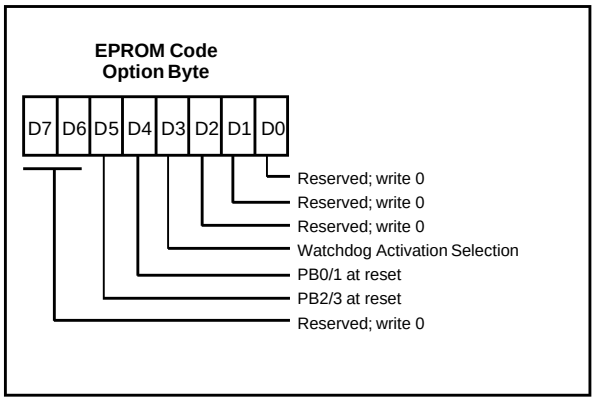
The recommended erasure procedure of the ST62E94 EPROM is the exposure to short wave ultraviolet light which have a wave-length 2537A. The integrated dose (i.e. U.V. intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000µW/cm^2 power rating. The ST62E94 should be placed within 2.5cm (1Inch) of the lamp tubes during erasure.

Table 2. ST62E94/T94 OTP Memory Map

Device Address	Description
0000h-007Fh	Reserved
0080h-0F9Fh	User Program ROM 3856 Bytes
0FA0h-0FEFh 0FF0h-0FF7h 0FF8h-0FFBh 0FFCh-0FFDh 0FFEh-0FFFh	Reserved Interrupt Vectors Reserved NMI Vector User Reset Vector

Note. Reserved Areas should be filled with FFh

Figure 8. EPROM Code Option Byte



D7-D6. These bits are not used.

D5. This bit selects the configuration of the ports PB2 and PB3 during reset. If set to zero, PB2 and PB3 are configured with pull-up during reset. If set to one, PB2 and PB3 are configured as high impedance ports.

D4. Same as D5 for PB0 and PB1.

D3. This bit selects the on-chip Watchdog activation. If cleared to zero this bit selects the software activation, if set to one, it selects the hardware activation option.

D2-D0. Must be cleared to zero.

D1. Must be set to zero.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

This product contains devices to protect the inputs against damage due to high static voltages, however it is advised to take normal precaution to avoid application of any voltage higher than maximum rated voltages.

For proper operation it is recommended that V_I and V_O must be higher than V_{SS} and smaller V_{DD}. Reliability is enhanced if unused inputs are connected to an appropriated logic voltage level (V_{DD} or V_{SS}).

Power Considerations. The average chip-junction temperature, Tj, in Celsius can be obtained from :

$Tj = T_A + PD \times RthJA$

Where : T_A = Ambient Temperature.

RthJA = Package thermal resistance (junction-to ambient).

PD = Pint + Pport.

Pint = $I_{DD} \times V_{DD}$ (chip internal power).

Pport = Port power dissipation (determinated by the user).

Symbol	Parameter	Value	Unit	
V_{DD}	Supply Voltage		-0.3 to 7.0	V
V_I	Input Voltage		V_{SS} - 0.3 to V_{DD} + 0.3(1)	V
V_O	Output Voltage		V_{SS} - 0.3 to V_{DD} + 0.3(1)	V
I_O	Current Drain per Pin Excluding V_{DD}, V_{SS}		10	mA
I_{INJ+}	Pin Injection current (positive), All I/O, V_{DD} = 4.5V		+5	mA
I_{INJ-}	Pin Injection current (negative), All I/O, VDD = 4.5V		-5	mA
IV_{DD}	Total Current into V_{DD} (source)		50	mA
IV_{SS}	Total Current out of V_{SS} (sink)		50	mA
Tj	Junction Temperature		150	°C
T_{STG}	Storage Temperature		-60 to 150	°C

Notes :

- Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device . This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

- (1) Within these limits, clamping diodes are guarantee to be not conductive. Voltages outside these limits are authorised as long as injection current is kept within the specification.

THERMAL CHARACTERISTIC

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
RthJA	Thermal Resistance	PDIP28		55		°C/W
		PSO28		75		

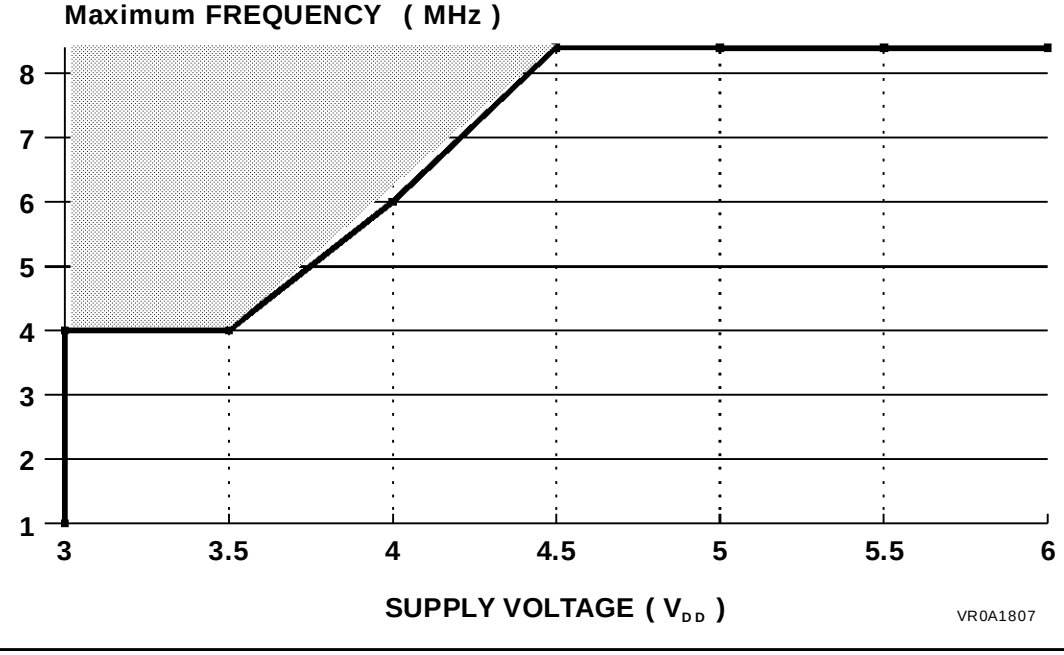
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
T_A	Operating Temperature	8 Suffix Version 1 Suffix Version	-25 0		85 70	°C
V_{DD}	Operating Supply Voltage	f_{OSC}= 4MHz f_{INT} = 4MHz f_{OSC} = 8MHz f_{INT} = 8MHz	3.0 4.5		6.0 6.0	V V
f_{INT}	Internal Frequency (3)	V_{DD} = 3V V_{DD} = 4.5V	0 0		4.0 8.0	MHz MHz
I_{INJ+}	Pin Injection Current (positive) Digital Input (1) Analog Inputs(2)	V_{DD} = 4.5 to 5.5V			+5	mA
I_{INJ-}	Pin Injection Current (negative) Digital Input (1) Analog Inputs	V_{DD} = 4.5 to 5.5V			-5	mA

Notes :

1. A current of ± 5mA can be forced on each pin of the digital section without affecting the functional behaviour of the device. For a positive current injected into one pin, a part of this current (~ 10%) can be expected to flow from the neighbouring pins.
2. If a total current of +1 mA is flowing into the single analog channel or if the total current flowing into all the analog inputs is of 1mA, all the resulting conversions are shifted by +1 LSB. If a total positive current is flowing into the single analog channel or if the total current flowing into all the analog inputs is of 5mA, all the resulting conversions are shifted by +2 LSB.
3. An oscillator frequency above 1MHz is recommended for reliable A/D results.

Maximum Operating FREQUENCY (Fmax) Versus SUPPLY VOLTAGE (V_{DD})



The shaded area is outside the device operating range, device functionality is not guaranteed.

DC ELECTRICAL CHARACTERISTICS

(T_A = -25 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IL}	Input Low Level Voltage All inputs				V_{DD} x 0.3	V
V_{IH}	Input High Level Voltage All inputs		V_{DD} x 0.7		V	
V_{OL}	Low Level Output Voltage	V_{DD}=5V I_{OL} = 10µA, All I/O pins CKOUT I_{OL} = 5.0mA, Standard I/O CKOUT I_{OL} = 10mA, Port B I_{OL} = 20mA, Port B			0.1 0.8 0.8 1.3	V
V_{OH}	High Level Output Voltage	V_{DD}=5V I_{OH} = -10µA I_{OH}= -5.0mA I_{OH} = -1.5mA, V_{DD}=3V	4.9 3.5 2.0			V
I_{PU}	Input Pull-up Current Input Mode with Pull-up Port A, B, C	V_{IN} = V_{SS}, V_{DD}=3.0-6V			100	µA
I_{IL} I_{IH}	Input Leakage Current(1)	V_{IN} = V_{SS} V_{IN} = V_{DD}			1.0	µA
I_{DD}	Supply Current in RESET Mode	V_{RESET}=V_{SS},f_{OSC}=4MHz V_{DD}<3.8V V_{DD}<6.0V			0.70 1.25	mA
	Supply Current in RUN Mode (2)	V_{DD}=6.0V, f_{INT}=8MHz All peripherals on (1)			6.6	mA
		V_{DD}=3.8V, f_{INT}=4MHz All peripherals on (1)			1.50	mA
		V_{DD}=3.8V, f_{INT}=1MHz f_{OSC}=4MHz Peripherals disabled (2)			0.65	mA
	Supply Current in WAIT Mode (3)	V_{DD}=6.0V, f_{INT}=8MHz Peripherals disabled (3) V_{DD}=3.8V, f_{INT}=4MHz Peripherals disabled (3)			1.30 0.35	mA
	Supply Current in STOP Mode	V_{DD}=6.0V			20	µA

Notes :

1. A/D Converter running, EEPROM enabled; Timer 1 and AR Timer running; CKOUTpin enabled. When the EEPROM is in write cycle, an additional 300µA must be added to I_{DD}max
2. A/D Converter in Stand-by; EEPROM in Stand-by; CKOUT pin disabled
3. A/D Converter in Stand-by; EEPROM in Stand-by; CKOUT pin disabled; Timer 1 and AR Timer stopped
4. Hysteresis voltage between switching levels

AC ELECTRICAL CHARACTERISTICS

(T_A = -25 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
f_{OSC}	Oscillator Frequency	V_{DD} = 3.0V V_{DD} = 4.5V			4 8	MHz
t_{OHL}	High to Low Transition Time	Port A, B, C, CKOUT C_L=100pF		40		ns
t_{OLH}	Low to High Transition Time	Port A, B, C, CKOUT C_L=100pF		40		
t_{SU}	Oscillator Start-up Time	$C_{L1} = C_{L2}$ = 22pF V_{DD}=5V		5	10	ms
t_{REC}	Supply Recovery Time (1)		100			
T_{WR}	Minimum Pulse Width (V_{DD} = 5V) RESET pin, NMI pin		100 100			ns
T_{WEE}	EEPROM Write Time	T_A = 25°C One Byte		5	10	ms
Endurance	EEPROM WRITE/ERASE Cycle	Q_A L_{OT} Acceptance	300,000			cycles
Retention	EEPROM Data Retention	T_A = 25°C	10		years	
C_{IN}	Input Capacitance	All Inputs Pins			10	pF
C_{OUT}	Output Capacitance	All Outputs Pins			10	pF

Note:

1. Period for which V_{DD} has to be connected at 0V to allow internal Reset function at next power-up.

I/O PORT CHARACTERISTICS

(T_A = -25 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IL}	Input Low Level Voltage	I/O Pins			0.3x V_{DD}	V
V_{IH}	Input High Level Voltage	I/O Pins	0.7x V_{DD}			V
V_{OL}	Low Level Output Voltage	V_{DD}= 5.0V I_{OL}= 10µA , All I/O Pins, CKOUT I_{OL}= 5mA , Standard I/O, CKOUT I_{OL}= 10mA , Port B I_{OL}= 20mA , Port B			0.1 0.8 0.8 1.3	V
V_{OH}	High Level Output Voltage	I_{OH}= – 10µA I_{OH}= – 5mA, V_{DD}= 5.0V I_{OH}= – 1.5mA, V_{DD}= 3.0V	V_{DD}-0.1 3.5 2.0			V
I_{IL} I_{IH}	Input Leakage Current I/O Pins (pull-up resistor off)	Vin= V_{DD} or V_{SS} V_{DD}= 3.0V V_{DD}= 5.5V		0.1 0.1	1.0 1.0	µA
R_{PU}	Pull-up Resistor	Vin= 0V; All I/O Pins	50	100	200	KΩ

SPI CHARACTERISTICS

(T_A = -25 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
f_{CL}	Clock Frequency at SCK				500	kHz
t_{SV}	Data Set up time on Sin			TBD		
t_H	Data hold time on Sin			TBD		
t_{TS}	Delay Transmission started on Sin	8MHz	0	Note 1		µs

Note :

1. Minimum time: 0µs
Maximum time: 1 instruction cycle

TIMER1 CHARACTERISTICS

(T_A = -25 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
t_{RES}	Resolution		$\frac{12}{f_{INT}}$			s
f_{IN}	Input Frequency on TIM1 Pin				$\frac{f_{INT}}{8}$	MHz
t_W	Pulse Width at TIM1 Pin	V_{DD} = 3.0V $V_{DD} \geq$ 4.5V	1 125			µs ns

AR TIMER CHARACTERISTICS

(T_A = -25 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
t_{RES}	Resolution		$\frac{1}{f_{INT}}$			s
f_{ARin}	Input Frequency on ARTIMin pin	STOP Mode RUN and WAIT Modes			2 $\frac{f_{INT}}{4}$	MHz MHz
t_W	Pulse Width at ARTIMin Pin	V_{DD} = 3.0V $V_{DD} \geq$4.5V	125 125			ns ns

A/D CONVERTER CHARACTERISTICS

(T_A= -25 to +85°C unless otherwise specified)

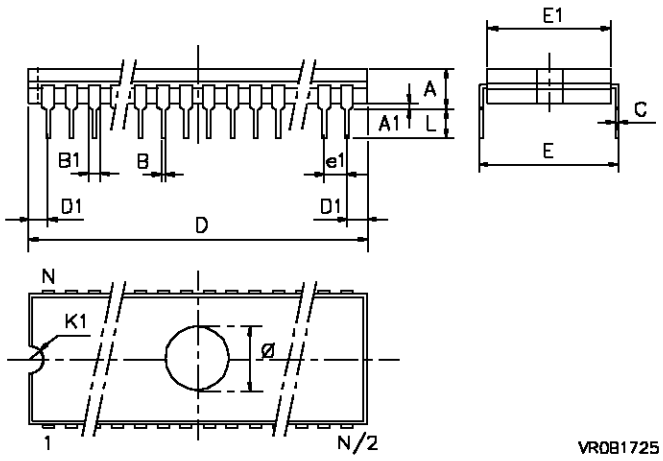
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Res	Resolution (1)			8		Bit
A_{TOT}	Total Accuracy (1)	f_{OSC} > 1.2MHz f_{OSC} > 32kHz			±2 ±4	LSB
t_C (2)	Conversion Time	f_{OSC} = 8MHz		70		µs
V_{AN}	Conversion Range		V_{SS}		V_{DD}	V
ZIR	Zero Input Reading	Conversion result when Vin = V_{SS}	00			Hex
FSR	Full Scale Reading	Conversion result when Vin = V_{DD}			FF	Hex
AD_I	Analog Input Current During Conversion	V_{DD}= 4.5V			1.0	µA
AC_{IN} (3)	Analog Input Capacitance			2	5	pF
ASI	Analog Source Impedance				30	KΩ
SSI	Analog Reference Supply Impedence				2	KΩ

Notes:

1. Noise at V_{DD}, V_{SS} <10mV
2. With oscillator frequencies less than 1MHz, the A/D Converter accuracy is decreased.
3. Excluding Pad Capacitance.
4. ASI can be increased as long as the load of the A/D Converter input capacitor is ensured before conversion start.

PACKAGE MECHANICAL DATA

Figure 9. 28-Lead Frit Seal Ceramic Dual in Line Package, 600-Mil Widht



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.71			0.225
A1	0.50		1.78	0.020		0.070
B	0.40		0.55	0.016		0.022
B1	1.17		1.42	.046		.056
C	0.22		0.31	0.009		0.012
D			38.10			1.500
D1	1.52		2.49	.060		.098
E	–	–	–	–	–	–
E1	13.05		13.36	.514		.526
L	3.00			.118		
e1	2.29		2.79	0.090		0.110
Ø	6.86		7.36	.270		.290
	Number of Pins					
N	28					

ORDERING INFORMATION

ORDERING INFORMATION TABLE

Sales Type	OTP/EPROM	I/O	Additional Features	Temperature Range	Package
ST62T94B8	OTP 4K Bytes	21	CKOUT Pin	-25° to + 85°C	PDIP28
ST62T94M8					PSO28
ST62E94F1	EPROM 4K Bytes	21	CKOUT Pin	0 to + 70°C	CDIP28