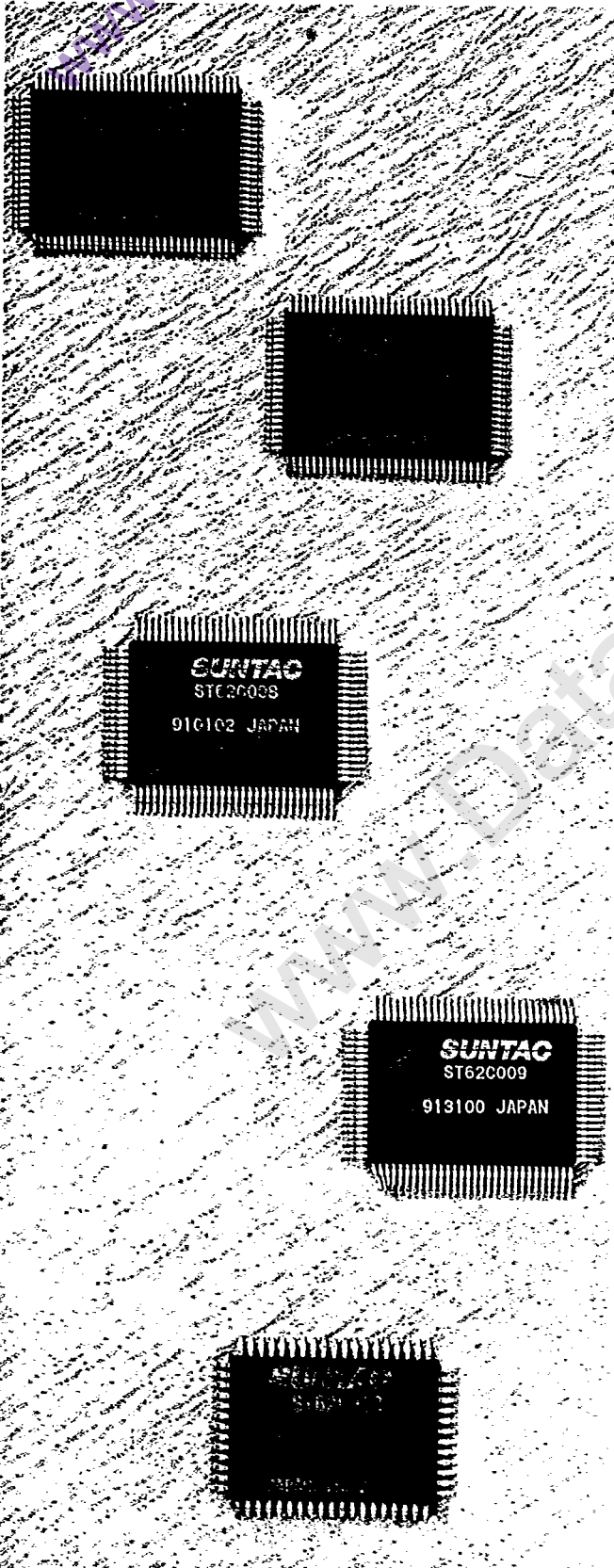




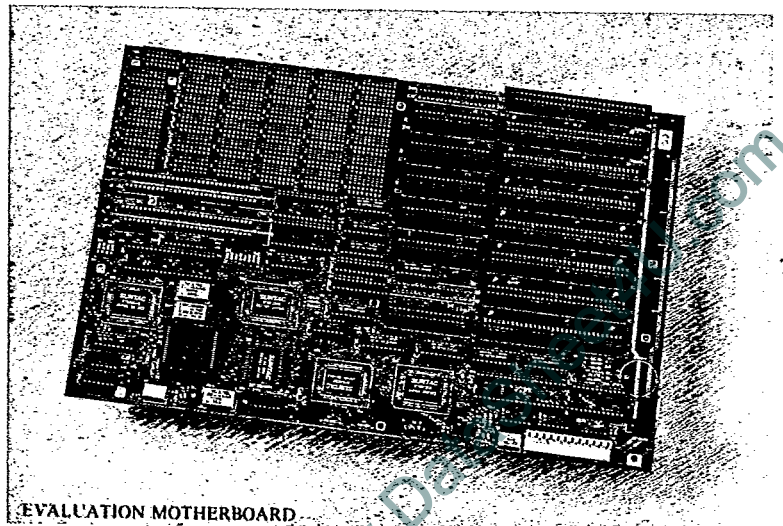
SUNTAC™

SUPER286

ST62CS20-B SUNTAC 62 CHIP SET



- Supports 16MHz and 20MHz operations
- 4-way page-interleaved memory operation; Supports up to 8MB onboard memory.
- 57 modes of memory mapping configuration.
- Supports DRAM access time ranging from 150ns to 70ns with 16 various timing combinations.
- Flexible and efficient shadow RAM implementation
- Supports LIM EMS 4.0 and EEMS (Enhanced EMS).
- Supports 8-bit/16-bit BIOS PROM.
- Synchronous and asynchronous AT bus clock options
- Register setting by either hardware switch or software setup without BIOS modification.
- Quick reset and gate A20 control for OS/2 optimization.



EVALUATION MOTHERBOARD

Above specification is subject change without notice



Modes of DRAM Access Time Selection

DRAM Access Time	System Speed			
	25MHz*	20MHz	16MHz	12MHz
150 ns	---	---	3	6
120ns	---	---	6	7
100 ns	---	4	7	1
80 ns	---	6	1	0
70 ns	4	7	1	0
60 ns	6	7	0	0
FP 120 ns**		3	6	1
FP 100 ns	2	4	7	1
FP 80ns	3	6	1	0

Average Wait State Reference Table*

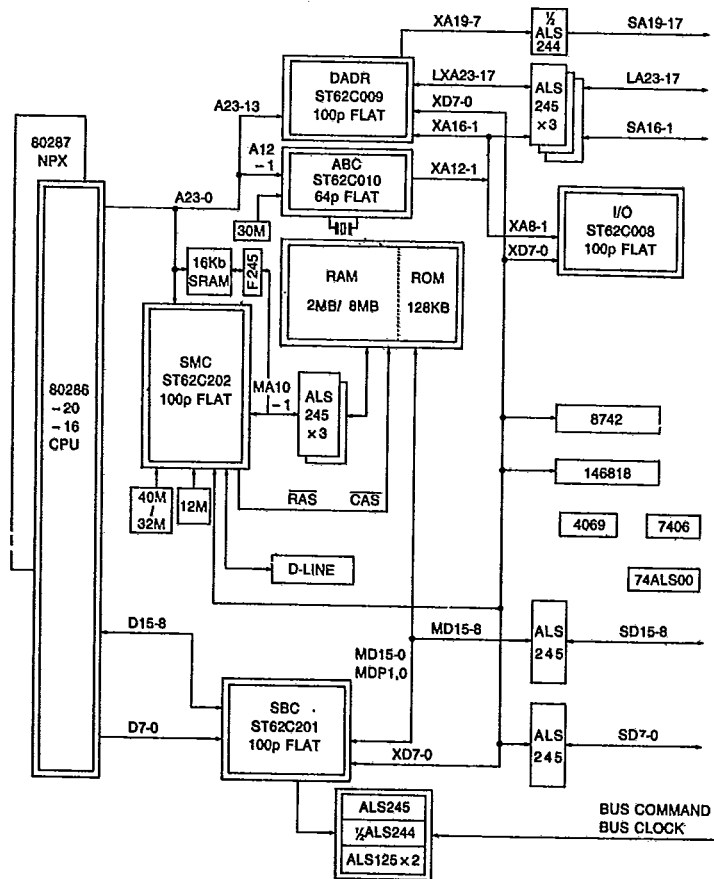
Mode Number	Interleave		
	No	2 Way	4Way
0	0.58	0.28	0.10
1	0.76	0.45	0.18
7	0.84	0.54	0.30
6 or 5	0.98	0.64	0.37
4	1.12	0.78	0.46
3	1.36	0.88	0.54
2	N/A	N/A	N/A

* For reference only.

** FP = Fast page mode

* All wait states are simulated results from Power Meter Aggregate System Test Program.

BLOCK DIAGRAM



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