Sitronix

ST7035

96 x 4 Dots Segment-type LCD Controller/Driver

1. INTRODUCTION

ST7035 is a LCD driver & controller LSI for graphic dot-matrix liquid crystal display systems. It contains 96 segment and 4 common driver circuits. ST7035 can be connected directly to a microprocessor with 3-Line serial peripheral interface (3-SPI) or I^2C compatible interface. Display data written by MPU is stored in an on-chip Display Data RAM (DDRAM) of 96 x 4 bits. ST7035 performs Display Data RAM write-operation without external clock to minimize power consumption. In addition, the built-in LED backlight control circuit can setup an LED backlight system with minimal components if necessary.

2. FEATURES

Single-chip LCD Controller & Driver

Driving Waveform

- A-Type & B-Type

Driver Output Circuits

- 4 common / 96 segment outputs

On-chip Display Data RAM

- Capacity: 96x4=384bits

Support Master/Slave to extend display area

Microprocessor Interface

- 3-Line (9-bits) SPI (serial peripheral interface)
- I^2C compatible interface

With External /RST (hardware reset) Pin

Built-in Oscillator requires no external component

Power Operating Voltage Range

- Digital Power (VDD1,VDD3): 3.0V~5.0V (TYP.)
- Analog Power (VDD2): 3.0V~5.0V (TYP.)

On-chip Low Power Analog Circuit

- Built-in Voltage Booster generates high voltage (x2~x4) (support external VLCD supply)
- Built-in Voltage Regulator generates LCD Vop (support external Vop supply)
- Built-in Voltage Follower generates LCD Bias voltages

LCD Driving Voltage Range

- Vop (V0-VSS2): 4V to 15V (Programmable)

Fast LCD Display Frame Frequency

- Maximum LCD frame frequency: 295Hz

Built-in LED Backlight Control Circuit

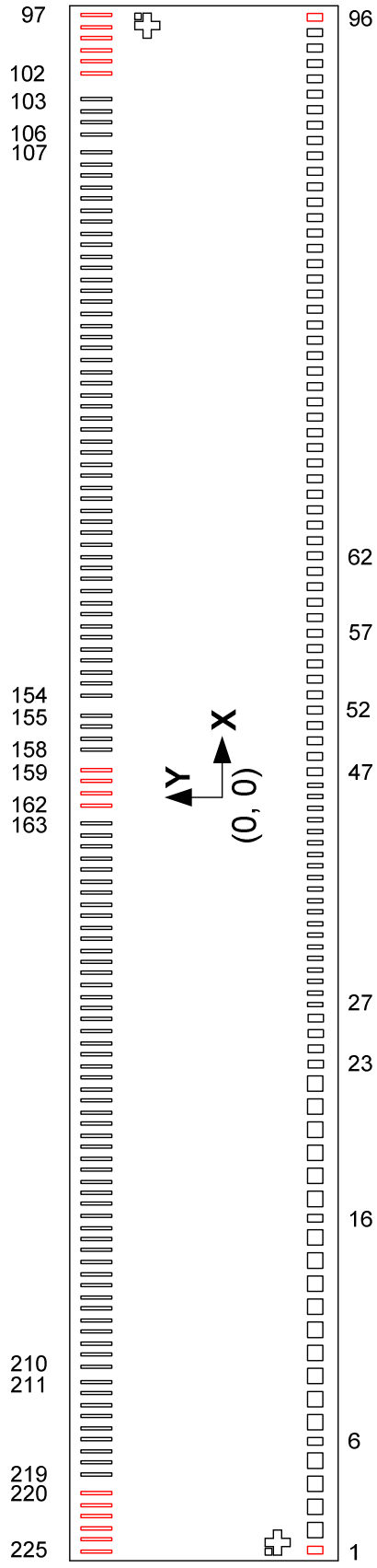
- PWM signal is synchronized with LCD frame
- Programmable PWM Frequency: 50~14.4K (Hz)

Operation Temperature: -40 ~80℃

Package Type: COG

ST7035	**3-Line Serial Interface**	ST
	I^2C Compatible Interface	I²C BUS

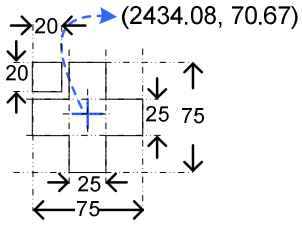
3. PACKAGE INFORMATION



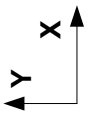
Chip Size	5380 x 904 um		
Chip Thickness	480 um	Bump Height	12um
PAD			**Pitch (min)**
2~5, 7~15, 17~22			80
1, 6, 16, 23~26, 47~96			50
27~46			40
97~101, 103~105, 107~153, 155~157, 159~161, 163~209, 211~218, 220~224			38
102, 106, 154, 210, 219			68
158, 162			98
PAD			**Size**
2~5, 7~15, 17~22			63 x 65
1, 6, 16, 23~26, 47~96			33 x 65
27~46			23 x 65
97~225			21 x 96

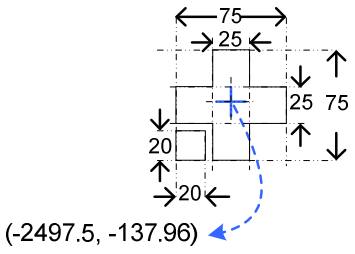
Note:

Please refer to the coordinates for the detailed information.



Unit: um





4. PIN FUNCTION

PAD NO.	PIN Name	X	Y
1	DUMMY	-2567	-329
2	SYNC	-2502	-329
3	DON	-2422	-329
4	CL	-2342	-329
5	LEDPWM	-2262	-329
6	VSS1	-2197	-329
7	TYPMD	-2132	-329
8	IF	-2052	-329
9	I2CMS0	-1972	-329
10	I2CMS1	-1892	-329
11	PRT0	-1812	-329
12	PRT1	-1732	-329
13	T0	-1652	-329
14	CLS	-1572	-329
15	M/S	-1492	-329
16	VDD1	-1427	-329
17	/RST	-1362	-329
18	/CS	-1282	-329
19	TCAP	-1202	-329
20	SCK	-1122	-329
21	SDA	-1042	-329
22	SDA	-962	-329
23	VD1	-897	-329
24	VD1	-847	-329
25	VD1OUT	-797	-329
26	VD1OUT	-747	-329
27	T18	-702	-329
28	T17	-662	-329
29	T16	-622	-329
30	T15	-582	-329
31	T14	-542	-329
32	TCOM0	-502	-329
33	T13	-462	-329
34	T12	-422	-329
35	T11	-382	-329
36	T10	-342	-329
37	T9	-302	-329
38	T8	-262	-329
39	T7	-222	-329
40	T6	-182	-329
41	TCOM1	-142	-329
42	T5	-102	-329
43	T4	-62	-329

PAD NO.	PIN Name	X	Y
44	T3	-22	-329
45	T2	18	-329
46	T1	58	-329
47	VDD2	103	-329
48	VDD2	153	-329
49	VDD2	203	-329
50	VDD2	253	-329
51	VDD1	303	-329
52	VDD1	353	-329
53	VDD1	403	-329
54	VDD1	453	-329
55	VDD3	503	-329
56	VDD3	553	-329
57	VSS3	603	-329
58	VSS3	653	-329
59	VSS1	703	-329
60	VSS1	753	-329
61	VSS1	803	-329
62	VSS1	853	-329
63	VSS2	903	-329
64	VSS2	953	-329
65	VSS2	1003	-329
66	VSS2	1053	-329
67	Reserved	1103	-329
68	V1	1153	-329
69	V1	1203	-329
70	V2	1253	-329
71	V2	1303	-329
72	V3	1353	-329
73	V3	1403	-329
74	V0IN	1453	-329
75	V0IN	1503	-329
76	V0IN	1553	-329
77	V0IN	1603	-329
78	V0OUT	1653	-329
79	V0OUT	1703	-329
80	CAP3P	1753	-329
81	CAP3P	1803	-329
82	CAP1N	1853	-329
83	CAP1N	1903	-329
84	CAP1P	1953	-329
85	CAP1P	2003	-329
86	CAP2P	2053	-329

PAD NO.	PIN Name	X	Y
87	CAP2P	2103	-329
88	CAP2N	2153	-329
89	CAP2N	2203	-329
90	VLCDOUT	2253	-329
91	VLCDOUT	2303	-329
92	VLCDIN	2353	-329
93	VLCDIN	2403	-329
94	VLCDIN	2453	-329
95	VLCDIN	2503	-329
96	DUMMY	2553	-329
97	DUMMY	2567	313
98	DUMMY	2529	313
99	DUMMY	2491	313
100	DUMMY	2453	313
101	DUMMY	2415	313
102	DUMMY	2377	313
103	COM0	2309	313
104	COM1	2271	313
105	COM2	2233	313
106	COM3	2195	313
107	SEG95	2127	313
108	SEG94	2089	313
109	SEG93	2051	313
110	SEG92	2013	313
111	SEG91	1975	313
112	SEG90	1937	313
113	SEG89	1899	313
114	SEG88	1861	313
115	SEG87	1823	313
116	SEG86	1785	313
117	SEG85	1747	313
118	SEG84	1709	313
119	SEG83	1671	313
120	SEG82	1633	313
121	SEG81	1595	313
122	SEG80	1557	313
123	SEG79	1519	313
124	SEG78	1481	313
125	SEG77	1443	313
126	SEG76	1405	313
127	SEG75	1367	313
128	SEG74	1329	313
129	SEG73	1291	313
130	SEG72	1253	313
131	SEG71	1215	313

PAD NO.	PIN Name	X	Y
132	SEG70	1177	313
133	SEG69	1139	313
134	SEG68	1101	313
135	SEG67	1063	313
136	SEG66	1025	313
137	SEG65	987	313
138	SEG64	949	313
139	SEG63	911	313
140	SEG62	873	313
141	SEG61	835	313
142	SEG60	797	313
143	SEG59	759	313
144	SEG58	721	313
145	SEG57	683	313
146	SEG56	645	313
147	SEG55	607	313
148	SEG54	569	313
149	SEG53	531	313
150	SEG52	493	313
151	SEG51	455	313
152	SEG50	417	313
153	SEG49	379	313
154	SEG48	341	313
155	COM3	273	313
156	COM2	235	313
157	COM1	197	313
158	COM0	159	313
159	DUMMY	61	313
160	DUMMY	23	313
161	DUMMY	-15	313
162	DUMMY	-53	313
163	SEG47	-151	313
164	SEG46	-189	313
165	SEG45	-227	313
166	SEG44	-265	313
167	SEG43	-303	313
168	SEG42	-341	313
169	SEG41	-379	313
170	SEG40	-417	313
171	SEG39	-455	313
172	SEG38	-493	313
173	SEG37	-531	313
174	SEG36	-569	313
175	SEG35	-607	313
176	SEG34	-645	313

PAD NO.	PIN Name	X	Y
177	SEG33	-683	313
178	SEG32	-721	313
179	SEG31	-759	313
180	SEG30	-797	313
181	SEG29	-835	313
182	SEG28	-873	313
183	SEG27	-911	313
184	SEG26	-949	313
185	SEG25	-987	313
186	SEG24	-1025	313
187	SEG23	-1063	313
188	SEG22	-1101	313
189	SEG21	-1139	313
190	SEG20	-1177	313
191	SEG19	-1215	313
192	SEG18	-1253	313
193	SEG17	-1291	313
194	SEG16	-1329	313
195	SEG15	-1367	313
196	SEG14	-1405	313
197	SEG13	-1443	313
198	SEG12	-1481	313
199	SEG11	-1519	313
200	SEG10	-1557	313
201	SEG9	-1595	313
202	SEG8	-1633	313
203	SEG7	-1671	313
204	SEG6	-1709	313
205	SEG5	-1747	313
206	SEG4	-1785	313
207	SEG3	-1823	313
208	SEG2	-1861	313
209	SEG1	-1899	313
210	SEG0	-1937	313
211	Reserved	-2005	313
212	Reserved	-2043	313
213	Reserved	-2081	313
214	Reserved	-2119	313
215	Reserved	-2157	313
216	COM3	-2195	313
217	COM2	-2233	313
218	COM1	-2271	313
219	COM0	-2309	313
220	DUMMY	-2377	313
221	DUMMY	-2415	313
222	DUMMY	-2453	313
223	DUMMY	-2491	313
224	DUMMY	-2529	313
225	DUMMY	-2567	313

Unit: um

5. BLOCK DIAGRAM

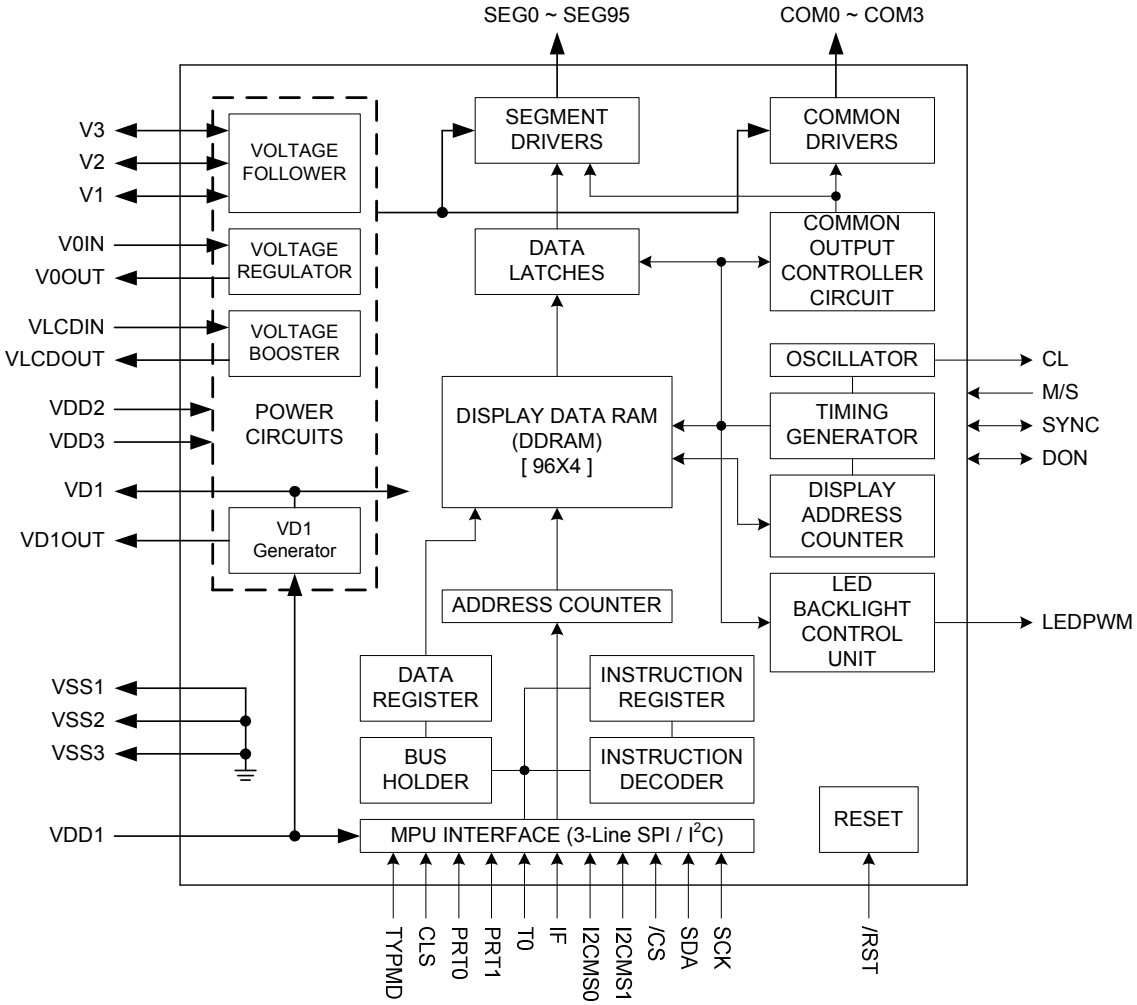


Fig. 1

6. PIN DESCRIPTION

MICROPROCESSOR INTERFACE PINS

<table>
<tr><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td>/CS</td><td>Input</td><td>Chip select input pin.
When using 3-Line serial interface, SDA & SCK pins are enabled only when /CS is "L".
When use I^{2}C interface. /CS pin is unused, please fix to “H” or “L”.</td></tr>
<tr><td>/RST</td><td>Input</td><td>Reset input pin.
When /RST is "L", initialization is executed.</td></tr>
<tr><td>SDA</td><td>I/O</td><td>For 3-Line serial interface mode: serial data input and output.
For I^{2}C compatible interface: this pin is serial data input and ACK signal output.
Note: SDA 2 pins should be connected together.</td></tr>
<tr><td>SCK</td><td>Input</td><td>Serial clock input.</td></tr>
<tr><td>IF</td><td>Input</td><td>Interface type select input:
<table>
<tr><th>IF</th><th>MPU Interface Type</th></tr>
<tr><td>L</td><td>I^{2}C Interface</td></tr>
<tr><td>H</td><td>3-Line SPI (9-bit serial)</td></tr>
</table></td></tr>
<tr><td>I2CMS0
I2CMS1</td><td>Input</td><td>Select pin of I^{2}C interface slave address:
<table>
<tr><th>I2CMS1</th><th>I2CMS0</th><th>I2C Address</th></tr>
<tr><td>0</td><td>0</td><td>0111000</td></tr>
<tr><td>0</td><td>1</td><td>0111001</td></tr>
<tr><td>1</td><td>0</td><td>0111010</td></tr>
<tr><td>1</td><td>1</td><td>0111011</td></tr>
</table></td></tr>
<tr><td>TYPMD</td><td>Input</td><td>Select pin of driving waveform:
<table>
<tr><th>TYPMD</th><th>LCD Drive Waveform</th></tr>
<tr><td>L</td><td>B-Type</td></tr>
<tr><td>H</td><td>A-Type</td></tr>
</table></td></tr>
</table>

LCD DRIVER PINS

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>SEG0 ~ SEG95</td><td>Output</td><td>These pins are LCD driver segment outputs.
The display data and internal frame signal control the output voltage of segment driver.
<table>
<tr><th>Frame</th><th colspan="2">Negative Frame</th><th colspan="2">Posistive Frame</th></tr>
<tr><th>Display Data</th><th>ON</th><th>OFF</th><th>ON</th><th>OFF</th></tr>
<tr><td>1/4 Bias</td><td>V0</td><td>V2</td><td>VSS</td><td>V2</td></tr>
<tr><td>1/3 Bias</td><td>V0</td><td>V2</td><td>VSS</td><td>V1</td></tr>
<tr><td>1/2 Bias</td><td>V0</td><td>VSS</td><td>VSS</td><td>V0</td></tr>
</table></td></tr>
<tr><td>COM0 ~ COM3</td><td>Output</td><td>These pins are LCD driver common outputs.
The internal scan data and frame signal control the output voltage of common driver.
<table>
<tr><th>Frame</th><th colspan="2">Negative Frame</th><th colspan="2">Posistive Frame</th></tr>
<tr><th>Scan Data</th><th>ON</th><th>OFF</th><th>ON</th><th>OFF</th></tr>
<tr><td>1/4 Bias</td><td>VSS</td><td>V1</td><td>V0</td><td>V3</td></tr>
<tr><td>1/3 Bias</td><td>VSS</td><td>V1</td><td>V0</td><td>V2</td></tr>
<tr><td>1/2 Bias</td><td>VSS</td><td>V1</td><td>V0</td><td>V1</td></tr>
</table></td></tr>
<tr><td>PRT1
PRT0</td><td>Input</td><td>Select pin of display duty option:
<table>
<tr><th>PRT1</th><th>PRT0</th><th>Duty</th></tr>
<tr><td>0</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>1/2</td></tr>
<tr><td>1</td><td>0</td><td>1/3</td></tr>
<tr><td>1</td><td>1</td><td>1/4</td></tr>
</table></td></tr>
</table>

LCD POWER SUPPLY PINS

<table>
<tr><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td>VLCDIN
VLCDOUT</td><td>Power</td><td>When using internal Voltage Booster, VLCDIN & VLCDOUT should be connected together and then connect it with a capacitor to VSS2.
When using external booster, please apply the external high voltage power to VLCDIN. In this case, VLCDIN & VLCDOUT should be connected together FPC or PCB and then connect it with a capacitor to VSS2.</td></tr>
<tr><td>V0IN
V0OUT
V1
V2
V3</td><td>Power</td><td>LCD driver supply voltages.
V0IN is the V0 supply of LCD drivers.
V0OUT is the output voltage of V0 generated by ST7035.
When the internal power circuits are turned ON, these voltages are generated and the relations are listed in the following table.
Please connect V0IN and V0OUT together by FPC or PCB and then connect it with a capacitor to VSS2.
<table>
<tr><th>Bias Setting</th><th>V0</th><th>V1</th><th>V2</th><th>V3</th><th>VSS</th></tr>
<tr><td>1/2</td><td>V0</td><td>1/2*V0</td><td>1/2*V0</td><td>1/2*V0</td><td>VSS</td></tr>
<tr><td>1/3</td><td>V0</td><td>2/3*V0</td><td>1/3*V0</td><td>1/3*V0</td><td>VSS</td></tr>
<tr><td>1/4</td><td>V0</td><td>3/4*V0</td><td>2/4*V0</td><td>1/4*V0</td><td>VSS</td></tr>
</table></td></tr>
<tr><td>CAP1N</td><td>Power</td><td>DC/DC voltage converter.
Connect a non-polar capacitor between this terminal and the CAP1P, CAP3P terminal.</td></tr>
<tr><td>CAP2N</td><td>Power</td><td>DC/DC voltage converter.
Connect a non-polar capacitor between this terminal and the CAP2P terminal.</td></tr>
<tr><td>CAP1P</td><td>Power</td><td>DC/DC voltage converter for LCD circuit.
Connect a non-polar capacitor between this terminal and the CAP1N terminal.</td></tr>
<tr><td>CAP2P</td><td>Power</td><td>DC/DC voltage converter.
Connect a non-polar capacitor between this terminal and the CAP2N terminal.</td></tr>
<tr><td>CAP3P</td><td>Power</td><td>DC/DC voltage converter for LCD circuit.
Connect a non-polar capacitor between this terminal and the CAP1N terminal.</td></tr>
</table>

Note : Booster is controlled by CAPs, please refer to Page 3.

POWER SUPPLY PINS

Pin Name	Type	Description
VDD1	**Power**	VDD1 is the power of Interface I/O circuit and OSC circuit. VDD1 and VDD3 are separated in ITO and connected together by FPC or PCB.
VDD2	**Power**	VDD2 is the analog power for booster circuit and OP.
VDD3	**Power**	VDD3 is the power of VREF circuit. VDD1 and VDD3 are separated in ITO and connected together by FPC or PCB.
VSS1	**Power**	Ground of interface, logic and OSC circuit. Ground system should be connected by FPC or PCB.
VSS2	**Power**	Ground of booster circuit and OP. Ground system should be connected by FPC or PCB.
VSS3	**Power**	Ground of VREF circuit. Ground system should be connected by FPC or PCB.
VD1 VD1OUT	**Power**	VD1 is the power source of digital circuit. VD1OUT is the VD1 output. VD1 and VD1OUT should be connected together by FPC or PCB.

MASTER/SLAVE CONTROL PINS

<table>
<tr><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td>M/S</td><td>Input</td><td>Select Master/Slave mode pin.
<table>
<tr><th>M/S</th><th>Mode</th></tr>
<tr><td>0</td><td>Slave</td></tr>
<tr><td>1</td><td>Master</td></tr>
</table></td></tr>
<tr><td>CLS</td><td>Input</td><td>Select pin of clock external or Internal:
<table>
<tr><th>CLS</th><th>CLOCK</th></tr>
<tr><td>0</td><td>External</td></tr>
<tr><td>1</td><td>Internal</td></tr>
</table></td></tr>
<tr><td>CL</td><td>I/O</td><td>When using Master/Slave mode. All of CL should be connected.
Please note only when M/S & CLS are both “H”, CL can be set to Output PWM Clock.
<table>
<tr><th>M/S</th><th>CLS</th><th>CL</th><th>DON</th><th>SYNC</th></tr>
<tr><td>0</td><td>0</td><td>Clock Input</td><td>Input</td><td>Input</td></tr>
<tr><td>0</td><td>1</td><td>Clock Input</td><td>Input</td><td>Input</td></tr>
<tr><td>1</td><td>0</td><td>Clock Input</td><td>Output</td><td>Output</td></tr>
<tr><td>1</td><td>1</td><td>Clock Output</td><td>Output</td><td>Output</td></tr>
</table></td></tr>
<tr><td>SYNC</td><td>I/O</td><td>When using Master/Slave mode. All of SYNC should be connected.
If not, this pin should be open.</td></tr>
<tr><td>DON</td><td>I/O</td><td>When using Master/Slave mode. All of DON should be connected.
If not, this pin should be floating.</td></tr>
</table>

LED BACKLIGHT CONTROL PIN

Pin Name	Type	Description
LEDPWM	**Output**	LED backlight control pin. This pin controls signals, not LED power pin. .

*Please refer to the “LED Backlight connection” section for the LED backlight control application notes.

TEST PIN

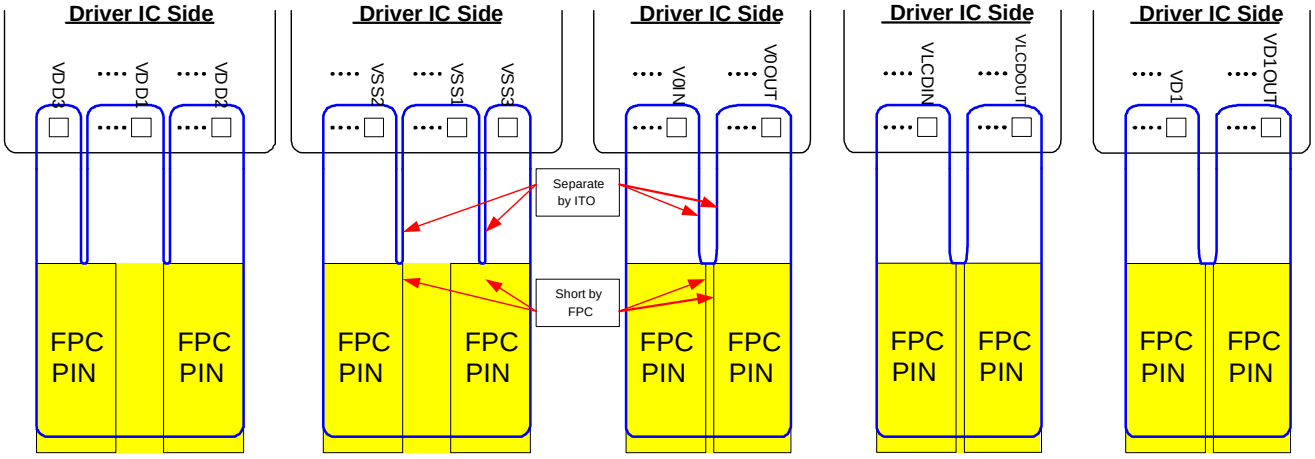
Pin Name	Type	Description
DUMMY	-	Dummy pins. Keep open.
T0	-	Connect to VSS
Vref	-	Test pin. Keep open.
T1~T18	-	Test pins. Keep open.
TCAP	-	Test pin. Keep open.
TCOM0 TCOM1	-	Test pins. Keep open.
Reserved	-	Keep open.

ITO RESISTANCE (for COG application)

Pin Name	ITO Resistance
DUMMY T1~T18, TCAP, TCOM0, TCOM1, Vref	Floating
VDD1, VDD2, VDD3, VD1, VD1OUT, VLCDIN, VLCDOUT, VSS1, VSS2, VSS3	< 100Ω
CAP1P, CAP1N, CAP2P, CAP2N,CAP3P, V3,V2, V1,V0IN,V0OUT	< 150Ω
/CS, LEDPWM, SDA, SCK	< 1KΩ
SYNC, DON, CL	< 3KΩ
M/S, IF, CLS, I2CMS0, I2CMS1, PRT0, PRT1, T0, TYPMD, /RST	< 5KΩ

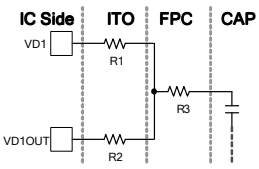
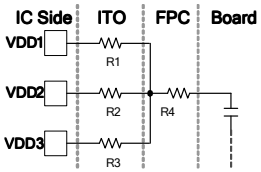
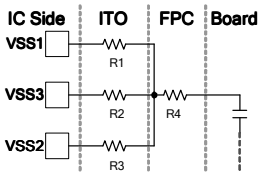
Note:

1. The Limitations include the bottleneck of ITO layout.
2. Make sure that the ITO resistance of COM0 ~ COM8 is equal, and so is it of SEG0 ~ SEG95.
3. To avoid the noise in different power systems affect other power system, please separate them on ITO layout.
4. The V0, VLCD and VD1 power circuits have output pins and input pins. To avoid the power noise affects the sensor of the power circuits. The trace should be separated by ITO and should be connected together by FPC.



5. If panel layout cannot meet recommended ITO resistance and traces must be connected on ITO to lower the resistance, below layout rule must be followed.

The equivalent circuit is shown below:

VD1 & VD1OUT	VDD	VSS
		
Ideal Layout: => R3=0 Ohm. R1>R2. **Acceptable Layout:** => R3≠0. R1≥R2 >R3. **Not Acceptable:** => R3 ≥ (R1 or R2)	**Ideal Layout:** =>R4=0Ohm. R3>>R1>R2. **Acceptable Layout:** =>R4≠0. R3>>R1>R2>R4. **Not Acceptable:** =>R4≥(R1or R2or R3).	**Ideal Layout:** =>R4=0Ohm. R2>>R1>R3. **Acceptable Layout:** =>R4≠0. R2>>R1>R3>R4. **Not Acceptable:** =>R4≥(R1or R2 or R3).

7. FUNCTIONS DESCRIPTION

MICROPROCESSOR INTERFACE

The microprocessor interface of ST7035 can be selected by IF pin to communicate with different type of MPU. Please refer to the table below:

IF Setting	Interface Mode	Available Pins for MPU
H	3-Line SPI (Serial Peripheral Interface)	SDA, SCK, /CS, /RST
L	I^2C compatible interface	SDA, SCK, /RST

3-Line SPI Interface (9-bit)

The 3-Line SPI (9-bit) uses 3 pins (/CS, SDA & SCK) to communicate with MPU. When /CS is "L", IC is active and the SDA and SCK pins are enabled. Serial data is latched at the rising edge of serial clock. The internal shift register collects serial bits and reformat them into 8-bit data after the last (9^{th}) clock. After /CS returns to "H", IC is inactive and the internal shift register and counter are reset. The parameter/command indicator is the "A0" bit: the 1^{st} bit of each 9-bit serial data.

Write Parameter by 3-Line SPI (A0=1)

When A0 is "1", the transferred 8-bit is parameter.

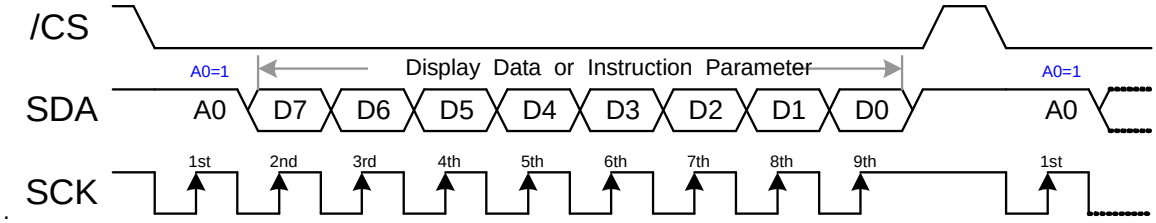


Fig. 2 Write Parameter in 3-Line SPI

Write Instruction by 3-Line SPI (A0=0)

When A0 is "0", the transferred 8-bit is instruction.

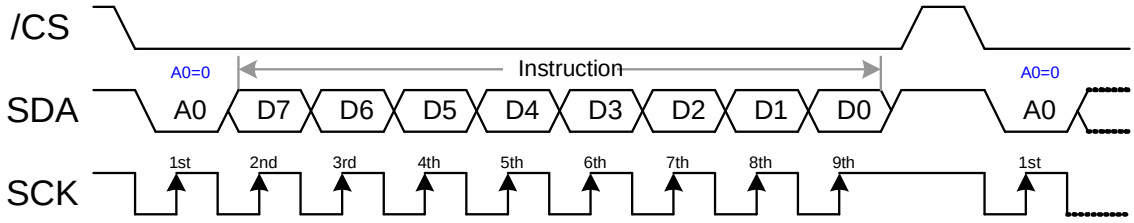


Fig. 3 Write Instruction in 3-Line SPI

I²C Compatible Interface

The I²C Compatible Interface is for bi-directional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines must be connected with a pull-up resistor which drives SDA and SCL to high when the bus is not busy. Data transfer can be initiated only when the bus is not busy.

BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes of SDA line at this time will be interpreted as START or STOP. Bit transfer is illustrated in Fig. 4.

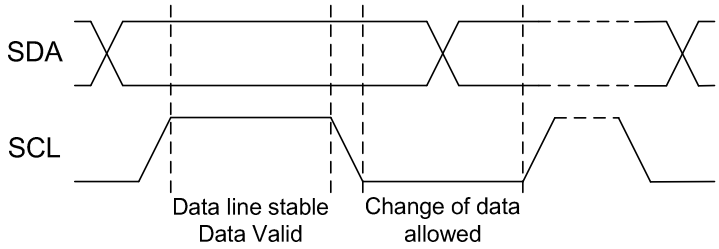


Fig. 4 Bit Transfer

START AND STOP CONDITIONS

Both SDA and SCL lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of SDA while SCL is HIGH, is defined as the START condition (S). A LOW-to-HIGH transition of SDA while SCL is HIGH, is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig. 5.

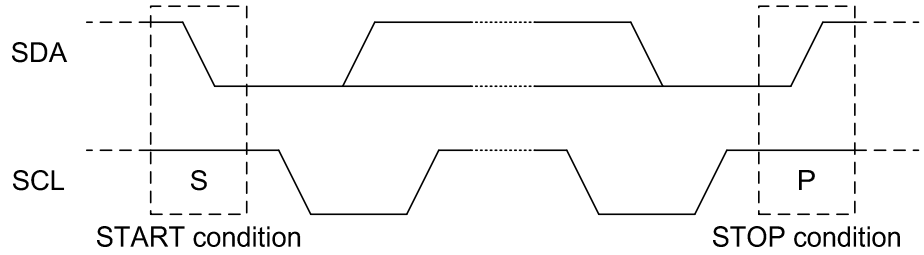


Fig. 5 Definition of START and STOP Condition

SYSTEM CONFIGURATION

The system configuration is illustrated in Fig. 6. Word-definitions are explained below:

- Transmitter: the device which sends the data to the bus.
- Receiver: the device which receives the data from the bus.
- Master: the device which initiates a transfer, generates clock signals and terminates a transfer.
- Slave: the device which is addressed by a master.

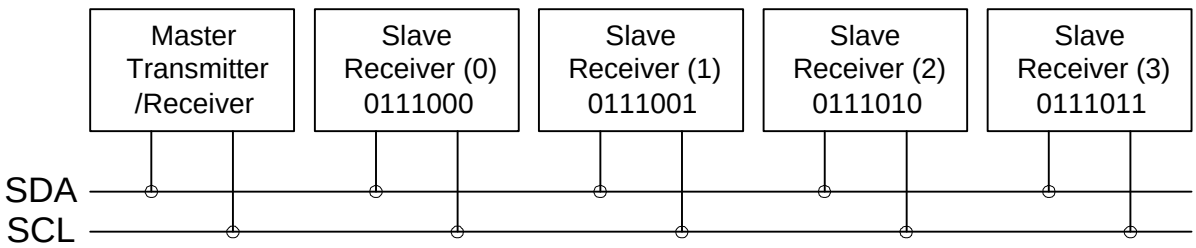


Fig. 6 System Configuration

ACKNOWLEDGEMENT

Each byte of eight bits is followed by an acknowledge-bit. The acknowledge-bit is a HIGH signal put on SDA by the transmitter when the master generates an extra acknowledge-related clock pulse. A slave receiver addressed must generate an acknowledge-bit after the reception of each byte. The device that acknowledges must pull-down the SDA line during the acknowledge-clock pulse, so that the SDA line stays LOW during the HIGH period of the acknowledge-related clock pulse (set-up and hold times must be taken into consideration). Acknowledgement on the I^2C Interface is illustrated in Fig. 7.

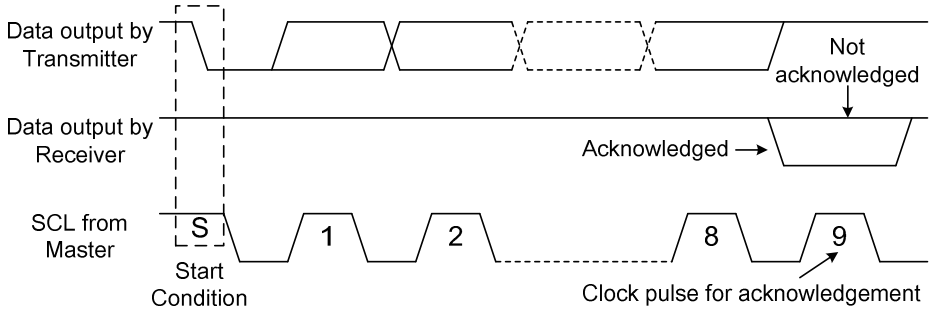


Fig. 7 Acknowledgement of I^2C Interface

I²C INTERFACE PROTOCOL

ST7035 supports command/data write to addressed slaves on the bus.

Before any data is transmitted on the I²C Interface, the device which should respond is addressed first. For 7-bit slave addresses (0111**00**, 0111**01**, 0111**10** and 0111**11**) are reserved for ST7035. The least significant 2 bits of the slave address is set by connecting I2CMS0 and I2CMS1 to either logic 0 (VSS1) or logic 1 (VDD1).

The I²C Interface protocol is illustrated in Fig. 8.

The sequence is initiated with a START condition (S) from the I²C Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C Interface transfer. After acknowledgement, one or more command are followed and the status of the addressed slaves is defined. A command word consists of a control byte, which defines Co and A0, and a data byte.

The last control byte is tagged with a cleared bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data byte(s) will follow. The state of the A0 bit defines whether the following data bytes are interpreted as commands or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte, either a series of display data bytes or command data bytes may follow (depending on the A0 bit setting).

If the A0 bit of the last control byte is set to logic 1, these data bytes (display data bytes) will be stored in the display RAM at the address specified by the internal data pointer. The data pointer is automatically updated and the data is directed to the intended ST7035 device.

If the A0 bit of the last control byte is set to logic 0, these data bytes (command data byte) will be decoded and the setting of ST7035 will be changed according to the received commands.

Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the bus master issues a STOP condition (P). If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

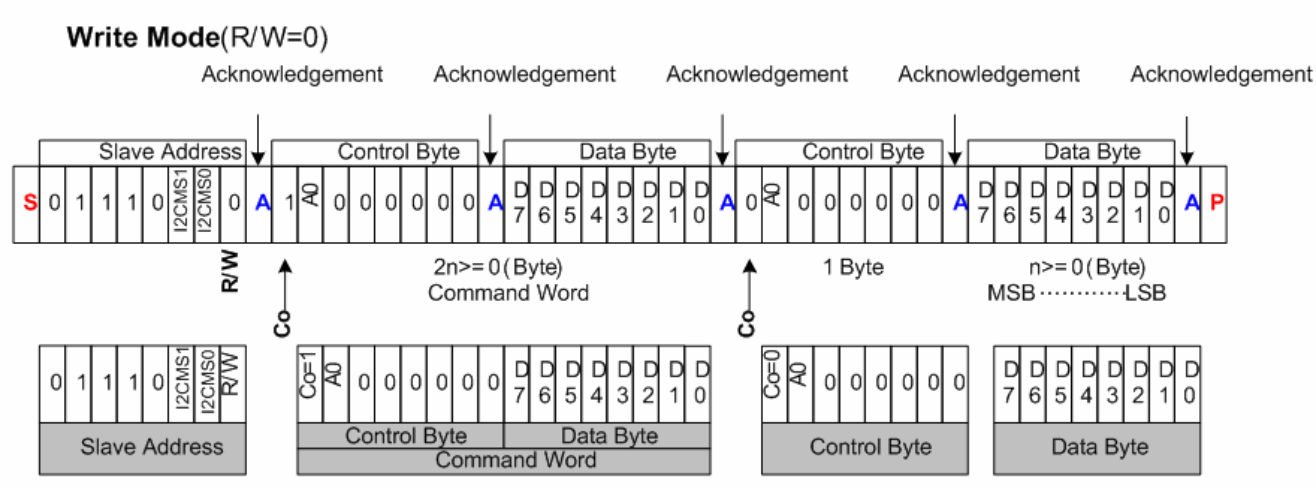


Fig. 8 I²C Interface Protocol

Co	0	Last control byte. Only a stream of data bytes is allowed to follow. This stream may only be terminated by a STOP or RE-START condition.
	1	Another control byte will follow the data byte.

MASTER/SLAVE Application

When ST7035 set in I^2C interface, ST7035 supports maximum 4 ICs to drive display. By setting “I2CMS0” & “I2CMS1”, ST7035 would choose master or slave type. There are three modes in master/slave application.

Enhance Mode

By using 2~4 ST7035 and link Com0~Com3 from left-side and right-side of the display together can enhance driving ability to drive a large display resolution. Row data are controlled by left-side and right-side ST7035 as show in 9 In this mode, ST7035 support to 4 x 384 dots.

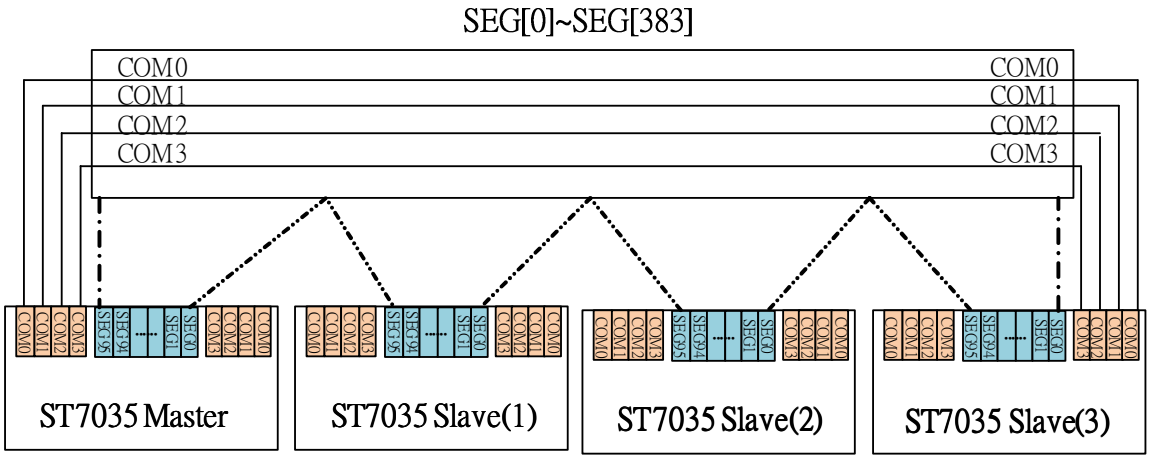


Fig. 9 Enhance Mode

Master/Slave Mode

For Master/ Slave mode, please using 2~4 ST7035 and link Com0 & Com1 from left-side of display and link Com2 & Com3 form right-side of display. Com 0 & Com1 are controlled by left-side ST7035, Com2 & Com3 are controlled by right-side ST7035 as show in 10. In this mode, ST7035 supports to 4 x 384 dots.

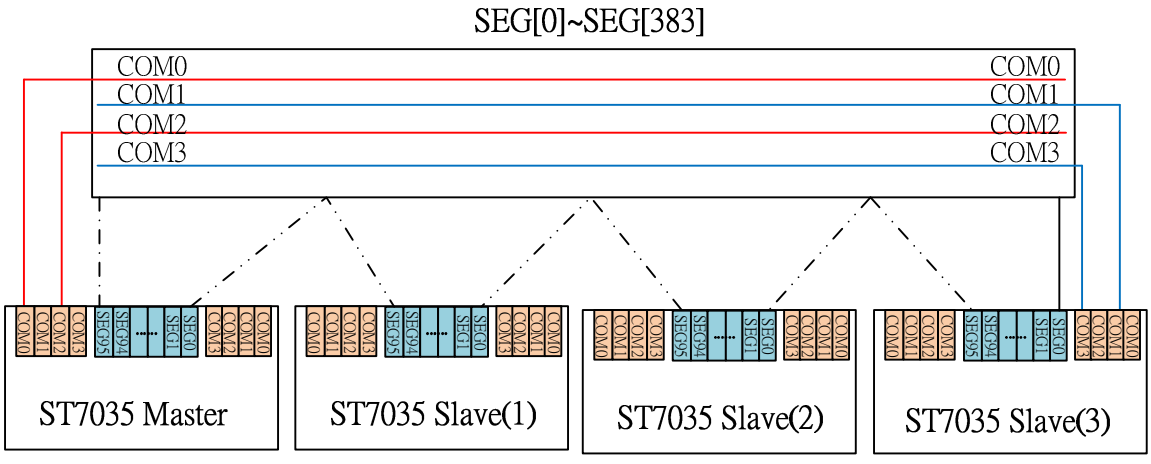


Fig. 10 Master/Slave Mode

Extend Mode

In Extend mode, ST7035 can supports the largest display resolution to 4 x 384 dots by I^2C interface. When using extend mode, all of the com signals are controlled by the left-side ST7035 as show in 11.

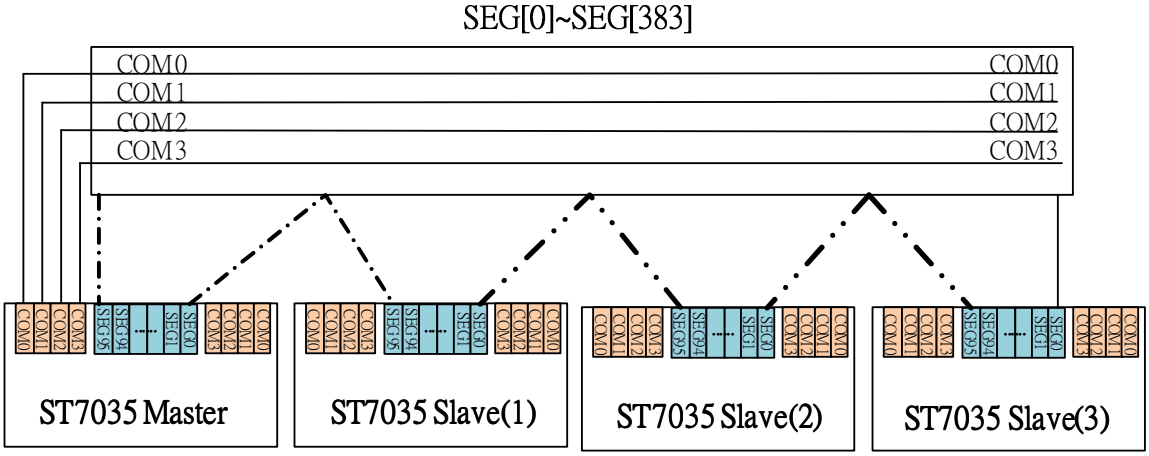


Fig. 11 Extend Mode

DISPLAY DATA RAM (DDRAM)

ST7035 contains a 96x4 bit static RAM which stores the display data (the Display Data RAM, DDRAM). It stores the dot-matrix data for the LCD. DDRAM is a 4-row by 96-column addressable array and there is a direct correspondence between X-address and column output number. Each pixel can be selected when the row and column addresses are specified. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

Data Format & DDRAM Structure

The display data is written through D0 to D7.

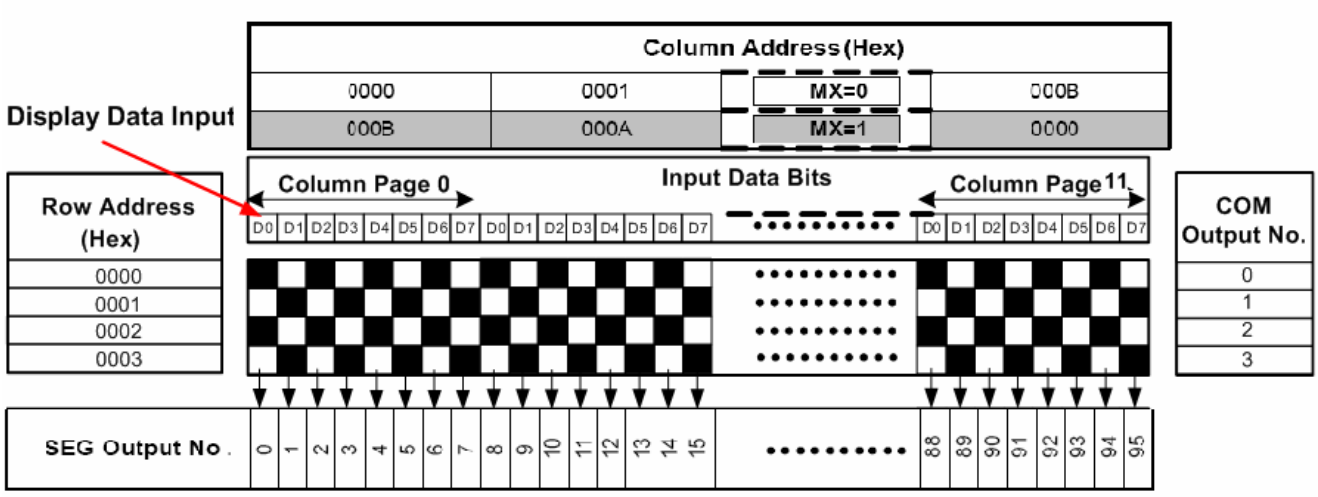


Fig. 12 Data Format and DDRAM Structure

Sometimes, a mirrored DDRAM map is easier for manual data mapping.

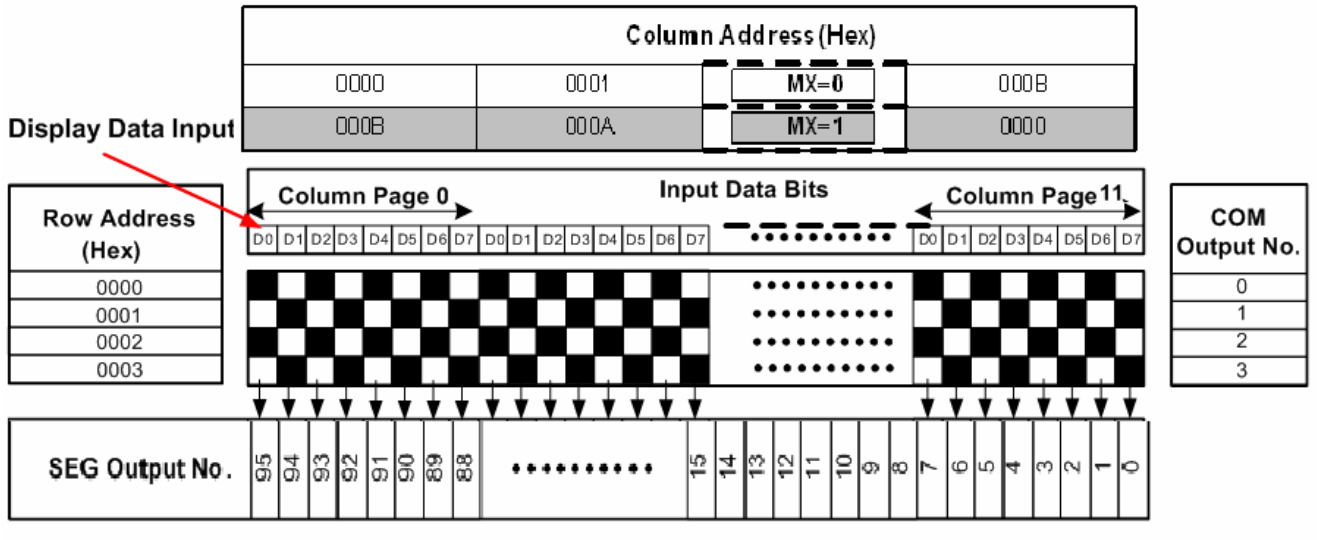


Fig. 13 Transferred DDRAM Map

Row Address Circuit

Row address circuit has a 4-bit present counter which points to the current row address of DDRAM. The row address can be specified by the Row Address Set command.

Column Address Circuit

The internal column address circuit has a 4-bit preset counter which points to the current column address of DDRAM. A column address mapping to a “column page” send 8-bits data information to DDRAM. ST7035 has 12 column pages and the column address is from 0x00 to 0x0B. The column addresses can be specified by the Column Address Set command.

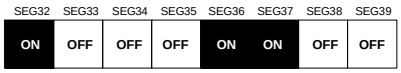
DDRAM Addressing

In order to speed up the throughput of sequential display data transfer, the column address will be increased by 1 automatically after updating 8-bit data. In this way, the Host doesn’t have to set column/page address for each data transfer. The column address will be incremented (+1) after receiving each byte of display data. This allows MPU accessing display data continuously. When the column address points to the last column address (0x0B), the next DDRAM access will let the column address return to 0 and the row address will be increased by 1 (points to the next row). If the row address is also the last row (0x08), both of the column address and the row address are returned to 0.

The following example illustrates how to write display data into DDRAM (the pattern is shown in the figure below):

```
Write_command(0x2A);    // Column address set
Write_data(0x05);       // set start address at 5 (for SEG32 and SEG39)
Write_data(0x0B);       // set end address at 11 (for SEG88 and SEG95)
Write_command(0x2C);    // Memory write
Write_data(0x31);       // SEG32, 36, 37 = ON , SEG33, 34, 35, 38, 39 = OFF
```

DDRAM write result:



INTERNAL LCD POWER CIRCUITS

The following figure illustrates the external connection when using internal LCD power circuits. The internal voltage booster can be connected as x2 ~ x4 voltage booster.

Note:

1. The maximum VLCD voltage is 16.5V.
2. Booster is only produced by external connection of capacitances.

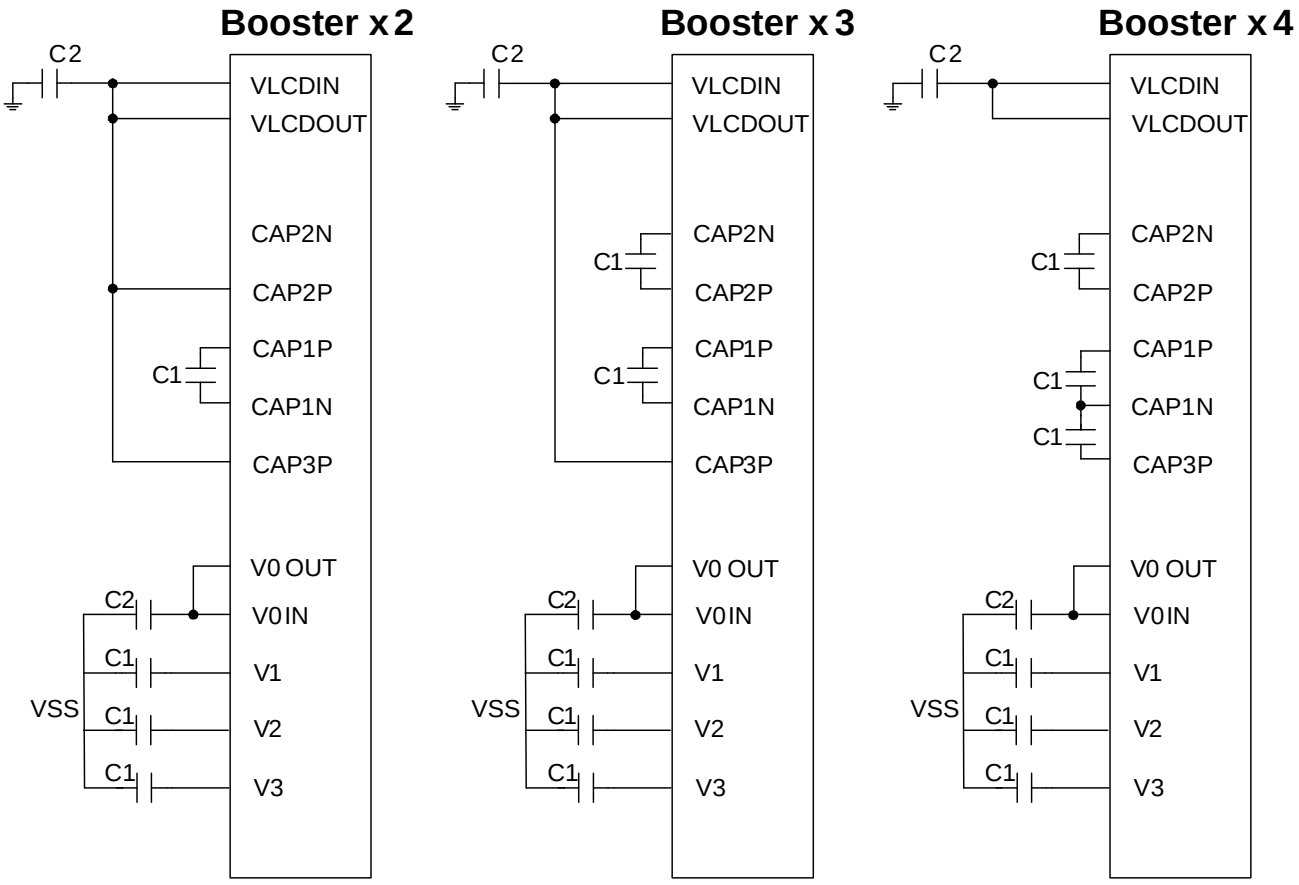
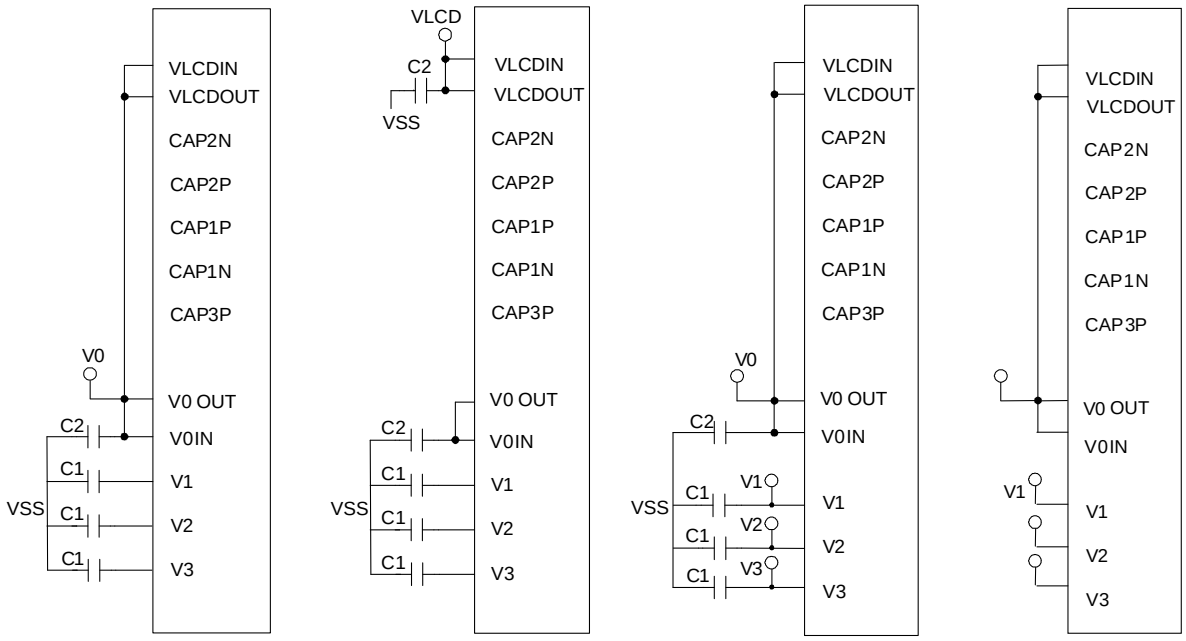


Fig. 14 External Connection for Internal Power Circuits

For external power system, some typical applications are shown below:

Case 1: External Regulator **Case 2: External Booster** **Case 3: All External Powers** **Case 4: All External Powers (No External Capacitor)**



External: V0 Internal: V1, V2 & V3 * Bias control can be used.	External: VLCD Internal: V0, V1, V2, & V3 * V0 control TC & Bias can be used.	External: V0, V1, V2 & V3 Internal: None * Adjust all power circuits externally.	External: V0, V1, V2 & V3 Internal: None * Adjust all power circuits externally. * If the external power is stable enough, It could have no any external capacitors.

Fig. 15 External Connection for External Power Circuits

External Components of Power Circuit

The optimum values of C1 and C2 depend on the loading of LCD panel. The value should be determined by customer. When determining the capacitor value, customer can display a pattern with large loading and than check if the capacitor makes the voltage stable or not. The following table is a quick reference for the initial setting.

Symbol	Reference Value (uF)
C1	1 uF / 25V
C2	1 uF / 25V

Note:

1. Please place all these capacitors close to the related pin of IC.
2. If the LCD panel is large or the ITO resistance is not good, the capacitor value maybe larger than the reference value. If the value is more than 10uF, customer should consider the following suggestion.
3. When the LCD panel size is large and desired display quality is unavailable by increasing the value of capacitor, it is recommended to use the external power system.

INTERNAL LED BACKLIGHT CONTROL CIRCUIT

LED Power Switch Pin (LEDPWM)

The built-in LED Backlight Control Circuit generates PWM signal (LEDPWM pin) to control the external LED backlight power circuit (such as VLED booster or VLED power switch).

Please note this pin can not be used to drive LED backlight directly, it is used to switch the external LED backlight power circuit ON/OFF.

LED PWM Field

In order to achieve the smooth LED backlight control, there are 4 kinds of LED PWM cycles can be chosen. LED PWM cycles could be 1,2,4,8. LED PWM cycles sync with system clock, that means LED PWM cycles occur during COM is triggered. The PWM High/Low ratio is based on the value of LEDRT[7:0], LEDRT[7:0] set the number of “High” cycles in one PWM period. The definition of a frame is defined as the following figure.

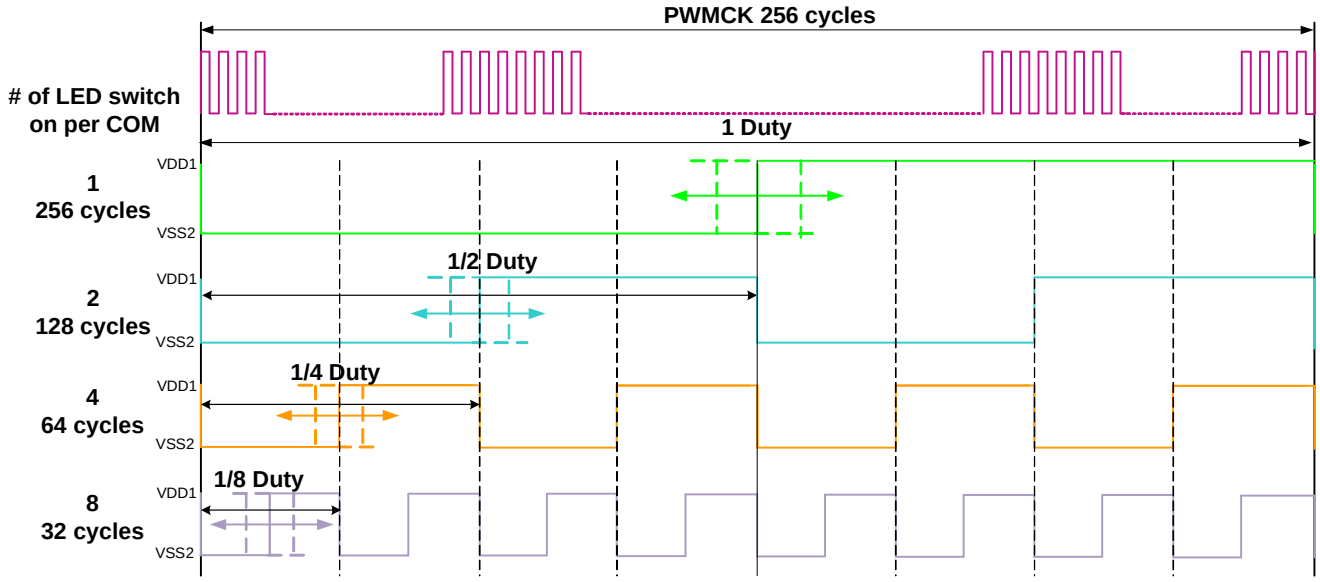


Fig. 16 LED PWM cycles

# of PWM cycles in one COM	Legal LEDRT bits	PWMCK counting # in one PWM period	LEDRT usable range
1	LEDRT[7:0]	256	0~255
2	LEDRT[6:0]	128	0~127
4	LEDRT[5:0]	64	0~63
8	LEDRT[4:0]	32	0~31

LED Backlight connection

Dependent on different LED backlight circuit, there are two methods to control LED backlight by LEDPWM pin. When LED backlight circuit is parallel connection, LEDPWM connects to a MOS and output High/Low signal to control the LED backlight. When LED backlight circuit is series connection, LEDPWM need to control backlight ON/OFF by a Boost IC. Fig. 7 shows the LEDPWM application circuit for parallel LED connection. Fig. 18 shows the suggestion of LEDPWM application method for series LED connection.

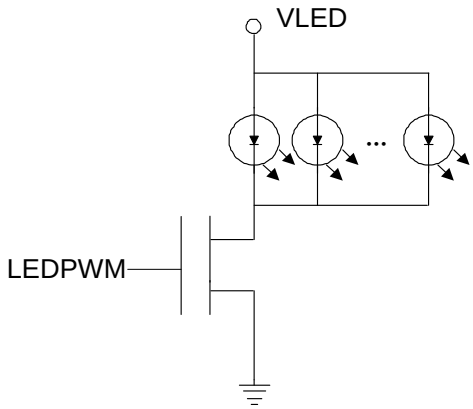


Fig. 17 LEDPWM application for LED parallel connection

Note:

If the ITO resistance of LEDPWM is larger, the RC-delay of the ITO resistance and the Gate-capacitance (the capacitance value is larger for power MOSFET) should be considered.

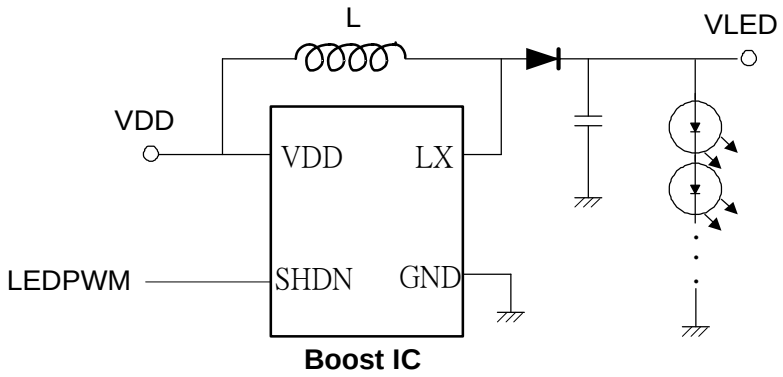


Fig. 18 The suggestion of LEDPWM application for LED Series connection

Driving Waveform Control

ST7035 supports 2 kinds of driving waveform: A-type and B-type. A-type and B-Type is chosen by TYPMD pin. For different bias setting, the driving voltage is different. The definition of driving waveform are as the following figures.

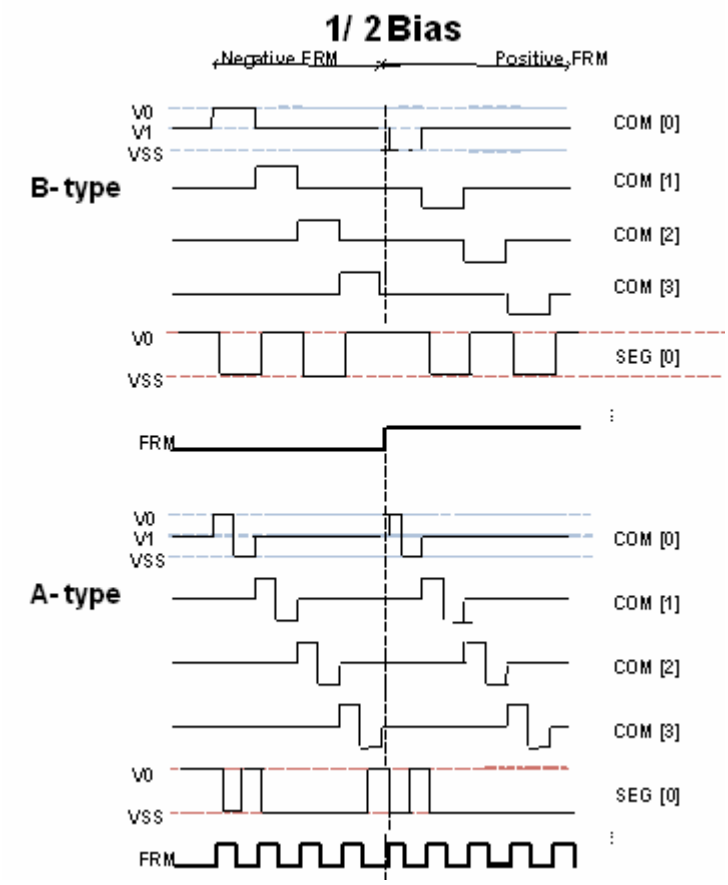


Fig. 19 A-type & B-type of 1/2 Bias waveform

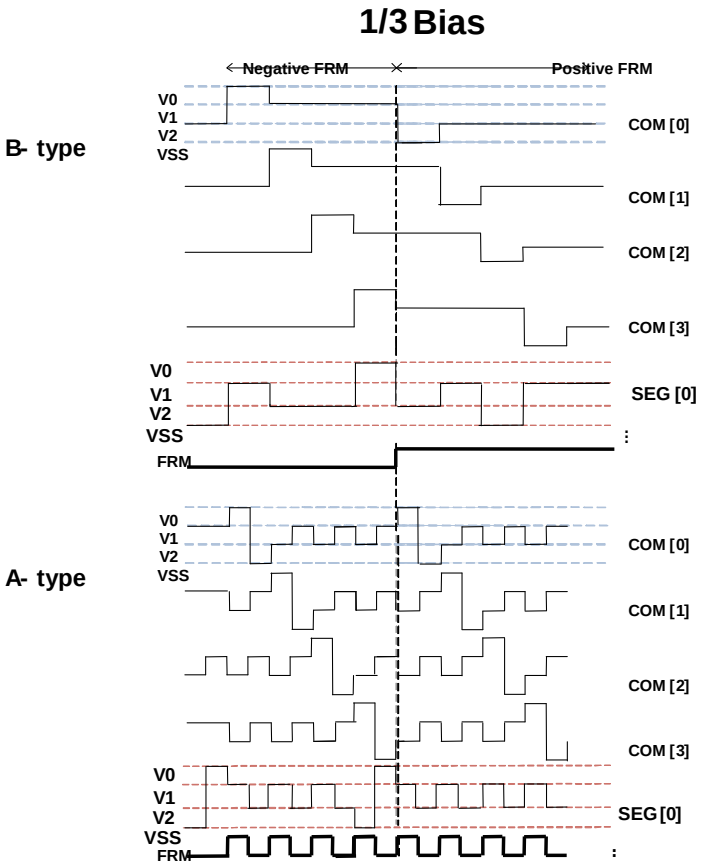


Fig. 20 A-type & B-type of 1/3 Bias waveform

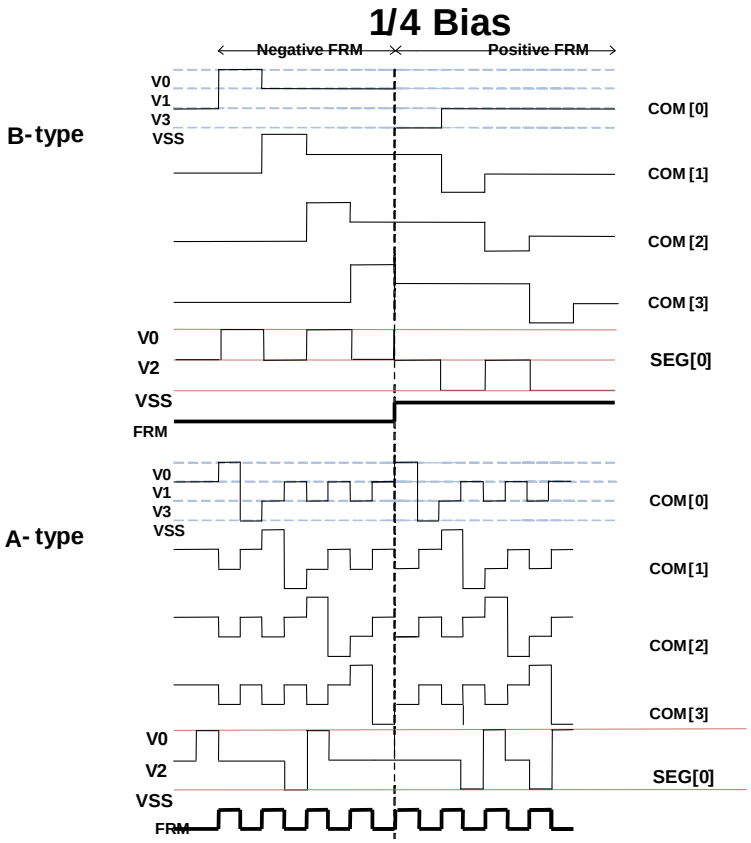


Fig. 21 A-type & B-type of 1/4 Bias waveform

8. RESET CIRCUIT

Setting /RST to “L” (hardware reset) can initialize internal function. /RST pin must connect to the reset pin of MPU and initialization by /RST pin is essential before operating. When /RST becomes “L” or “SRESET” instruction is issued, the internal reset procedure will start. The procedure is listed below:

Internal oscillator: OFF
Internal LCD PWM circuits: OFF
Display: OFF (all SEGs/COMs output VSS level)
Display all-point: Exit
Inverse Display: OFF
Row address: 0
Column address: 0
Power control [OSC, BST, FOL, V0] = All OFF
All registers are default value

After power-on, display data in DDRAM is undefined and the display status is “Display OFF”. The contents in DDRAM will not be cleared by internal reset procedure. It’s better to initialize whole DDRAM (ex: fill all 00h or write a display pattern) before turning the Display ON. Besides, the power is not stable when it is just turned ON. A hardware reset is needed to initialize those internal registers after the power is stable.

9. INSTRUCTION TABLE

Instruction

Command	Instruction Code										Description
	Hex	A0	D7	D6	D5	D4	D3	D2	D1	D0	
NOP	00	0	0	0	0	0	0	0	0	0	No Operation
SRESET	01	0	0	0	0	0	0	0	0	1	Software reset
Sleep In	10	0	0	0	0	1	0	0	0	0	Enter Sleep-in mode
Sleep Out	11	0	0	0	0	1	0	0	0	1	Exit Sleep-in mode
Inverse Display OFF	20	0	0	0	1	0	0	0	0	0	Display Inversion off
Inverse Display	21	0	0	0	1	0	0	0	0	1	Display Inversion on
Exit All-Pixel ON	22	0	0	0	1	0	0	0	1	0	All-pixel OFF
All-Pixel ON	23	0	0	0	1	0	0	0	1	1	All-pixel ON
Display OFF	28	0	0	0	1	0	1	0	0	0	Display OFF
Display ON	29	0	0	0	1	0	1	0	0	1	Display ON
Set Column Address	2A	0	0	0	1	0	1	0	1	0	Set column address
	-	1	-	-	-	-	CS3	CS2	CS1	CS0	Column start address
	-	1	-	-	-	-	CE3	CE2	CE1	CE0	Column end address
Set Row Address	2B	0	0	0	1	0	1	0	1	1	Set row address
	-	1	-	-	-	-	0	0	RS1	RS0	Row start address
	-	1	-	-	-	-	0	0	RE1	RE0	Row end address
Display Data Length	0F	0	0	0	0	0	1	1	1	1	Set display data length before writing DDRAM (3-Line SPI only)
	-	1	DL7	DL6	DL5	DL4	DL3	DL2	DL1	DL0	
Memory Write	2C	0	0	0	1	0	1	1	0	0	Write data into DDRAM
Power Discharge	D0	0	1	1	0	1	0	0	0	0	Power discharge
	-	1	0	0	0	0	0	0	AD1	AD0	
Set Frame Frequency	B2	0	1	0	1	1	0	0	1	0	Set LCD frame frequency
	-	1	0	0	0	1	FR3	FR2	FR1	FR0	
Set LED PWM	B3	0	1	0	1	1	0	0	1	1	Set PWM waveform for LED backlight
	-	1	-	-	-	-	-	0	LP1	LP0	
	-	1	LEDRT[7:0]								
RAM Counter Direction	B7	0	1	0	1	1	0	1	1	1	Set RAM Counter Direction MX, MY
	-	1	-	-	-	-	-	-	MY	MX	
Set Vop	C0	0	1	1	0	0	0	0	0	0	Set Vop for contrast control. Range: 4V~15V
	-	1	Vop7	Vop6	Vop5	Vop4	Vop3	Vop2	Vop1	Vop0	
	-	1	0	0	0	0	0	0	0	Vop8	
Set Bias	C3	0	1	1	0	0	0	0	1	1	Select Bias for multi-duty
	-	1	0	0	0	0	0	0	BS1	BS0	
Power Control	D2	0	1	1	0	1	0	0	1	0	Power Control
	-	1	0	0	0	OSC	BST	FOL	V0	0	
Set Booster Clock	BA	0	1	0	1	1	1	0	1	0	Set booster clock
	-	1	-	-	-	-	-	BE2	BE1	BE0	

10. INSTRUCTION DESCRIPTION

NOP (00h)

Non-operation! This instruction is no operation of IC.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	0	0	0	0	0	No Operation

SRESET (01h)

This command will trigger internal reset procedure and internal registers will return to default status. The DDRAM contents will not be changed.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	0	0	0	0	1	Software reset

Sleep In (10h)

This command causes the LCD module to enter the minimum power consumption mode.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	0	0	0	0	Sleep in mode

Sleep Out (11h)

This command turns off sleep in mode.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	0	0	0	1	Sleep out mode

Inverse Display OFF (20h)

This command is used to leave inverse display mode. This command will not change any status or memory data.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	0	0	0	0	0	Inverse display off (Normal display)

Inverse Display (21h)

This command is used to enter inverse display mode. This command will not change any status or memory data.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	0	0	0	0	1	Inverse display on

Exit All-Pixel ON (22h)

This command is used to exit all display points on mode. This command will not change any status or memory data.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	0	0	0	1	0	Exit all point on

All-Pixel ON (23h)

This command is used to enter all display points on mode. This command will not change any status or memory data.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	0	0	0	1	1	Enter all point on

Display OFF (28h)

This command is used to enter into display off mode.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	0	1	0	0	0	Display off

Display ON (29h)

This command is used to enter into display on mode.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	0	1	0	0	1	Display on

Set Column Address (2Ah)

This command defines column start address and end address data will be written. (Available range: 00h~0Bh)

After setting the column start and end address, the RAM window is also decided.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	0	1	0	1	0	Column address set
1	-	-	-	-	CS3	CS2	CS1	CS0	Column start address
1	-	-	-	-	CE3	CE2	CE1	CE0	Column end address

Set Row address (2Bh)

This command defines row start address, and end address data will be written. (Available range: 00h~03h)

After setting the row start and end address, the RAM window is also decided.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	0	1	0	1	1	Row address set
1	-	-	-	-	0	0	RS1	RS0	Row start address
1	-	-	-	-	0	0	RE1	RE0	Row end address

Display Data Length (0Fh)

This command defines the numbers of data bytes written to DDRAM. (3-Line SPI only, available range: 00h~6Bh)

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	0	1	1	1	1	Display data length set
1	DL7	DL6	DL5	DL4	DL3	DL2	DL1	DL0	Row start address

The data length calculation formula is data length = DL[7:0]+1

Ex:: DL[7:0] = 0x00 means the data length is 1 byte.

DL[7:0] = 0x0B means the data length is 11+1=12 bytes.

Memory Write (2Ch)

This command is executed before data is written to memory.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	0	1	1	0	0	Write data to memory

Power Discharge (D0h)

This instruction is to discharge IC power when “Sleep In” command is executed or VDD2 off.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	1	1	0	1	0	0	0	0	Power discharge
1	0	0	0	0	0	0	AD1	AD0	

Flag	Description
AD1	AD1=0: Power discharge off. AD1=1: Discharge VLCDOUT when “Sleep In” command is executed or VDD2 off.
AD0	AD0=0: Power discharge off. AD0=1: Discharge V0 when “Sleep In” command is executed or VDD2 off.

Set Frame Frequency (B2h)

This command is used to set LCD frame frequency.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	1	0	1	1	0	0	1	0	Frame frequency set
1	0	0	0	1	FR3	FR2	FR1	FR0	Frame frequency registers set

FR[3:0]				LCD Frame Frequency	FR[3:0]				LCD Frame Frequency
0	0	0	0	50 Hz	1	0	0	0	160 Hz
0	0	0	1	60 Hz	1	0	0	1	180 Hz
0	0	1	0	70 Hz (Default)	1	0	1	0	200 Hz
0	0	1	1	80 Hz	1	0	1	1	220 Hz
0	1	0	0	90 Hz	1	1	0	0	240 Hz
0	1	0	1	100 Hz	1	1	0	1	260 Hz
0	1	1	0	120 Hz	1	1	1	0	295 Hz
0	1	1	1	140 Hz	1	1	1	1	Reserved

Set LED PWM (B3h)

This command sets LED PWM waveform which controls external LED switch. LEDRT[7:0] set the number of “High” cycles in one PWM period.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	1	1	0	1	0	0	1	1	Set LED PWM
1	-	-	-	-	-	0	LP1	LP0	# of LED switch on per Com setting
1	LEDRT[7:0]								Set LED PWM Field width

LP1	LP0	LED On/Off numbers in one duty	Legal LEDRT bits	PWMCK counting # in one PWM period	LEDRT usable range
0	0	1 (defult)	LEDRT[7:0]	256	0~255 (Default 80h)
0	1	2	LEDRT[6:0]	128	0~127 (Default 00h)
1	0	4	LEDRT[5:0]	64	0~63 (Default 00h)
1	1	8	LEDRT[4:0]	32	0~31 (Default 00h)

Set RAM Counter Direction (B7h)

This command is used to set RAM counter direction.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	1	0	1	1	0	1	1	1	Set RAM counter direction
1	-	-	-	-	-	-	0	MX	MX: RAM counter direction

Flag	Description
MX	MX=0: Column Page 0 to Column Page 11 (Default) MX=1: Column Page 11 to Column Page 0 Please re-send DDRAM data after change MX logic.

Set Vop (C0h)

This command is used to set the LCD supply voltage V0 (Vop). Please note the maximum voltage level of Vop available is limited by VLCD voltage level and the loading of LCD module.

Please note: The minimum setting of Vop = VDD2 – 1.2V

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	1	1	0	0	0	0	0	0	Vop set
1	Vop7	Vop6	Vop5	Vop4	Vop3	Vop2	Vop1	Vop0	Set the registers of Vop
1	-	-	-	-	-	-	-	Vop8	Vop[8:0]=64h (Default) Range: 4~15V

The Vop calculation formula is: **V0 = a + (Vop[8:0]) x b**

Symbol	Value	Unit
a	4	V
b	0.04	V

Vop[8:0] = 000000000 (000H)~100010011(113H)

Vop(V) = 4 V ~ 15 V

Set Bias (C3h)

This command is used to select LCD bias ratio of the voltage required to drive LCD.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	1	1	0	0	0	0	1	1	Bias selection
1	0	0	0	0	0	0	BS1	BS0	Set the registers of bias

BS	BS	Bias Value
0	0	1/2 bias
0	1	1/3 bias
1	0	1/4 bias (Default)
1	1	

Power Control (D2h)

This command is used to set power register.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	1	1	0	1	0	0	1	0	Power Control
1	0	0	0	OSC	BST	FOL	V0	0	

Flag	Set to '0'	Set to '1'
OSC	OSC on	OSC off (Default)
BST	Booster on	Booster off (Default)
FOL	Follower on	Follower off (Default)
V0	V0 regulator on	V0 regulator off (Default)

Set Booster Clock (Bah)

This command is used to set booster clock.

Please note different frame rate and duty cause different BOSC clock. Please find the mapping BOSC clock and set BE[2:0] from the below table. The available value of booster is between 15KHz~40KHz.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	1	0	1	1	1	0	1	0	Set booster clock
1	-	-	-	-	-	BE2	BE1	BE0	

BE2	BE1	BE0	Booster Clock (KHz)
0	0	0	BOSC / 3
0	0	1	BOSC / 4
0	1	0	BOSC / 5
0	1	1	BOSC / 6
1	0	0	BOSC / 8
1	0	1	BOSC / 12
1	1	0	BOSC / 16
1	1	1	BOSC / 24

BOSC (KHz)		Duty			
		1	2	3	4
Frame rate (Hz)	50	102.4	102.4	115.2	102.4
	60	122.88	122.88	138.24	122.88
	70	143.36	143.36	161.28	143.36
	80	163.84	163.84	184.32	163.84
	90	184.32	184.32	207.36	184.32
	100	204.8	204.8	230.4	204.8
	120	245.76	245.76	276.48	245.76
	140	286.72	286.72	322.56	286.72
	160	327.68	327.68	368.64	327.68
	180	368.64	368.64	414.72	368.64
	200	409.6	409.6	460.8	409.6
	220	450.56	450.56	506.88	450.56
	240	491.52	491.52	552.96	491.52
	260	532.48	532.48	599.04	532.48
	295	573.44	573.44	645.12	573.44
	320	614.4	614.4	691.2	614.4

Ex: Frame rate is 70Hz, duty is . The mapping BOSC is 143.36 KHz.

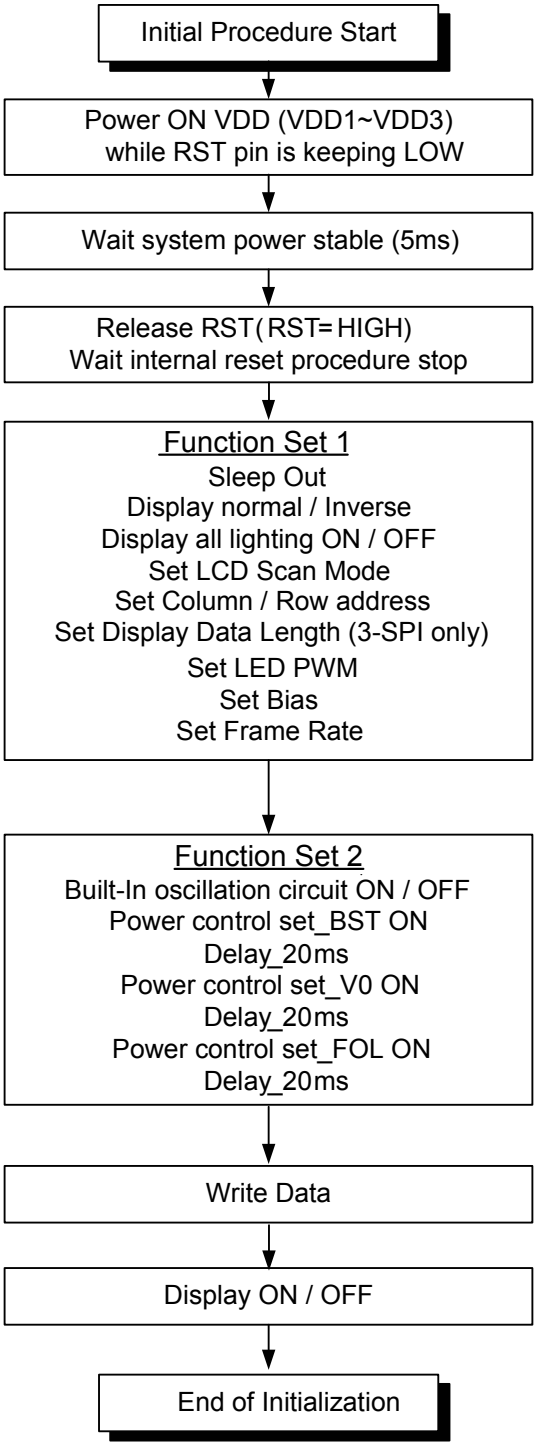
Booster clock is as below:

BE2	BE1	BE0	Booster Clock (KHz)
0	0	0	53.8
0	0	1	40.3
0	1	0	32.3
0	1	1	26.9
1	0	0	20.2
1	0	1	13.4
1	1	0	10.1
1	1	1	6.7

The available booster clock range is from 15KHz to 40KHz, please choose 32.3, 26.9, 20.2 KHz as booster clock.

11. OPERATION FLOW

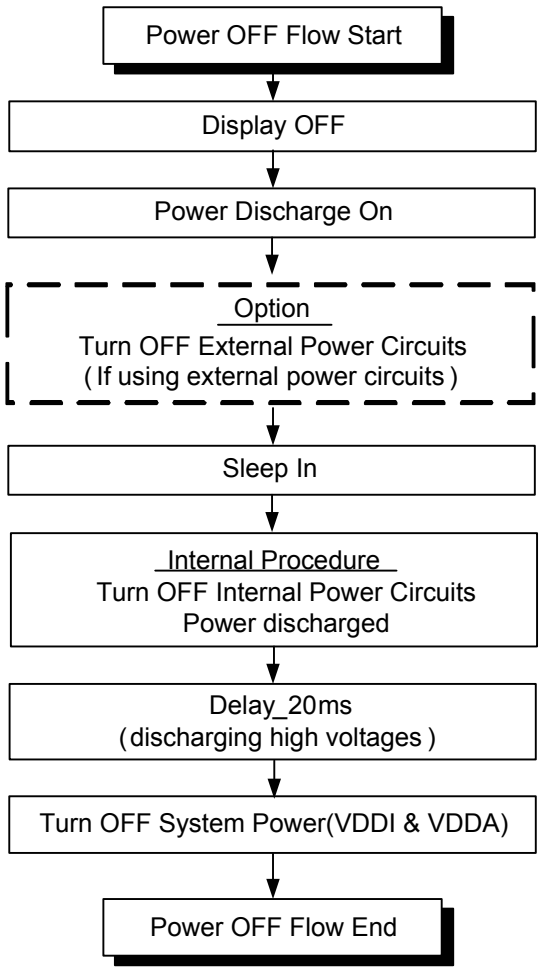
(1) Initial Flow (with built-in Power Circuits)



Power ON and Initial Flow Notes:

1. To prevent power ON noise, please hold RST LOW until the system power is stable (generally 5ms)
2. After releasing RST signal (RST=High), do NOT issue instruction immediately. An internal reset time (tR) is required for finishing internal reset procedure.
3. The delay time for Power Control flow depends on LCD module. The delay time should be increased if the ITO resistance or capacitor value increases.
4. The build-in DDRAM content is unknown after power ON. The content cannot be reset by hardware or software reset. It is recommended to add a DDRAM initial flow to prevent unexpected display pattern after turning ON the display.

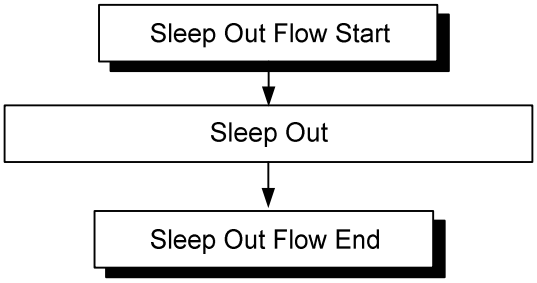
(2) Power OFF Flow



Power OFF Flow Notes:

1. Be Sure “Power Discharge” is turn on before issuing “Sleep In” instruction.
2. For external power application, please issue discharge instruction after turning external power circuit OFF.

(3) Sleep Out Flow

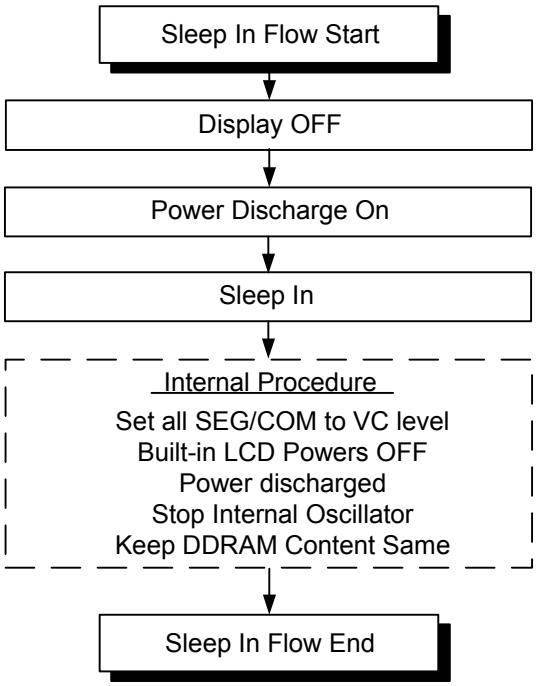


Sleep Out Flow Notes:

1. After issue “Sleep Out” instruction, oscillator and power system will automatically return to the states before issuing the “Sleep In” instruction.

(4) Sleep In Flow

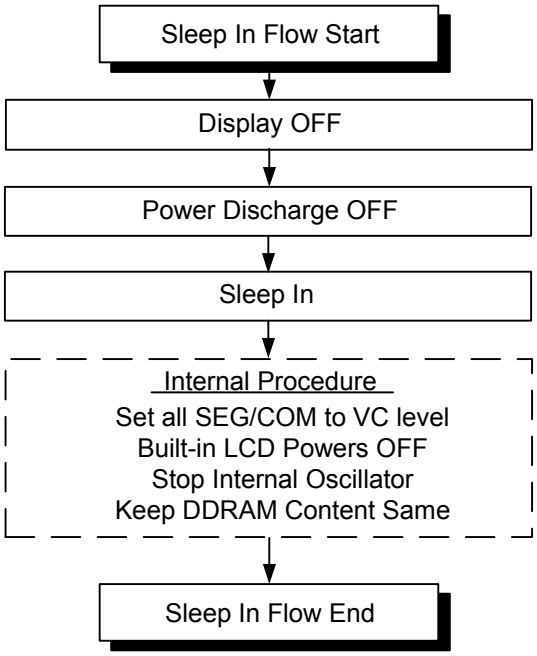
Internal Power Circuits



Internal Power Circuits Sleep In Flow Notes:

1. Be Sure “Power Discharge” is turn on before issuing “Sleep In” instruction.

External Power Circuits



External Power Circuits Sleep In Flow Notes:

1. Be Sure “Power Discharge” is turn off before issuing “Sleep In” instruction.

Example initial code:

Initial Code	For Master/Slave Extend Mode	
	Master	Slave
wrins(0x11); // sleep out	wrins_m(0x11); // sleep out	wrins_s(0x11); // sleep out

wrins_m(0xB7); // LCD Scan set
wrdata(0x00); // MX=0
	wrins_m(0xB7); // LCD Scan set
	wrdata(0x00); // MX=0
		wrins_s(0xB7); // LCD Scan set
		wrdata(0x00); // MX=0

wrins(0xC0); // set Vop
wrdata(0x32); // set Vop 6V
wrdata(0x00);
	wrins_m(0xC0); // set Vop
	wrdata_m(0x32); // set Vop 6V
	wrdata_m(0x00);	

wrins(0xC3); // set Bias
wrdata(0x01); // set 1/3 Bias
	wrins_m(0xC3); // set Bias
	wrdata_m(0x01); // set 1/3 Bias
		wrins_s(0xC3); // set Bias
		wrdata_s(0x01); // set 1/3 Bias

wrins(0xB3); // set LED waveform
wrdata(0xFF); // set LED width 0xFF
	wrins(0xB3); // set LED waveform
	wrdata(0xFF); // set LED width 0xFF	

wrins(0x2A); // set SEG address
wrdata(0x00); // set Start at SEG0
wrdata(0x0B); // set End at SEG95
	wrins(0x2A); // set SEG address
	wrdata(0x00); // set Start at SEG0
	wrdata(0x0B); // set End at SEG95
		wrins(0x2A); // set SEG address
		wrdata(0x00); // set Start at SEG0
		wrdata(0x0B); // set End at SEG95

wrins(0x2B); // set COM address
wrdata(0x00); // set Start at COM0
wrdata(0x03); // set Start at COM3
	wrins(0x2B); // set COM address
	wrdata(0x00); // set Start at COM0
	wrdata(0x03); // set Start at COM3	

wrins(0xB2); // set fFR
wrdata(0x13); // set fFR=80Hz
	wrins(0xB2); // set fFR
	wrdata(0x13); // set fFR=80Hz
		wrins(0xB2); // set fFR
		wrdata(0x13); // set fFR=80Hz

wrins(0xD2); // set power control
wrdata(0x06); // OSC & Booster on
delay_ms(20); // delay 20ms
wrins(0xD2); // set power control
wrdata(0x04); // V0 on
delay_ms(20); // delay 20ms
wrins(0xD2); // set power control
wrdata(0x00); // FOL on
delay_ms(20); // delay 20ms
	wrins(0xD2); // set power control
	wrdata(0x06); // OSC & Booster on
	delay_ms(20); // delay 20ms
	wrins(0xD2); // set power control
	wrdata(0x04); // V0 on
	delay_ms(20); // delay 20ms
	wrins(0xD2); // set power control
	wrdata(0x00); // FOL on
	delay_ms(20); // delay 20ms
		wrins_s(0xD2); // set power control
		wrdata_s(0x1E); // power all off

wrins(0x0F); // set data length (3-SPI only)
wrdata(0x6B); // full range
Wrins(0x2C); // Memory Write
wr_pattern(0x00); // DDRAM data (black)
wrins(0x29); // Display on
	wrins(0x0F); // set data length (3-SPI only)
	wrdata(0x6B); // full range
	Wrins(0x2C); // Memory Write
	wr_pattern(0x00); // DDRAM data (black)
	wrins_m(0x29); // Display on
		wrins(0x0F); // set data length (3-SPI only)
		wrdata(0x6B); // full range
		Wrins(0x2C); // Memory Write
		wr_pattern(0x00); // DDRAM data (black)
		wrins_m(0x29); // Display on

12. ABSOLUTE MAXIMUM VALUES

Please refer to the below for the Absolute Maximum Rating System.

Parameter	Symbol	Conditions	Unit
Digital Power Supply Voltage	VDD1 & VDD3	-0.3 ~ 6	V
Analog Power Supply Voltage	VDD2	-0.3 ~ 6	V
LCD Power Supply Voltage 1	V0 ,VLCD	-0.3 ~ 18	V
LCD Power Supply Voltage 2	V1, V2, V3	-0.3 ~ 18	V
MPU Interface Input Voltage	V_{IN}	-0.3 ~ VDDI+0.3	V
MPU Interface Output Voltage	V_O	-0.3 ~ VDDI+0.3	V
Operating Temperature	T_{OPR}	-40 to +80	℃
Storage Temperature	T_{STR}	-55 to +105	℃

Notes

1. Stresses above listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.
3. Insure that the voltage levels of V1, V2 & V3 are always per the below:
   V0 ≥ V1 ≥ V2 ≥ V3 ≥ VSS

13. HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to prevent risk completely, it is suggested to take normal precautions appropriate to handling MOS devices.

14. DC CHARACTERISTICS

Unless otherwise specified, VSS=0V and Ta=25℃.

Item	Symbol	Condition	Rating			Unit	Related Pin
			Min.	Typ.	Max.		
Digital Operating Voltage	VDDI		2.7	-	5.5	V	VDD1 VDD3
Analog Operating Voltage	VDDA	Booster x 2, x3	2.7	-	5.5		VDD2
		Booster x 4			5		
High-level Input Voltage	V_{IH}		0.8*VDD1	-	VDD1		*1
Low-level Input Voltage	V_{IL}		VSS1	-	0.2*VDD1		*1
High-level Output Voltage	V_{OH}		0.8*VDD1	-	VDD1		*2
Low-level Output Voltage	V_{OL}		VSS1	-	0.2*VDD1		*2
Input leakage current	I_{LI}	V_{IN}=VDD or VSS	-	-	0.1	uA	*1
Liquid Crystal Driver ON Resistance	R_{ON}	Ta=25℃, ΔV=10%	-	2	-	KΩ	SEGn
		V0=8.0V, Bias = 1/3	-	2	-		COMn
Frame frequency	f_{FR}	FR[3:0]=0x02, T=25˚C, Duty=1/4	-	70	-	Hz	
Regulator Supply Voltage Booster Output Voltage	VLCD		-	-	16.5	V	VLCD *3
LCD Vop	V0	VDD=3.3V	4	6	15		V0 *3 *4
		VDD=5V	5				

Notes

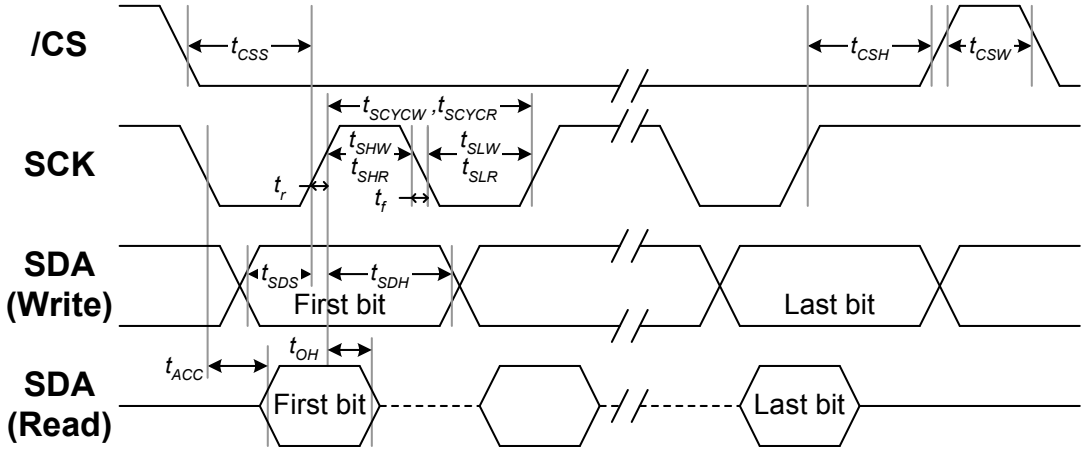
1. Related Pin: IF, SDA, SCK, /RST, /CS, CLS, SYNC, DON & CL, PRT0, PRT1, TYPMD, MS
2. Related Pin: SDA, SYNC, DON & CL.
3. Insure that the voltage level of V0 always follows that: VLCD -0.5 ≥ V0.
4. The maximum possible V0 voltage that may be generated is dependent on voltage, temperature and (display) load.

The DC Current Consumption of bare chip is shown below: (with internal power circuits and internal clock)

Test pattern	Symbol	Condition	Rating			Units	Note
			Min.	Typ.	Max.		
Display Pattern SNOW	ISS	VDD=5.0V, Booster x4, FR=70Hz, V0=8V, Ta=25℃	-	550	-	uA	
Sleep In Mode	ISS	VDD=5.0V, Booster x4, FR=70Hz, V0=8V, Ta=25℃	-	50	-	uA	

15. AC CHARACTERISTICS

SPI 3-LINE SERIAL INTERFACE TIMING



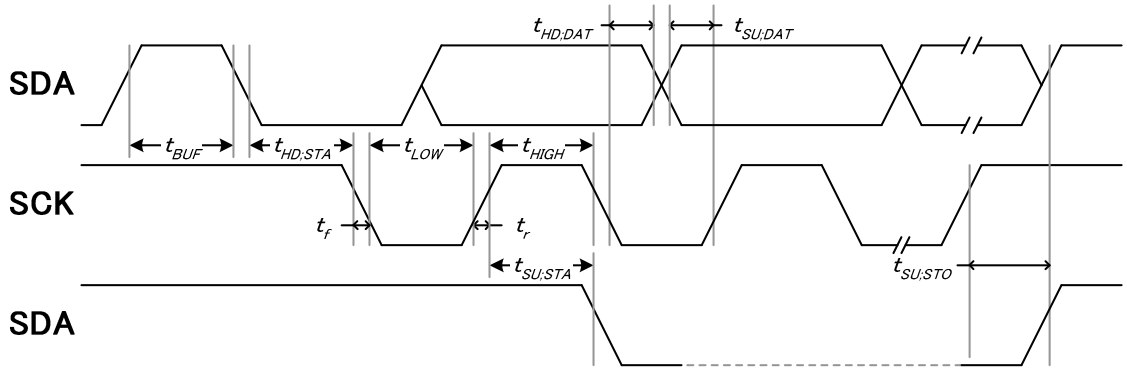
(VDD1=3~5V Ta=25℃)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period (Write)	SCK	tSCYCW		250	—	ns
SCK “H” pulse width		tSHW		100	—	
SCK “L” pulse width		tSLW		100	—	
Data setup time	SDA	tSDS		100	—	
Data hold time		tSDH		100	—	
Chip select setup time	/CS	tCSS		150	—	
Chip select hold time		tCSH		150	—	
Chip select wait time		tCSW		20	—	

*1 The rise and fall time (tr, tf) of the input signal are specified at 15 ns or less.

*2 All timings take 20% and 80% of VDD as standard.

I²C INTERFACE TIMING

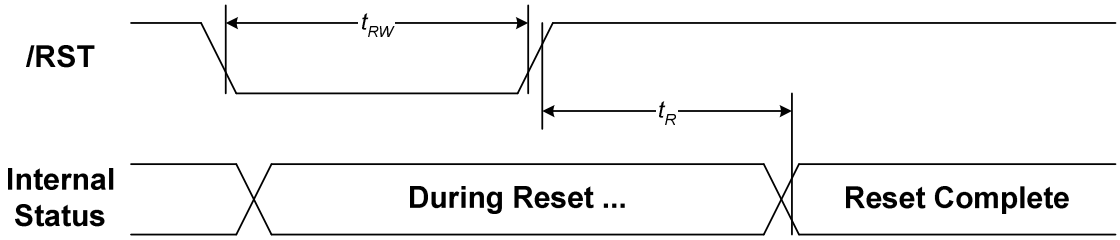


(VDD=3~5V, Ta=25℃)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock frequency	SCK	fSCL		-	400	KHz
SCL clock LOW period		tLOW		1.3	-	us
SCL clock HIGH period		tHIGH		0.6	-	
BUS free time between a STOP and START		tBUF		1.3	—	
Data setup time	SDA	tSU;Data		0.1	—	
Data hold time		tHD;Data		0.02	—	
Setup time for a repeated START condition		tSU;STA		0.6	—	
Start condition hold time		tHD;STA		0.6	—	
Setup time for STOP condition		tSU;STO		0.6	—	
Signal rise time (Min: C_L=40pF; Max: C_L=400pF)	SDA SCK	tr		—	300	ns
Signal fall time (Min: C_L=40pF; Max: C_L=400pF)		tf		—	300	
Tolerable spike width on bus		tSW		—	15	

*1 All timings take 20% and 80% of VDD as standard.

RESET TIMING



(VDD=3~5V Ta=25℃)

Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		-	2	us
Reset “L” pulse width	tRW		2.5	-	

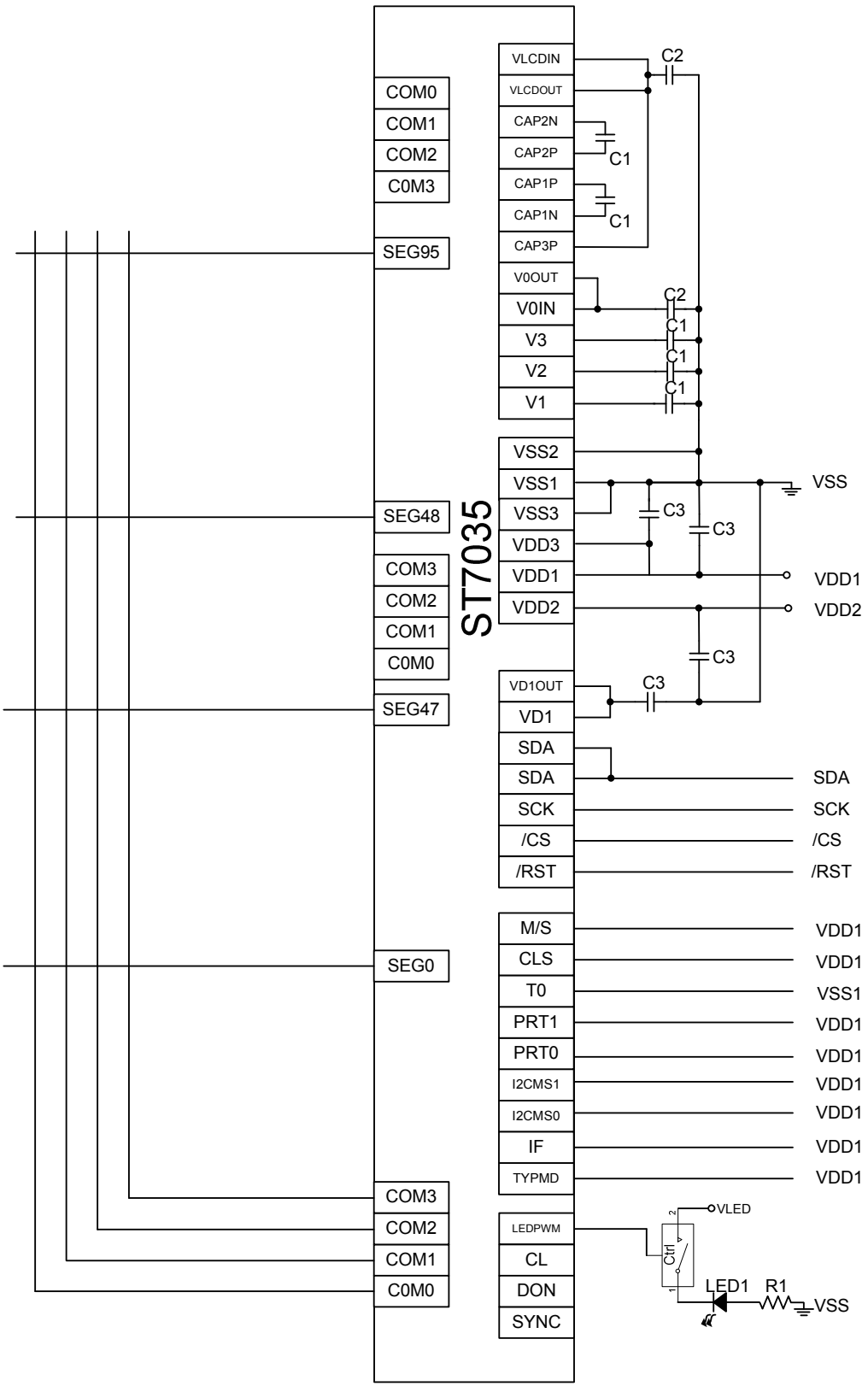
*1 The rise and fall time (tr, tf) input signal are specified at 15 ns or less.

*2 All timings take 20% and 80% of VDD as standard.

APPLICATION NOTE

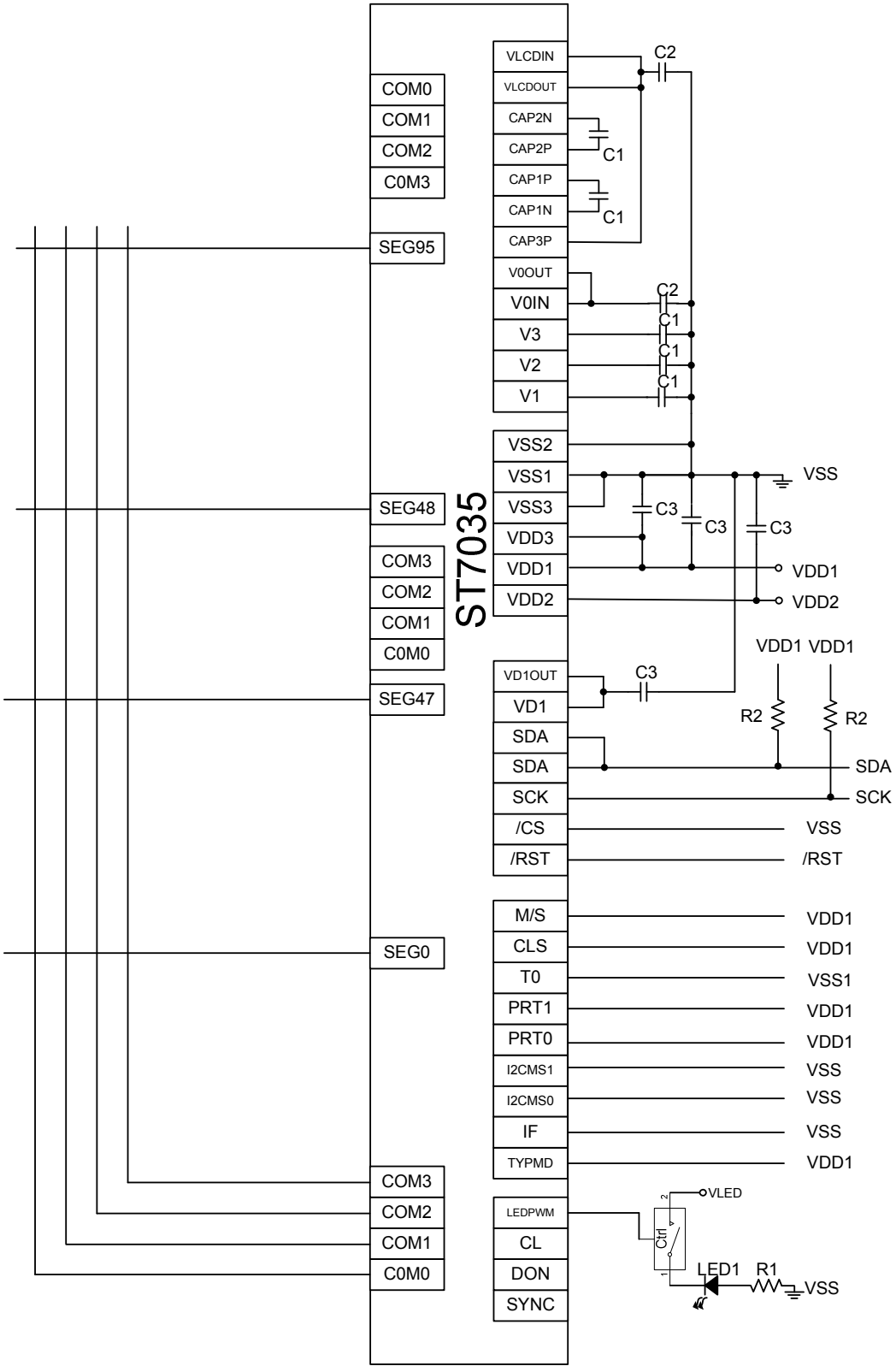
Application Circuit for 3-Line SPI Interface

Symbol	Reference Value (uF)
C1, C2 ,C3	1 uF



Application Circuit for I²C Interface

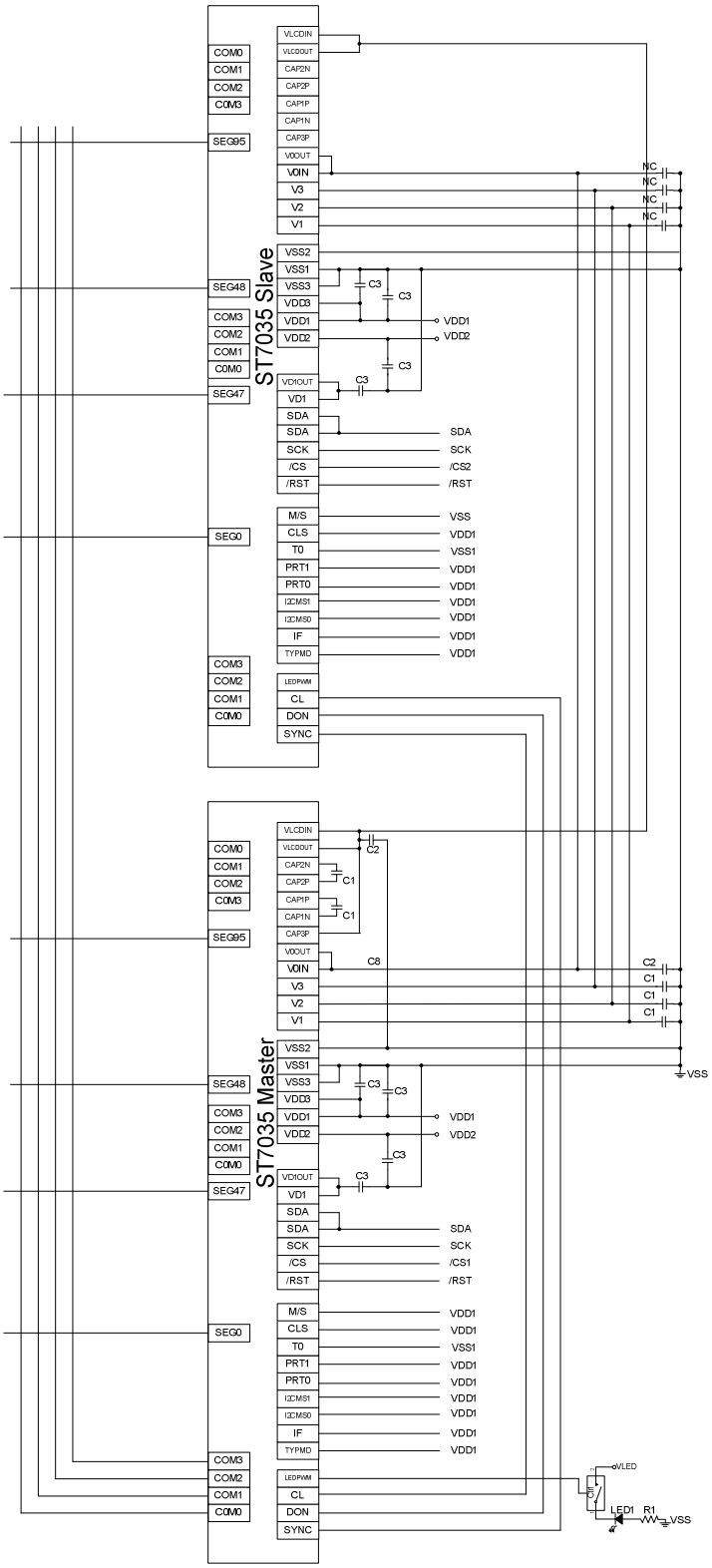
Symbol	Reference Value (uF)
C1, C2 ,C3	1 uF



Application Circuit for 3-Line SPI Interface Master/Slave

Symbol	Reference Value (uF)
C1, C2 ,C3	1 uF

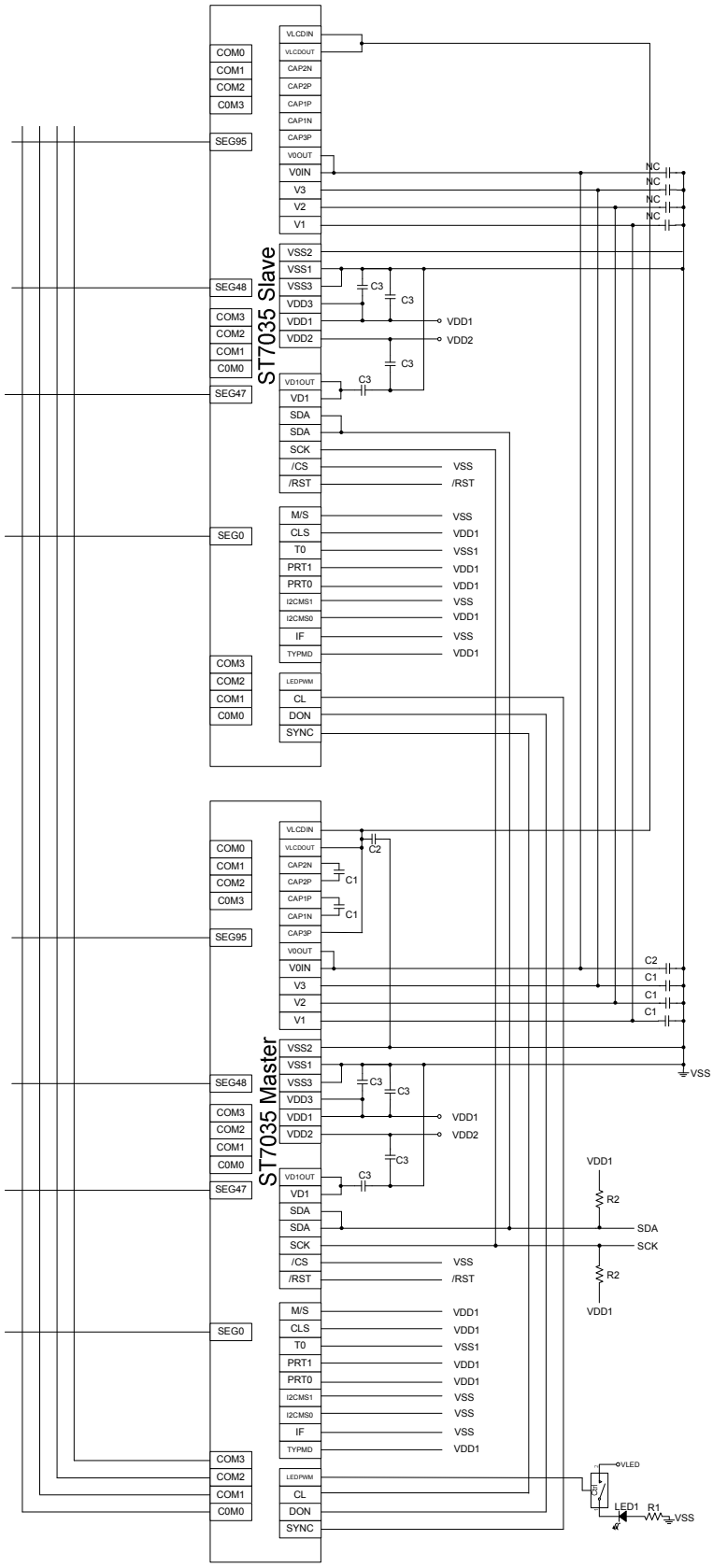
Please provide low noise, low via trace for “CL”,”DON” & ”SYNC” signal.



Application Circcuit for I²C Interface Master/Slave

Symbol	Reference Value (uF)
C1, C2 ,C3	1 uF

Please provide low noise, low via trace for “CL”,”DON” & ”SYNC” signal.



Revision History		
Version	**Date**	**Description**
1.0	2013/10/29	● Modify operating temperature range.
1.0a	2013/11/11	● Add master/slave application
1.0b	2014/04/23	● Add the application about all external power without external capacitor.