Sitronix

ST7063

80CH Segment Driver for Dot Matrix LCD

Functions

- Dot matrix LCD driver with two 40 channel outputs
- Bias voltage (V1 ~ V4)
- input/output signals
  - Input : Serial display data and control pulse from controller IC
  - Output : 40 X 2 channels waveform for LCD driving

Features

- Display driving bias : static to 1/5
- Power supply for logic : 2.7V ~ 5.5V
- Power supply for LCD voltage (V_{DD}~V_{EE}) : 3V ~ 11V

100 Pin QFP package and bare chip available

Description

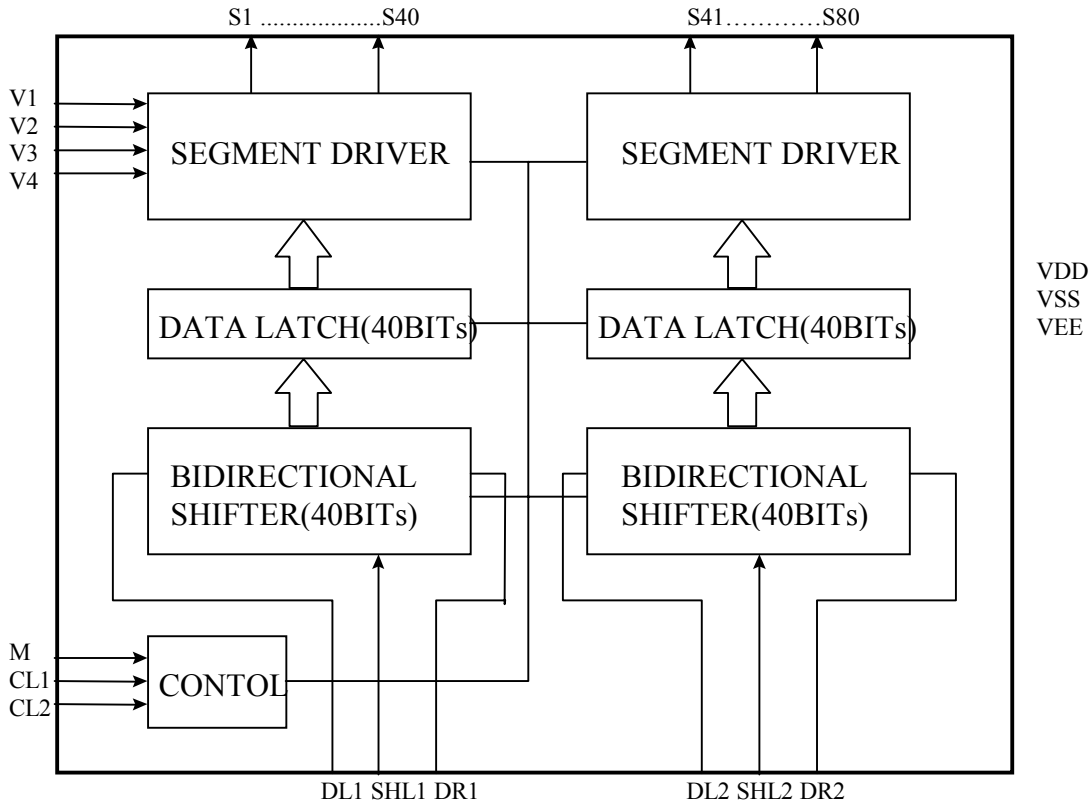
ST7063 is a segment driver for dot matrix type LCD display. It features 80 channels with 40 X 2 bits bi-directional shift registers, data latches, LCD drivers and logic control circuits. It is fabricated by high voltage CMOS process with low current consumption.

The **ST7063** can convert serial data received from an LCD controller, such as **ST7066**, into parallel data and send out LCD driving waveforms to the LCD panel. The **ST7063** is designed for general purpose LCD drivers. It can drive both static and dynamic drive LCD. The LSI can be used as segment driver.

The **ST7063** has pin function compatibility with the KS0063(B) that allows the user to easily replace it with an **ST7063**.

ST7063 Specification Revision History		
Version	Date	Description
1.1	2000/07/31	First Edition
1.2	2000/11/14	Added QFP Pad Configuration(Page 6)
1.2a	2001/02/26	Changed Application Circuit(Page 11)

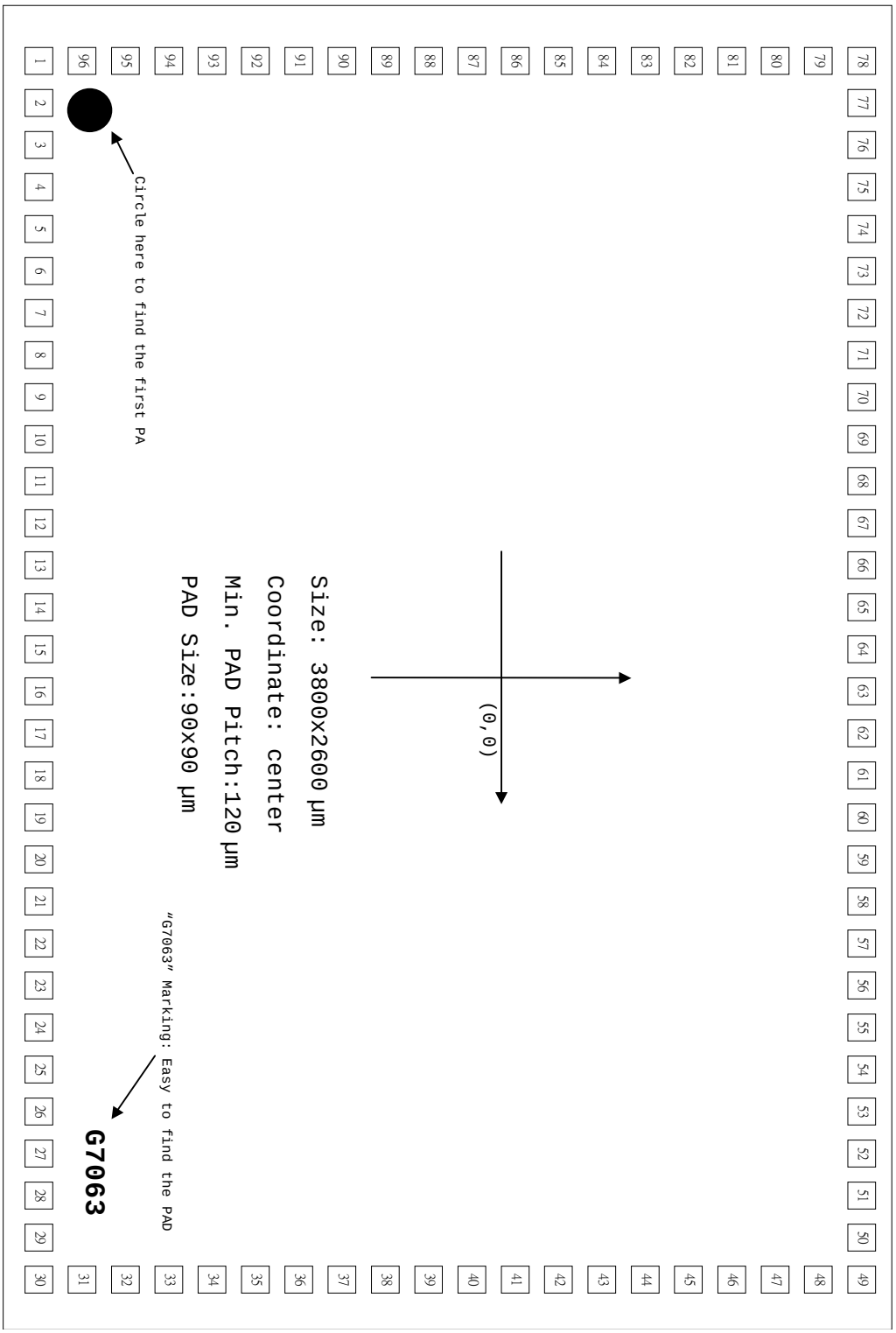
ST7063 FUNCTIONAL BLOCK



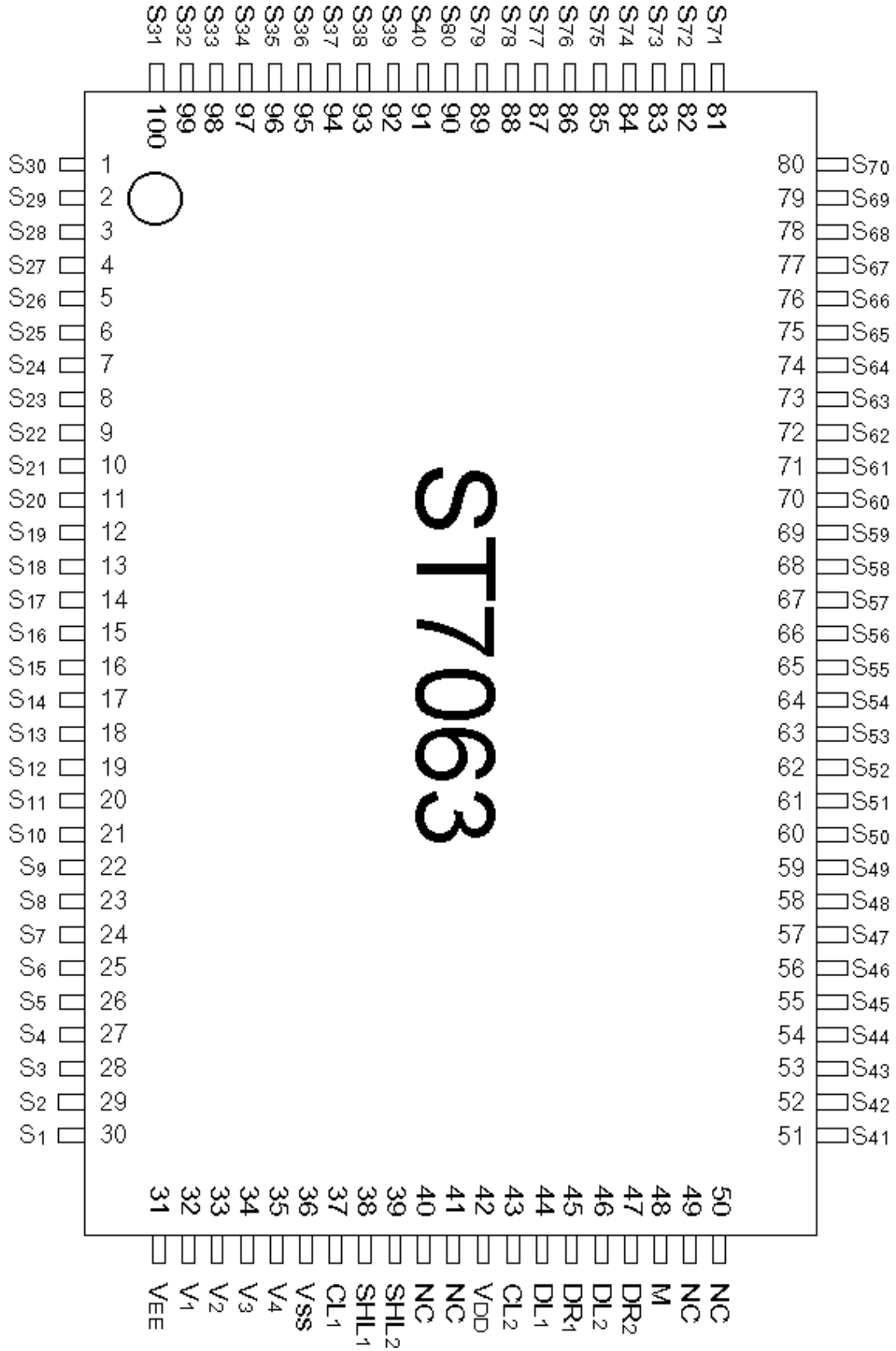
Pin Description

PIN NAME	PURPOSE	DESCRIPTION	I/O
VDD	POWER	for logic	N/A
VSS	GROUND	for logic	N/A
VEE	LCD GND	for LCD driving voltage	N/A
V1 V2	LCD output	used as select voltage level	I
V3 V4	LCD output	used as non select voltage level	I
S1-S40	segment	LCD driver output for part 1	O
SHL1	direction	direction control for part 1 segments	I
DL1, DR1	data in /out	If SHL1 = 1 then DL1=out, DR1=in If SHL1 = 0 then DL1=in, DR1=out	I/O
S41-S80	segment	LCD driver output for part 2	O
SHL2	direction	direction control for part 2 segments	I
DL2, DR2	data in/out	If SHL2 = 1 then DL2=out, DR2=in If SHL2 = 0 then DL2=in, DR2=out	I/O
M	alternation	Alternate the LCD driving waveform	I
CL1	latch clock	latch the data after shift is completed	I
CL2	shift clock	shift the data into the segments	I

PAD Arrangement



PIN Configuration



PAD NAMES AND COORDINATES

Pad No.	Pad Name	X	Y
1	S42	-1760	-1160
2	S43	-1630	-1160
3	S44	-1500	-1160
4	S45	-1380	-1160
5	S46	-1260	-1160
6	S47	-1140	-1160
7	S48	-1020	-1160
8	S49	-900	-1160
9	S50	-780	-1160
10	S51	-660	-1160
11	S52	-540	-1160
12	S53	-420	-1160
13	S54	-300	-1160
14	S55	-180	-1160
15	S56	-60	-1160
16	S57	60	-1160
17	S58	180	-1160
18	S59	300	-1160
19	S60	420	-1160
20	S61	540	-1160
21	S62	660	-1160
22	S63	780	-1160
23	S64	900	-1160
24	S65	1020	-1160
25	S66	1140	-1160
26	S67	1260	-1160
27	S68	1380	-1160
28	S69	1500	-1160
29	S70	1630	-1160
30	S71	1760	-1160
31	S72	1760	-1030
32	S73	1760	-900
33	S74	1760	-780
34	S75	1760	-660
35	S76	1760	-540
36	S77	1760	-420
37	S78	1760	-300
38	S79	1760	-180
39	S80	1760	-60
40	S40	1760	60
41	S39	1760	180
42	S38	1760	300
43	S37	1760	420
44	S36	1760	540
45	S35	1760	660
46	S34	1760	780
47	S33	1760	900
48	S32	1760	1030
49	S31	1760	1160
50	S30	1630	1160
51	S29	1500	1160
52	S28	1380	1160
53	S27	1260	1160
54	S26	1140	1160
55	S25	1020	1160
56	S24	900	1160
57	S23	780	1160
58	S22	660	1160
59	S21	540	1160
60	S20	420	1160
61	S19	300	1160
62	S18	180	1160
63	S17	60	1160
64	S16	-60	1160
65	S15	-180	1160
66	S14	-300	1160
67	S13	-420	1160
68	S12	-540	1160
69	S11	-660	1160
70	S10	-780	1160
71	S9	-900	1160
72	S8	-1020	1160
73	S7	-1140	1160
74	S6	-1260	1160
75	S5	-1380	1160
76	S4	-1500	1160
77	S3	-1630	1160
78	S2	-1760	1160
79	S1	-1760	1030
80	VEE	-1760	900
81	V1	-1760	780
82	V2	-1760	660
83	V3	-1760	540
84	V4	-1760	420
85	VSS	-1760	300
86	CL1	-1760	180
87	SHL1	-1760	60
88	SHL2	-1760	-60
89	VDD	-1760	-180
90	CL2	-1760	-300
91	DL1	-1760	-420
92	DR1	-1760	-540
93	DL2	-1760	-660
94	DR2	-1760	-780
95	M	-1760	-900
96	S41	-1760	-1030

Functional Description

Clock

The CL1 is the clock to latch data on the falling edge. It latches the data input from the bi-directional shift register at the falling edge of CL1 and transfers its outputs to the LCD driver circuit. The CL2 is the clock to shift data on the falling edge. It shifts the serial data at the falling of CL2 and transfers the output of each bit of the register to the latch circuit.

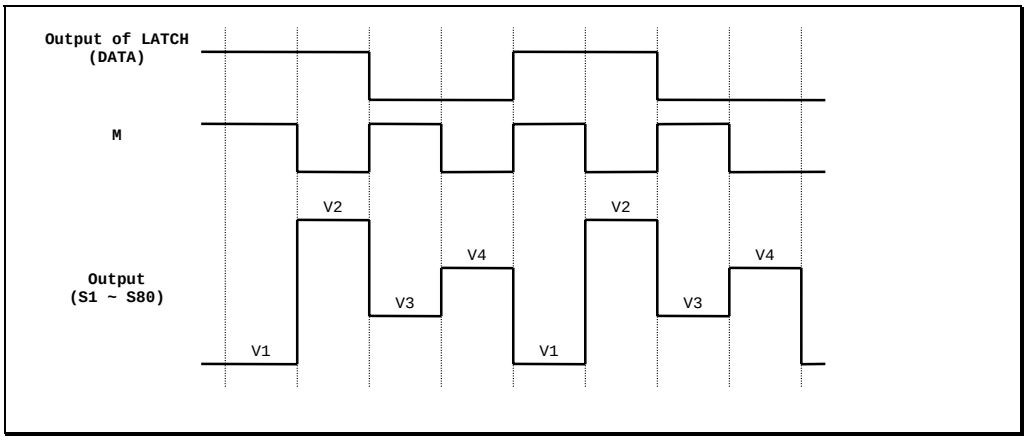
Shift Registers And Data I/O

The **ST7063** supplies two sets of 40-bit shift register, which controls the shift direction by SHL1 & SHL2. The SHL1 controls the 1st 40-bit shift register, and SHL2 controls the 2nd 40-bit shift register. When SHL1 is connected to VDD, the 1st shift direction is from S40 to S1; when SHL1 is connected to VSS, the shift direction changes from S1 to S40. When SHL2 is connected to VDD, the 2nd shift direction is from S80 to S41; when SHL2 is connected to VSS, the shift direction changes from S41 to S80.
The DL1, DR1, DL2, DR2 are data input or output option function.

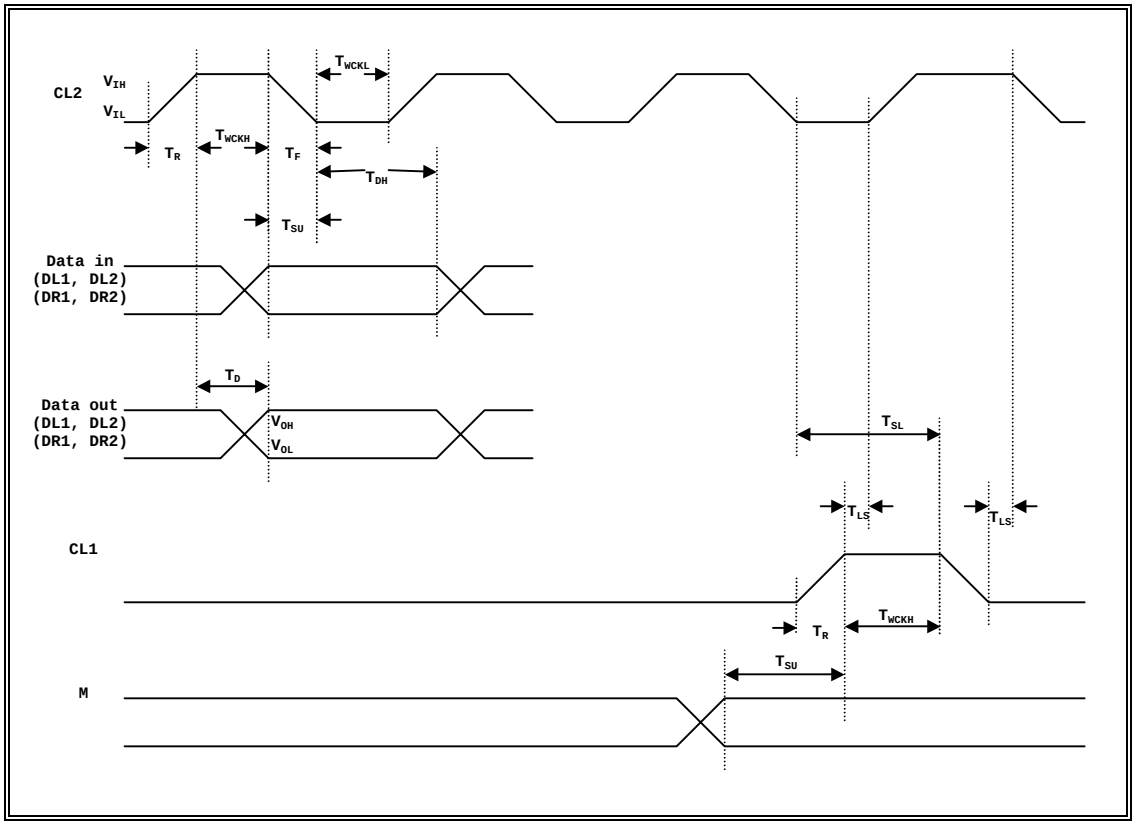
Shift Direction of Channel 1			
SHL1	Shift Direction	DL1	DR1
0	S1 → S40	IN	OUT
1	S40 → S1	OUT	IN

Shift Direction of Channel 2			
SHL2	Shift Direction	DL2	DR2
0	S41 → S80	IN	OUT
1	S80 → S41	OUT	IN

LCD Output Waveforms



Timing Characteristics



D.C Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Applicable pin
V_{DD}	Operating Voltage	-	2.7	-	5.5	V	-
V_{LCD}	Driver Supply Voltage	V_{DD}-V_{EE}	3	-	11	V	-
V_{IH}	Input High Voltage	-	0.7V_{DD}	-	V_{DD}	V	CL1,CL2,M,SHL1,SHL2 DL1,DL2,DR1,DR2
V_{IL}	Input Low Voltage	-	0	-	0.3V_{DD}	V	
I_{LKG}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}	-5	-	5	uA	
V_{OH}	Output High Voltage	I_{OH} = -0.4mA	V_{DD}-0.4	-	-	V	DL1,DL2,DR1,DR2 V1~V4, S1~S80
V_{OL}	Output Low Voltage	I_{OL} = +0.4mA	-	-	0.4	V	
I_{DD}	Operating Current	F_{CL2} = 400K_{HZ}	-	100	300	uA	V_{DD},V_{EE}
I_V	Leakage Current	V_{IN} = V_{DD} ~ V_{EE}	-10	-	10	uA	V1 ~ V4

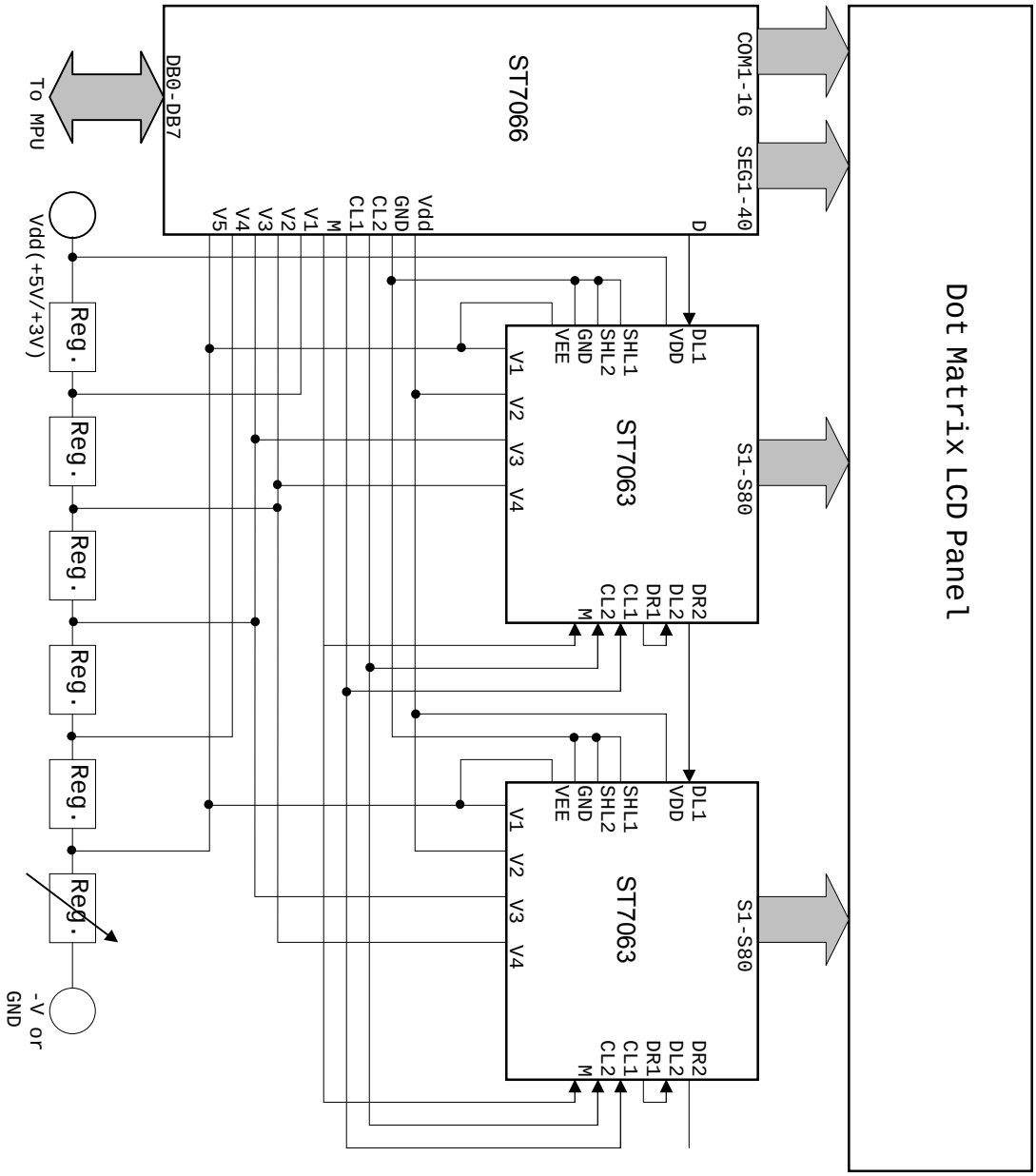
A.C Characteristics

Symbol	Parameter	Test Condition	Min.	Max.	Unit	Applicable pin
F_{CL}	Data Shift Frequency	-	-	400	K_{HZ}	CL2
T_{WCKH}	Clock High Level Width	-	800	-	ns	CL1,CL2
T_{WCKL}	Clock Low Level Width	-	800	-	ns	CL2
T_{SL}	Clock Set-up Time	CL2 → CL1	500	-	ns	CL1,CL2
T_{LS}	Clock Set-up Time	CL1 → CL2	500	-	ns	CL1,CL2
T_R/T_F	Clock Rise/Fall Time	-	-	200	ns	CL1,CL2
T_{SU}	Data Set-up Time	-	300	-	ns	DL1,DL2,DR1,DR2
T_{DH}	Data Hold Time	-	300	-	ns	DL1,DL2,DR1,DR2
T_D	Data Delay Time	CL = 15 pF	-	500	ns	DL1,DL2,DR1,DR2

Maximum Absolute Ratings

Symbol	Parameters	Min.	Max.	Unit
V_{DD}	Supply Voltage	-0.3	7	V
T_{OPR}	Operating Temperature	-20	75	^{0}C
T_{STG}	Storage Temperature	-55	125	^{0}C

Application Circuit : (2Line x 40Word)



Note: R= 2.2K ~ 10K, VR= 1K~30K

PACKAGE DIMENSIONS

100-QFP-1420C