Sitronix

ST7525

192 x 65 Dot Matrix LCD Controller/Driver

1. INTRODUCTION

ST7525 is a driver & controller LSI for graphic dot-matrix liquid crystal display systems. It contains 192-segment and 64-common with 1-icon-common driver circuits. This chip is connected directly to a microprocessor which accepts parallel interface (8-bit), serial peripheral interface (4-line SPI), I^2C interface. Display data stores in an on-chip display data RAM (DDRAM) of 192 x 65 bits. It performs Display Data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits to drive liquid crystal, it is possible to make a display system with the fewest components.

2. FEATURES

Single-chip LCD Controller & Driver

Driver Output Circuits

- 192-segment / 64-common+1-icon-common

On-chip Display Data RAM (DDRAM)

- Capacity: 192x65= 12,480 bits

Microprocessor Interface

- 8-bit parallel bi-directional interface supports 6800-series or 8080-series MPU
- 4-line SPI
- I^2C Interface

Built-in Oscillation Circuit

- Oscillator requires no external component
- Programmable frame frequency

External RST (hardware reset) Pin

Various Display Functions

- Partial display

Low Power Consumption Analog Circuit

- Voltage booster with internal capacitor (X6)
- Wide voltage regulator output range (4.78V~11.5V)
- Built-in temperature compensation circuit
  Voltage Gradient: -0.05%/℃
- Built-in voltage follower for LCD bias voltages: 1/6 ~ 1/9 Bias

Wide Supply Voltage Range

- Digital Power (VDD1): 1.8V~3.3V (typical)
- Analog Power (VDD2,VDD3): 2.7V~3.3V (typical)

Temperature Range: -30℃ ~ +80℃

Package: COG

ST7525	**6800 , 8080 , 4-Line Interface (without I^2C Interface)**
ST7525i	**I^2C Interface**

3. PAD ARRANGEMENT

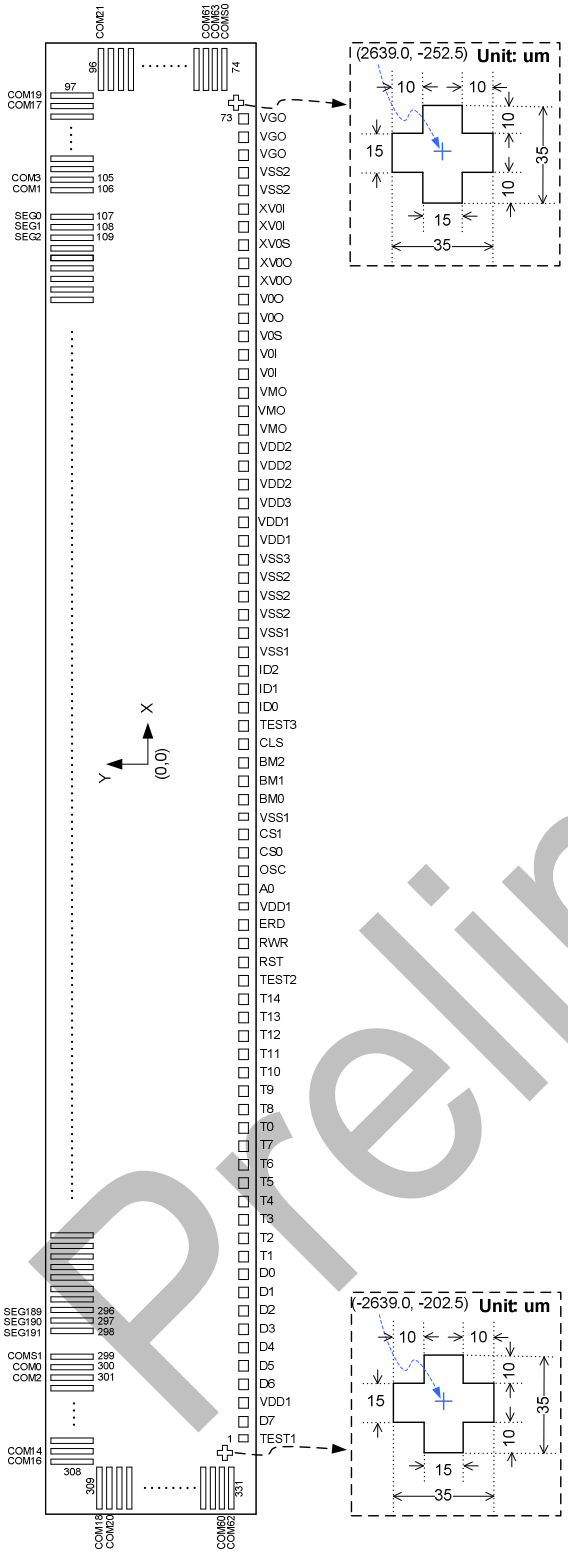


Fig 1.

Chip Size: um 7100x 660um **Unit: um**

Chip Thickness: 300um **Bump Height: 9um**

PAD No.	Bump Size
1, 30, 35	35 X 45
2~10, 26~29, 31~34, 36~73	60 X 45
11~25	45 X 45
74~96, 97~106, 107~298, 299~308, 309~331	13 X120

PAD No.	Bump Pitch (min)
1, 30, 35	62.5
2~10, 26~29, 31~34, 36~73	75
11~25	60
74~96, 97~106, 107~298, 299~308, 309~331	25

*** Refer "PAD CENTER COORDINATES" section for ITO layout.**

4. PAD CENTER COORDINATES

PAD NO.	PAD NAME	X	Y
1	TEST1	-2562.5	-274.5
2	D7	-2500	-274.5
3	VDD1	-2425	-274.5
4	D6	-2350	-274.5
5	D5	-2275	-274.5
6	D4	-2200	-274.5
7	D3	-2125	-274.5
8	D2	-2050	-274.5
9	D1	-1975	-274.5
10	D0	-1900	-274.5
11	T1	-1832.5	-274.5
12	T2	-1772.5	-274.5
13	T3	-1712.5	-274.5
14	T4	-1652.5	-274.5
15	T5	-1592.5	-274.5
16	T6	-1532.5	-274.5
17	T7	-1472.5	-274.5
18	T0	-1412.5	-274.5
19	T8	-1352.5	-274.5
20	T9	-1292.5	-274.5
21	T10	-1232.5	-274.5
22	T11	-1172.5	-274.5
23	T12	-1112.5	-274.5
24	T13	-1052.5	-274.5
25	T14	-992.5	-274.5
26	TEST2	-925	-274.5
27	RST	-850	-274.5
28	RWR	-775	-274.5
29	ERD	-700	-274.5
30	VDD1	-637.5	-274.5
31	A0	-575	-274.5
32	OSC	-500	-274.5
33	CS0	-425	-274.5
34	CS1	-350	-274.5
35	VSS1	-287.5	-274.5
36	BM0	-225	-274.5
37	BM1	-150	-274.5
38	BM2	-75	-274.5
39	CLS	0	-274.5
40	TEST3	75	-274.5
41	ID0	150	-274.5

PAD NO.	PAD NAME	X	Y
42	ID1	225	-274.5
43	ID2	300	-274.5
44	VSS1	375	-274.5
45	VSS1	450	-274.5
46	VSS2	525	-274.5
47	VSS2	600	-274.5
48	VSS2	675	-274.5
49	VSS3	750	-274.5
50	VDD1	825	-274.5
51	VDD1	900	-274.5
52	VDD3	975	-274.5
53	VDD2	1050	-274.5
54	VDD2	1125	-274.5
55	VDD2	1200	-274.5
56	VMO	1275	-274.5
57	VMO	1350	-274.5
58	VMO	1425	-274.5
59	V0I	1500	-274.5
60	V0I	1575	-274.5
61	V0S	1650	-274.5
62	V0O	1725	-274.5
63	V0O	1800	-274.5
64	XV0O	1875	-274.5
65	XV0O	1950	-274.5
66	XV0S	2025	-274.5
67	XV0I	2100	-274.5
68	XV0I	2175	-274.5
69	VSS2	2250	-274.5
70	VSS2	2325	-274.5
71	VGO	2400	-274.5
72	VGO	2475	-274.5
73	VGO	2550	-274.5
74	COMS0	2937	-277.5
75	COM63	2937	-252.5
76	COM61	2937	-227.5
77	COM59	2937	-202.5
78	COM57	2937	-177.5
79	COM55	2937	-152.5
80	COM53	2937	-127.5
81	COM51	2937	-102.5
82	COM49	2937	-77.5

PAD NO.	PAD NAME	X	Y
83	COM47	2937	-52.5
84	COM45	2937	-27.5
85	COM43	2937	-2.5
86	COM41	2937	22.5
87	COM39	2937	47.5
88	COM37	2937	72.5
89	COM35	2937	97.5
90	COM33	2937	122.5
91	COM31	2937	147.5
92	COM29	2937	172.5
93	COM27	2937	197.5
94	COM25	2937	222.5
95	COM23	2937	247.5
96	COM21	2937	272.5
97	COM19	2664	237
98	COM17	2639	237
99	COM15	2614	237
100	COM13	2589	237
101	COM11	2564	237
102	COM9	2539	237
103	COM7	2514	237
104	COM5	2489	237
105	COM3	2464	237
106	COM1	2439	237
107	SEG0	2387.5	237
108	SEG1	2362.5	237
109	SEG2	2337.5	237
110	SEG3	2312.5	237
111	SEG4	2287.5	237
112	SEG5	2262.5	237
113	SEG6	2237.5	237
114	SEG7	2212.5	237
115	SEG8	2187.5	237
116	SEG9	2162.5	237
117	SEG10	2137.5	237
118	SEG11	2112.5	237
119	SEG12	2087.5	237
120	SEG13	2062.5	237
121	SEG14	2037.5	237
122	SEG15	2012.5	237
123	SEG16	1987.5	237
124	SEG17	1962.5	237
125	SEG18	1937.5	237
126	SEG19	1912.5	237

PAD NO.	PAD NAME	X	Y
127	SEG20	1887.5	237
128	SEG21	1862.5	237
129	SEG22	1837.5	237
130	SEG23	1812.5	237
131	SEG24	1787.5	237
132	SEG25	1762.5	237
133	SEG26	1737.5	237
134	SEG27	1712.5	237
135	SEG28	1687.5	237
136	SEG29	1662.5	237
137	SEG30	1637.5	237
138	SEG31	1612.5	237
139	SEG32	1587.5	237
140	SEG33	1562.5	237
141	SEG34	1537.5	237
142	SEG35	1512.5	237
143	SEG36	1487.5	237
144	SEG37	1462.5	237
145	SEG38	1437.5	237
146	SEG39	1412.5	237
147	SEG40	1387.5	237
148	SEG41	1362.5	237
149	SEG42	1337.5	237
150	SEG43	1312.5	237
151	SEG44	1287.5	237
152	SEG45	1262.5	237
153	SEG46	1237.5	237
154	SEG47	1212.5	237
155	SEG48	1187.5	237
156	SEG49	1162.5	237
157	SEG50	1137.5	237
158	SEG51	1112.5	237
159	SEG52	1087.5	237
160	SEG53	1062.5	237
161	SEG54	1037.5	237
162	SEG55	1012.5	237
163	SEG56	987.5	237
164	SEG57	962.5	237
165	SEG58	937.5	237
166	SEG59	912.5	237
167	SEG60	887.5	237
168	SEG61	862.5	237
169	SEG62	837.5	237
170	SEG63	812.5	237

PAD NO.	PAD NAME	X	Y
171	SEG64	787.5	237
172	SEG65	762.5	237
173	SEG66	737.5	237
174	SEG67	712.5	237
175	SEG68	687.5	237
176	SEG69	662.5	237
177	SEG70	637.5	237
178	SEG71	612.5	237
179	SEG72	587.5	237
180	SEG73	562.5	237
181	SEG74	537.5	237
182	SEG75	512.5	237
183	SEG76	487.5	237
184	SEG77	462.5	237
185	SEG78	437.5	237
186	SEG79	412.5	237
187	SEG80	387.5	237
188	SEG81	362.5	237
189	SEG82	337.5	237
190	SEG83	312.5	237
191	SEG84	287.5	237
192	SEG85	262.5	237
193	SEG86	237.5	237
194	SEG87	212.5	237
195	SEG88	187.5	237
196	SEG89	162.5	237
197	SEG90	137.5	237
198	SEG91	112.5	237
199	SEG92	87.5	237
200	SEG93	62.5	237
201	SEG94	37.5	237
202	SEG95	12.5	237
203	SEG96	-12.5	237
204	SEG97	-37.5	237
205	SEG98	-62.5	237
206	SEG99	-87.5	237
207	SEG100	-112.5	237
208	SEG101	-137.5	237
209	SEG102	-162.5	237
210	SEG103	-187.5	237
211	SEG104	-212.5	237
212	SEG105	-237.5	237
213	SEG106	-262.5	237
214	SEG107	-287.5	237

PAD NO.	PAD NAME	X	Y
215	SEG108	-312.5	237
216	SEG109	-337.5	237
217	SEG110	-362.5	237
218	SEG111	-387.5	237
219	SEG112	-412.5	237
220	SEG113	-437.5	237
221	SEG114	-462.5	237
222	SEG115	-487.5	237
223	SEG116	-512.5	237
224	SEG117	-537.5	237
225	SEG118	-562.5	237
226	SEG119	-587.5	237
227	SEG120	-612.5	237
228	SEG121	-637.5	237
229	SEG122	-662.5	237
230	SEG123	-687.5	237
231	SEG124	-712.5	237
232	SEG125	-737.5	237
233	SEG126	-762.5	237
234	SEG127	-787.5	237
235	SEG128	-812.5	237
236	SEG129	-837.5	237
237	SEG130	-862.5	237
238	SEG131	-887.5	237
239	SEG132	-912.5	237
240	SEG133	-937.5	237
241	SEG134	-962.5	237
242	SEG135	-987.5	237
243	SEG136	-1012.5	237
244	SEG137	-1037.5	237
245	SEG138	-1062.5	237
246	SEG139	-1087.5	237
247	SEG140	-1112.5	237
248	SEG141	-1137.5	237
249	SEG142	-1162.5	237
250	SEG143	-1187.5	237
251	SEG144	-1212.5	237
252	SEG145	-1237.5	237
253	SEG146	-1262.5	237
254	SEG147	-1287.5	237
255	SEG148	-1312.5	237
256	SEG149	-1337.5	237
257	SEG150	-1362.5	237
258	SEG151	-1387.5	237

PAD NO.	PAD NAME	X	Y
259	SEG152	-1412.5	237
260	SEG153	-1437.5	237
261	SEG154	-1462.5	237
262	SEG155	-1487.5	237
263	SEG156	-1512.5	237
264	SEG157	-1537.5	237
265	SEG158	-1562.5	237
266	SEG159	-1587.5	237
267	SEG160	-1612.5	237
268	SEG161	-1637.5	237
269	SEG162	-1662.5	237
270	SEG163	-1687.5	237
271	SEG164	-1712.5	237
272	SEG165	-1737.5	237
273	SEG166	-1762.5	237
274	SEG167	-1787.5	237
275	SEG168	-1812.5	237
276	SEG169	-1837.5	237
277	SEG170	-1862.5	237
278	SEG171	-1887.5	237
279	SEG172	-1912.5	237
280	SEG173	-1937.5	237
281	SEG174	-1962.5	237
282	SEG175	-1987.5	237
283	SEG176	-2012.5	237
284	SEG177	-2037.5	237
285	SEG178	-2062.5	237
286	SEG179	-2087.5	237
287	SEG180	-2112.5	237
288	SEG181	-2137.5	237
289	SEG182	-2162.5	237
290	SEG183	-2187.5	237
291	SEG184	-2212.5	237
292	SEG185	-2237.5	237
293	SEG186	-2262.5	237
294	SEG187	-2287.5	237
295	SEG188	-2312.5	237
296	SEG189	-2337.5	237

PAD NO.	PAD NAME	X	Y
297	SEG190	-2362.5	237
298	SEG191	-2387.5	237
299	COMS1	-2439	237
300	COM0	-2464	237
301	COM2	-2489	237
302	COM4	-2514	237
303	COM6	-2539	237
304	COM8	-2564	237
305	COM10	-2589	237
306	COM12	-2614	237
307	COM14	-2639	237
308	COM16	-2664	237
309	COM18	-2937	272.5
310	COM20	-2937	247.5
311	COM22	-2937	222.5
312	COM24	-2937	197.5
313	COM26	-2937	172.5
314	COM28	-2937	147.5
315	COM30	-2937	122.5
316	COM32	-2937	97.5
317	COM34	-2937	72.5
318	COM36	-2937	47.5
319	COM38	-2937	22.5
320	COM40	-2937	-2.5
321	COM42	-2937	-27.5
322	COM44	-2937	-52.5
323	COM46	-2937	-77.5
324	COM48	-2937	-102.5
325	COM50	-2937	-127.5
326	COM52	-2937	-152.5
327	COM54	-2937	-177.5
328	COM56	-2937	-202.5
329	COM58	-2937	-227.5
330	COM60	-2937	-252.5
331	COM62	-2937	-277.5

Note: Unit: um

5. BLOCK DIAGRAM

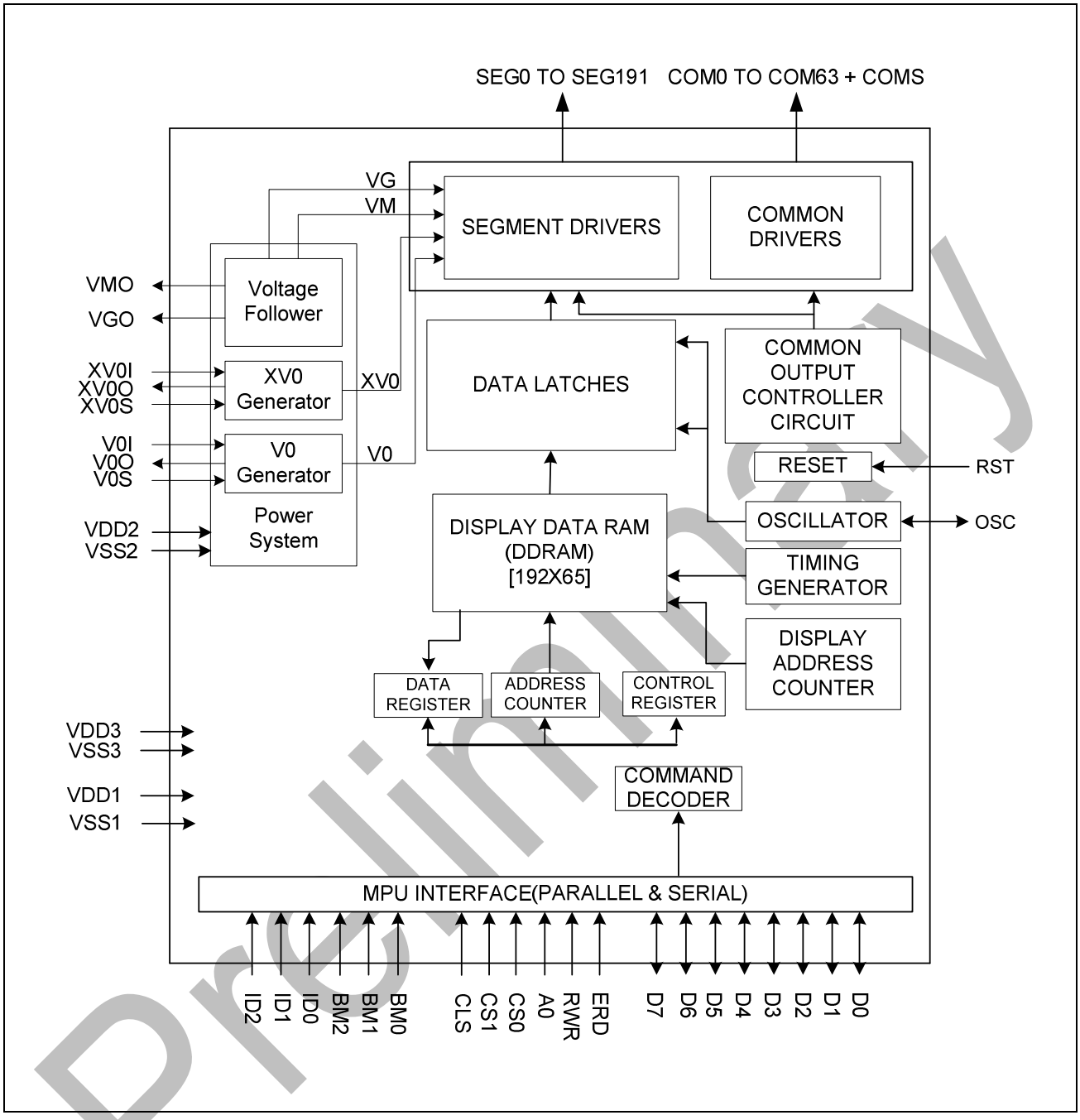


Fig 2. Block Diagram

6. PIN DESCRIPTIONS

LCD Driver Output Pins

<table>
<tr><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td>SEG[0:191]</td><td>O</td><td>LCD segment driver outputs.
The display data and the frame control the output voltage.
<table>
<tr><th rowspan="2">Display data</th><th rowspan="2">Frame</th><th colspan="2">Segment driver output voltage</th></tr>
<tr><th>Normal display</th><th>Reverse display</th></tr>
<tr><td>H</td><td>+</td><td>VG</td><td>VSS</td></tr>
<tr><td>H</td><td>-</td><td>VSS</td><td>VG</td></tr>
<tr><td>L</td><td>+</td><td>VSS</td><td>VG</td></tr>
<tr><td>L</td><td>-</td><td>VG</td><td>VSS</td></tr>
<tr><td colspan="2">Display OFF (Power Save)</td><td>VSS</td><td>VSS</td></tr>
</table></td></tr>
<tr><td>COM[0:63]</td><td>O</td><td>LCD common driver outputs.
The internal scanning signal and the frame control the output voltage.
<table>
<tr><th rowspan="2">Scan signal</th><th rowspan="2">Frame</th><th colspan="2">Common driver output voltage</th></tr>
<tr><th>Normal display</th><th>Reverse display</th></tr>
<tr><td>H</td><td>+</td><td colspan="2">XV0</td></tr>
<tr><td>H</td><td>-</td><td colspan="2">V0</td></tr>
<tr><td>L</td><td>+</td><td colspan="2">VM</td></tr>
<tr><td>L</td><td>-</td><td colspan="2">VM</td></tr>
<tr><td colspan="2">Display OFF (Power Save)</td><td colspan="2">VSS</td></tr>
</table></td></tr>
<tr><td>COMS1, COMS2
(COMS)</td><td>O</td><td>LCD common driver outputs for icons. These two pins are identical. Choose one of them if using icon. When icon is not used, left these pins open.</td></tr>
</table>

Clock System Input

Pin Name	Type	Description
CLS	**I**	Clock source selection pin. CLS=”H” : enable internal clock. CLS=”L” : disable internal clock and use external clock.
OSC	**I/O**	For external clock. If CLS=”H” : this pin should be left open. If CLS=”L” : this pin should apply the external clock (for testing only).

Power Supply Pins

Pin Name	Type	Description
VDD1	**Power**	Digital power. If VDD1=VDD2, connect to VDD2 by FPC. For select pins that are set to be “H”, connect them to this power (use VDD1 for “H”).
VDD2	**Power**	Analog power. If VDD1=VDD2, connect to VDD1 by FPC.
VDD3	**Power**	Analog power. Connect to VDD2 by FPC.
VSS1	**Power**	Digital ground. Connect to VSS2 by FPC. For select pins that are set to be “L”, connect them to this power (use VSS1 for “L”).
VSS2	**Power**	Analog ground. Connect to VSS1 by FPC.
VSS3	**Power**	Analog ground. Connect to VSS1 by FPC.

Built-in Power System Pins

<table>
<tr><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td>V0O
V0I
V0S</td><td>Power</td><td>LCD driving voltage for commons at negative frame.
V0O, V0I & V0S should be separated in ITO layout.
V0O, V0I & V0S should be connected together in FPC layout.</td></tr>
<tr><td>XV0O
XV0I
XV0S</td><td>Power</td><td>LCD driving voltage for commons at positive frame.
XV0O, XV0I & XV0S should be separated in ITO layout.
XV0O, XV0I & XV0S should be connected together in FPC layout.</td></tr>
<tr><td>VGO</td><td>Power</td><td>LCD driving voltage for segments.
Be aware that: 1.8 ≤ VG < VDD2-0.4V.</td></tr>
<tr><td>VMO</td><td>Power</td><td>LCD driving voltage for commons.
Be aware that: 0.9 ≤ VM < VG.
When the internal power circuit is active, the VG and VM are generated according to the bias setting as shown below:
<table>
<tr><th>LCD bias</th><th>VG</th><th>VM</th></tr>
<tr><td>1/N bias</td><td>(2/N) x V0</td><td>(1/N) x V0</td></tr>
</table>
</td></tr>
</table>

Microprocessor Interface Pins

<table>
<tr><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td>BM[2:0]</td><td>I</td><td>Microprocessor interface select pins.
<table>
<tr><th>D7</th><th>BM2</th><th>BM1</th><th>BM0</th><th>Interface Mode</th></tr>
<tr><td>H</td><td>--</td><td>L</td><td>L</td><td>4-line serial interface</td></tr>
<tr><td>H</td><td>--</td><td>L</td><td>H</td><td>I^2C serial interface</td></tr>
<tr><td>D7</td><td>H</td><td>H</td><td>L</td><td>8-bit 8080 parallel interface</td></tr>
<tr><td>D7</td><td>H</td><td>H</td><td>H</td><td>8-bit 6800 parallel interface</td></tr>
</table>
Note : The un-used pins are marked as “--” and should be fixed to “H” or “L” by VDD1 or VSS1.</td></tr>
<tr><td>RST</td><td>I</td><td>Reset input pin.
When RST is “L”, internal initialization is executed.</td></tr>
<tr><td>CS[1:0]</td><td>I</td><td>Chip select input pins and slave address pins (I^2C).
Interface access is enabled when CS0 is “L” and CS1 is “H” in parallel interface (8080/6800) and SPI interface (4-SPI).
CS[1:0] pins are used for slave address pins (SA[1:0]) in I^2C.</td></tr>
<tr><td>A0</td><td>I</td><td>It determines whether the access is related to data or command.
A0=“H” : Indicates that D[7:0] are display data.
A0=“L” : Indicates that D[7:0] are control data.
There is no A0 pin in I^2C interface and should fix to “H” by VDD1.</td></tr>
</table>

<table>
<tr><td>RWR</td><td>I</td><td>Read/Write execution control pin. When parallel interface is selected:
<table>
<tr><th>MPU Type</th><th>RWR</th><th>Description</th></tr>
<tr><td>6800 series</td><td>R/W</td><td>Read/Write control input pin.
R/W=“H”: read.
R/W=“L”: write.</td></tr>
<tr><td>8080 series</td><td>/WR</td><td>Write enable input pin.
Signals on D[7:0] will be latched at the rising edge of /WR signal.</td></tr>
</table>
Note : RWR is not used in serial interfaces and should fix to “H” by VDD1.</td></tr>
<tr><td>ERD</td><td>I</td><td>Read/Write execution control pin. When parallel interface is selected:
<table>
<tr><th>MPU Type</th><th>ERD</th><th>Description</th></tr>
<tr><td>6800 series</td><td>E</td><td>Read/Write control input pin.
R/W=”H“: When E is “H”, D[7:0] are in an output status.
R/W=”L“: Signals on D[7:0] are latched at the falling edge of E signal.</td></tr>
<tr><td>8080 series</td><td>/RD</td><td>Read enable input pin.
When /RD is “L”, D[7:0] are in output status.</td></tr>
</table>
Note : ERD is not used in serial interfaces and should fix to “H” by VDD1.</td></tr>
<tr><td rowspan="3">D[7:0]</td><td>I/O</td><td>When using 8-bit parallel interface: 6800 or 8080 mode
8-bit bi-directional data bus. Connect to the data bus of 8-bit microprocessor.
Note :When CS0 is non-active (CS0=“H”), D[7:0] pins are high impedance.</td></tr>
<tr><td>I/O</td><td>When using serial interface: 4-line SPI mode
D[0] : serial input clock (SCL).
D[3:1] : serial input data (SDA).
D[4] : serial input clock (SCL).
D[7:5] : fix to “H” by VDD1.
<u>D0 and D4 must be connected together for SCL.</u>
<u>D1 to D3 must be connected together for SDA.</u>
Note : When CS0 is non-active (CS0=“H”), D[7:0] pins are high impedance.</td></tr>
<tr><td>I/O</td><td>When using I²C interface
D[0] : SCL, serial clock input.
D[1] : SDA_IN, serial input data.
D[3:2] : SDA_ OUT, serial data acknowledge for the I²C interface.
D[4] : SCL, serial clock input.
D[7:5] : fix to “H” by VDD1.
<u>D0 and D4 must be connected together for SCL.</u>
<u>D1 to D3 must be connected together for SDA.</u>
Note : SA[1:0] = CS[1:0], I²C slave address bits of ST7525. Must connect to VDD1 or VSS1.</td></tr>
</table>

Note:

1. By connecting SDA_OUT to SDA_IN externally, the SDA line becomes fully I^{2}C interface compatible. Separating acknowledge-output from serial data input is advantageous for chip-on-glass (COG) applications. In COG applications, the ITO resistance and the pull-up resistor will form a voltage divider, which affects acknowledge-signal level. Larger ITO resistance will raise the acknowledged-signal level and system cannot recognize this level as a valid logic “0” level. By separating SDA_IN from SDA_OUT, the IC can be used in a mode that ignores the acknowledge-bit. For applications which check acknowledge-bit, it is necessary to minimize the ITO resistance of the SDA_OUT trace to guarantee a valid low level.
2. After VDD1 is turned ON, any MPU interface pins cannot be left floating.

Test Pin

Pin Name	Type	Description
T[0]	**Test**	This pin is reserved for test only, recommend connecting to TEST[1].
T[14:1]	**Test**	These pins are reserved for test only, recommend setting to floating.
ID[2:0]	**Test**	These pins are reserved for test only, recommend setting to VSS1.
TEST[1]	**Test**	This pin is reserved for test only, recommend connecting to T[0].
TEST[2]	**Test**	This pin is reserved for test only, recommend setting to floating.
TEST[3]	**Test**	This pin is reserved for test only, recommend setting to VDD1.

Recommend ITO Resistance

Pin Name	ITO Resistance
VDD1, VDD2, VSS1, VSS2	< 100Ω
VMO, VGO, V0(V0I, V0O, V0S), XV0(XV0I, XV0O, XV0S), VDD3, VSS3, SDA(I^2C), SCL(I^2C)	< 100Ω
A0, RWR, ERD, CS[1:0], D[7:0], T[14:0], TEST[2:1]	< 1KΩ
BM[2:0], ID[2:0], TEST[3], OSC, CLS	< 5KΩ
RST *1	3KΩ ~ 10KΩ

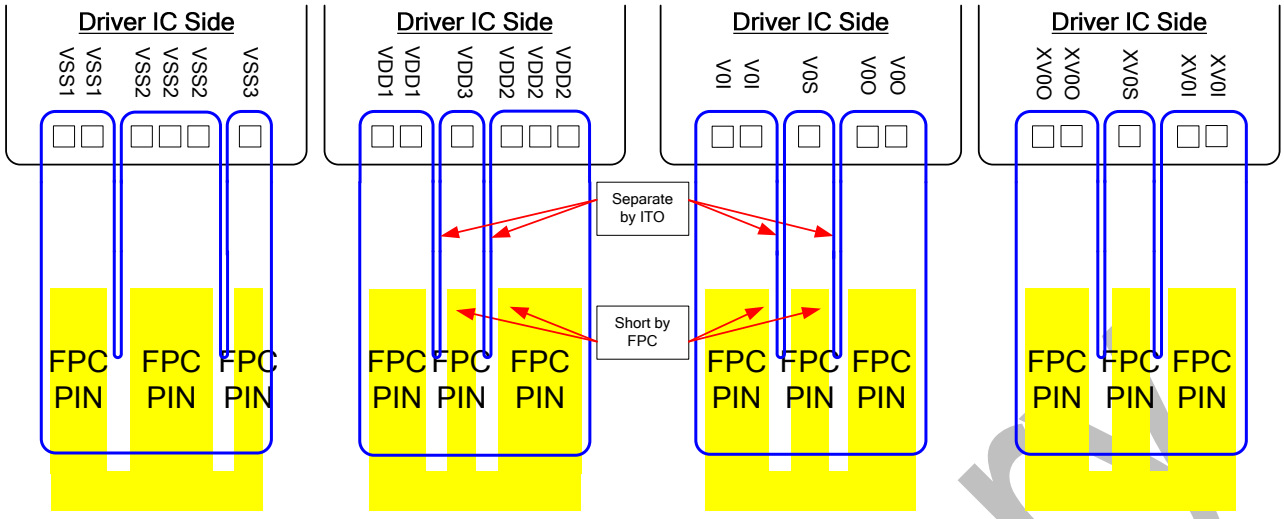
Note:

1. The RST pin has the most priority over other control signals. It is important to prevent the ESD pulse or external noise flow into this pin. By adding a series resistor externally or increase the ITO resistance at this pin, the unexpected reset condition can be solved. The recommended resistance is around 3K~10K Ohm (the optimized value depends on the LCD module and application system).
2. If using I^2C interface mode, the resistance of SDA signal is recommended to be lower than 100Ω (if the system pull up resistor is 4.7KΩ).
3. If using 4-Line SPI interface with VDD1 less than 2.4V, the SDA signal resistance should be less than 100Ω.
4. This table defines the actual ITO resistance. The actual ITO resistance should in these ranges, not the calculated ITO resistance value. The ITO tolerance should be considered.
5. The option setting to be “H” should connect to VDD1.
6. The option setting to be “L” should connect to VSS1.

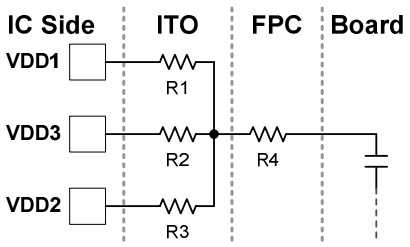
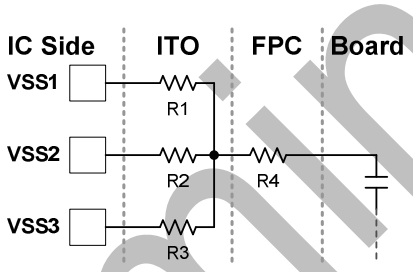
ITO Layout Notes

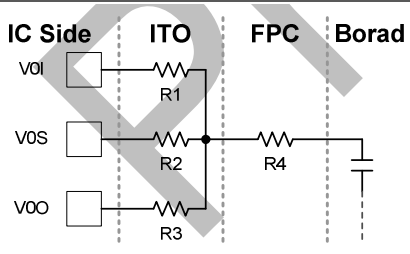
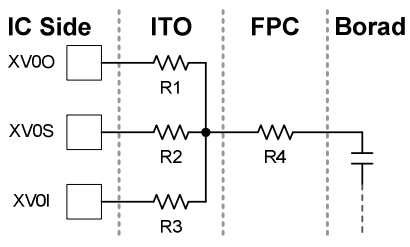
1. The Limitations include the bottleneck of ITO layout.
2. Make sure that the ITO resistance of all COM outputs are equal, and so are SEG outputs.
3. To avoid the noise in different power systems affect other power system, please separate them on ITO layout.
4. The V0 and XV0 circuits have output pins, input pins and a sensor input. To avoid the power noise affects the sensor of the power circuits. The trace should be separated by ITO and should be connected together by FPC. The FPC layout and the equivalent circuit are shown below:

The FPC layout is shown below:



The equivalent circuit is shown below:

VDD	VSS
	
Ideal Layout: => R4=0 Ohm. R2>>R1>R3. **Acceptable Layout:** => R4≠0. R2>>R1>R3>R4. **Not Acceptable:** => R4 ≥ (R1 or R2 or R3).	**Ideal Layout:** => R4=0 Ohm. R3>>R1>R2. **Acceptable Layout:** => R4≠0. R3>>R1>R2>R4. **Not Acceptable:** => R4 ≥ (R1 or R2 or R3).

V0	XV0
	
Ideal Layout: => R4=0 Ohm. R2>>R3>R1. **Acceptable Layout:** => R4≠0. R2>>R3>R1>R4. **Not Acceptable:** => R4 ≥ (R1 or R2 or R3).	**Ideal Layout:** => R4=0 Ohm. R2>>R1>R3. **Acceptable Layout:** => R4≠0. R2>>R1>R3>R4. **Not Acceptable:** => R4 ≥ (R1 or R2 or R3).

7. FUNCTIONS DESCRIPTION

Microprocessor Interface

Chip Select Input

CS0 and CS1 pins are used for chip selection. ST7525 can interface with an MPU when CS0 is "L" and CS1 is “H”. When CS0 is “H”, the inputs of A0, ERD and RWR with any combination will be ignored and D[7:0] are high impedance. In 4-Line serial interface, the internal shift register and serial counter are reset when CS0 is “H”.

Parallel / Serial Interface

ST7525 has types of interface for kinds of MPU. The MPU interface is selected by BM[2:0] and D7 pins as shown in Table 1.

Table 1. Parallel/Serial Interface Mode

Type	D7	BM2	BM1	BM0	Interface mode
Parallel	D7	H	H	L	8bit 8080-series MPU mode
	D7	H	H	H	8 bit 6800-series MPU mode
Serial	H	--	L	L	4-line serial interface
	H	--	L	H	I^2C serial interface

Note : The un-used pins are marked as “--” and should be fixed to “H” or “L” by VDD1 or VSS1.

Parallel Interface

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by BM[2:0] as shown in Table 2. The data transfer type is determined by signals of A0, ERD and RWR as shown in Table 3.

Table 2. Microprocessor Selection for Parallel Interface

BM2	BM1	BM0	CS0	CS1	A0	ERD	RWR	D[7:0]	MPU Interface
H	H	L	CS0	CS1	A0	/RD	/WR	D[7:0]	8080-series
H	H	H				E	R/W		6800-series

Table 3. Parallel Data Transfer

Common	6800-series		8080-series		Description
A0	E (ERD)	R/W (RWR)	/RD (ERD)	/WR (RWR)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Internal status read
L	H	L	H	L	Writes to internal register (instruction)

Setting Serial Interface

Interface	CS0	CS1	A0	ERD	RWR	D[7:0]
4-Line SPI	CS0	CS1	A0	--	--	D[7:5]=fix to “H” , D[4]=SCL, D[3:1]=SDA, D[0]=SCL
I^2C	SA0	SA1	--	--	--	D[7:5]=fix to “H”, D[4]=SCL, D[3:2]= SDA_ OUT, D[1]=SDA_ IN, D[0]=SCL, CS[1:0]=SA[1:0]. Refer to I^2C interface.

* The un-used pins are marked as “--” and should be fixed to “H” by VDD1.

Note:

1. The option setting to be “H” should connect to VDD1.
2. The option setting to be “L” should connect to VSS1.

4-Line Serial interface

ST7525 is active when CS0 is “L” and CS1 is “H”, then serial data (SDA) and serial clock (SCL) inputs are enabled. When CS0 and CS1 are “H”, ST7525 is not active, and the internal 8-bit shift register and 3-bit counter are reset. Display data read feature and some specified information (status byte) are supported in this mode. The DDRAM column address pointer will be increased by one automatically after writing each byte of DDRAM.

The display data/command indication is controlled by the register selection pin (A0). The signals transferred on data bus will be display data when A0 is high and will be instruction when A0 is low. Serial data (SDA) is latched at the rising edge of serial clock (SCL). After the 8th serial clock, the serial data will be processed as 8-bit parallel data. The DDRAM column address pointer will be increased by one automatically after each byte of DDRAM access.

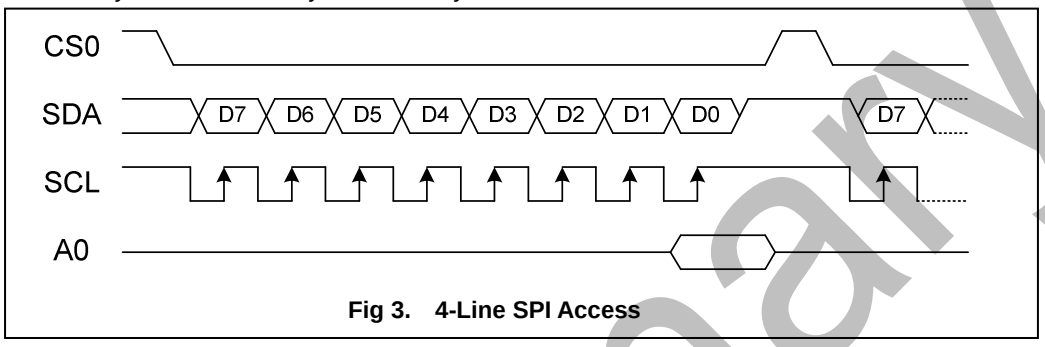


Fig 3. 4-Line SPI Access

I^{2}C Interface

The I^{2}C Interface is for bi-directional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines must be connected with a pull-up resistor which drives SDA and SCL to high when the bus is not busy. Data transfer can be initiated only when the bus is not busy.

BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes of SDA line at this time will be interpreted as START or STOP. Bit transfer is illustrated in Fig 5.

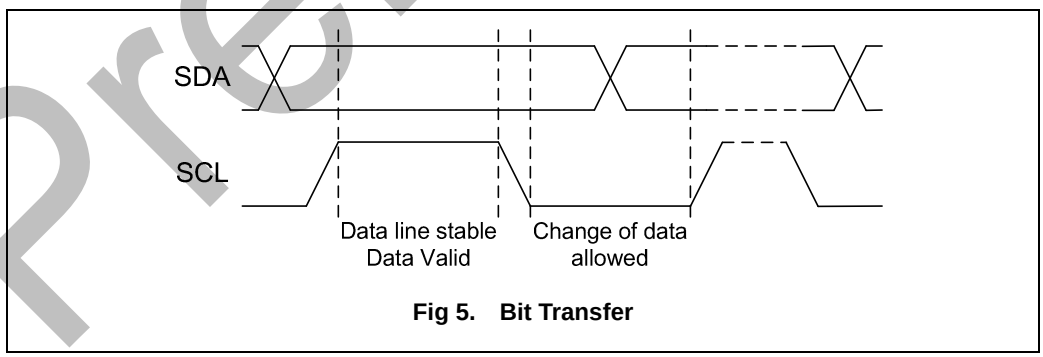


Fig 5. Bit Transfer

START AND STOP CONDITIONS

Both SDA and SCL lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of SDA, while SCL is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of SDA while SCL is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig 6.

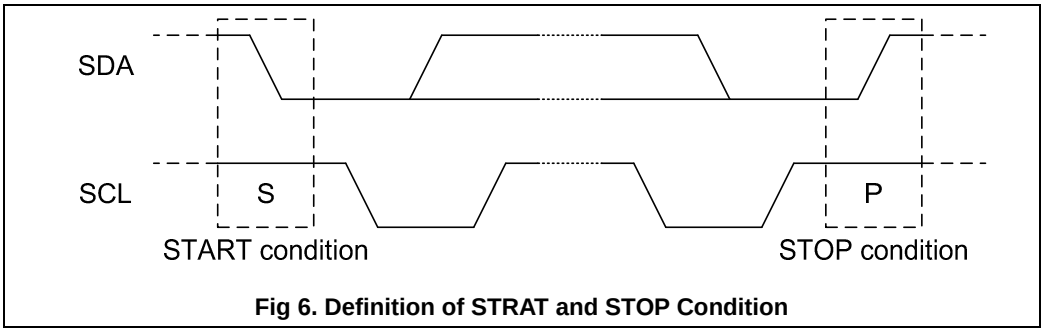


Fig 6. Definition of STRAT and STOP Condition

SYSTEM CONFIGURATION

The system configuration is illustrated in Fig 7. and some word-definitions are explained below:

- Transmitter: the device which sends the data to the bus.
- Receiver: the device which receives the data from the bus.
- Master: the device which initiates a transfer, generates clock signals and terminates a transfer.
- Slave: the device which is addressed by a master.
- Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message.
- Arbitration: the procedure to ensure that, if more than one master tries to control the bus simultaneously, only one is allowed to do so and the message is not corrupted.
- Synchronization: procedure to synchronize the clock signals of two or more devices.

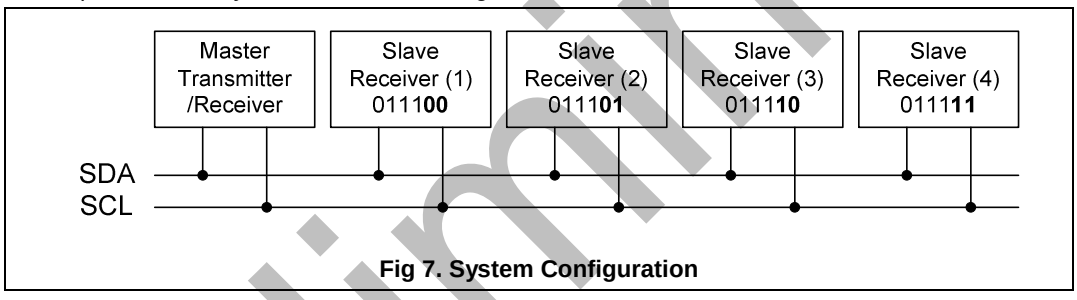


Fig 7. System Configuration

ACKNOWLEDGEMENT

Each byte of eight bits is followed by an acknowledge-bit. The acknowledge-bit is a HIGH signal put on SDA by the transmitter during the time when the master generates an extra acknowledge-related clock pulse. A slave receiver which is addressed must generate an acknowledge-bit after the reception of each byte. A master receiver must also generate an acknowledge-bit after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge-clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge-bit on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the I^2C Interface is illustrated in Fig 8.

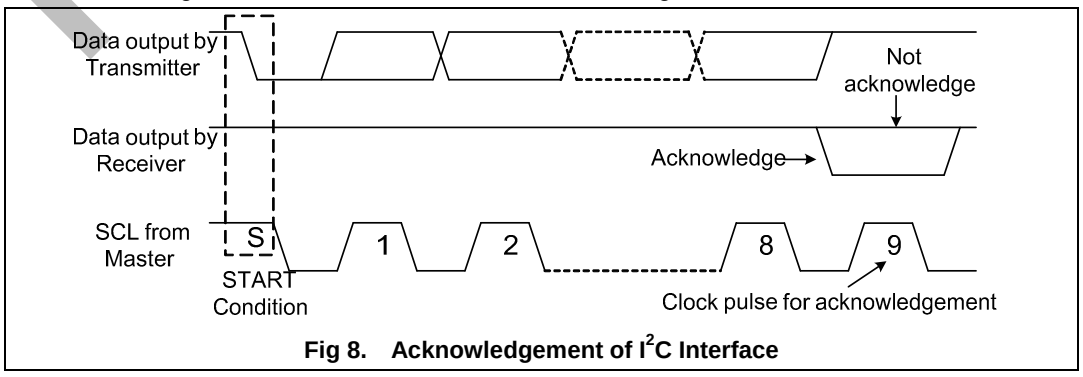


Fig 8. Acknowledgement of I^2C Interface

I²C INTERFACE PROTOCOL

ST7525 supports command/data write to addressed slaves on the bus.

Before any data is transmitted on the I²C Interface, the device, which should respond, is addressed first. Four 6-bit slave addresses (0111**00**, 0111**01**, 0111**10** and 0111**11**) and A0 (011100**0** or 011100**1**) are reserved for ST7525. The bit 2 and bit 1 are slave address that set by connecting SA0 and SA1 to either logic 0 (VSS1) or logic 1 (VDD1). The I²C Interface protocol is illustrated in Fig 9.

The sequence is initiated with a START condition (S) from the I²C Interface master, which is followed by the slave address and A0. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C Interface transfer. After acknowledgement, one or more command or data words are followed and define the status of the addressed slaves.

The slave address and control byte is tagged with a cleared most significant bit. The state of the A0 bit defines whether the following data bytes are interpreted as commands or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte either a series of display data bytes or command data bytes may follow (depending on the A0 bit setting).

If the A0 bit of the last control byte is set to logic 1, these data bytes (display data bytes) will be stored in the display RAM at the address specified by the internal data pointer. The data pointer is automatically updated and the data is directed to the intended ST7525 device.

If the A0 bit of the last control byte is set to logic 0, these data bytes (command data byte) will be decoded and the setting of ST7525 will be changed according to the received commands.

Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the bus master issues a STOP condition (P). If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

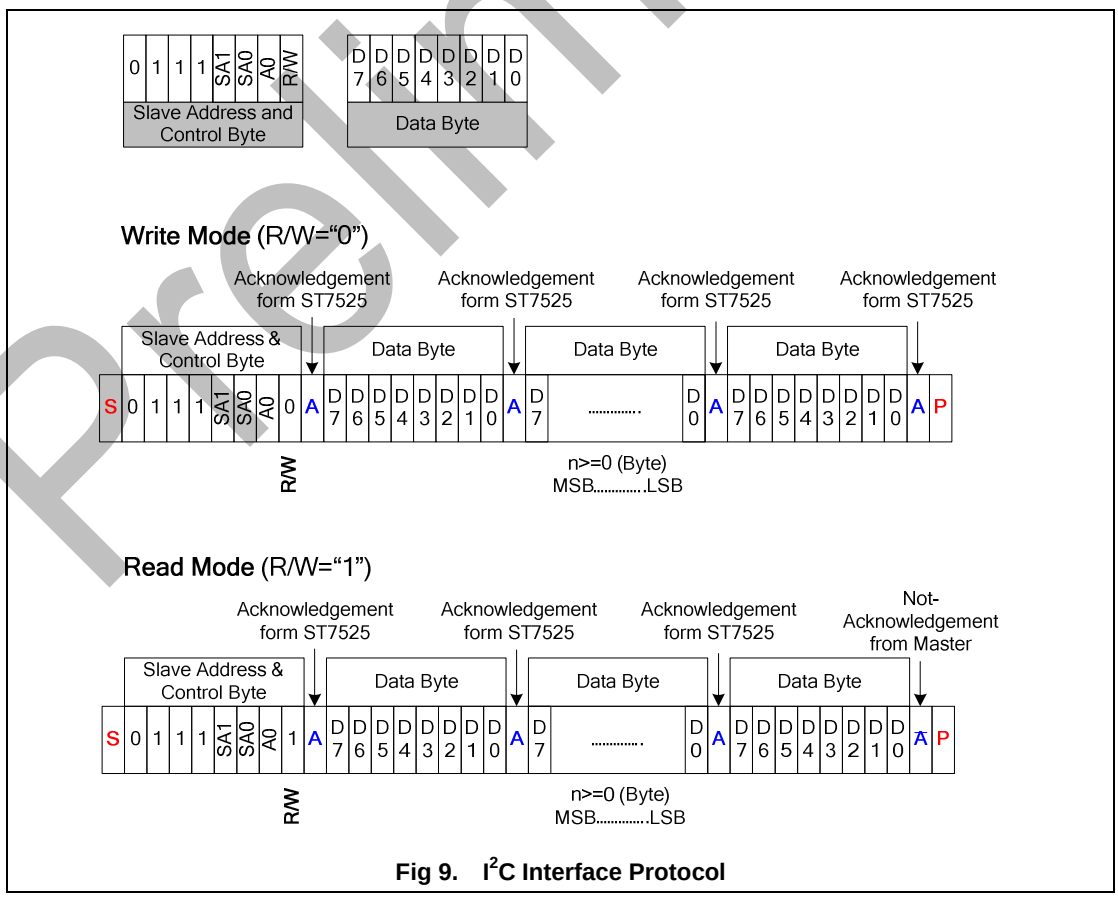


Fig 9. I²C Interface Protocol

Data Transfer

ST7525 uses bus holder and internal data bus for data transfer with MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in Fig 10. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in Fig 11. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

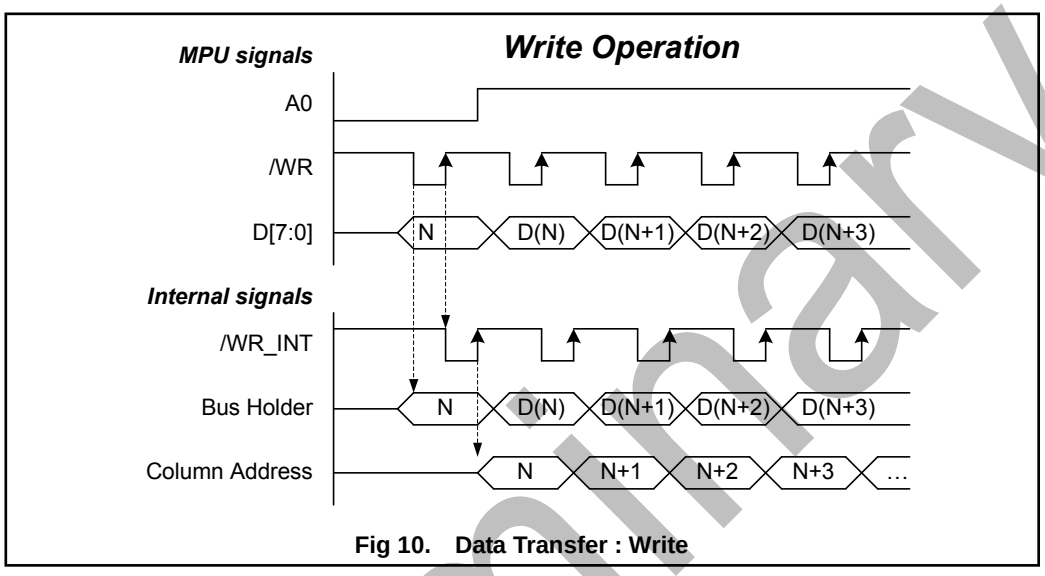


Fig 10. Data Transfer : Write

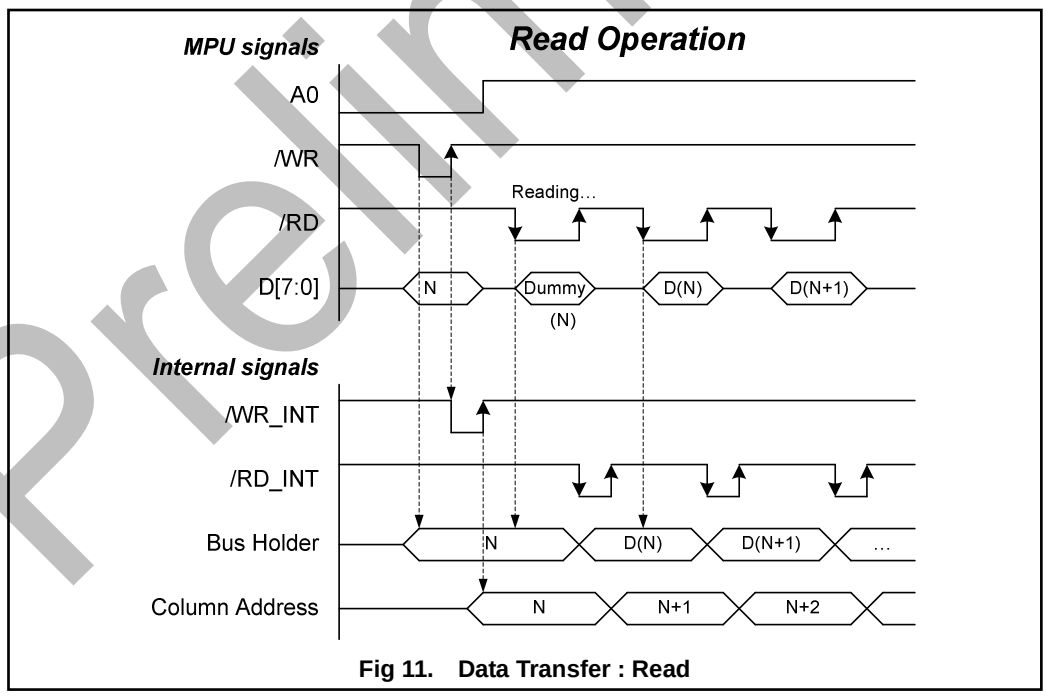


Fig 11. Data Transfer : Read

DISPLAY DATA RAM (DDRAM)

The Display Data RAM stores pixel data for the LCD. It is 65-row by 192-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 65 rows are divided into 8 pages of 8 lines and the 9th page with a single line (D0 only). Data is written to the 8 lines of each page directly through D0 to D7. The display data of D0 to D7 from the microprocessor correspond to the LCD common lines. The LCD controller and MPU interface operate independently, data can be written into RAM at the same time when data is being displayed without flicker on LCD.

Page Address Circuit

This circuit is for providing a Page Address to Display Data RAM. It incorporates 4-bit Page Address register changed by only the "Set Page Address" instruction. The 9th page is a special RAM area for the icons and display data D0 is only valid.

Line Address Circuit

This circuit assigns DDRAM a Line Address corresponding to the first line (COM0) of the display. Therefore, by setting Line Address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on-chip RAM. It incorporates 7-bit Line Address register changed by only the initial display line instruction and 7-bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the line address for transferring the 192-bit RAM data to the display data latch circuit. When icon is selected by setting icon page address, display data of icons are not scrolled because the MPU cannot access Line Address of icons.

Column Address Circuit

Column Address Circuit has a 8-bit preset counter that provides Column Address to the Display Data RAM (DDRAM). The DDRAM column address is specified by the "Set Column Address" command. The specified column address is incremented (+1) with each display data read/write access. This allows the MPU display data to be accessed continuously.

Control flag MY can invert the output order of the COM pads. And the MX flag makes it possible to invert the relationship between the Column Address and the SEG outputs. It is necessary to rewrite the display data into DDRAM after changing MX flag setting.

SEG Output

MX	Segment Pads	
	SEG0	SEG191
0	Col-0 → Column Address → Col-191	
1	Col-191 ← Column Address ← Col-0	

COM Output

MY	Common Pads		
	COM0	COM63	COMS
0	Com0 → Common Address → Com63 →		COMS
1	Com63 ← Common Address ←	Com0 →	COMS

DDRAM Organization

When accessing to RAM, sixteen addressing mode are provided:

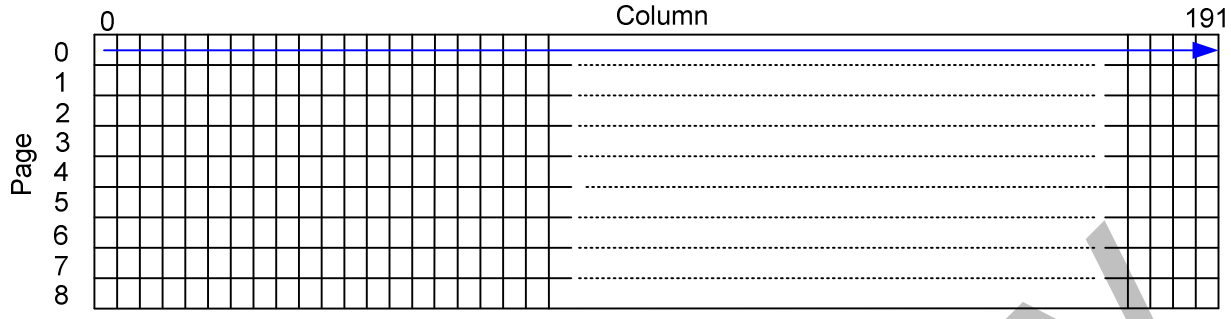


Fig 12. DDRAM Access Mapping (MX=0, AC[2:0]=(0, 0, 0))

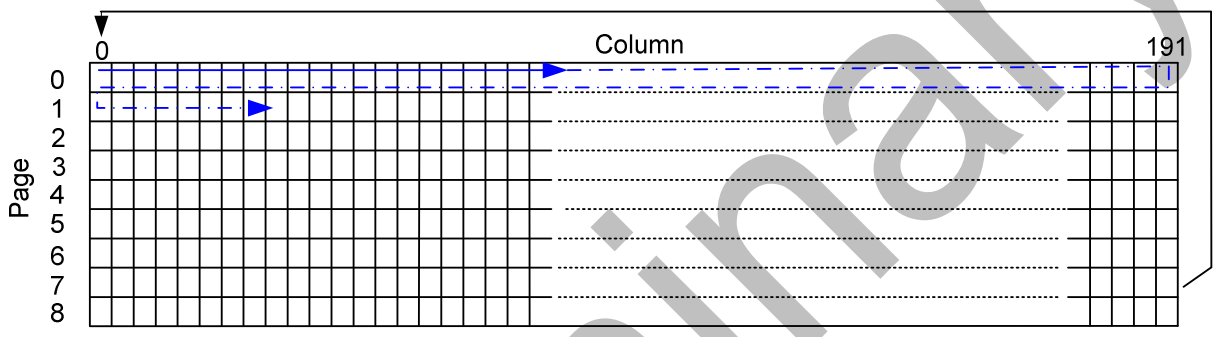


Fig 13. DDRAM Access Mapping (MX=0, AC[2:0]=(0, 0, 1))

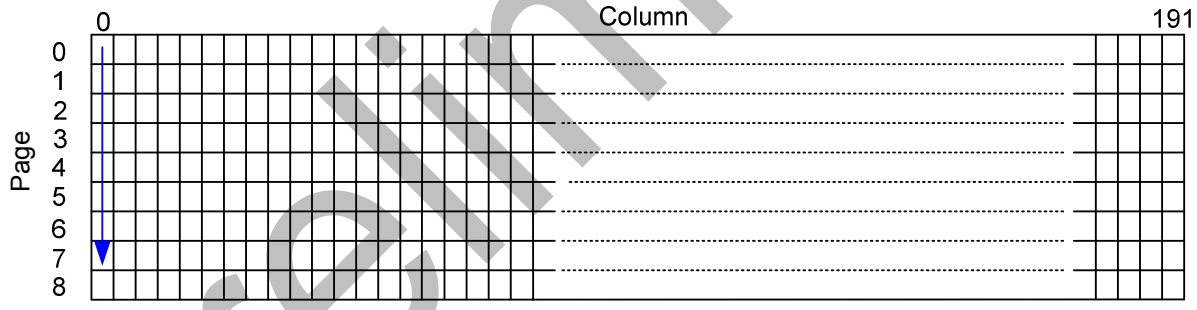


Fig 14. DDRAM Access Mapping (MX=0, AC[2:0]=(0, 1, 0))

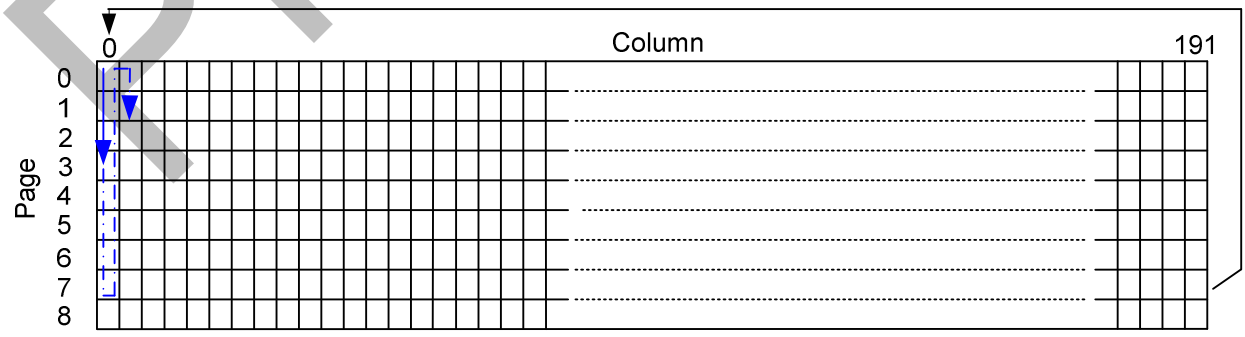


Fig 15. DDRAM Access Mapping (MX=0, AC[2:0]=(0, 1, 1))

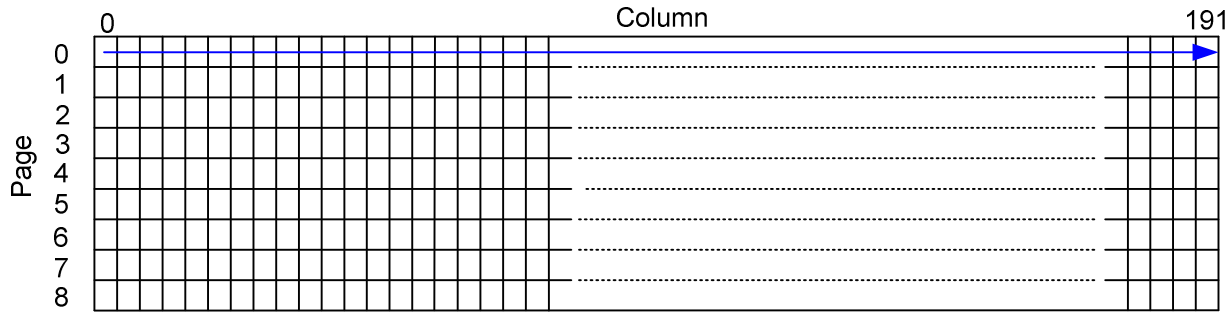


Fig 16. DDRAM Access Mapping (MX=0, AC[2:0]=(1, 0, 0))

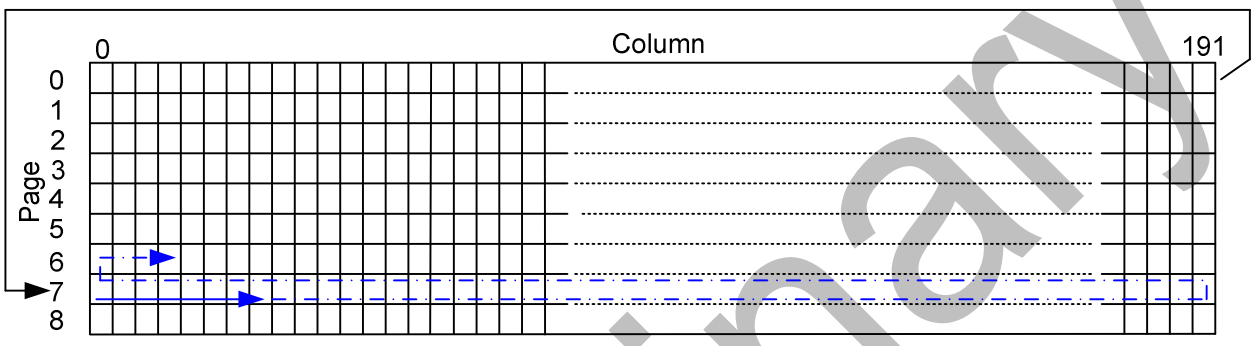


Fig 17. DDRAM Access Mapping (MX=0, AC[2:0]=(1, 0, 1))

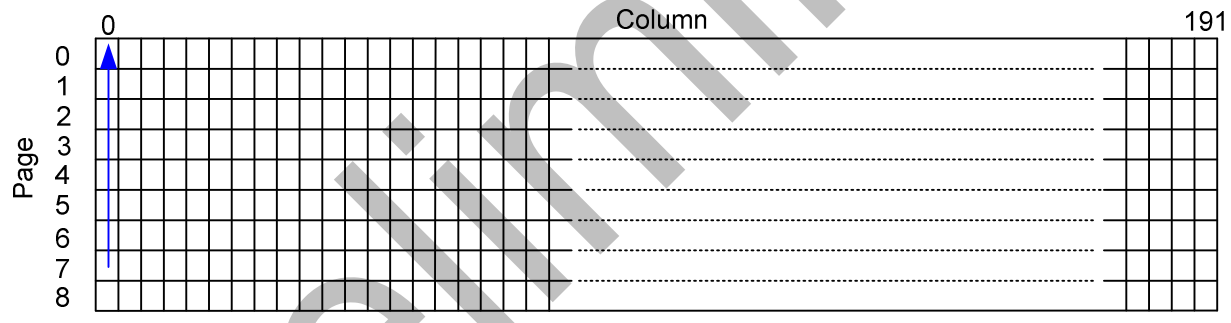


Fig 18. DDRAM Access Mapping (MX=0, AC[2:0]=(1, 1, 0))

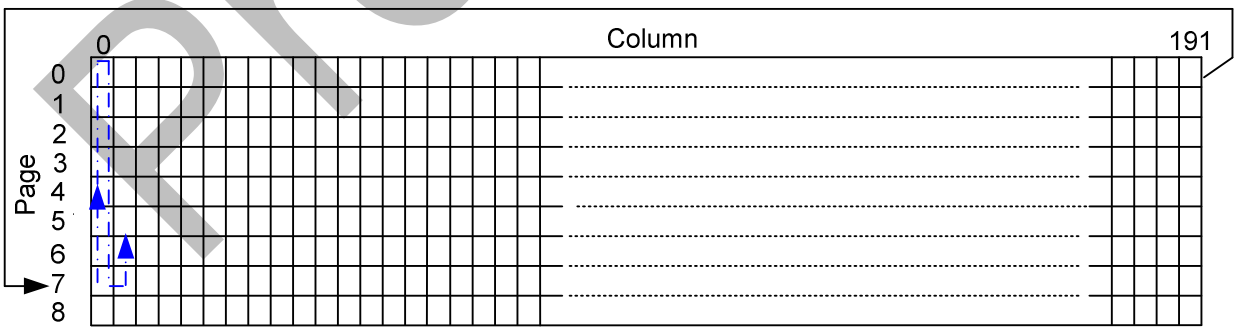


Fig 19. DDRAM Access Mapping (MX=0, AC[2:0]=(1, 1, 1))

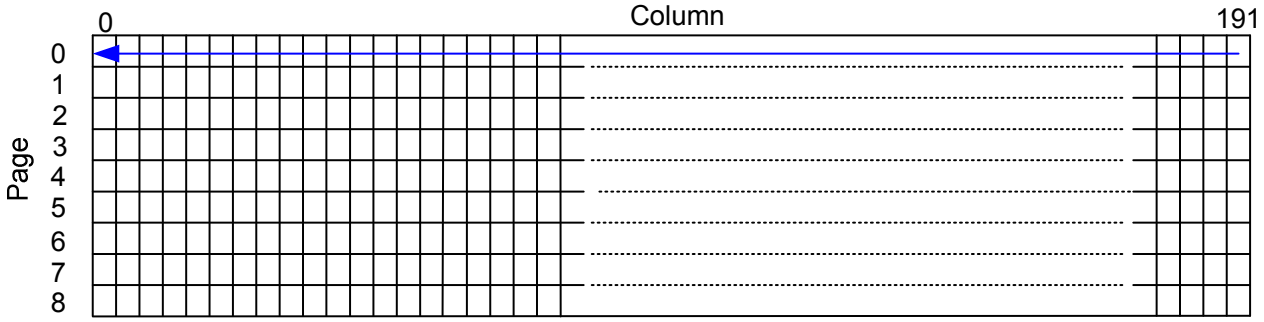


Fig 20. DDRAM Access Mapping (MX=1, AC[2:0]=(0, 0, 0))

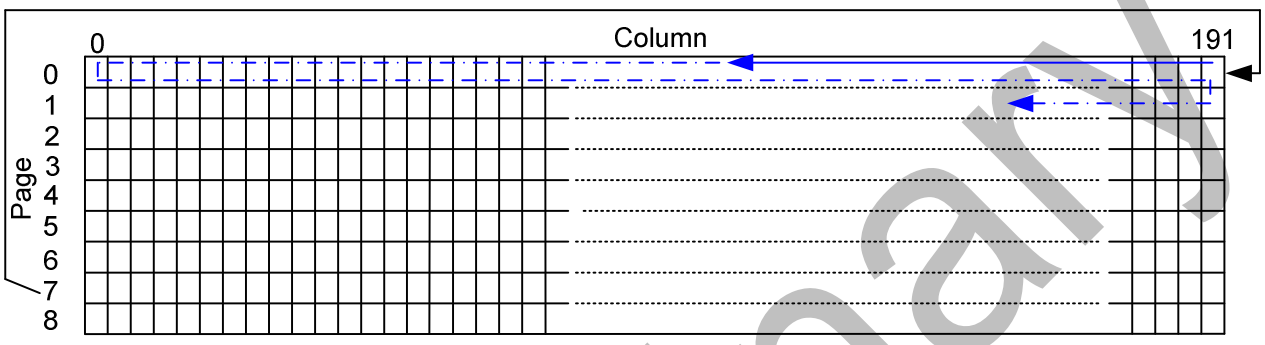


Fig 21. DDRAM Access Mapping (MX=1, AC[2:0]=(0, 0, 1))

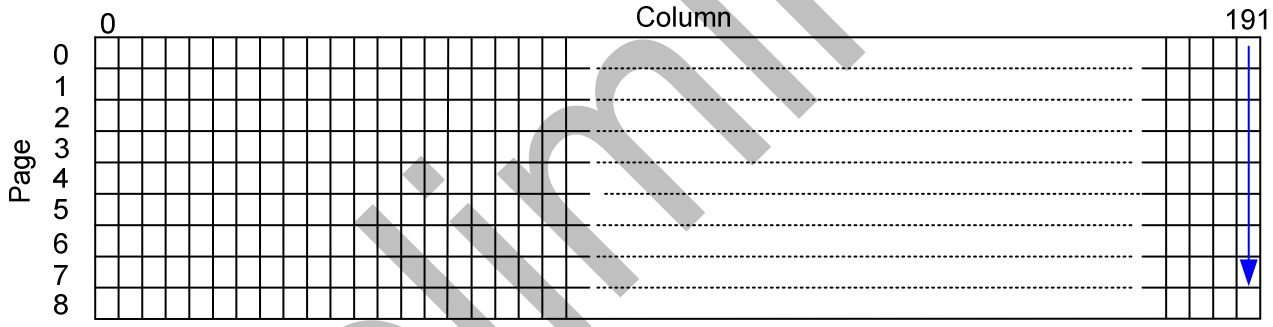


Fig 22. DDRAM Access Mapping (MX=1, AC[2:0]=(0, 1, 0))

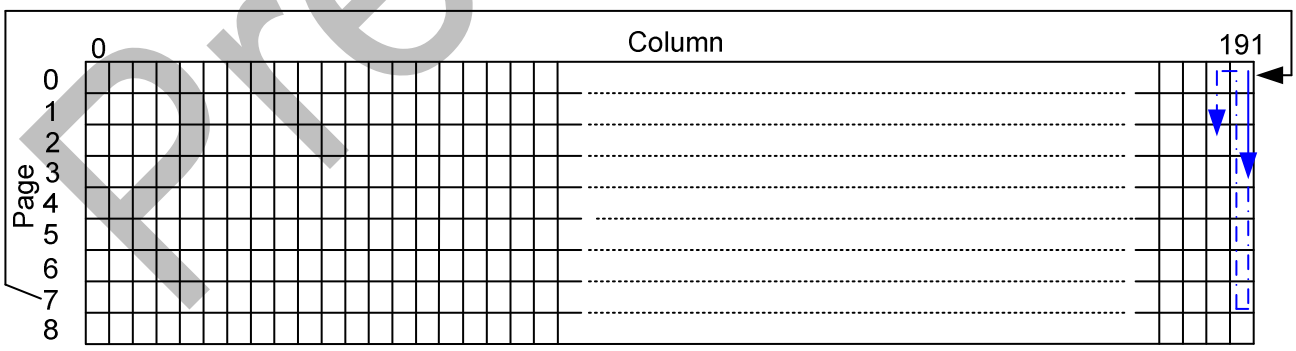


Fig 23. DDRAM Access Mapping (MX=1, AC[2:0]=(0, 1, 1))

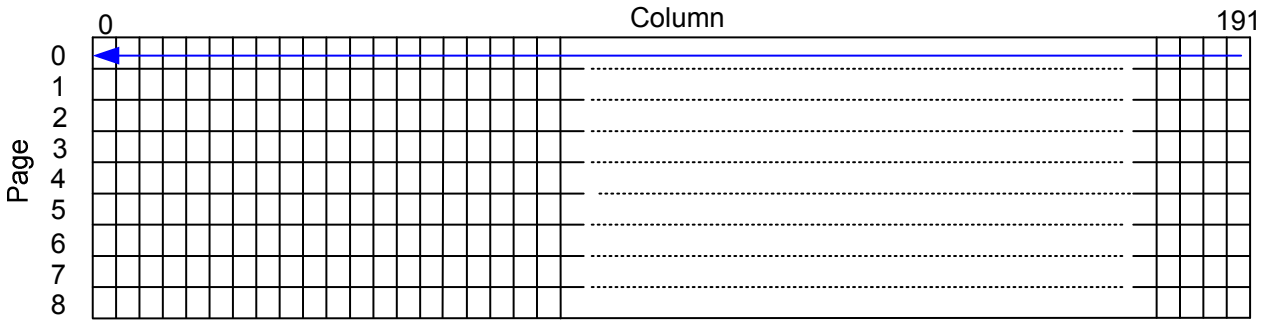


Fig 24. DDRAM Access Mapping (MX=1, AC[2:0]=(1, 0, 0))

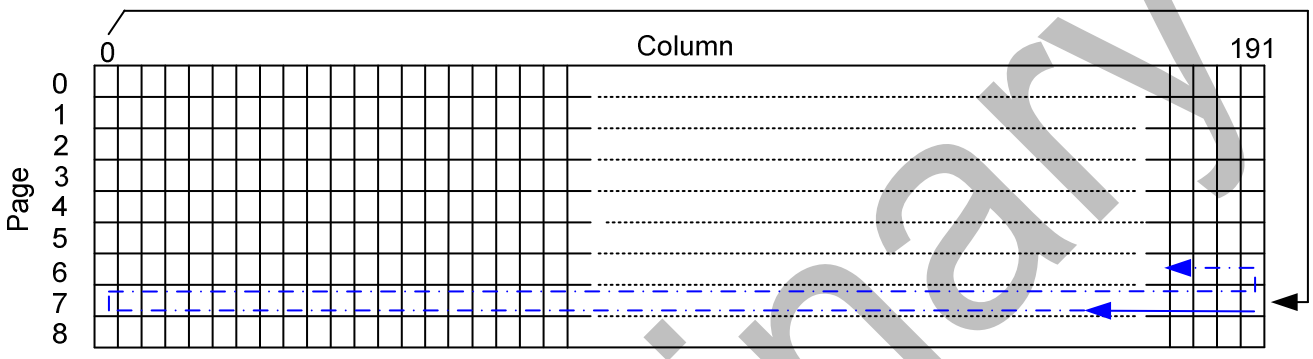


Fig 25. DDRAM Access Mapping (MX=1, AC[2:0]=(1, 0, 1))

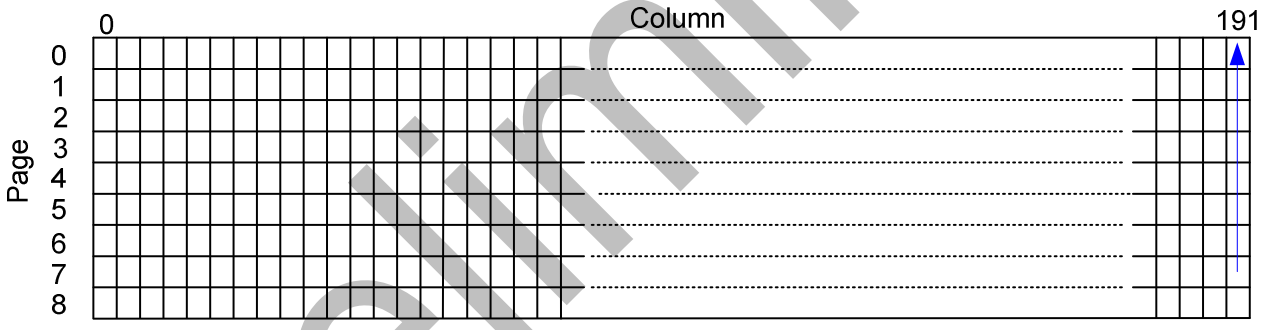


Fig 26. DDRAM Access Mapping (MX=1, AC[2:0]=(1, 1, 0))

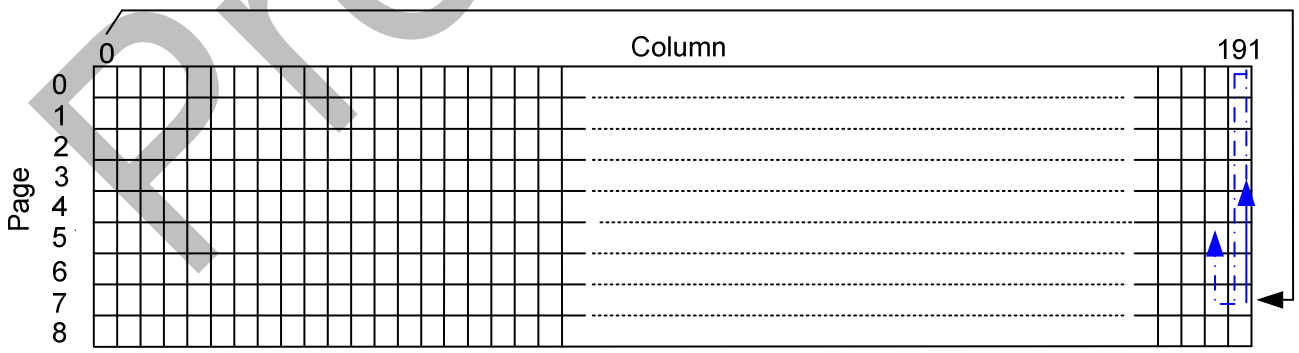


Fig 27. DDRAM Access Mapping (MX=1, AC[2:0]=(1, 1, 1))

Partial Display on LCD

ST7525 realizes the Partial Display function on LCD with low-duty driving for saving power consumption and showing the various display duty. To show the various display duty on LCD, LCD driving duty and bias ratio are programmable via the instruction. Moreover, built-in power supply circuits are controlled by the instruction for adjusting the LCD driving voltages. If the partial display region is out of the maximum display range, it would be abnormal. When the partial mode is active, the setting rule of “Partial Start Address” and “Partial End Address” are according to below relationship:

CEN[5:0] ≥ DEN[5:0] ≥ DST[5:0] + 9.

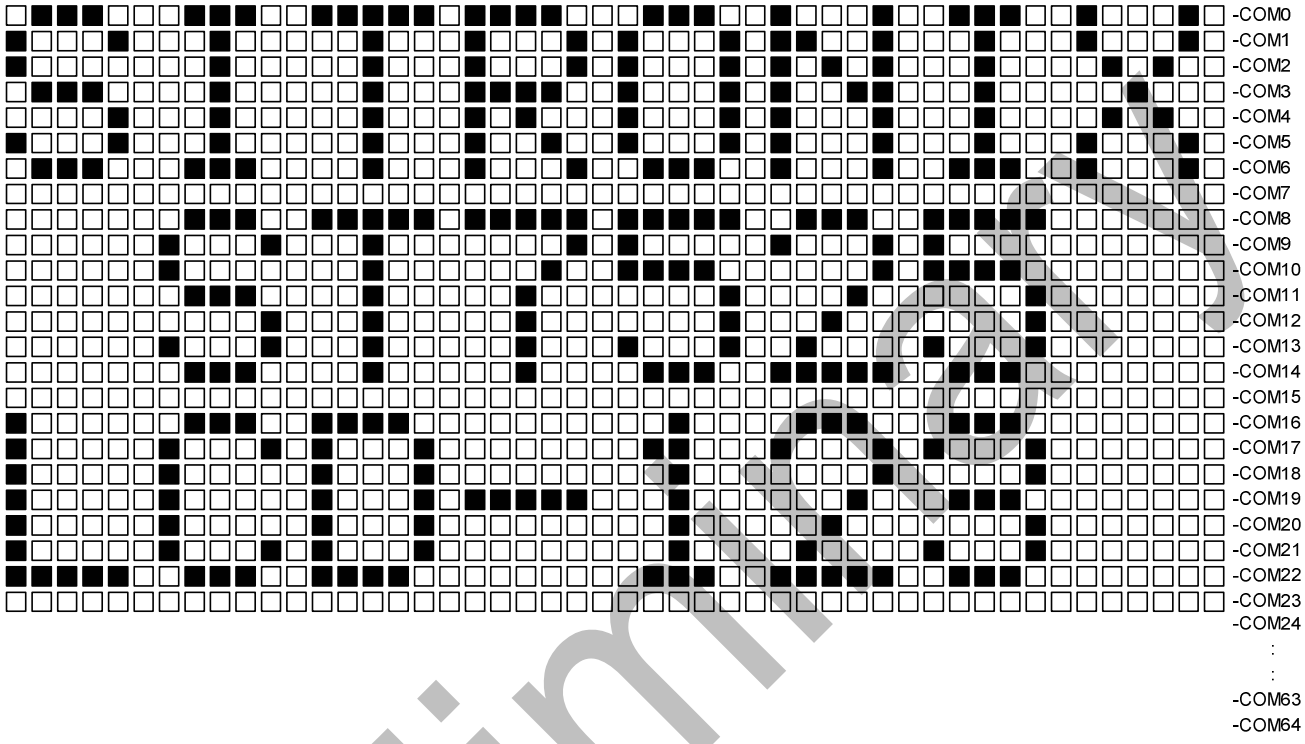


Fig 28. Partial Display (CEN[5:0]=23, SL[5:0]=0, PS=0)

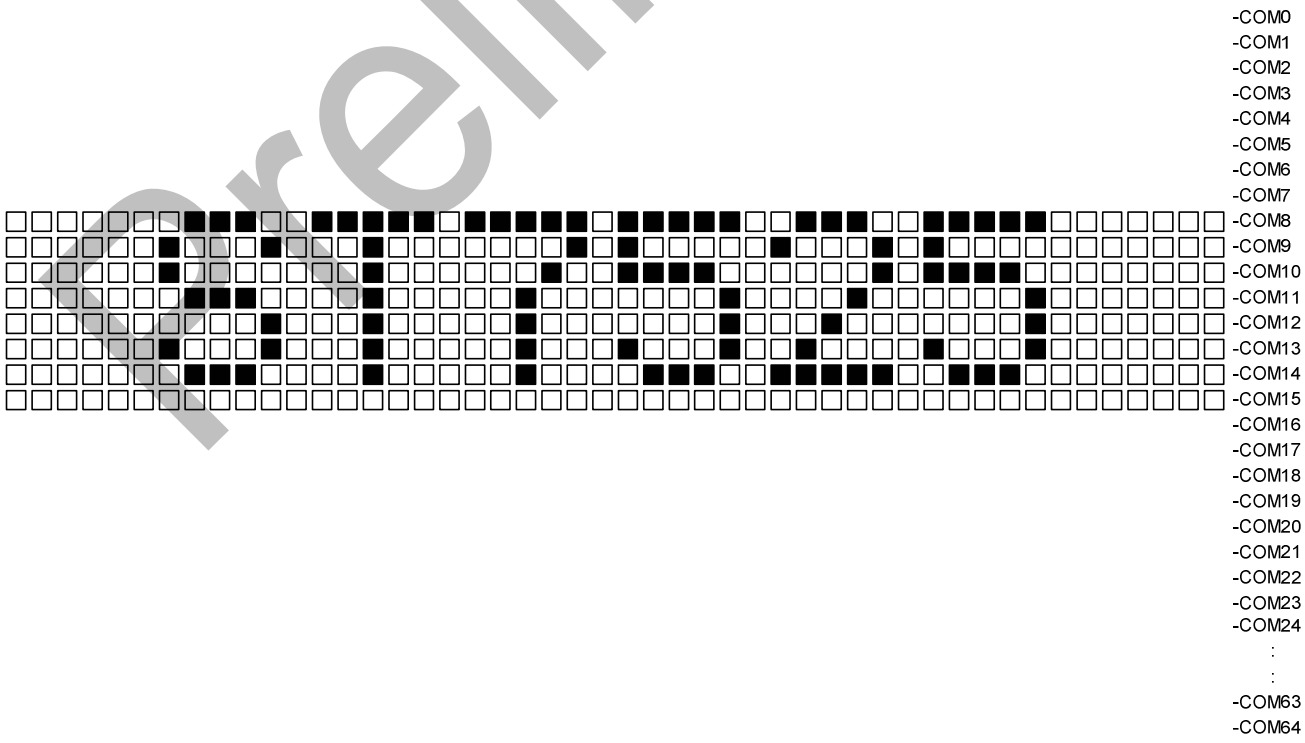


Fig 29. Partial Display (CEN[5:0]=23, SL[5:0]=0, DST[5:0]=8, DEN[5:0]=15, PS=1)

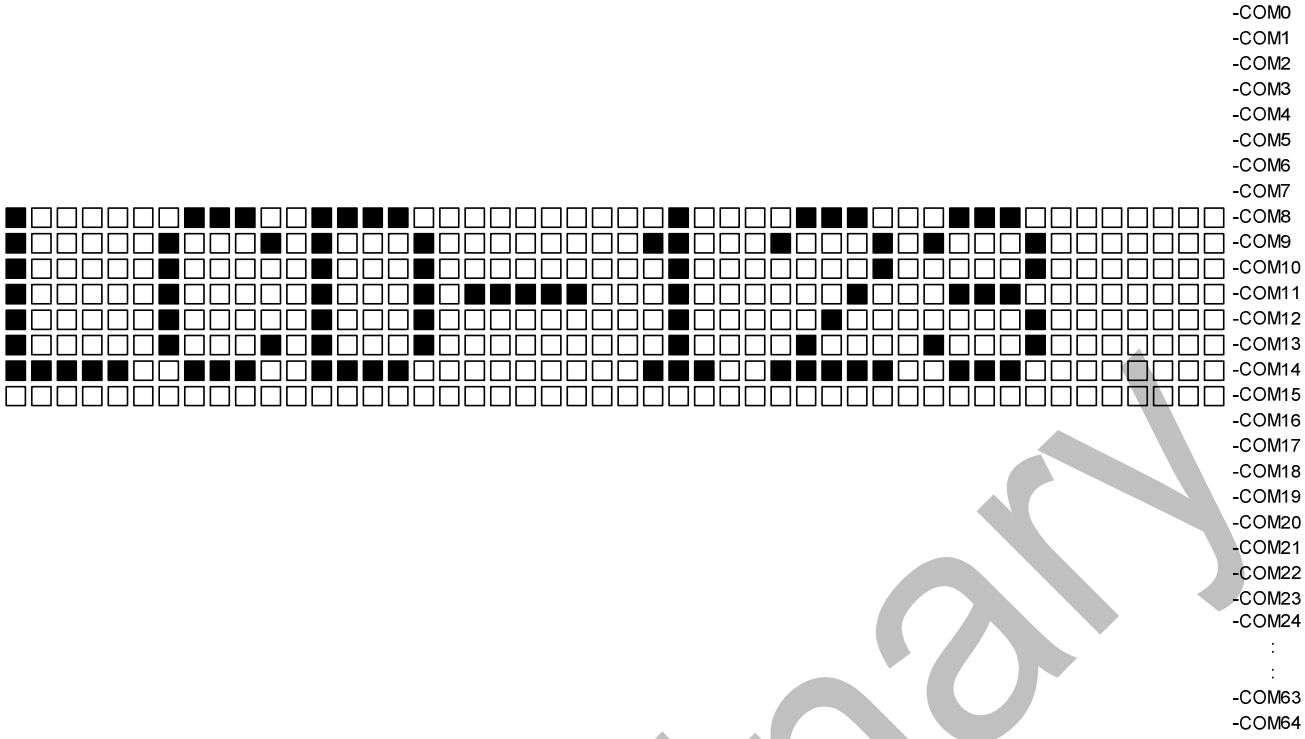


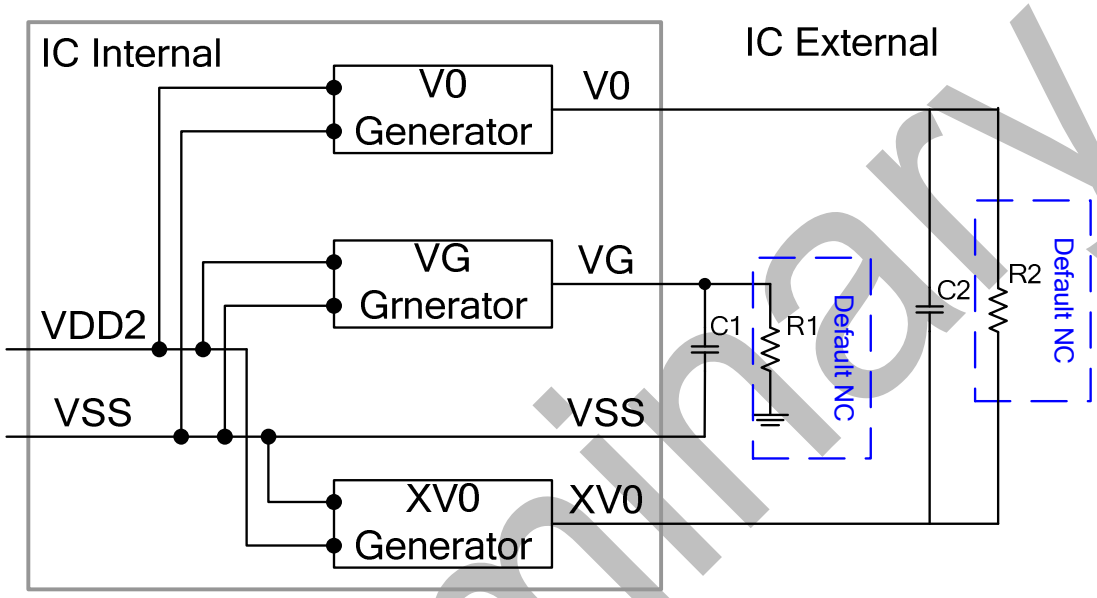
Fig 30. Partial Display (CEN[5:0]=23, SL[5:0]=8, DST[5:0]=8, DEN[5:0]=15, PS=1)

Power Supply Circuit

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are controlled by Set Display Enable instruction.

External Power Components

The default external power component is only 2 capacitors. It is connection method and capacitance value is shown below. The detailed values are determined by the panel size and loading.



The referential external component values are listed below.

1. The resistors are reserved only. Please reserve the space for them on FPC (or system).
2. C1=0.1uF~2.2uF (Non-Polar/6.3V, default 1uF.)
3. C2=0.1uF~2.2uF (Non-Polar/25V, default 1uF)
4. R1~R2=47KΩ~100KΩ (default N.C.)

Components selection notes:

- Higher capacitor values are recommended for ripple reduction.
- In order to avoid the characteristic differences of the LCD panel. The capacitor values should be verified according to the display performance on LCD panel.
- The resistor is reserved for discharge in the worse case, when VDD suddenly drops to 0.
- Those values of capacitor can be determined by customer's LCD module (panel loading and ITO resistance) and application (VDD, V0, bias...etc).

Voltage Regulator Circuits

The internal Voltage Regulator circuit provides the liquid crystal operating voltage (Vop) by adjusting registers (BR[1:0] and EV[7:0]). The Vop calculation formula is shown below:

$$Vop = (C_{V0} + C_{EV} \times EV) \times (1 + (T - 25) \times C_T\%)$$

Where

1. C_{V0} and C_{EV} are two constants, whose value depends on the setting of bias register (BR[1:0]).
2. **EV** is the register setting by EV[7:0].
3. **T** is ambient temperature in ℃
4. C_T is the temperature compensation coefficient as -0.05%/℃.

BR	C_{V0}	C_{EV} (mV)	EV	Vop Range (V)
6	4.80	12.24	0	4.80
			255	7.92
7	5.60	14.28	0	5.60
			255	9.24
8	6.40	16.32	0	6.40
			255	10.56
9	7.20	18.36	0	7.20
			234	11.50

Fig 31 shows Vop voltage measured by adjusting bias register and electronic volume registers for each temperature coefficient at Ta = 25℃.

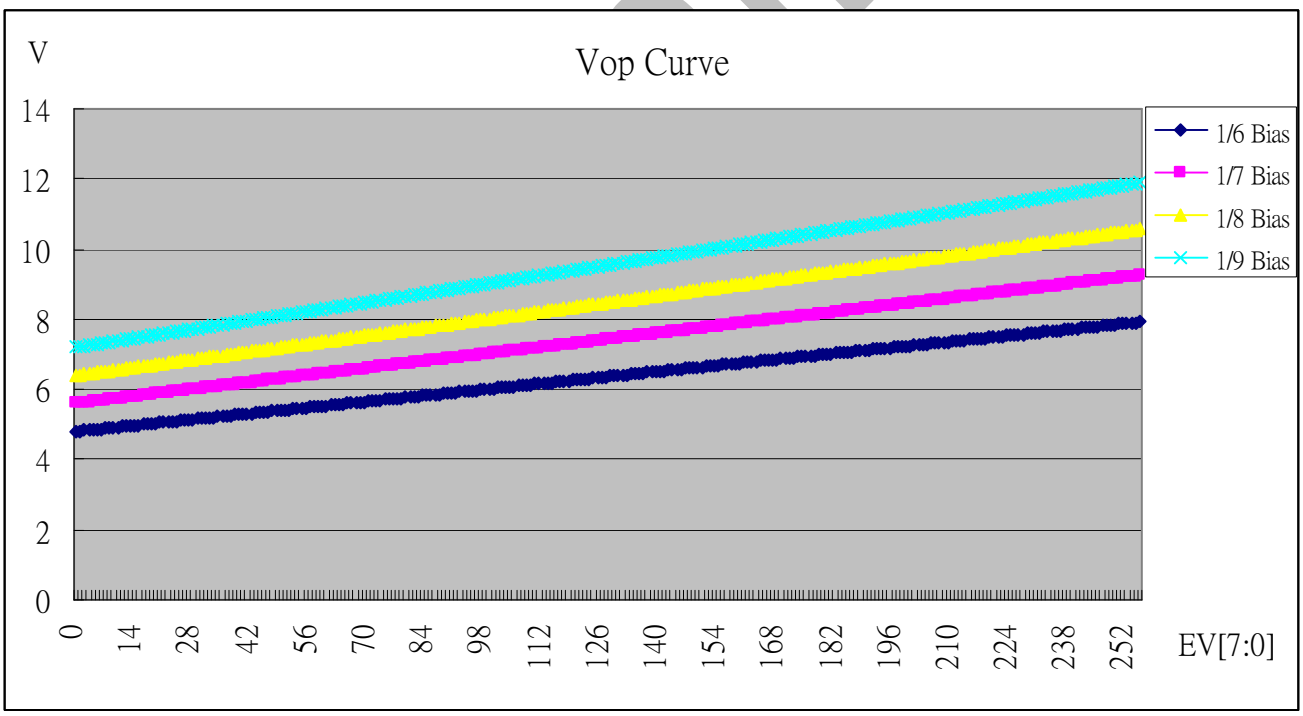


Fig 31. Electronic Volume Level (25℃)

8. RESET CIRCUIT

Setting RST to “L” can initialize internal function. While RST is “L”, no instruction can be accepted. RST pin must connect to the reset pin of MPU and initialization by RST pin is essential before operating. Please note the RST (hardware reset) function is not the same as the SRESET (software reset) function.

Procedure	Hardware Reset	Software Reset
DDRAM Content	No Change	No Change
Column Address Counter	CA[7:0]=0	CA[7:0]=0
Scroll Line	SL[5:0]=0	No Change
Page Address Counter	PA[3:0]=0	PA[3:0]=0
Contrast Control	EV[7:0]=49h	No Change
Partial Screen Enable	PS=0	No Change
Ram Address Control	AC[2:0]=1h	AC [2:0]=1h
Frame Rate	FR[1:0]=1h	No Change
All Pixel ON	AP=0	No Change
Inverse Display	INV=0	No Change
Display Enable	PD=0	No Change
Scan Direction	MX=0, MY=0	No Change
LCD Bias	BR[1:0]=3h	No Change
COM End	CEN[5:0]=3Fh	No Change
Partial Start Address	DST[5:0]=0	No Change
Partial End Address	DEN[5:0]= 3Fh	No Change

After power-on, RAM data are undefined and the display status is “Display OFF”. It’s better to initialize whole DDRAM (ex: fill all 00h or write a display pattern, such as logo) before turning the Display ON.

9-1. INSTRUCTION TABLE

Command Table											
INSTRUCTION	**A0**	**R/W (RWR)**	**COMMAND BYTE**								**DESCRIPTION**
			D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Write Data	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data to DDRAM
Read Data	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from DDRAM Only for parallel interface and I^2C
Read Status Byte (parallel interface)	0	1	ID0	MX	MY	WA	DE	0	0	0	Read status byte Only for parallel interface
			0	0	0	0	0	o	ID2	ID1	
Set Column Address LSB	0	0	0	0	0	0	CA3	CA2	CA1	CA0	Set column address of RAM
Set Column Address MSB	0	0	0	0	0	1	CA7	CA6	CA5	CA4	
Set Scroll Line	0	0	0	1	SL5	SL4	SL3	SL2	SL1	SL0	Specify line address for the 1st display line of DDRAM (vertical scrolling)
Set Page Address	0	0	1	0	1	1	PA3	PA2	PA1	PA0	Set page address of RAM
Set Contrast	0	0	1	0	0	0	0	0	0	1	2-byte instruction. Set Vop voltage
			EV7	EV6	EV5	EV4	EV3	EV2	EV1	EV0	
Set Partial Screen Mode	0	0	1	0	0	0	0	1	0	PS	PS=1: Enable partial mode
Set RAM Address Control	0	0	1	0	0	0	1	AC2	AC1	AC0	Set column and page address behavior
Set Frame Rate	0	0	1	0	1	0	0	0	FR1	FR0	Set frame frequency
Set All Pixel ON	0	0	1	0	1	0	0	1	0	AP	Set all display segments on
Set Inverse Display	0	0	1	0	1	0	0	1	1	INV	Set inverse display
Set Display Enable	0	0	1	0	1	0	1	1	1	PD	PD=0: Chip is in power down mode
Scan Direction	0	0	1	1	0	0	0	MY	MX	0	Set COM and SEG scan direction
Software Reset	0	0	1	1	1	0	0	0	1	0	Set software reset
NOP	0	0	1	1	1	0	0	0	1	1	No operation
Set Bias	0	0	1	1	1	0	1	0	BR1	BR0	Set internal bias circuit
Set COM End	0	0	1	1	1	1	0	0	0	1	2-byte instruction. Set display duty
			--	--	CEN5	CEN4	CEN3	CEN2	CEN1	CEN0	
Partial Start Address	0	0	1	1	1	1	0	0	1	0	Set partial start for partial display screen
			--	--	DST5	DST 4	DST 3	DST 2	DST 1	DST 0	
Partial End Address	0	0	1	1	1	1	0	0	1	1	Set partial end for partial display screen
			--	--	DEN5	DEN4	DEN3	DEN2	DEN1	DEN0	
Test Control	0	0	1	1	1	1	0	0	0	0	Set test command table
			--	--	--	--	--	--	H1	H0	

Serial Read Command Table (Enabled only in 4 line SPI)										
INSTRUCTION	A0	R/W (RWR)	COMMAND BYTE							DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Read Status Byte	0	0	1	1	1	1	1	1	1	0	Read status byte
	0	1	ID0	MX	MY	WA	DE	0	0	0	
			0	0	0	0	0	0	ID2	ID1	
Read Data	0	0	1	1	1	1	1	1	1	1	Read data from DDRAM
	1	1	D7	D6	D5	D4	D3	D2	D1	D0	

Note: 1. Do not use instructions not listed in these tables (Command Table).
2. “--” = Disabled bit. It can be either logic 0 or 1.

9-2. INSTRUCTION DESCRIPTION

Write Data

8-bit data of Display Data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page. During auto-increment, the column address wraps to 0 after the last column is written.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Read Data

8-bit data of Display Data from the RAM location specified by the column address and page address can be read to the microprocessor.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read Status Byte

Indicate the status of ST7525.

Parallel interface (8080/ 6800)

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	ID0	MX	MY	WA	DE	0	0	0
0	1	0	0	0	0	0	0	ID2	ID1

Flag	Description
MX	SEG bi-direction selection MY=0:normal direction (SEG0→SEG191); MY=1:reverse direction (SEG191→SEG0)
MY	COM bi-direction selection MY=0:normal direction (COM0→COM63); MY=1:reverse direction (COM63→COM0)
WA	AC0 status
DE	Display enable or disable
ID0	ID0 setting
ID1	ID1 setting
ID2	ID2 setting

Set Column Address

These instructions set the specified Column Address of DDRAM into the internal CA address (Column Address). The CA address register points to the address of DDRAM for accessing display data. The CA address register is automatically increased by 1 when the microprocessor accesses the display data in DDRAM.

1. Set Column Address (LSB)

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	CA3	CA2	CA1	CA0

2. Set Column Address (MSB)

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	CA7	CA6	CA5	CA4

CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	Column Address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	1	1	3
:	:	:	:	:	:	:	:	:
1	0	1	1	1	1	0	0	188
1	0	1	1	1	1	0	1	189
1	0	1	1	1	1	1	0	190
1	0	1	1	1	1	1	1	191

Set Scroll Line

The 2-byte instruction sets the line address of DDRAM to determine the first display line. The display data of the selected line will be displayed at the top of row (COM0) on the LCD panel.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	SL5	SL4	SL3	SL2	SL1	SL0

SL5	SL4	SL3	SL2	SL1	SL0	Line Address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
0	0	0	0	1	1	3
:	:	:	:	:	:	:
1	1	1	1	0	0	60
1	1	1	1	0	1	61
1	1	1	1	1	0	62
1	1	1	1	1	1	63

Set Page Address

This instruction sets the Page Address of display data RAM from the microprocessor into the page address register. Any RAM data bit can be accessed when its page address and column address are specified. Along with the CA address, the PA address defines the address of the display RAM to write display data. Changing the page address doesn't affect the display status.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	1	PA3	PA2	PA1	PA0

PA3	PA2	PA1	PA0	Page Address	Allowed CA-Range
0	0	0	0	Page0 (display RAM)	0 to 191
0	0	0	1	Page1 (display RAM)	0 to 191
0	0	1	0	Page2 (display RAM)	0 to 191
0	0	1	1	Page3 (display RAM)	0 to 191
0	1	0	0	Page4 (display RAM)	0 to 191
0	1	0	1	Page5 (display RAM)	0 to 191
0	1	1	0	Page6 (display RAM)	0 to 191
0	1	1	1	Page7 (display RAM)	0 to 191
1	0	0	0	Page8 (icon RAM)	0 to 191

Set Contrast

This instruction sets operating voltage Vop.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	0	0	0	0	1
0	0	EV7	EV6	EV5	EV4	EV3	EV2	EV1	EV0

EV7	EV6	EV5	EV4	EV3	EV2	EV1	EV0	EV Value
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	0	254
1	1	1	1	1	1	1	1	255

Set Partial Screen Mode

This instruction controls partial display enable.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	0	0	1	0	PS

Flag	Description
PS	Full display mode or partial screen mode selection. PS=0 : Full display mode. PS=1 : Partial screen mode.

Set RAM Address Control

This instruction controls DDRAM display scan behaviors.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	0	1	AC2	AC1	AC0

Flag	Description
AC0	Automatic column or page wrap around. AC1 = 0, AC0 = 0: Column address will stop increasing by 1 while reaching each boundary. AC1 = 0, AC0 = 1: Column address will go on next page after reaching each boundary. AC1 = 1, AC0 = 0: Page address will stop increasing by 1 while reaching each boundary. AC1 = 1, AC0= 1: Page address will go on next column after reaching each boundary.
AC1	Address auto increase order. AC1=0 : Column address increase by 1 first until column address reach each boundary, then page address will increase or decrease by 1(depend on AC2). AC1=1 : Page address increase by 1 first until page address reach each boundary, then column address will increase by 1.
AC2	Page address auto increment direction. AC2=0 : Page address increase by 1 (PA +1, downward). AC2=1 : Page address decrease by 1 (PA -1, upward).

Set Frame Rate

This command is used to set the frame frequency.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	0	FR1	FR0

FR1	FR0	Frame Frequency
0	0	76 fps ± 15%
0	1	95 fps ± 15%
1	0	132 fps ± 15%
1	1	168 fps ± 15%

Set All Pixel ON

This instruction sets all segments output ON.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	1	0	AP

Flag	Description
AP	Force all display segments on. AP=0 : Normal display mode. AP=1 : All segments output ON.

Set Inverse Display

This instruction sets the display inverse mode.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	1	1	INV

Flag	Description
INV	Inverse video mode. INV=0 : Normal display mode. INV=1 : Inverse display mode.

Set Display Enable

This instruction sets display off and enters power down mode. All LCD outputs at VSS (display off) bias generator and power generator off, oscillator off (external clock possible), RAM contents not cleared and RAM data can be written.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	1	1	1	PD

Flag	Description
PD	Display off and power down mode. PD=0 : Display off and power down mode. PD=1 : Display on and power on mode.

Scan Direction

This instruction sets COM and SEG bi-direction selection.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	0	0	MY	MX	0

Flag	Description
MY	COM bi-direction selection. MY=0 : Normal direction (COM0 → COM63) MY=1 : Reverse direction (COM63 → COM0)
MX	SEG bi-direction selection. MX=0 : Normal direction (SEG0 → SEG191) MX=1 : Reverse direction (SEG191 → SEG0)

Software Reset

This is software reset. It resets internal registers. This instruction cannot initialize the LCD power supply, which is initialized by a hardware reset.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	0	0	1	0

NOP

No operation.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	0	0	1	1

Set Bias

Select LCD bias ratio of the voltage required for driving the LCD.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	1	0	BR1	BR0

BR1	BR0	Bias
0	0	1/6
0	1	1/7
1	0	1/8
1	1	1/9

Set COM End

This 2-byte instruction sets the display duty within the range of 1/(9+1) to 1/(64+1) to realize partial display.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	1	0	0	0	1
0	0	--	--	CEN5	CEN4	CEN3	CEN2	CEN1	CEN0

CEN5	CEN4	CEN3	CEN2	CEN1	CEN0	Selected Partial Duty Ratio
0	0	0	0	0	0	Reserved
:	:	:	:	:	:	
:	:	:	:	:	:	
0	0	1	0	0	0	1/(9+1)
0	0	1	0	0	1	1/(10+1)
:	:	:	:	:	:	:
1	1	1	1	1	0	1/(63+1)
1	1	1	1	1	1	1/(64+1)

Set Partial Start Address

This instruction can select partial screen display start line address.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	1	0	0	1	0
0	0	--	--	DST5	DST4	DST3	DST2	DST1	DST0

DST5	DST4	DST3	DST2	DST1	DST0	Selected Partial Start Line Address
0	0	0	0	0	0	1
0	0	0	0	0	1	2
:	:	:	:	:	:	:
1	1	1	1	1	0	63
1	1	1	1	1	1	64

Set Partial End Address

This instruction can select partial screen display end line address.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	1	0	0	1	1
0	0	--	--	DEN5	DEN4	DEN3	DEN2	DEN1	DEN0

DEN5	DEN 4	DEN 3	DEN 2	DEN 1	DEN 0	Selected Partial End Line Address
0	0	0	0	0	0	1
0	0	0	0	0	1	2
:	:	:	:	:	:	:
1	1	1	1	1	0	63
1	1	1	1	1	1	64

Set Test Control

This instruction can select test command table.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	1	0	0	0	0
0	0	--	--	--	--	--	--	H1	H0

Read Status Byte (for 4 line SPI)

Indicate the status used by 4-line SPI

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	1	1	1	1	0
0	1	ID0	MX	MY	WA	DE	0	0	0
0	1	0	0	0	0	0	0	ID2	ID1

Read Data (for 4 line SPI)

8-bit data of Display Data from the RAM location specified by the column address and page address can be read to the microprocessor.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	1	1	1	1	1
1	1	D7	D6	D5	D4	D3	D2	D1	D0

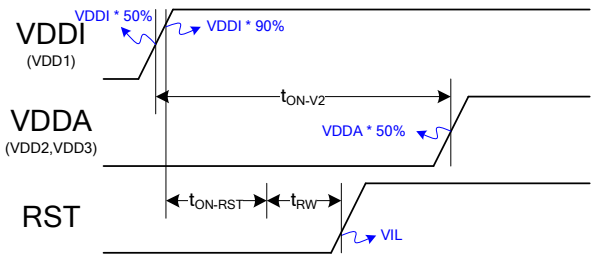
10. COMMAND SEQUENCE

This section introduces some reference operation flows.

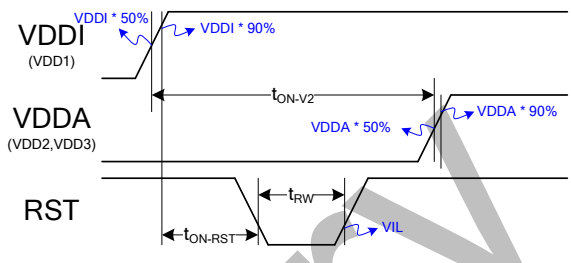
Power ON flow and instruction sequence:

Power ON Sequence

Case 1: RSTB=L while Power ON



Case 2: RSTB=H while Power ON



Note:

The detailed description can be found in the respective sections listed below.

1. Be sure the power is stable and the internal reset is finished (refer to RST timing specification).
2. Power stable is defined as the time that the later power (VDDI or VDDA) reaches 90% of its rated voltage.

Timing Requirement:

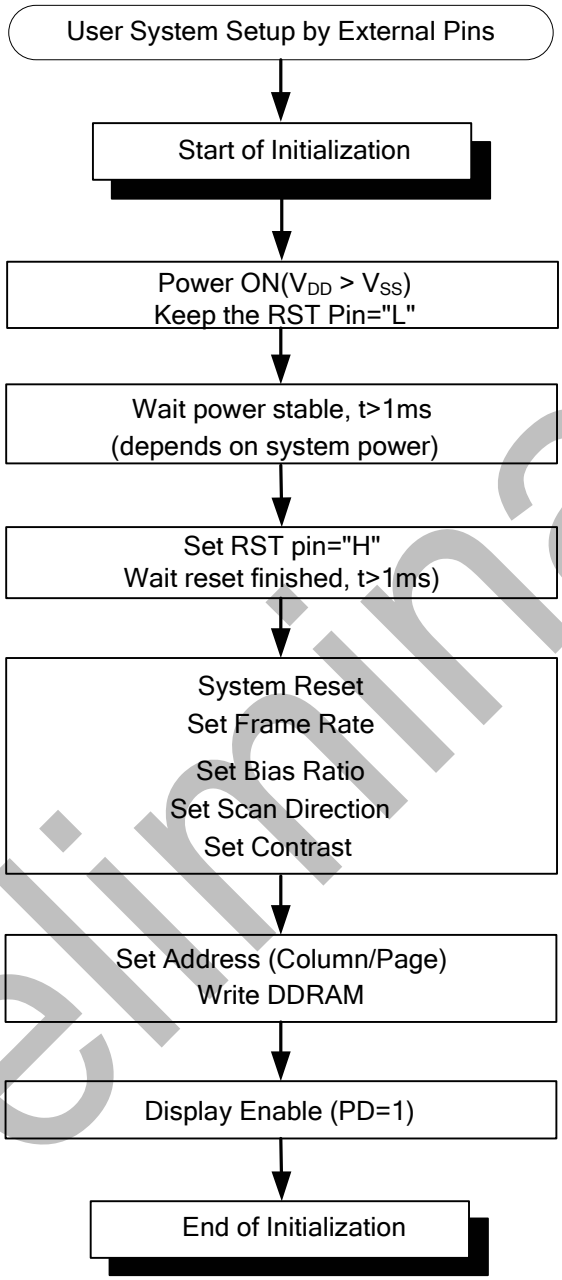
Item	Symbol	Requirement	Note
VDDA power delay	t_{ON-V2}	$0 \le t_{ON-V2}$	● Applying VDDI and VDDA in any order will not damage IC.
RST input time	t_{ON-RST}	No Limitation	● If RST is Low, High or unstable during power ON, a successful hardware reset by RST is required after VDDI is stable. ● RST=L can be input at any time after power is stable. ● t_{RW} & t_R should match the timing specification of RST. ● To prevent abnormal display, the recommended timing is: $0 \le t_{ON-RST} \le 30$ ms.

Note :

IC will NOT be damaged if either VDDI or VDDA is OFF while another is ON. The specification listed here is to prevent abnormal display on LCD module.

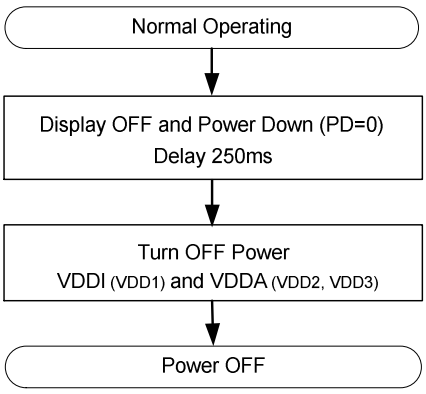
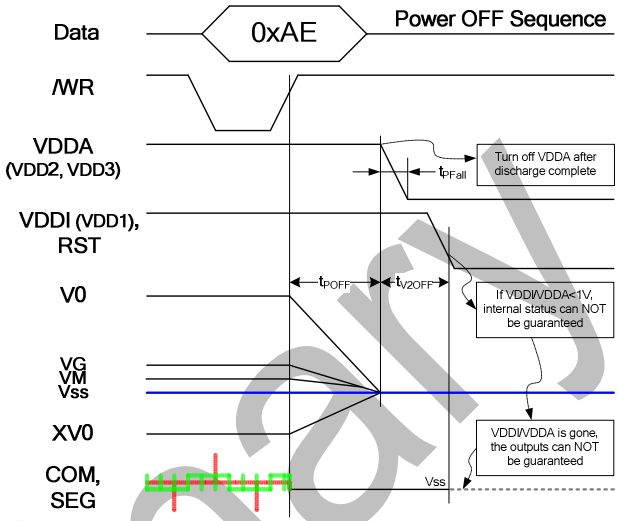
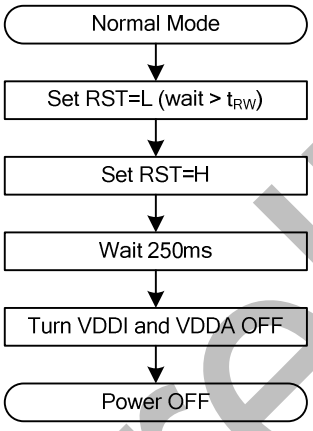
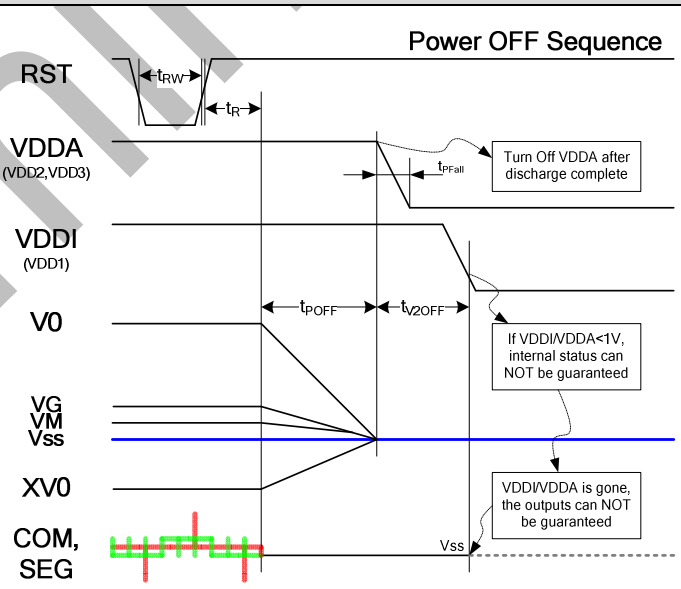
Referential Operation Flow : Initializing with internal power system

The detailed instruction functionality is described in Section “INSTRUCTION DESCRIPTION”.



Power OFF Flow and Sequence

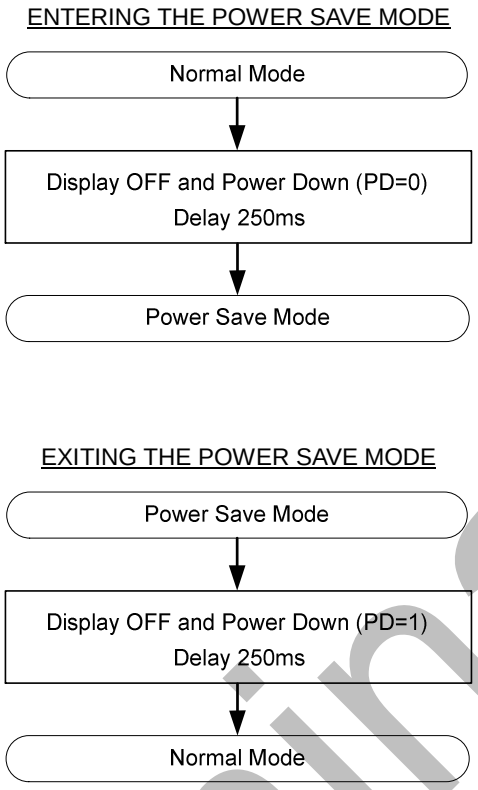
By setting PD="0", the power down procedure starts. The LCD driving outputs are fixed to VSS, built-in power circuits are turned OFF and a discharge process starts. The power off mode can be triggered by the following two methods.

Referential Power OFF Flow	Operation Sequence
CASE 1: Use Display OFF Instruction	
 After the built-in power circuits are turned OFF and completely discharged, the power (VDDI and VDDA) can be removed.	
CASE 2: Use Hardware Reset Function	
 After the built-in power circuits are OFF and completely discharged, the power (VDDI, VDDA) can be removed.	

Note:

1. t_{POFF}: Internal Power discharge time. => 250ms (max).
2. t_{V2OFF}: Period between VDDI and VDDA OFF time. => 0 ms (min).
3. It is NOT recommended to turn VDDI OFF before VDDA. Without VDDI, the internal status cannot be guaranteed and internal discharge-process maybe stopped. The un-discharged power maybe flows into COM/SEG output(s) and the liquid crystal in panel maybe polarized.
4. IC will NOT be damaged if either VDDI or VDDA is OFF while another is ON.
5. The timing is dependent on panel loading and the external capacitor(s).
6. The timing in these figures is base on the condition that: LCD Panel Size = 1.8" with C1 = 1uF and C2 = 1uF.
7. When turning VDDA OFF, the falling time should follow the specification:
   300ms ≤ t_{PFall} ≤ 1sec

Power-Save Flow



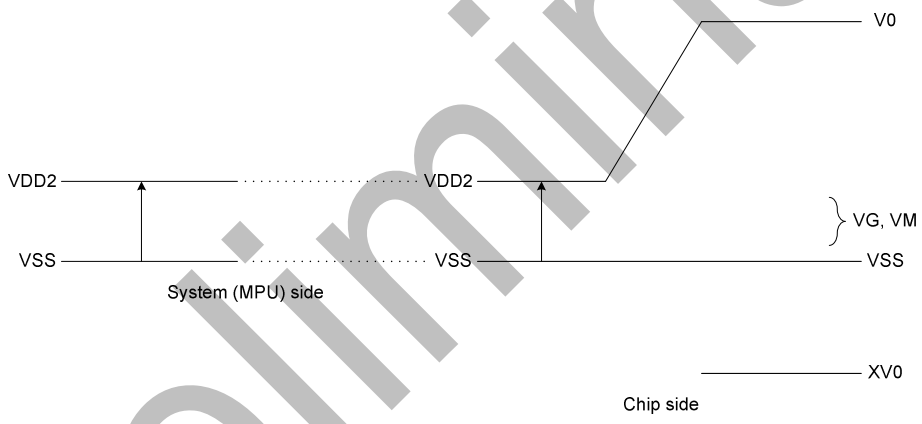
11. HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

12. LIMITING VALUES

In accordance with the Absolute Maximum Rating System; please refer to notes 1~ 4.

Parameter	Symbol	Conditions	Unit
Digital Power Supply Voltage	VDDI (VDD1)	-0.3 ~ 4.0	V
Analog Power supply voltage	VDDA (VDD2 & VDD3)	-0.3 ~ 4.0	V
LCD Power supply voltage	V0-XV0	-0.3 ~ 18	V
LCD Power supply voltage	VG	-0.3 ~ 4.0	V
LCD Power supply voltage	VM	-0.3 ~ 4.0	V
Input voltage	VIN	–0.3 ~ VDD1+0.3 *4	V
Operating temperature	TOPR	–30 to +80	°C
Storage temperature	TSTR	–55 to +125	°C



Notes

1. Insure the voltage levels of V0, VDDA, VG, VM, VSS and XV0 always match the correct relation while operating:
   V0 ≥ VDDA > VG > VM > VSS ≥ XV0
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.
3. Stresses exceed the Limiting Values listed above may cause permanent damage to IC. These values are stresses only. IC should be operated under DC/Timing Characteristics condition for normal operation. If this condition is not met, IC operation may be error and the reliability may be deteriorated.
4. Interface input voltage range can not exceed the maximum limitation of digital power supply voltage.
   VIN ≤ 3.6V

13. DC CHARACTERISTICS

VSS=VSS1=VSS2=VSS3=0V; Bare chip; Temp. = -30°C to +80°C; unless otherwise specified.

Item	Symbol	Condition		Rating			Unit	Applicable Pin
				Min.	Typ.	Max.		
Operating Voltage (1)	VDD1			1.65	—	3.6	V	VDD1
Operating Voltage (2)	VDD2 VDD3			2.5	—	3.6	V	VDD2 VDD3
Input High-level Voltage	V_{IHC}			0.7 x VDD1	—	VDD1	V	MPU Interface
Input Low-level Voltage	V_{ILC}			VSS1	—	0.3 x VDD1	V	MPU Interface
Output High-level Voltage	V_{OHC}	I_{OUT}=1mA, VDD1=1.8V		0.8 x VDD1	—	VDD1	V	D[7:0]
Output Low-level Voltage	V_{OLC}	I_{OUT}=-1mA, VDD1=1.8V		VSS1	—	0.2 x VDD1	V	D[7:0]
Input Leakage Current	I_{LI}			-1.0	—	1.0	μA	MPU Interface
LCD Driver ON Resistance	R_{ON}	Ta=25°C Bias=1/9	Vop=10V, ΔV=1V	—	—	—	KΩ	COMx
			VG=2.2V, ΔV=0.22V	—	—	—	KΩ	SEGx
Frame Frequency	fFR	1/65 Duty, FR[1:0]=(1,0), Ta = 25℃			—		Hz	

Note:

- The LCD Output Voltage (Vop) range of the measurement environment is as follows:
  1. V0 to XV0 : 0.1uF
  2. VG to VSS : 1uF
  3. VM to VSS : 1uF
- The heavy loading pattern may cause variation of Vop output voltage. It means the Vop voltage maybe exceed the range of LCD operation voltage with heavy loading.

Bare chip current consumption with internal power system:

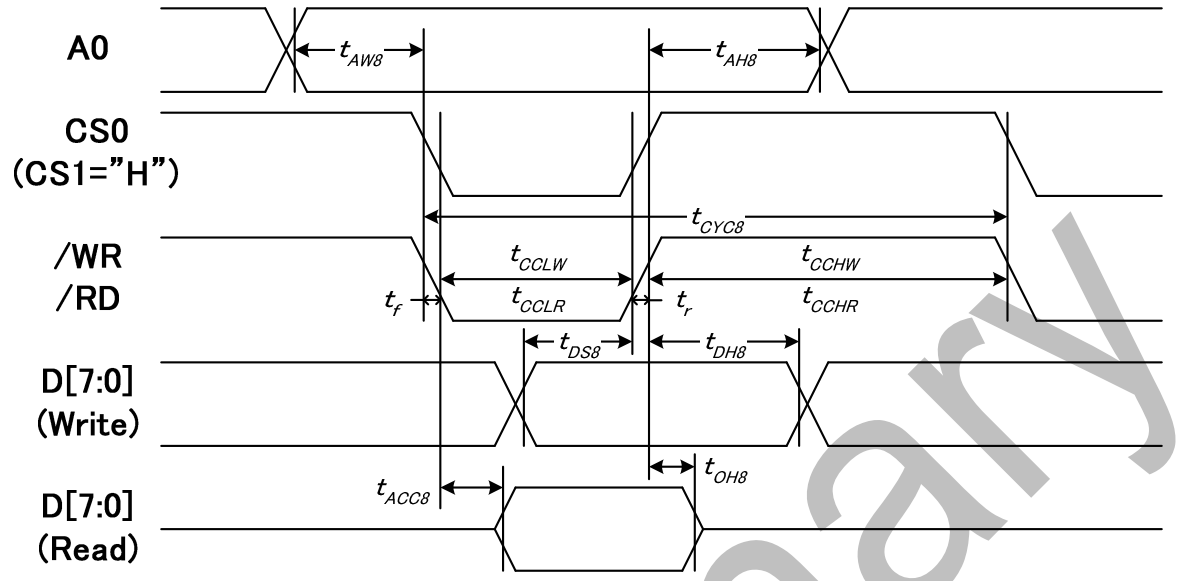
Test Pattern	Symbol	Condition	Rating			Unit	Note
			Min.	Typ.	Max.		
Display Pattern: SNOW (Static)	ISS	VDD1=VDD2=VDD3=3V, Booster X6, FR[1:0]=(1,0), Vop=10V, Bias=1/9, Ta=25°C	—			μA	
Power Down	ISS	VDD1=VDD2=VDD3=3V, Ta=25°C	—			μA	

Note:

The Current Consumption is DC characteristics.

14. TIMING CHARACTERISTICS

System Bus Read/Write Characteristics (For the 8080 Series MPU)



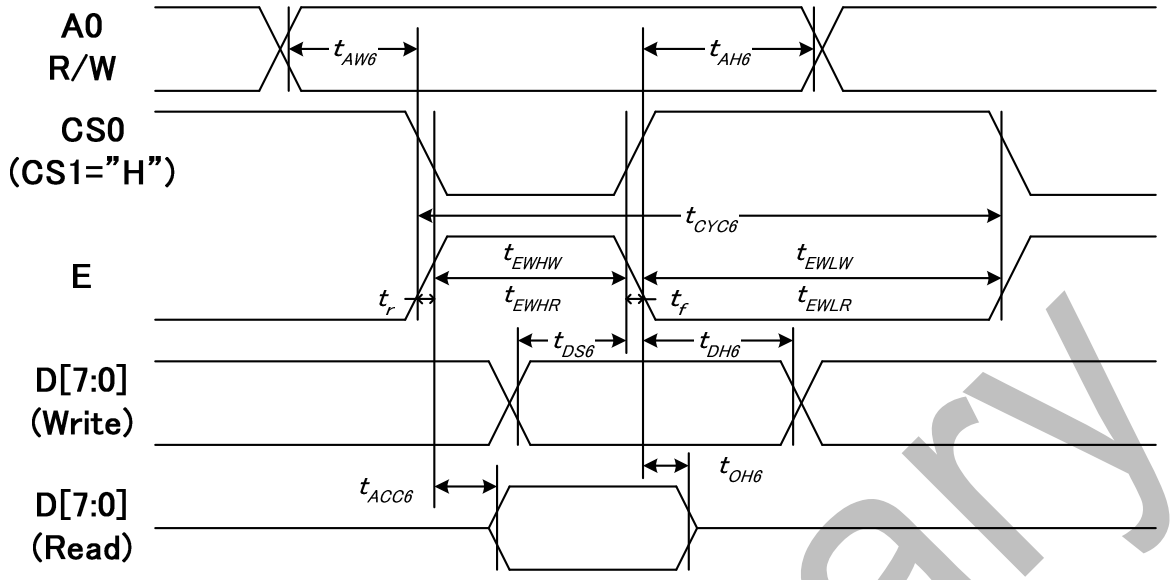
(VDD1 = 3.0V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8			-	ns
Address hold time		tAH8			-	
System write cycle time	/WR	tCYC8			-	
Write L pulse width		tCCLW			-	
Write H pulse width		tCCHW			-	
Read L pulse width	/RD	tCCLR			-	
Read H pulse width		tCCHR			-	
Data setup time (Write)	D[7:0]	tDS8			-	
Write Data hold time (Write)		tDH8			-	

Note:

1. All timing is specified using 20% and 80% of VDD1 as the reference.
2. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≤ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≤ (tCYC8 – tCCLR – tCCHR) are specified.
3. tCCLW (tCCLR) is specified as the overlap between CS0 being "L" and /WR (/RD) being "L".

System Bus Read/Write Characteristics (For the 6800 Series MPU)



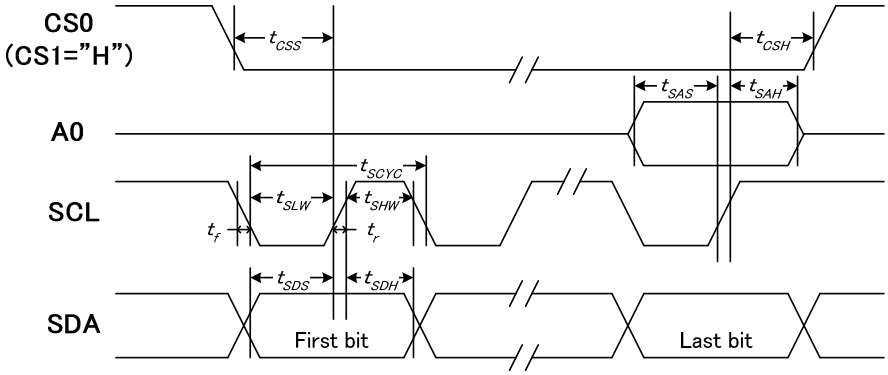
(VDD1 = 3.0V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Control setup time	A0	tAW6			-	ns
Control hold time	R/W	tAH6			-	
System cycle time	E	tCYC6			-	
Enable H pulse width (WRITE)		tEWHW			-	
Enable L pulse width (WRITE)		tEWLW			-	
Enable H pulse width (READ)		tEWHR			-	
Enable L pulse width (READ)		tEWLR			-	
Write data setup time	D[7:0]	tDS6			-	
Write data hold time		tDH6			-	

Note:

1. All timing is specified using 20% and 80% of VDD1 as the reference.
2. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≤ (tCYC6 – tEWLW – tEWHW) for (tr + tf) ≤ (tCYC6 – tEWLR – tEWHR) are specified.
3. tEWLW and tEWLR are specified as the overlap between CS0 being "L" and E being "H".

SERIAL INTERFACE (4-Line Interface)



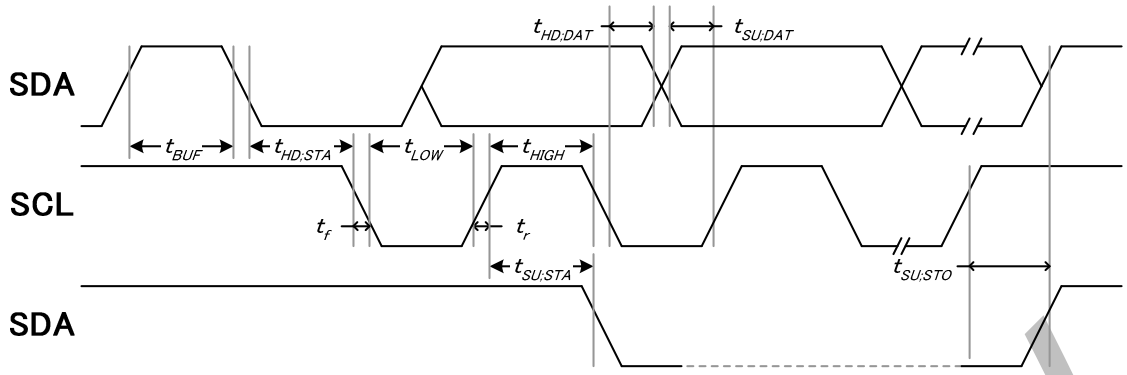
(VDD1 = 3.0V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCL	tSCYC			-	ns
SCL "H" pulse width		tSHW			-	
SCL "L" pulse width		tSLW			-	
Address setup time	A0	tSAS			-	
Address hold time		tSAH			-	
Data setup time	SDA	tSDS			-	
Data hold time		tSDH			-	
CS0 setup time	CS0	tCSS			-	
CS0 hold time		tCSH			-	

Note:

1. All timing is specified using 20% and 80% of VDD1 as the standard.
2. The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

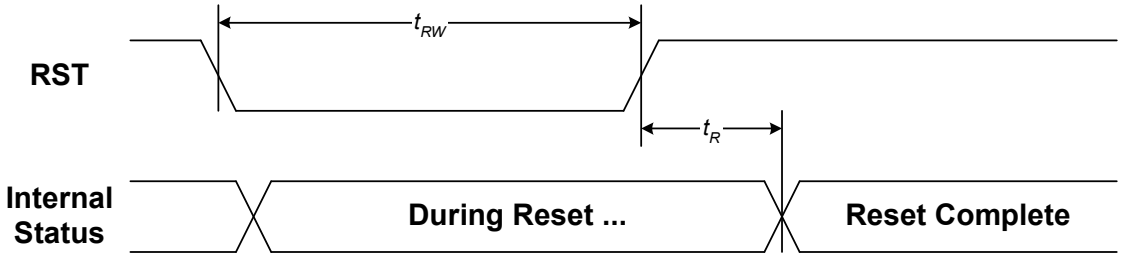
SERIAL INTERFACE (I²C Interface)



(VDD1 = 3.0V , Ta =25°C)

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
SCL clock frequency	SCL	fSCL		-		kHZ
SCL clock low period		tLOW			-	ns
SCL clock high period		tHIGH			-	
Data set-up time	SDA	tSU;Data			-	
Data hold time		tHD;Data			-	
Setup time for a repeated START condition		tSU;STA			-	
Start condition hold time	SDA	tHD;STA			-	
Setup time for STOP condition		tSU;STO			-	
Bus free time between a STOP and START		tBUF			-	

RESET TIMING



(VDD1 = 3.0V , Ta =25°C)

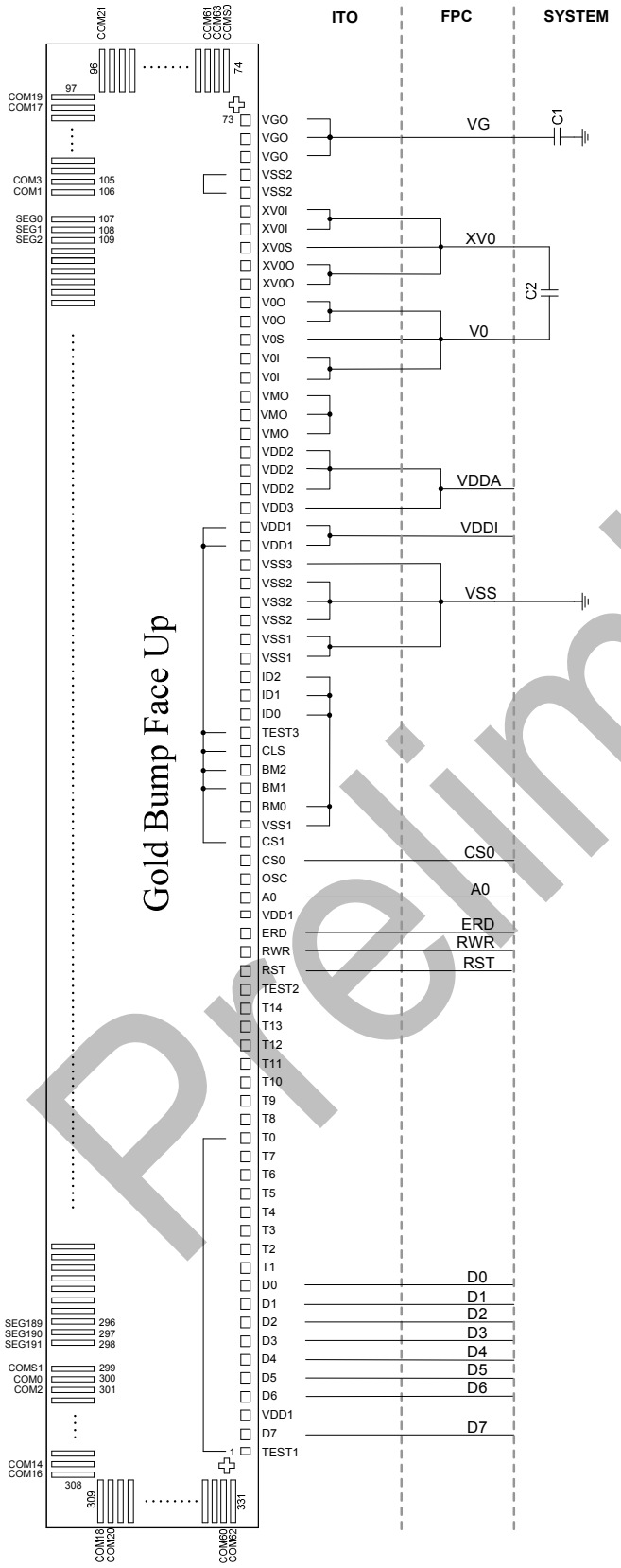
Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		-		us
Reset “L” pulse width	tRW			-	

APPLICATION NOTE

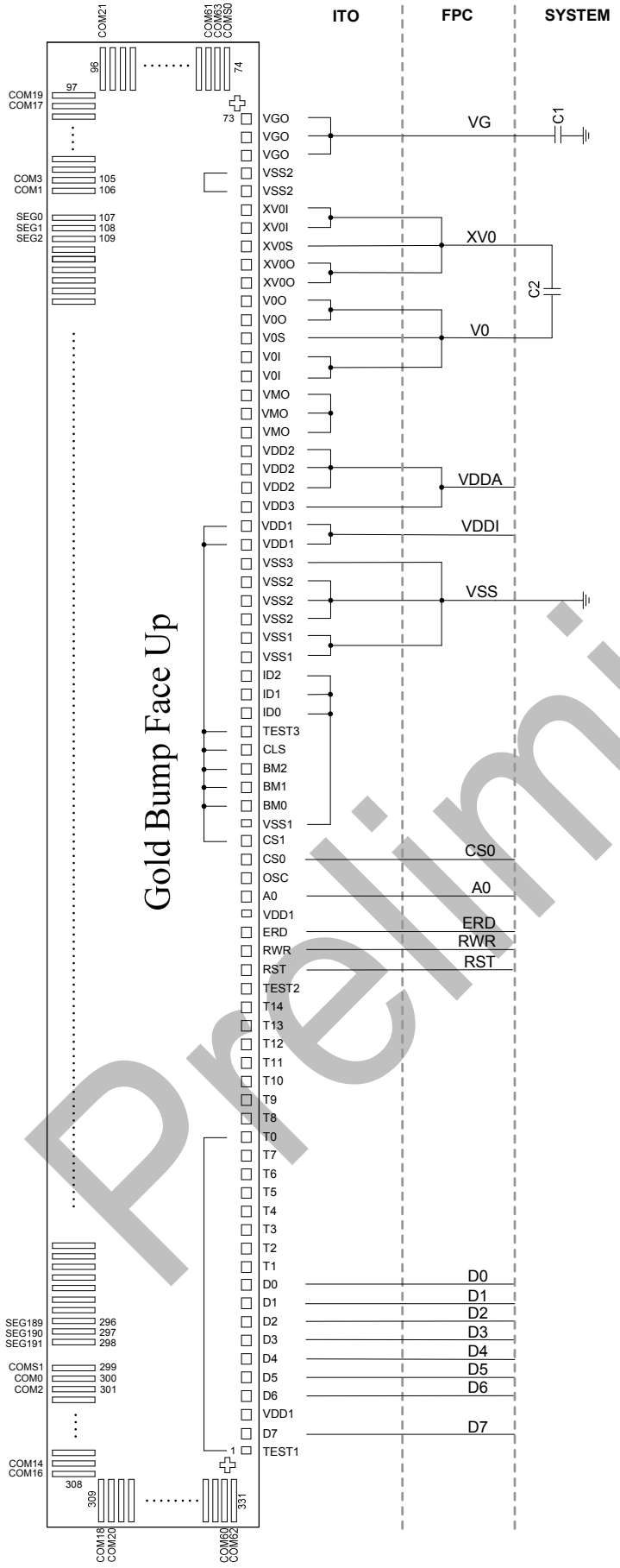
Application Circuits

The application circuits are for reference only and actual settings are dependent on LCD module characteristics.

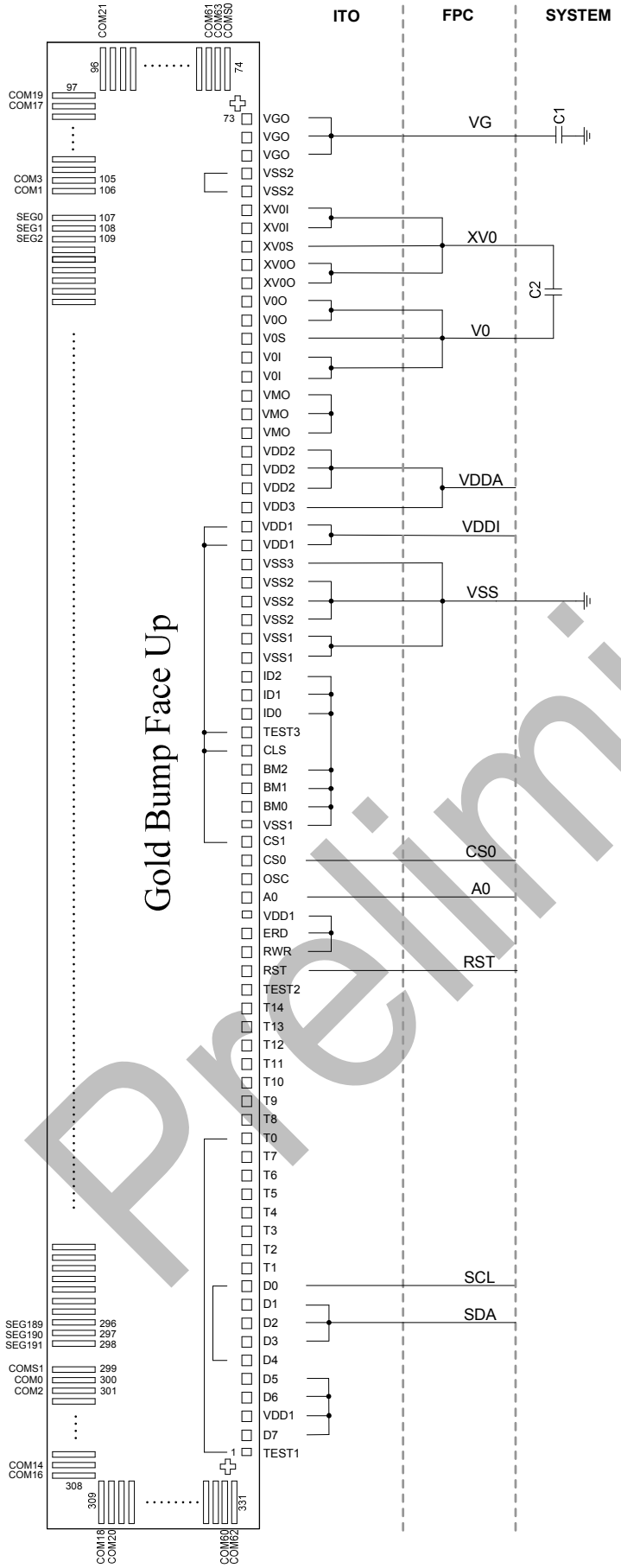
8080 Interface



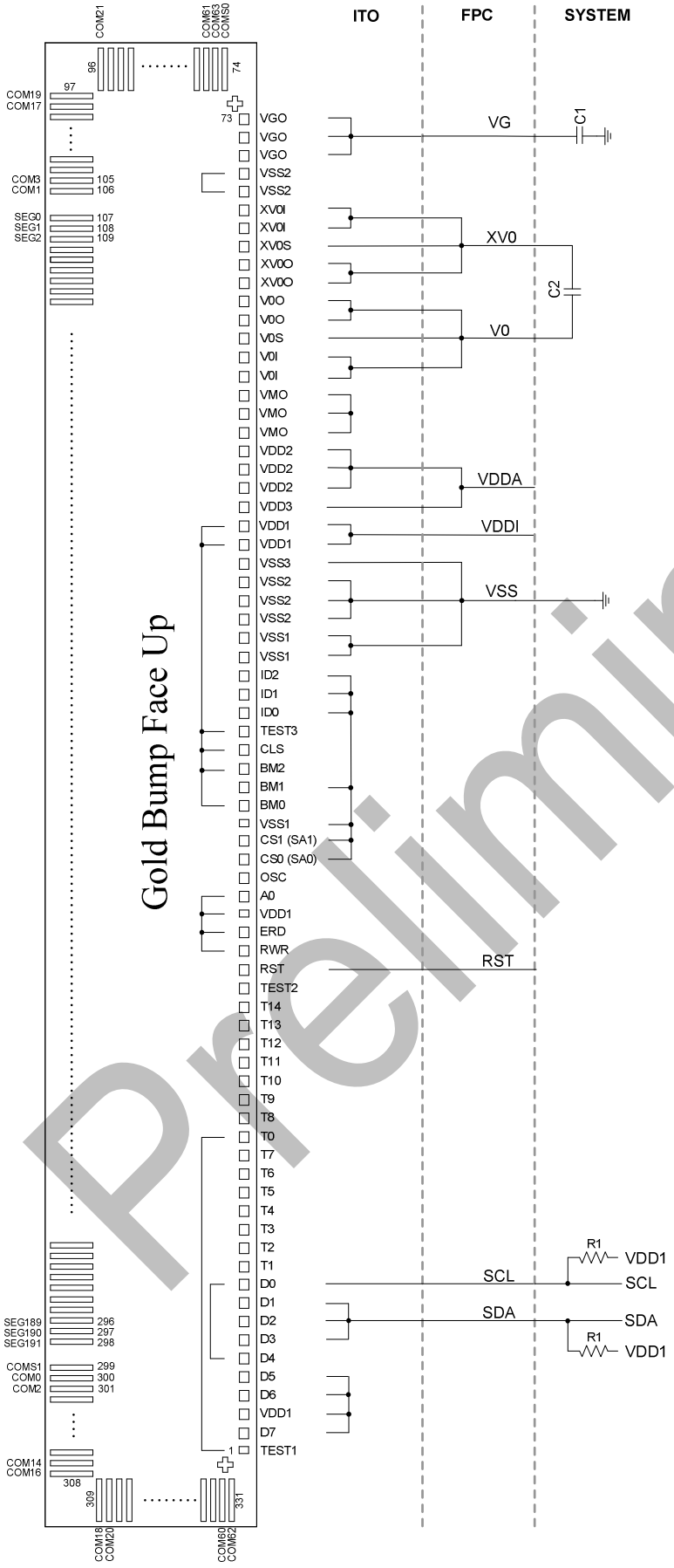
6800 Interface



4 Line SPI Interface



I²C Interface



REVERSION HISTORY

Version	Date	Description
0.0	2012/06/07	Preliminary.
0.1	2012/06/15	Modified the typing error
0.2	2012/07/12	1. Remove temp compensation command and fix it to -0.05%/℃. 2. Modify temperature range. 3. Modify test pins description. 4. Modify FPC layout diagram and equivalent circuit. 5. Modify serial interface pin description and setting. 6. Add read display data feature description in the 4-line SPI interface. 7. Add partial display diagrams. 8. Modify command table of read status and test control. 9. Modify application circuit.
0.3	2012/08/03	1. Modify ITR pin and fix it to interlace mode. 2. Modify D[7:0] pin description of serial interface. 3. Modify application circuit.