Sitronix

ST7533

33 x 96 Dot Matrix LCD Controller/Driver

FEATURES

- Direct display of RAM data through the display data RAM.
- RAM capacity : 33 x 96 = 3168 bits
- Display duty selectable by select pin
  1/33 duty : 33 common x 96 segment
  1/17 duty : 17 common x 96 segment
- High-speed 8-bit MPU interface (The chip can be connected directly to the both the 80x86 series MPUs and the 68000 series MPUs)
  /Serial interfaces are supported.
- Abundant command functions
  Display data Read/Write, display ON/OFF, Normal/ Reverse display mode, page address set, display start line set, column address set, status read, display all points ON/OFF, LCD bias set, electronic volume, read/modify/write, segment driver direction select, power saver, static indicator, common output status select, V_5 voltage regulation internal resistor ratio set.
- Static drive circuit equipped internally for indicators. (1 system, with variable flashing speed.)
- Low-power liquid crystal display power supply circuit equipped internally.
  Booster circuit (with Boost ratios of 2X/3X/4X , where the step-up voltage reference power supply can be input externally).
  High-accuracy voltage adjustment circuit (Thermal gradient –0.15%/°C) V_5 voltage regulator resistors equipped internally, V_1 to V_4 voltage divider resistors equipped internally, electronic volume function equipped internally, voltage follower.
- CR oscillator circuit equipped internally (external clock can also be input)
- Extremely low power consumption Operating power when the built-in power supply is used (an example)
  70uA (V_{DD} – V_{SS} = V_{DD} – V_{SS2} =3.0 V, Quad voltage, V_5 – V_{DD} = – 11.0 V).
  Conditions: When displays pattern OFF and the normal mode is selected.
- Power supply operate on the low 1.8 voltage
  Logic power supply
  V_{DD} – V_{SS} = 1.8V to 3.3V (+10% Range)
  Boost reference voltage: V_{DD} – V_{SS2} = 1.8V to 3.3V
  Booster maximum voltage limited
  V_{OUT}= -13V (+10% Range)
  Liquid crystal drive power supply:
  V_{DD} – V_5 = 4.0V to 13.0 V
- Wide range of operating temperatures: –40 to 85°C
- CMOS process
- These chips not designed for resistance to light or resistance to radiation.

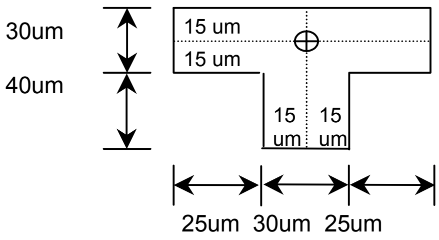
GENERAL DESCRIPTION

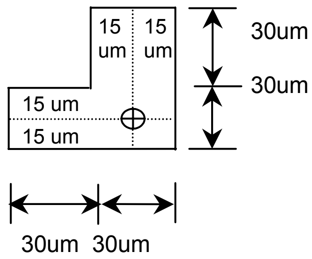
The ST7533 is a single-chip dot matrix LCD drivers that can be connected directly to a microprocessor bus. 8-bit parallel or serial display data sent from the microprocessor is stored in the internal display data RAM and the chip generates a LCD drive signal independent of the microprocessor. Because the chips in the ST7533 contain 33x96 bits of display data RAM and there is a 1-to-1 correspondence between the LCD panel pixels and the internal RAM bits, these chips enable displays with a high degree of freedom.
The ST7533 chips contain 33 common output circuits and 96 segment output circuits, so that a single chip can drive a 33x96 dot display (capable of displaying 8 columnsx4 rows of a 16x16 dot kanji font).
Moreover, the capacity of the display can be extended through the use of master/slave structures between chips.
The chips are able to minimize power consumption because no external operating clock is necessary for the display data RAM read/write operation. Furthermore, because each chip is equipped internally with a low-power LCD driver power supply, resistors for LCD driver power voltage adjustment and a display clock CR oscillator circuit, the ST7533 can be used to create the lowest power display system with the fewest components for high-performance portable devices.

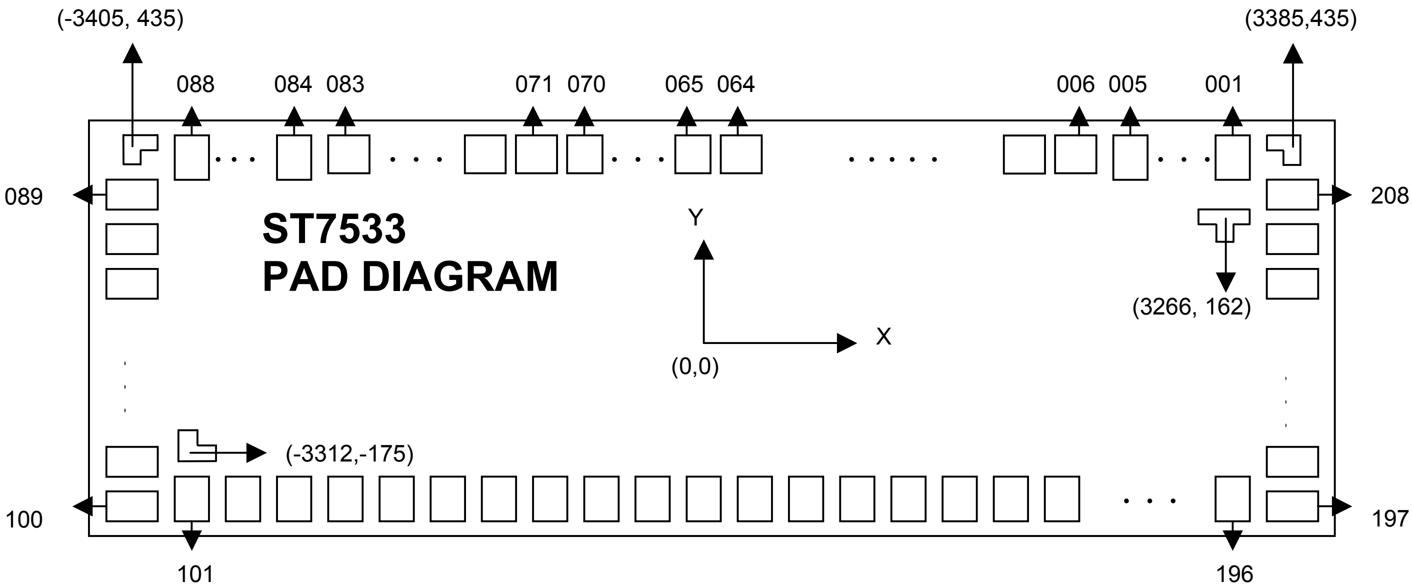
PART NO.	V_{RS} temperature gradient	V_{RS} range
ST7533	-0.15%/°C	-2.1V ±0.03V

ST7533 Pad Arrangement

Chip Size:	7240 μm x 1,000 μm	
Origin: Chip Center		
Bump Pitch:	69.1 μm(Min.)	
Bump Size:	PAD No. 001～005	49.1 μm x 70.5 μm
	PAD No. 006～064	56 μm x 60 μm
	PAD No. 065～070	51 μm x 60 μm
	PAD No. 071～083	56 μm x 60 μm
	PAD No. 084～088	49.1 μm x 70.5 μm
	PAD No. 089～100	70.5 μm x 49.1 μm
	PAD No. 101～196	49.1 μm x 70.5 μm
	PAD No. 197～208	70.5 μm x 49.1 μm
Bump Height:	18 μm(Typ)	
Chip Thickness:	660 μm	







Pad Center Coordinates (1/33 Duty)

PAD No.	PIN Name	X	Y
1	COM[28]	3290	409
2	COM[29]	3221	409
3	COM[30]	3152	409
4	COM[31]	3083	409
5	COMS1	3014	409
6	FRS	2919	414
7	FR	2843	414
8	CL	2767	414
9	/DOF	2691	414
10	VSS	2614	414
11	/CS1	2538	414
12	CS2	2462	414
13	VDD	2386	414
14	/RES	2310	414
15	A0	2234	414
16	VSS	2157	414
17	/WR(R/W)	2081	414
18	/RD(E)	2005	414
19	VDD	1929	414
20	D0	1853	414
21	D1	1777	414
22	D2	1701	414
23	D3	1624	414
24	D4	1548	414
25	D5	1472	414
26	D6	1396	414
27	D7	1320	414
28	VDD	1244	414
29	VDD	1168	414
30	VDD	1091	414
31	VSS	1015	414
32	VSS	939	414
33	VSS2	863	414
34	VSS2	787	414
35	VOUT	711	414
36	VOUT	634	414
37	CAP3-	558	414
38	CAP3-	482	414
39	CAP1+	406	414
40	CAP1+	330	414
41	CAP1-	254	414
42	CAP1-	178	414
43	CAP2-	101	414
44	CAP2-	25	414
45	CAP2+	-51	414
46	CAP2+	-127	414
47	VSS	-203	414
48	VSS	-279	414
49	VRS	-355	414
50	VDD	-432	414
51	VDD	-508	414
52	V1	-584	414

PAD No.	PIN Name	X	Y
53	V1	-660	414
54	V2	-736	414
55	V2	-812	414
56	V3	-889	414
57	V3	-965	414
58	V4	-1041	414
59	V4	-1117	414
60	V5	-1193	414
61	V5	-1269	414
62	VR	-1345	414
63	VDD	-1422	414
64	VDD	-1498	414
65	TEST0	-1571	414
66	TEST1	-1642	414
67	TEST2	-1713	414
68	TEST3	-1784	414
69	TEST4	-1855	414
70	TEST5	-1926	414
71	VDD	-2000	414
72	M/S	-2076	414
73	CLS	-2152	414
74	VSS	-2228	414
75	C86	-2305	414
76	P/S	-2381	414
77	VDD	-2457	414
78	/HPM	-2533	414
79	VSS	-2609	414
80	IRS	-2685	414
81	VDD	-2762	414
82	SEL1	-2838	414
83	VSS	-2914	414
84	COM[15]	-3011	409
85	COM[14]	-3080	409
86	COM[13]	-3150	409
87	COM[12]	-3219	409
88	COM[11]	-3288	409
89	COM[10]	-3529	351
90	COM[9]	-3529	282
91	COM[8]	-3529	213
92	COM[7]	-3529	144
93	COM[6]	-3529	75
94	COM[5]	-3529	6
95	COM[4]	-3529	-64
96	COM[3]	-3529	-133
97	COM[2]	-3529	-202
98	COM[1]	-3529	-271
99	COM[0]	-3529	-340
100	COMS2	-3529	-409
101	SEG[0]	-3280	-409
102	SEG[1]	-3211	-409
103	SEG[2]	-3142	-409
104	SEG[3]	-3073	-409

PAD No.	PIN Name	X	Y
105	SEG[4]	-3004	-409
106	SEG[5]	-2935	-409
107	SEG[6]	-2866	-409
108	SEG[7]	-2797	-409
109	SEG[8]	-2728	-409
110	SEG[9]	-2658	-409
111	SEG[10]	-2589	-409
112	SEG[11]	-2520	-409
113	SEG[12]	-2451	-409
114	SEG[13]	-2382	-409
115	SEG[14]	-2313	-409
116	SEG[15]	-2244	-409
117	SEG[16]	-2175	-409
118	SEG[17]	-2106	-409
119	SEG[18]	-2037	-409
120	SEG[19]	-1967	-409
121	SEG[20]	-1898	-409
122	SEG[21]	-1829	-409
123	SEG[22]	-1760	-409
124	SEG[23]	-1691	-409
125	SEG[24]	-1622	-409
126	SEG[25]	-1553	-409
127	SEG[26]	-1484	-409
128	SEG[27]	-1415	-409
129	SEG[28]	-1346	-409
130	SEG[29]	-1276	-409
131	SEG[30]	-1207	-409
132	SEG[31]	-1138	-409
133	SEG[32]	-1069	-409
134	SEG[33]	-1000	-409
135	SEG[34]	-931	-409
136	SEG[35]	-862	-409
137	SEG[36]	-793	-409
138	SEG[37]	-724	-409
139	SEG[38]	-655	-409
140	SEG[39]	-585	-409
141	SEG[40]	-516	-409
142	SEG[41]	-447	-409
143	SEG[42]	-378	-409
144	SEG[43]	-309	-409
145	SEG[44]	-240	-409
146	SEG[45]	-171	-409
147	SEG[46]	-102	-409
148	SEG[47]	-33	-409
149	SEG[48]	36	-409
150	SEG[49]	106	-409
151	SEG[50]	175	-409
152	SEG[51]	244	-409
153	SEG[52]	313	-409
154	SEG[53]	382	-409
155	SEG[54]	451	-409
156	SEG[55]	520	-409

PAD No.	PIN Name	X	Y
157	SEG[56]	589	-409
158	SEG[57]	658	-409
159	SEG[58]	727	-409
160	SEG[59]	797	-409
161	SEG[60]	866	-409
162	SEG[61]	935	-409
163	SEG[62]	1004	-409
164	SEG[63]	1073	-409
165	SEG[64]	1142	-409
166	SEG[65]	1211	-409
167	SEG[66]	1280	-409
168	SEG[67]	1349	-409
169	SEG[68]	1418	-409
170	SEG[69]	1488	-409
171	SEG[70]	1557	-409
172	SEG[71]	1626	-409
173	SEG[72]	1695	-409
174	SEG[73]	1764	-409
175	SEG[74]	1833	-409
176	SEG[75]	1902	-409
177	SEG[76]	1971	-409
178	SEG[77]	2040	-409
179	SEG[78]	2109	-409
180	SEG[79]	2179	-409
181	SEG[80]	2248	-409
182	SEG[81]	2317	-409
183	SEG[82]	2386	-409
184	SEG[83]	2455	-409
185	SEG[84]	2524	-409
186	SEG[85]	2593	-409
187	SEG[86]	2662	-409
188	SEG[87]	2731	-409
189	SEG[88]	2800	-409
190	SEG[89]	2870	-409
191	SEG[90]	2939	-409
192	SEG[91]	3008	-409
193	SEG[92]	3077	-409
194	SEG[93]	3146	-409
195	SEG[94]	3215	-409
196	SEG[95]	3284	-409
197	COM[16]	3529	-409
198	COM[17]	3529	-340
199	COM[18]	3529	-271
200	COM[19]	3529	-202
201	COM[20]	3529	-133
202	COM[21]	3529	-64
203	COM[22]	3529	6
204	COM[23]	3529	75
205	COM[24]	3529	144
206	COM[25]	3529	213
207	COM[26]	3529	282
208	COM[27]	3529	351

Pad Center Coordinates (1/17 Duty)

PAD No.	PIN Name	X	Y
1	COM[12]	3290	409
2	COM[13]	3221	409
3	COM[14]	3152	409
4	COM[15]	3083	409
5	COMS1	3014	409
6	FRS	2919	414
7	FR	2843	414
8	CL	2767	414
9	/DOF	2691	414
10	VSS	2614	414
11	/CS1	2538	414
12	CS2	2462	414
13	VDD	2386	414
14	/RES	2310	414
15	A0	2234	414
16	VSS	2157	414
17	/WR(R/W)	2081	414
18	/RD(E)	2005	414
19	VDD	1929	414
20	D0	1853	414
21	D1	1777	414
22	D2	1701	414
23	D3	1624	414
24	D4	1548	414
25	D5	1472	414
26	D6	1396	414
27	D7	1320	414
28	VDD	1244	414
29	VDD	1168	414
30	VDD	1091	414
31	VSS	1015	414
32	VSS	939	414
33	VSS2	863	414
34	VSS2	787	414
35	VOUT	711	414
36	VOUT	634	414
37	CAP3-	558	414
38	CAP3-	482	414
39	CAP1+	406	414
40	CAP1+	330	414
41	CAP1-	254	414
42	CAP1-	178	414
43	CAP2-	101	414
44	CAP2-	25	414
45	CAP2+	-51	414
46	CAP2+	-127	414
47	VSS	-203	414
48	VSS	-279	414
49	VRS	-355	414
50	VDD	-432	414
51	VDD	-508	414
52	V1	-584	414

PAD No.	PIN Name	X	Y
53	V1	-660	414
54	V2	-736	414
55	V2	-812	414
56	V3	-889	414
57	V3	-965	414
58	V4	-1041	414
59	V4	-1117	414
60	V5	-1193	414
61	V5	-1269	414
62	VR	-1345	414
63	VDD	-1422	414
64	VDD	-1498	414
65	TEST0	-1571	414
66	TEST1	-1642	414
67	TEST2	-1713	414
68	TEST3	-1784	414
69	TEST4	-1855	414
70	TEST5	-1926	414
71	VDD	-2000	414
72	M/S	-2076	414
73	CLS	-2152	414
74	VSS	-2228	414
75	C86	-2305	414
76	P/S	-2381	414
77	VDD	-2457	414
78	/HPM	-2533	414
79	VSS	-2609	414
80	IRS	-2685	414
81	VDD	-2762	414
82	SEL1	-2838	414
83	VSS	-2914	414
84	Reserve	-3011	409
85	Reserve	-3080	409
86	Reserve	-3150	409
87	Reserve	-3219	409
88	Reserve	-3288	409
89	Reserve	-3529	351
90	Reserve	-3529	282
91	Reserve	-3529	213
92	COM[7]	-3529	144
93	COM[6]	-3529	75
94	COM[5]	-3529	6
95	COM[4]	-3529	-64
96	COM[3]	-3529	-133
97	COM[2]	-3529	-202
98	COM[1]	-3529	-271
99	COM[0]	-3529	-340
100	COMS2	-3529	-409
101	SEG[0]	-3280	-409
102	SEG[1]	-3211	-409
103	SEG[2]	-3142	-409
104	SEG[3]	-3073	-409

PAD No.	PIN Name	X	Y
105	SEG[4]	-3004	-409
106	SEG[5]	-2935	-409
107	SEG[6]	-2866	-409
108	SEG[7]	-2797	-409
109	SEG[8]	-2728	-409
110	SEG[9]	-2658	-409
111	SEG[10]	-2589	-409
112	SEG[11]	-2520	-409
113	SEG[12]	-2451	-409
114	SEG[13]	-2382	-409
115	SEG[14]	-2313	-409
116	SEG[15]	-2244	-409
117	SEG[16]	-2175	-409
118	SEG[17]	-2106	-409
119	SEG[18]	-2037	-409
120	SEG[19]	-1967	-409
121	SEG[20]	-1898	-409
122	SEG[21]	-1829	-409
123	SEG[22]	-1760	-409
124	SEG[23]	-1691	-409
125	SEG[24]	-1622	-409
126	SEG[25]	-1553	-409
127	SEG[26]	-1484	-409
128	SEG[27]	-1415	-409
129	SEG[28]	-1346	-409
130	SEG[29]	-1276	-409
131	SEG[30]	-1207	-409
132	SEG[31]	-1138	-409
133	SEG[32]	-1069	-409
134	SEG[33]	-1000	-409
135	SEG[34]	-931	-409
136	SEG[35]	-862	-409
137	SEG[36]	-793	-409
138	SEG[37]	-724	-409
139	SEG[38]	-655	-409
140	SEG[39]	-585	-409
141	SEG[40]	-516	-409
142	SEG[41]	-447	-409
143	SEG[42]	-378	-409
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146	SEG[45]	-171	-409
147	SEG[46]	-102	-409
148	SEG[47]	-33	-409
149	SEG[48]	36	-409
150	SEG[49]	106	-409
151	SEG[50]	175	-409
152	SEG[51]	244	-409
153	SEG[52]	313	-409
154	SEG[53]	382	-409
155	SEG[54]	451	-409
156	SEG[55]	520	-409

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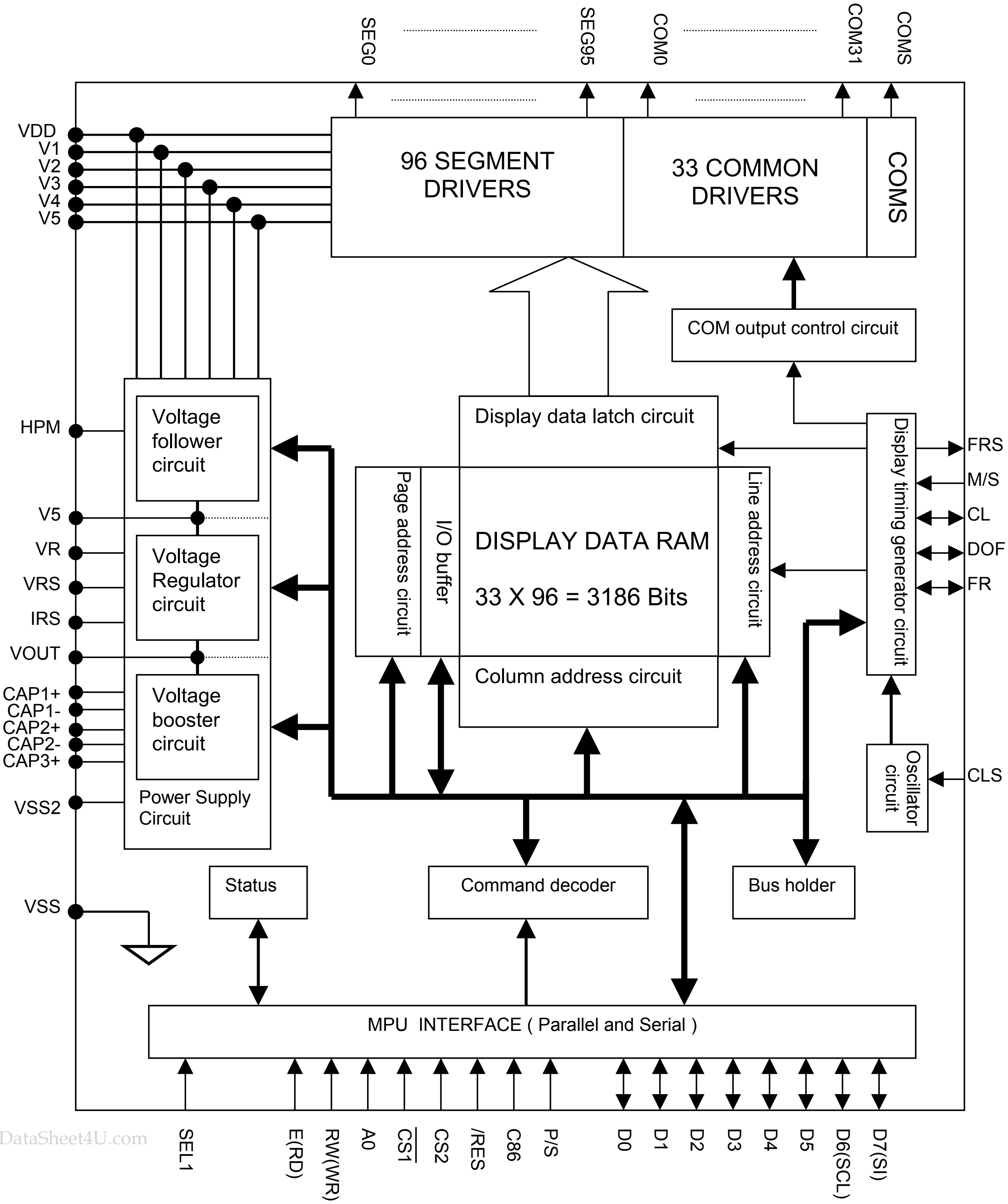
159	SEG[58]	727	-409
160	SEG[59]	797	-409
161	SEG[60]	866	-409
162	SEG[61]	935	-409
163	SEG[62]	1004	-409
164	SEG[63]	1073	-409
165	SEG[64]	1142	-409
166	SEG[65]	1211	-409
167	SEG[66]	1280	-409
168	SEG[67]	1349	-409
169	SEG[68]	1418	-409
170	SEG[69]	1488	-409
171	SEG[70]	1557	-409
172	SEG[71]	1626	-409
173	SEG[72]	1695	-409
174	SEG[73]	1764	-409
175	SEG[74]	1833	-409
176	SEG[75]	1902	-409
177	SEG[76]	1971	-409
178	SEG[77]	2040	-409
179	SEG[78]	2109	-409
180	SEG[79]	2179	-409
181	SEG[80]	2248	-409
182	SEG[81]	2317	-409
183	SEG[82]	2386	-409
184	SEG[83]	2455	-409
185	SEG[84]	2524	-409
186	SEG[85]	2593	-409
187	SEG[86]	2662	-409
188	SEG[87]	2731	-409
189	SEG[88]	2800	-409
190	SEG[89]	2870	-409
191	SEG[90]	2939	-409
192	SEG[91]	3008	-409
193	SEG[92]	3077	-409
194	SEG[93]	3146	-409
195	SEG[94]	3215	-409
196	SEG[95]	3284	-409
197	Reserve	3529	-409
198	Reserve	3529	-340
199	Reserve	3529	-271
200	Reserve	3529	-202
201	Reserve	3529	-133
202	Reserve	3529	-64
203	Reserve	3529	6
204	Reserve	3529	75
205	COM[8]	3529	144
206	COM[9]	3529	213
207	COM[10]	3529	282
208	COM[11]	3529	351

BLOCK DIAGRAM



PIN DESCRIPTIONS

Power Supply Pins

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>VDD</td><td>Power Supply</td><td>Shared with the MPU power supply terminal Vcc.</td><td>12</td></tr>
<tr><td>VSS</td><td>Power Supply</td><td>This is a 0V terminal connected to the system GND.</td><td>9</td></tr>
<tr><td>VSS2</td><td>Power Supply</td><td>This is the reference power supply for the step-up voltage circuit for the liquid crystal drive.</td><td>2</td></tr>
<tr><td>VRS</td><td>Power Supply</td><td>This is the internal-output VREG power supply for the LCD power supply voltage regulator.</td><td>1</td></tr>
<tr><td>V1, V2, V3, V4, V5</td><td>Power Supply</td><td>This is a multi-level power supply for the liquid crystal drive. The voltage Supply applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an op. amp. Voltage levels are determined based on VDD, and must maintain the relative magnitudes shown below.

VDD (= V0) ≧V1 ≧V2 ≧V3 ≧V4 ≧V5

When the power supply turns ON, the internal power supply circuits produce the V1 to V4 voltages shown below. The voltage settings are selected using the LCD bias set command.
<table>
<tr><th></th><th>1/33 DUTY</th><th>1/17 DUTY</th></tr>
<tr><td>V1</td><td>1/6*V5,1/5*V5</td><td>1/6*V5,1/5*V5</td></tr>
<tr><td>V2</td><td>2/6*V5,2/5*V5</td><td>2/6*V5,2/5*V5</td></tr>
<tr><td>V3</td><td>4/6*V5,3/5*V5</td><td>4/6*V5,3/5*V5</td></tr>
<tr><td>V4</td><td>5/6*V5,4/5*V5</td><td>5/6*V5,4/5*V5</td></tr>
</table></td><td>10</td></tr>
</table>

LCD Power Supply Pins

Pin Name	I/O	Function	No. of Pins
CAP1+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.	2
CAP1–	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal.	2
CAP2+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.	2
CAP2–	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2+ terminal.	2
CAP3–	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal.	2
VOUT	O	DC/DC voltage converter. Connect a capacitor between this terminal and VSS.	2
VR	I	Output voltage regulator terminal. Provides the voltage between VDD and V5 through a resistive voltage divider. IRS = “L” : the V5 voltage regulator internal resistors are not used . IRS = “H” : the V5 voltage regulator internal resistors are used .	2

System Bus Connection Pins

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>D5 to D0
D6 (SCL)
D7 (SI)</td><td>I/O</td><td>This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus.
When the serial interface is selected (P/S = “L”) :
D7 : serial data input (SI) ; D6 : the serial clock input (SCL).
D0 to D5 are set to high impedance.
When the chip select is not active, D0 to D7 are set to high impedance.</td><td>8</td></tr>
<tr><td>A0</td><td>I</td><td>This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command.
A0 = “H”: Indicates that D0 to D7 are display data.
A0 = “L”: Indicates that D0 to D7 are control data.</td><td>1</td></tr>
<tr><td>/RES</td><td>I</td><td>When /RES is set to “L,” the settings are initialized.

The reset operation is performed by the /RES signal level.</td><td>1</td></tr>
<tr><td>/CS1
CS2</td><td>I</td><td>This is the chip select signal. When /CS1 = “L” and CS2 = “H,” then the chip select becomes active, and data/command I/O is enabled.</td><td>2</td></tr>
<tr><td>/RD
(E)</td><td>I</td><td>• When connected to an 8080 MPU, this is active LOW.
(E) This pin is connected to the /RD signal of the 8080 MPU, and the ST7533 series data bus is in an output status when this signal is “L”.
• When connected to a 6800 Series MPU, this is active HIGH.
This is the 6800 Series MPU enable clock input terminal.</td><td>1</td></tr>
<tr><td>/WR
(R/W)</td><td>I</td><td>• When connected to an 8080 MPU, this is active LOW.
(R/W) This terminal connects to the 8080 MPU/WR signal. The signals on the data bus are latched at the rising edge of the /WR signal.
• When connected to a 6800 Series MPU:
This is the read/write control signal input terminal.
When R/W = “H”: Read.
When R/W = “L”: Write.</td><td>1</td></tr>
<tr><td>C86</td><td>I</td><td>This is the MPU interface switch terminal.
C86 = “H”: 6800 Series MPU interface.
C86 = “L”: 8080 MPU interface.</td><td>1</td></tr>
<tr><td>P/S</td><td>I</td><td>This is the parallel data input/serial data input switch terminal.
P/S = “H”: Parallel data input.
P/S = “L”: Serial data input.
The following applies depending on the P/S status:
<table>
<tr><th>P/S</th><th>Data/Command</th><th>Data</th><th>Read/Write</th><th>Serial Clock</th></tr>
<tr><td>“H”</td><td>A0</td><td>D0 to D7</td><td>/RD, /WR</td><td>X</td></tr>
<tr><td>“L”</td><td>A0</td><td>SI (D7)</td><td>Write only</td><td>SCL (D6)</td></tr>
</table>
When P/S = “L”, D0 to D5 fixed to either “H”.
/RD (E) and /WR (R/W) are fixed to either “H” or “L”.
With serial data input, It is impossible read data from RAM .</td><td>1</td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>CLS</td><td>I</td><td>Terminal to select whether or enable or disable the display clock internal oscillator circuit.
CLS = “H” : used Internal oscillator circuit .
CLS = “L” : used external clock input .(internal oscillator is disable)
When CLS = “L”, input the display clock through the CL terminal.</td><td>1</td></tr>
<tr><td>M/S</td><td>I</td><td>This terminal selects the master/slave operation for the ST7533 Series chips.
Master operation outputs the timing signals that are required for the LCD display, while slave operation input the timing signals required for the liquid crystal display,
Synchronizing the liquid crystal display system.
M/S = “H” Master operation
M/S = “L” Slave operation
<table>
<tr><th>M/S</th><th>CLS</th><th>Oscillator Circuit</th><th>Power Supply Circuit</th><th>CL</th><th>FR</th><th>FRS</th><th>DOF</th></tr>
<tr><td rowspan="2">“H”</td><td>“H”</td><td>Enabled</td><td>Enabled</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>“L”</td><td>Disabled</td><td>Enabled</td><td>Input</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td rowspan="2">“L”</td><td>“H”</td><td>Disabled</td><td>Disabled</td><td>Input</td><td>Input</td><td>Output</td><td>Input</td></tr>
<tr><td>“L”</td><td>Disabled</td><td>Disabled</td><td>Input</td><td>Input</td><td>Output</td><td>Input</td></tr>
</table></td><td>1</td></tr>
<tr><td>CL</td><td>I/O</td><td>This is the display clock input terminal
The following is true depending on the M/S and CLS status.
<table>
<tr><th>M/S</th><th>CLS</th><th>CL</th></tr>
<tr><td rowspan="2">“H”</td><td>“H”</td><td>Output</td></tr>
<tr><td>“L”</td><td>Input</td></tr>
<tr><td rowspan="2">“L”</td><td>“H”</td><td>Input</td></tr>
<tr><td>“L”</td><td>Input</td></tr>
</table></td><td>1</td></tr>
<tr><td>FR</td><td>O</td><td>This is the liquid crystal alternating current signal terminal.</td><td>1</td></tr>
<tr><td>/DOF</td><td>O</td><td>This is the LCD blanking control terminal.</td><td>1</td></tr>
<tr><td>FRS</td><td>O</td><td>This is the output terminal for the static drive.
This terminal is only enabled when the static indicator display is ON and is used in conjunction with the FR terminal.</td><td>1</td></tr>
<tr><td>IRS</td><td>I</td><td>This terminal selects the resistors for the V5 voltage level adjustment.
IRS = “H”: Use the internal resistors
IRS = “L”: Do not use the internal resistors. The V5 voltage level is regulated by an external resistive voltage divider attached to the VR terminal</td><td>1</td></tr>
<tr><td>/HPM</td><td>I</td><td>This is the power control terminal for the power supply circuit for liquid crystal drive.
/HPM = “H”: Normal mode
/HPM = “L”: High power mode</td><td>1</td></tr>
<tr><td>SEL1</td><td>I</td><td>These pins are DUTY selection.
<table>
<tr><th>SEL 1</th><th>DUTY</th><th>BIAS</th></tr>
<tr><td>0</td><td>1/33</td><td>1/5 or 1/6</td></tr>
<tr><td>1</td><td>1/17</td><td>1/5 or 1/6</td></tr>
</table></td><td>1</td></tr>
<tr><td>TEST0 ~ 5</td><td>I</td><td>These are terminals for IC testing .
TEST0 (PAD No.65) must connect to VDD
TEST1 ~ 5 must floating</td><td>6</td></tr>
</table>

LCD Driver Pins

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>SEG0
to
SEG95</td><td>O</td><td>These are the LCD segment drive outputs. Through a combination of the contents of the display RAM and with the FR signal, a single level is selected from V_{DD}, V2, V3, and V5.
<table>
<tr><th rowspan="2">RAM DATA</th><th rowspan="2">FR</th><th colspan="2">Output Voltage</th></tr>
<tr><td>Normal Display</td><td>Reverse Display</td></tr>
<tr><td>H</td><td>H</td><td>V_{DD}</td><td>V_2</td></tr>
<tr><td>H</td><td>L</td><td>V_5</td><td>V_3</td></tr>
<tr><td>L</td><td>H</td><td>V_2</td><td>V_{DD}</td></tr>
<tr><td>L</td><td>L</td><td>V_3</td><td>V_5</td></tr>
<tr><td>Power save</td><td>----</td><td colspan="2">V_{DD}</td></tr>
</table>
</td><td>96</td></tr>
<tr><td>COM0
to
COMn</td><td>O</td><td>These are the LCD common drive outputs.
<table>
<tr><th>Part No.</th><th>COM</th><th>TOTAL</th></tr>
<tr><td>33 DUTY</td><td>COM0 ~ COM31</td><td>32</td></tr>
<tr><td>17 DUTY</td><td>COM0 ~ COM15</td><td>16</td></tr>
</table>
Through a combination of the contents of the scan data and with the FR signal, a single level is selected from V_{DD}, V_1, V_4, and V_5.
<table>
<tr><th>Scan Data</th><th>FR</th><th>Output Voltage</th></tr>
<tr><td>H</td><td>H</td><td>V_5</td></tr>
<tr><td>H</td><td>L</td><td>V_{DD}</td></tr>
<tr><td>L</td><td>H</td><td>V_1</td></tr>
<tr><td>L</td><td>L</td><td>V_4</td></tr>
<tr><td>Power save</td><td>----</td><td>V_{DD}</td></tr>
</table>
</td><td></td></tr>
<tr><td>COMS</td><td>O</td><td>These are the COM output terminals for the indicator. Both terminals output the same signal.
Leave these open if they are not used.</td><td>2</td></tr>
</table>

DESCRIPTION OF FUNCTIONS

The MPU Interface

Selecting the Interface Type

With the ST7533 chips, data transfers are done through an 8-bit parallel data bus (D7 to D0) or through a serial data input (SI). Through selecting the P/ S terminal polarity to the "H" or "L" it is possible to select either parallel data input or serial data input as shown in Table 1.

Table 1

P/S	/CS1	CS2	A0	/RD	/WR	C86	D7	D6	D5~D0
H: Parallel Input	/CS1	CS2	A0	/RD	/WR	C86	D7	D6	D5~D0
L: Serial Input	/CS1	CS2	A0	—	—	—	SI	SCL	(HZ)

"—" indicates fixed to either "H" or to "L"

The Parallel Interface

When the parallel interface has been selected (P/S ="H"), then it is possible to connect directly to either an 8080-system MPU or a 6800 Series MPU (shown in Table 2) by selecting the C86 terminal to either "H" or to "L".

Table 2

C86 (P/S=H)	/CS1	CS2	A0	/RD	/WR	D7~D0
H: 6800 Series	/CS1	CS2	A0	E	R/W	D7~D0
L: 8080 Series	/CS1	CS2	A0	/RD	/WR	D7~D0

Moreover, data bus signals are recognized by a combination of A0, /RD (E), /WR (R/W) signals, as shown in Table 3.

Table 3

Shared	6800 Series	8080 Series		Function
A0	R/W	/RD	/WR	
1	1	0	1	Reads the display data
1	0	1	0	Writes the display data
0	1	0	1	Status read
0	0	1	0	Write control data (command)

The Serial Interface

When the serial interface has been selected (P/S = "L") then when the chip is in active state (/CS1 = "L" and CS2 = "H") the serial data input (SI) and the serial clock input (SCL) can be received. The serial data is read from the serial data input pin in the rising edge of the serial clocks D7, D6 through D0, in this order. This data is converted to 8 bits parallel data in the rising edge of the eighth serial clock for the processing.

The A0 input is used to determine whether or the serial data input is display data or command data; when A0 = "H", the data is display data, and when A0 = "L" then the data is command data. The A0 input is read and used for detection every 8th rising edge of the serial clock after the chip becomes active. Figure 1 is a serial interface signal chart.

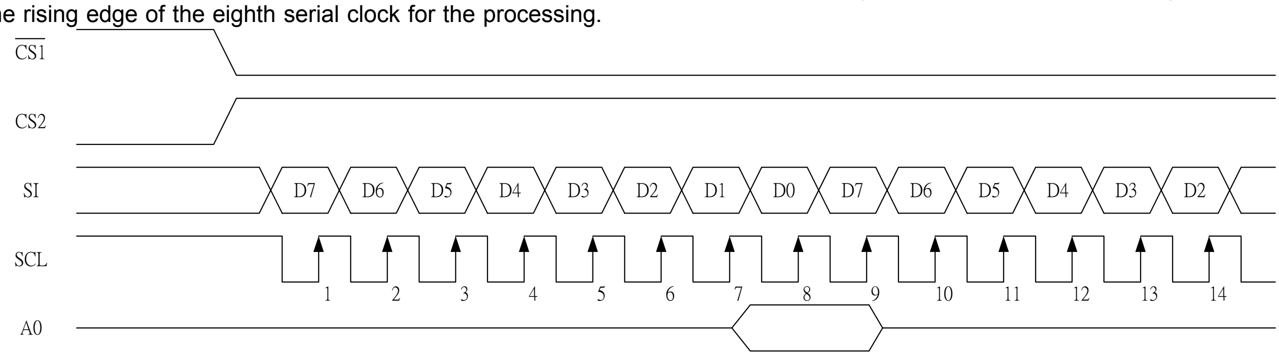


Figure 1

* When the chip is not active, the shift registers and the counter are reset to their initial states.
* Reading is not possible while in serial interface mode.
* Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend that operation be rechecked on the actual equipment.

The Chip Select

The ST7533 have two chip select terminals: /CS1 and CS2. The MPU interface or the serial interface is enabled only when /CS1 = "L" and CS2 = "H".

When the chip select is inactive, D0 to D7 enter a high impedance state, and the A0, /RD, and /WR inputs are inactive. When the serial interface is selected, the shift register and the counter are reset.

The Accessing the Display Data RAM and the Internal Registers

Data transfer at a higher speed is ensured since the MPU is required to satisfy the cycle time (t_{CYC}) requirement alone in accessing the ST7533. Wait time may not be considered.
And, in the ST7533, each time data is sent from the MPU, a type of pipeline process between LSIs is performed through the bus holder attached to the internal data bus. Internal data bus.
For example, when the MPU writes data to the display data RAM, once the data is stored in the bus holder, then it is written to the display data RAM before the next data write cycle. Moreover, when the MPU reads the display data RAM, the first data read cycle (dummy) stores the read data in the bus holder, and then the data is read from the bus holder to the system bus at the next data read cycle.
There is a certain restriction in the read sequence of the display data RAM. Please be advised that data of the specified address is not generated by the read instruction issued immediately after the address setup. This data is generated in data read of the second time. Thus, a dummy read is required whenever the address setup or write cycle operation is conducted.
This relationship is shown in Figure 2.

The Busy Flag

When the busy flag is "1" it indicates that the ST7533 is running internal processes, and at this time no command aside from a status read will be received. The busy flag is outputted to D7 pin with the read instruction. If the cycle time (tCYC) is maintained, it is not necessary to check for this flag before each command. This makes vast improvements in MPU processing capabilities possible.

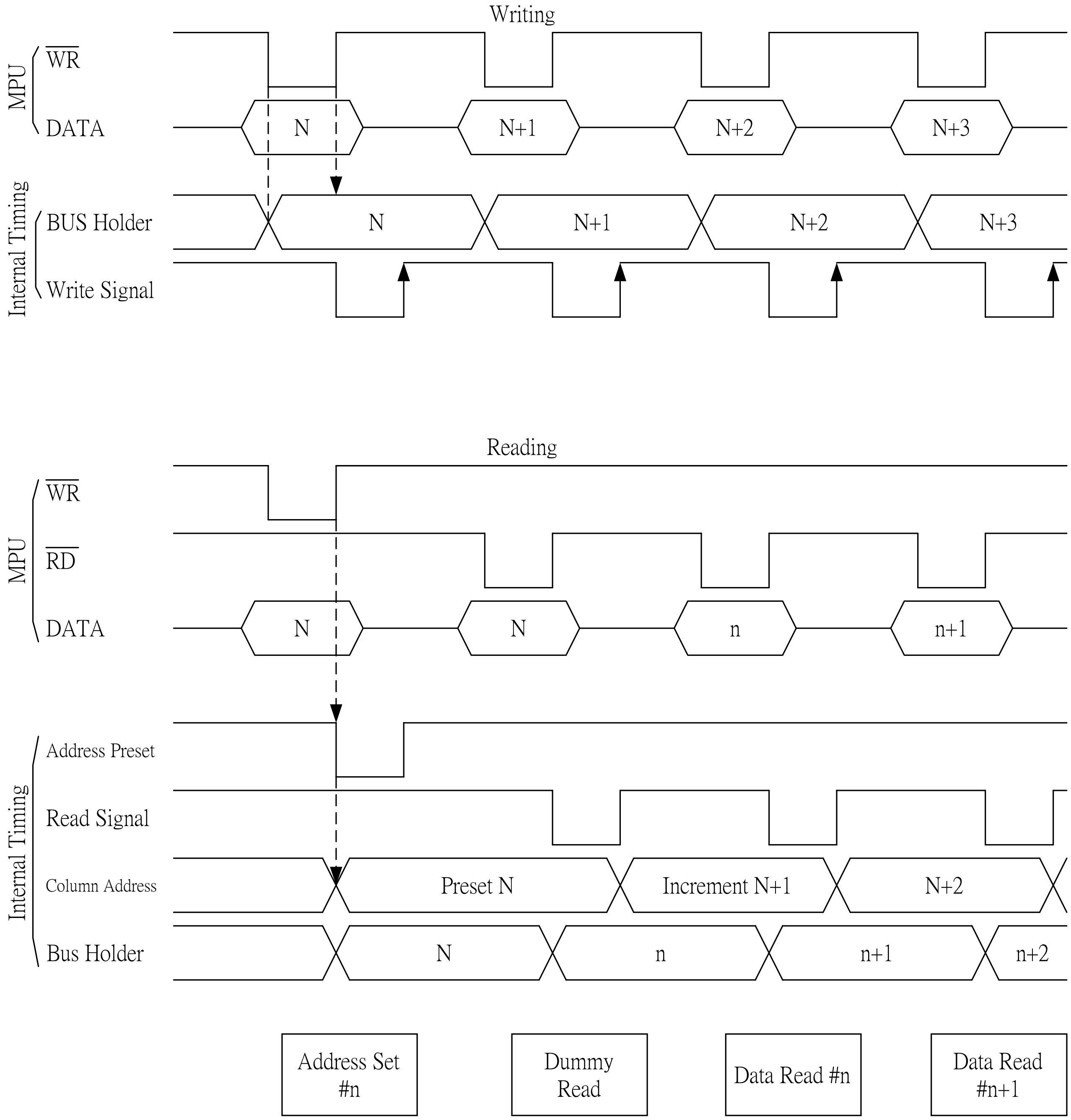
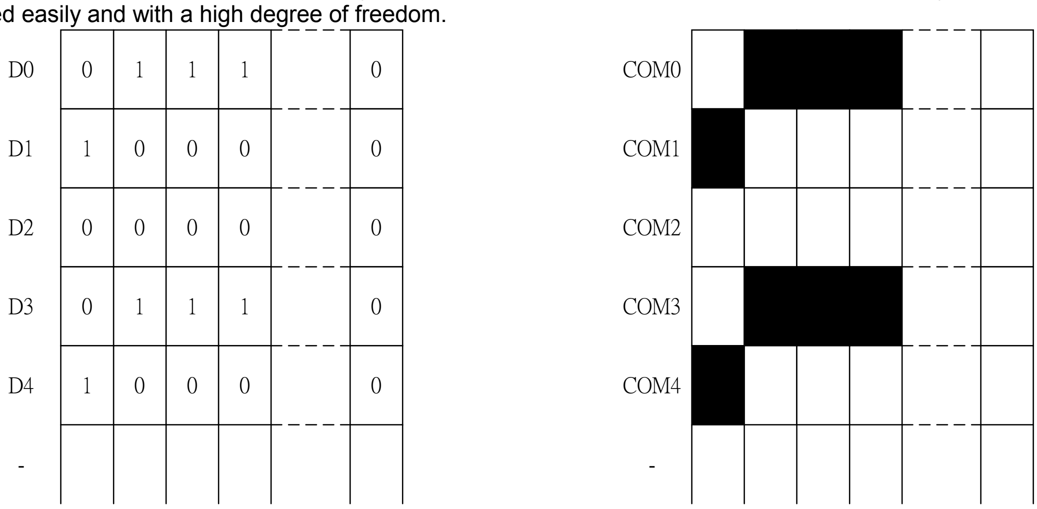


Figure 2

Display Data RAM

The display data RAM stores the dot data for the LCD. It has a 33 (4 page x 8 bit +1) x 96 bit structure.
as is shown in Figure 3, the D7 to D0 display data from the MPU corresponds to the LCD display common direction, there are few constraints at the time of display data transfer when multiple ST7533 are used, thus and display structures can be created easily and with a high degree of freedom.

Moreover, reading from and writing to the display RAM from the MPU side is performed through the I/O buffer, which is an independent operation from signal reading for the liquid crystal driver. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, it will not cause adverse effects on the display (such as flickering).



Display data RAM

Liquid crystal display

Figure 3

The Page Address Circuit

Page address of the display data RAM is specified through the Page Address Set Command. The page address must be specified again when changing pages to perform access.

Page address 8 (D3, D2, D1, D0 = 1, 0, 0, 0) is a special RAM for icons, and only display data D0 is used.
(see Figure 4)

The Column Addresses

The display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/write command. This allows the MPU display data to be accessed continuously. Moreover, the incrementing of column addresses stops with 5FH. Because the column address is independent of the page address, when moving, for example, from page 0 column 5FH to page 1 column 00H, it is necessary to respecify both the page address and the column address.
Furthermore, as is shown in Table 4, the ADC command (segment driver direction select command) can be used to reverse the relationship between the display data RAM column address and the segment output. Because of this, the constraints on the IC layout when the LCD module is assembled can be minimized. As is shown in Figure 4,

Table 4

SEG Output / **ADC**	**SEG0**		**SEG 95**
(D0) "0"	0 (H)	→ Column Address →	5F(H)
(D0) "1"	5F(H)	← Column Address ←	0 (H)

The Line Address Circuit

The line address circuit, as shown in Table 4, specifies the line address relating to the COM output when the contents of the display data RAM are displayed. Using the display start line address set command, what is normally the top line of the display can be specified (this is the COM0 output when the common output mode is normal, and the COM31 output for ST7533 , the detail is shown page.11 The display area is a 33 line area for the ST7533.
If the line addresses are changed dynamically using the display start line address set command, screen scrolling, page swapping, etc. can be performed.

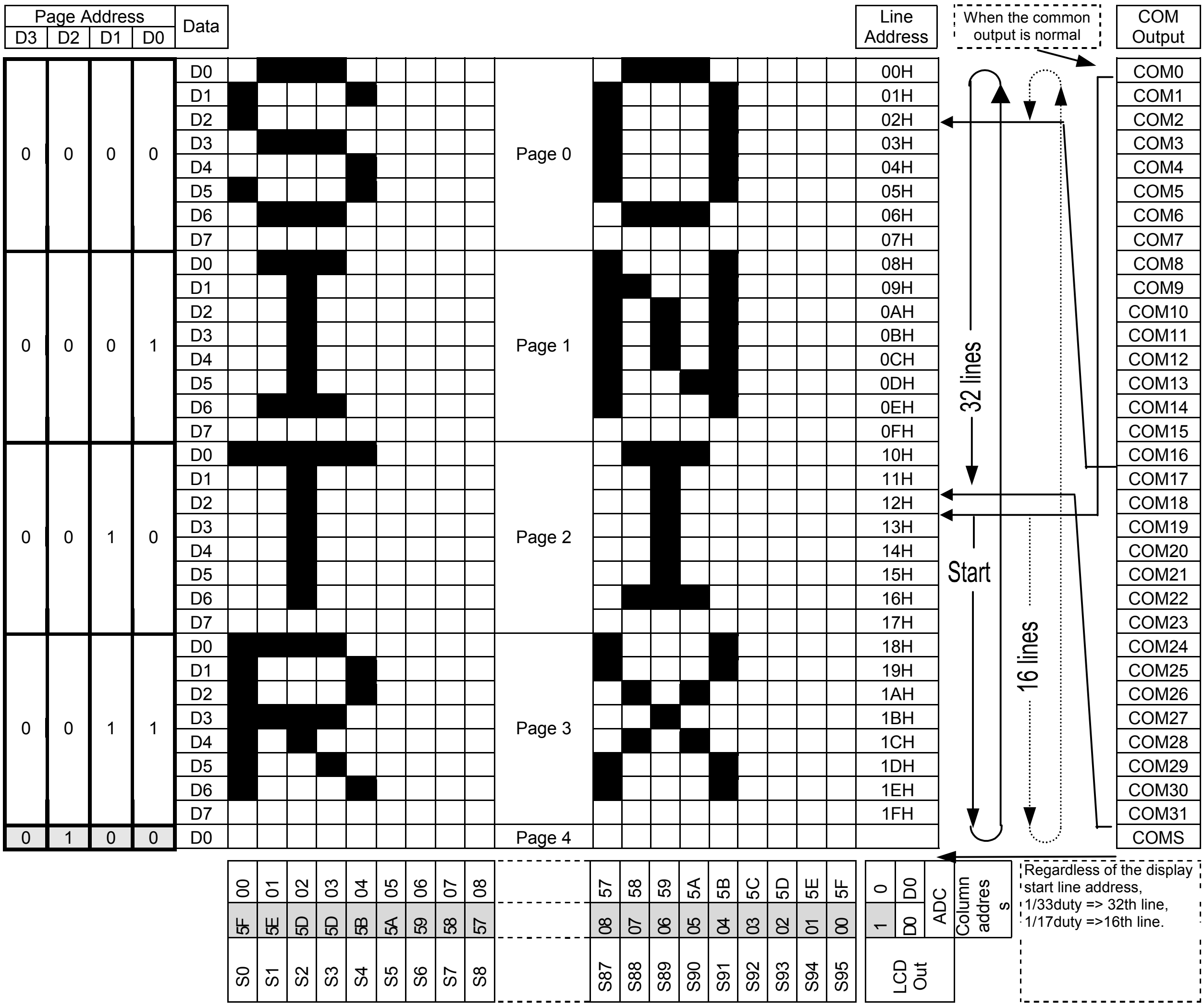

Page Address
D3 D2 D1 D0
Data
Line Address
When the common output is normal
COM Output
Page 0
Page 1
Page 2
Page 3
Page 4
32 lines
16 lines
Start
Regardless of the display start line address, 1/33duty => 32th line, 1/17duty =>16th line.
ADC
Column address
LCD Out
COMS

Figure 4

The Display Data Latch Circuit

The display data latch circuit is a latch that temporarily stores the display data that is output to the liquid crystal driver circuit from the display data RAM.
Because the display normal/reverse status, display ON/OFF status, and display all points ON/OFF commands control only the data within the latch, they do not change the data within the display data RAM itself.

The Oscillator Circuit

This is a CR-type oscillator that produces the display clock. The oscillator circuit is only enabled when M/S= “H” and CLS = “H”. When CLS = “L” the oscillation stops, and the external clock is input through the CL terminal.

Display Timing Generator Circuit

The display timing generator circuit generates the timing signal to the line address circuit and the display data latch circuit using the display clock. The display data is latched into the display data latch circuit synchronized with the display clock, and is output to the data driver output terminal. Reading to the display data liquid crystal driver circuits is completely independent of accesses to the display data RAM by the MPU. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, there is absolutely no adverse effect (such as flickering) on the display.
Moreover, the display timing generator circuit generates the common timing and the liquid crystal alternating current signal (FR) from the display clock. It generates a drive wave form using a 2 frame alternating current drive method, as is shown in Figure 5, for the liquid crystal drive circuit.

Two-frame alternating current drive waveform

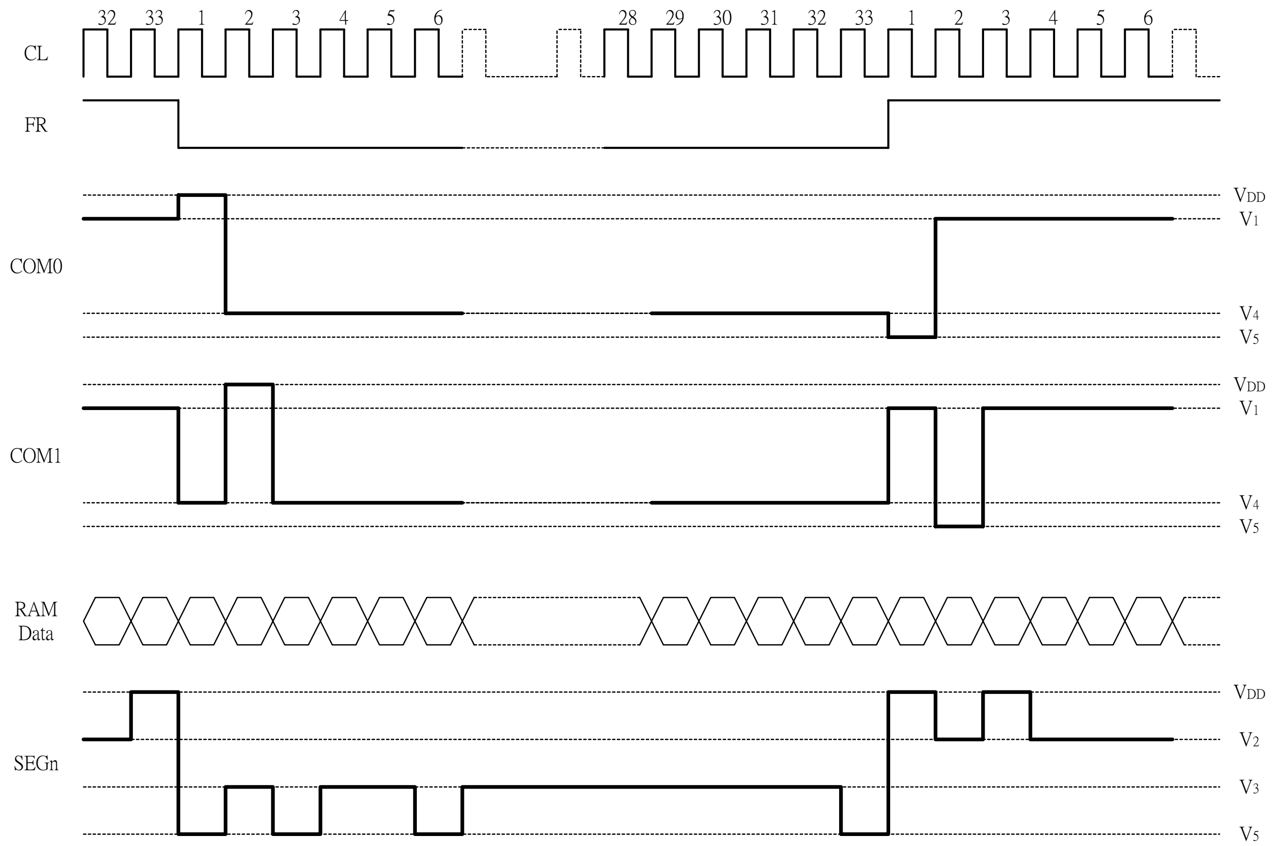


Figure 5

The Common Output Status Select Circuit

In the ST7533 chips, the COM output scan direction can be selected by the common output status select command. (See Table 6.) Consequently, the constraints in IC layout at the time of LCD module assembly can be minimized.

Table 6

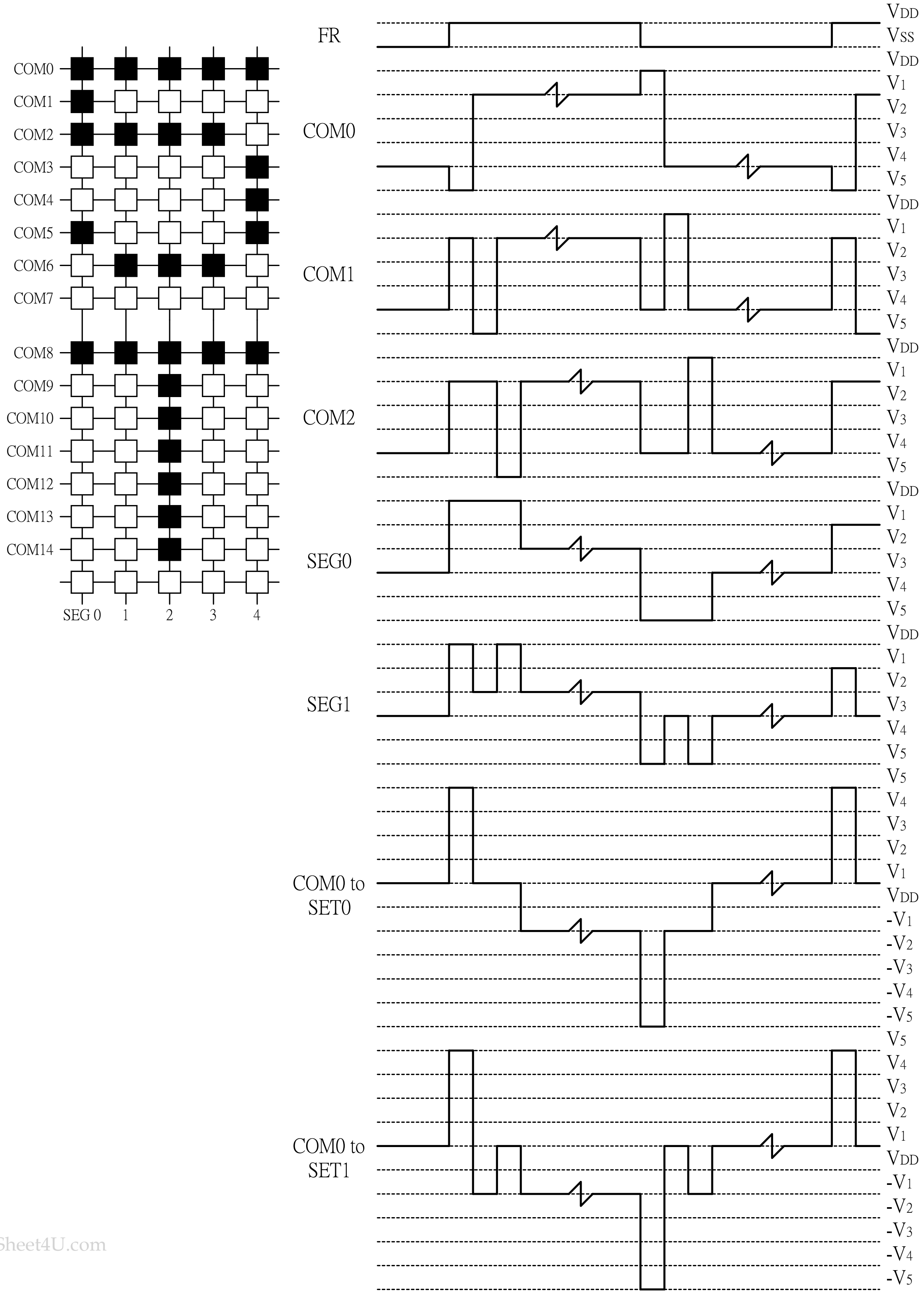
Status	COM Scan Direction	
	1/33 DUTY	**1/17 DUTY**
Normal	COM0 → COM31	COM0 → COM15
Reverse	COM31 → COM0	COM15 → COM0

Duty	Com dir	com[0:15] Common output pins com[16:31]																															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	**coms**
1/33	0	com[0:7]								com[8:15]								com[16:23]								com[23:31]								coms
	1	com[31:23]								com[23:16]								com[15:8]								com[7:0]								coms
1/17	0	com[0:7]								**reserve**																com[8:15]								coms
	1	com[15:8]								**reserve**																com[7:0]								coms

The LCD Driver Circuits

These are a 129-channel, that generate four voltage levels for driving the LCD . The combination of the display data, the COM scan signal, and the FR signal produces the liquid crystal drive voltage output.

Figure-6 shows examples of the SEG and COM output wave form.



COM0
COM1
COM2
COM3
COM4
COM5
COM6
COM7
COM8
COM9
COM10
COM11
COM12
COM13
COM14
SEG 0
1
2
3
4
FR
COM0
COM1
COM2
SEG0
SEG1
COM0 to SET0
COM0 to SET1
VDD
VSS
V1
V2
V3
V4
V5
-V1
-V2
-V3
-V4
-V5

Figure 6

The Power Supply Circuits

The power supply circuits are low-power consumption power supply circuits that generate the voltage levels required for the LCD drivers. They are Booster circuits, voltage regulator circuits, and voltage follower circuits. They are only enabled in master operation. The power supply circuits can turn the Booster circuits, the voltage regulator circuits, and the voltage follower circuits ON or OFF independently through the use of the Power Control Set command. Consequently, it is possible to make an external power supply and the internal power supply function somewhat in parallel. Table 7 shows the Power Control Set Command 3-bit data control function, and Table 8 shows reference combinations.

Table 7

bit	function	Status "1"	Status "0"
D2	Booster circuit control bit	ON	OFF
D1	Voltage regulator circuit control bit (V/R circuit)	ON	OFF
D0	Voltage follower circuit control bit (V/F circuit)	ON	OFF

The Control Details of Each Bit of the Power Control Set Command

Table 8

Use Settings	D2	D1	D0	Voltage booster	Voltage regulator	Voltage follower	External voltage input	Step-up voltage
Only the internal power supply is used	1	1	1	ON	ON	ON	V_{SS2}	Used
Only the voltage regulator circuit and the voltage follower circuit are used	0	1	1	OFF	ON	ON	V_{OUT}, V_{SS2}	Open
Only the V/F circuit is used	0	0	1	OFF	OFF	ON	V5, V_{SS2}	Open
Only the external power supply is used	0	0	0	OFF	OFF	OFF	V_1 to V_5	Open

Reference Combinations

* The "step-up system terminals" refer CAP1+, CAP1–, CAP2+, CAP2–, and CAP3–.
* While other combinations, not shown above, are also possible, these combinations are not recommended because they have no practical use.

The Step-up Voltage Circuits

Using the step-up voltage circuits equipped within the ST7533 chips it is possible to product a 2X,3X or 4X step-up of the V_{DD} – V_{SS2} voltage levels.

4X step-up: Connect capacitor C1 between CAP1+ and CAP1–, between CAP2+ and CAP2–, between CAP1+ and CAP3–, and between V_{SS2} and V_{OUT}, to produce a voltage level in the negative direction at the V_{OUT} terminal that is 4 times the voltage level between V_{DD} and V_{SS}2.

3X step-up: Connect capacitor C1 between CAP1+ and CAP1–, between CAP2+ and CAP2– and between V_{SS2} and V_{OUT}, and short and shor between CAP3– and V_{OUT} to produce a voltage level in the negative direction at the V_{OUT} terminal that is 3 times the voltage difference between V_{DD} and V_{SS}2.

2X step-up: Connect capacitor C1 between CAP1+ and CAP1–, and between V_{SS2} and V_{OUT}, leave CAP2+ open, and short between CAP2–, CAP3– and V_{OUT} to produce a voltage in the negative direction at the V_{OUT} terminal that Is twice the voltage between V_{DD} and V_{SS}2.

The step-up voltage relationships are shown in Figure 7

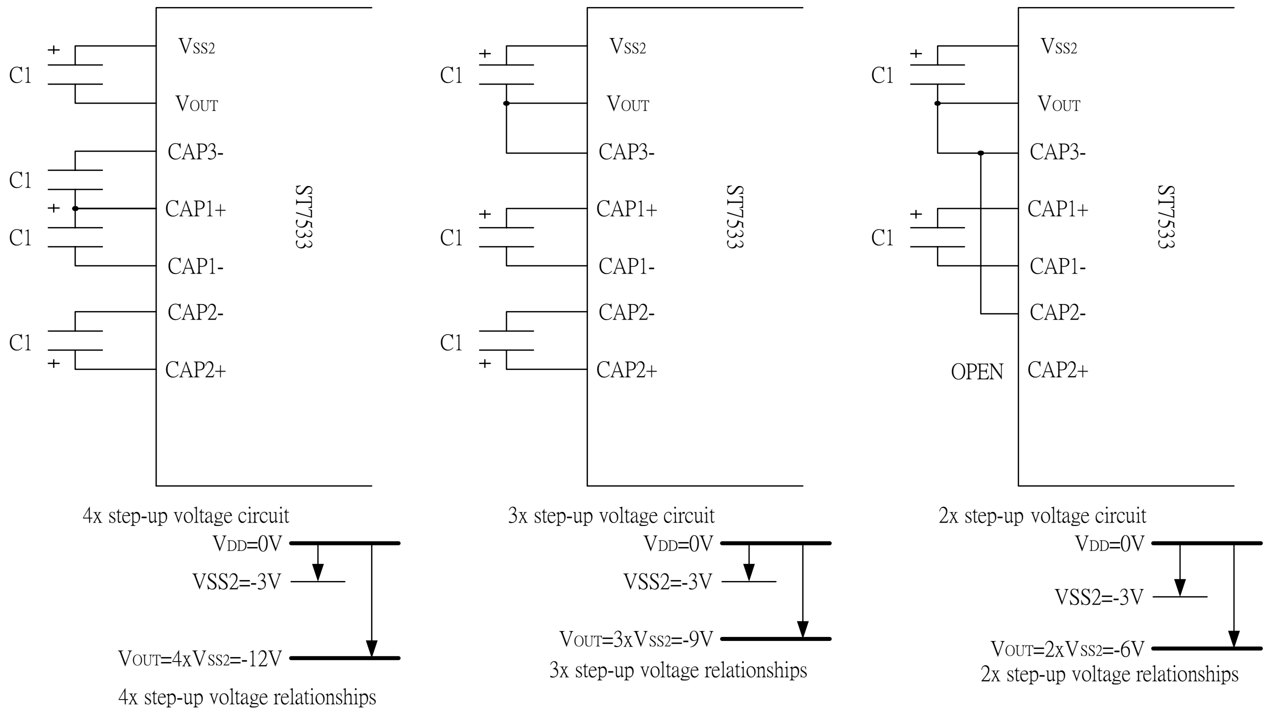


Figure 7

* The VSS2 voltage range must be set so that the VOUT terminal voltage does not exceed the absolute maximum rated value.

The Voltage Regulator Circuit

The step-up voltage generated at VOUT outputs the LCD driver voltage V5 through the voltage regulator circuit. Because the ST7533 chips have an internal high-accuracy fixed voltage power supply with a 64-level electronic volume function and internal resistors for the V5 voltage regulator, systems can be constructed without having to include high-accuracy voltage regulator circuit components. (VREG thermal gradients approximate -0.15%/°C)

The Voltage Regulator Circuit

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(A) When the V5 Voltage Regulator Internal Resistors Are Used

Through the use of the V5 voltage regulator internal resistors and the electronic volume function the liquid crystal power supply voltage V5 can be controlled by commands alone (without adding any external resistors), making it possible to adjust the liquid crystal display brightness. The V5 voltage can be calculated using equation A-1 over the range where | V5 | < | VOUT |.

$$V_5 = \left(1 + \frac{Rb}{Ra}\right) \bullet V_{EV}$$

$$= \left(1 + \frac{Rb}{Ra}\right) \bullet \left(1 - \frac{\alpha}{162}\right) \bullet V_{REG}$$

$$\left[\because\ V_{EV} = \left(1 - \frac{\alpha}{162}\right) \bullet V_{REG}\right]$$

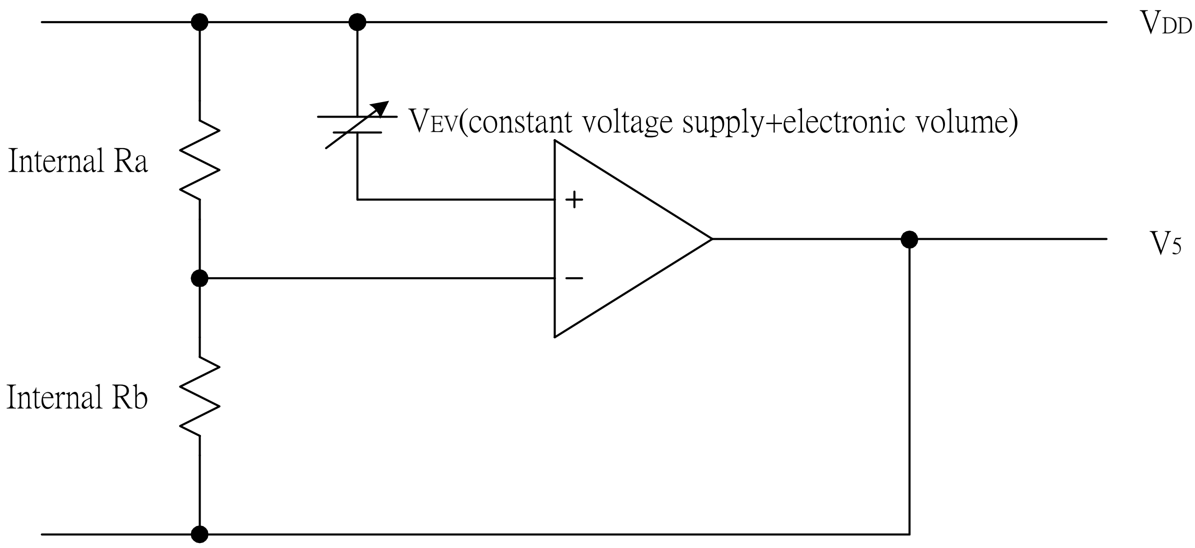


Figure 8

V_{REG} is the IC-internal fixed voltage supply, and its voltage at Ta = 25°C is as shown in Table 9.

Table 9

Part no.	Equipment Type	Thermal Gradient	VREG
ST7533	Internal Power Supply	–0.15 %/°C	–2.1V

α is set to 1 level of 64 possible levels by the electronic volume function depending on the data set in the 6-bit electronic volume register. Table 10 shows the value for α depending on the electronic volume register settings.
Rb/Ra is the V_5 voltage regulator internal resistor ratio, and can be set to 8 different levels through the V_5 voltage regulator internal resistor ratio set command. The (1 + Rb/Ra) ratio assumes the values shown in Table 11 depending on the 3-bit data settings in the V_5 voltage regulator internal resistor ratio register.

Table 10

D5	D4	D3	D2	D1	D0	α
0	0	0	0	0	0	63
0	0	0	0	0	1	62
0	0	0	0	1	0	61
		:				:
		:				:
1	1	1	1	0	1	2
1	1	1	1	1	0	1
1	1	1	1	1	1	0

V_5 voltage regulator internal resistance ratio register value and (1 + Rb/Ra) ratio (Reference value)

Table 11

Register			ST7533
D2	D1	D0	(1) –0.15 %/°C
0	0	0	3.0
0	0	1	3.5
0	1	0	4.0
0	1	1	4.5
1	0	0	5.0
1	0	1	5.5
1	1	0	6.0
1	1	1	6.5

Figures 9, 10 show V_5 voltage measured by values of the internal resistance ratio resistor for V_5 voltage adjustment and electric volume resister for each temperature grade model.

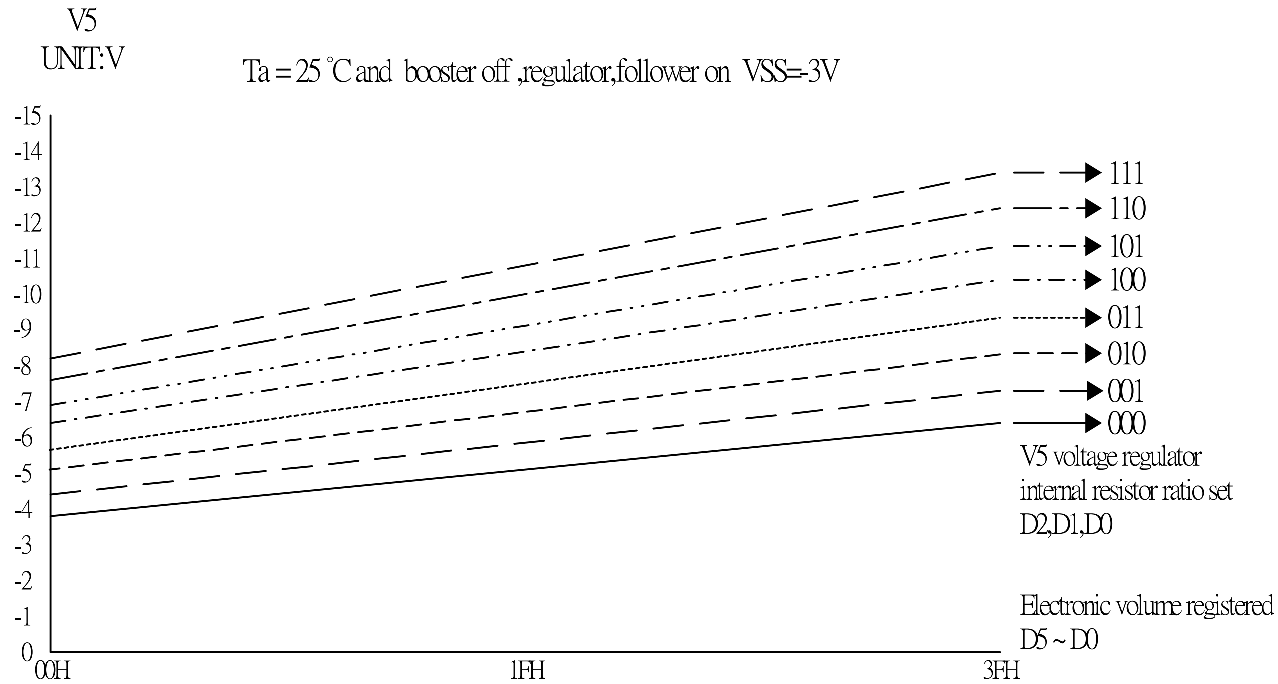


Figure 9 : (1) For ST7533 the Thermal Gradient = -0.15%/°C

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

Setup example: When selecting Ta = 25°C and V_5 = –7V for an ST7533 on which Temperature gradient = –0.15%/°C. Using Figure 9 and the equation A-1, the following setup is enabled.
At this time, the variable range and the notch width of the V_5 voltage is, as shown Table 13, as dependent on the electronic volume.

Table 12

Contents	Register					
	D5	**D4**	**D3**	**D2**	**D1**	**D0**
For V_5 voltage regulator	—	—	—	0	1	0
Electronic Volume	1	0	0	1	0	1

Table 13

V_5	Min	Typ	Max	Units
Variable Range	–8.4 (63 levels)	–7.0 (central value)	–5.1 (0 level)	[V]
Notch width		51		[mV]

(B) When an External Resistance is Used (The V5 Voltage Regulator Internal Resistors Are Not Used) (1)

The liquid crystal power supply voltage V_5 can also be set without using the V_5 voltage regulator internal resistors (IRS terminal = "L") by adding resistors Ra' and Rb' between V_{DD} and V_R, and between V_R and V_5, respectively. When this is done, the use of the electronic volume function makes it possible to adjust the brightness of the liquid crystal display by controlling the liquid crystal power supply voltage V_5 through commands.

In the range where $|V_5| < |V_{OUT}|$, the V_5 voltage can be calculated using equation B-1 based on the external resistances Ra' and Rb'.

$$V_5 = \left(1 + \frac{Rb'}{Ra'}\right) \bullet V_{EV}$$

$$= \left(1 + \frac{Rb'}{Ra'}\right) \bullet \left(1 - \frac{\alpha}{162}\right) \bullet V_{REG}$$

$$\left[\because\ V_{EV} = \left(1 - \frac{\alpha}{162}\right) \bullet V_{REG}\right]$$

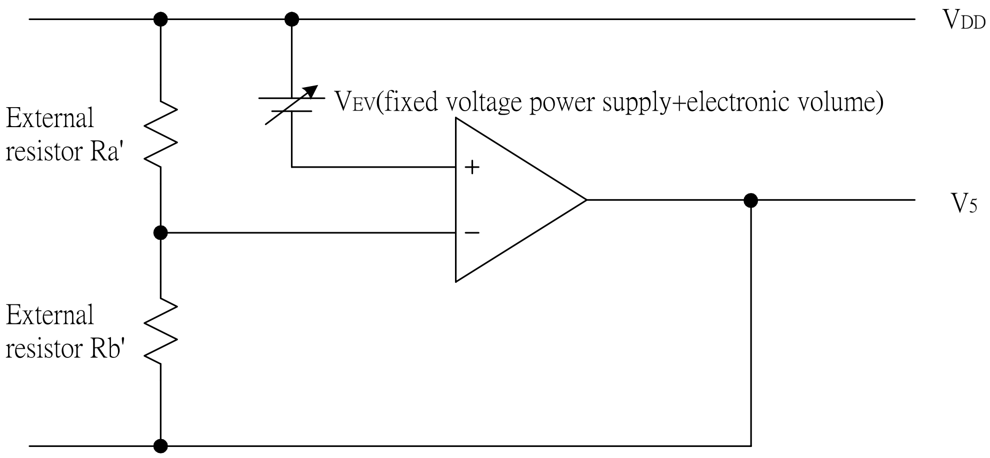


Figure 11

Setup example: When selecting Ta = 25°C and V_5 = –7 V for ST7533 the temperature gradient = –0.15%/°C.
When the central value of the electron volume register is (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0), then α = 31 and V_{REG} = –2.1V so, according to equation B-1,

$$V_5 = \left(1 + \frac{Rb'}{Ra'}\right) \bullet \left(1 - \frac{\alpha}{162}\right) \bullet V_{REG}$$

$$-7V = \left(1 + \frac{Rb'}{Ra'}\right) \bullet \left(1 - \frac{31}{162}\right) \bullet (-2.1)$$

Moreover, when the value of the current running through Ra' and Rb' is set to 5 uA,

$$Ra' + Rb' = 1.4M\Omega \qquad \text{(Equation B-3)}$$

Consequently, by equations B-2 and B-3,

$$\frac{Rb'}{Ra'} = 3.12$$

$$Ra' = 340k\Omega$$

$$Rb' = 1060k\Omega$$

At this time, the V_5 voltage variable range and notch width, based on the electron volume function, is as given in Table 14.

Table 14

V5	Min	Typ	Max	Units
Variable Range	–8.6 (63 levels)	–7.0 (central value)	–5.3 (0 level)	[V]
Notch width		52		[mV]

(C) When External Resistors are Used (The V5 Voltage Regulator Internal Resistors Are Not Used) (2)

When the external resistor described above are used, adding a variable resistor as well makes it possible to perform fine adjustments on Ra' and Rb', to set the liquid crystal drive voltage V_5. In this case, the use of the electronic volume function makes it possible to control the liquid crystal power supply voltage V_5 by commands to adjust the liquid crystal display brightness.

In the range where $|V_5| < |V_{OUT}|$ the V_5 voltage can be calculated by equation C-1 below based on the R_1 and R_2 (variable resistor) and R_3 settings, where R_2 can be subjected to fine adjustments (ΔR_2).

$$V_5 = \left(1 + \frac{R3+R2-\Delta R2}{R1+\Delta R2}\right) \bullet V_{EV}$$

$$= \left(1 + \frac{R3+R2-\Delta R2}{R1+\Delta R2}\right) \bullet \left(1 - \frac{\alpha}{162}\right) \bullet V_{REG}$$

$$\left[\because\ V_{EV} = \left(1 - \frac{\alpha}{162}\right) \bullet V_{REG}\right]$$

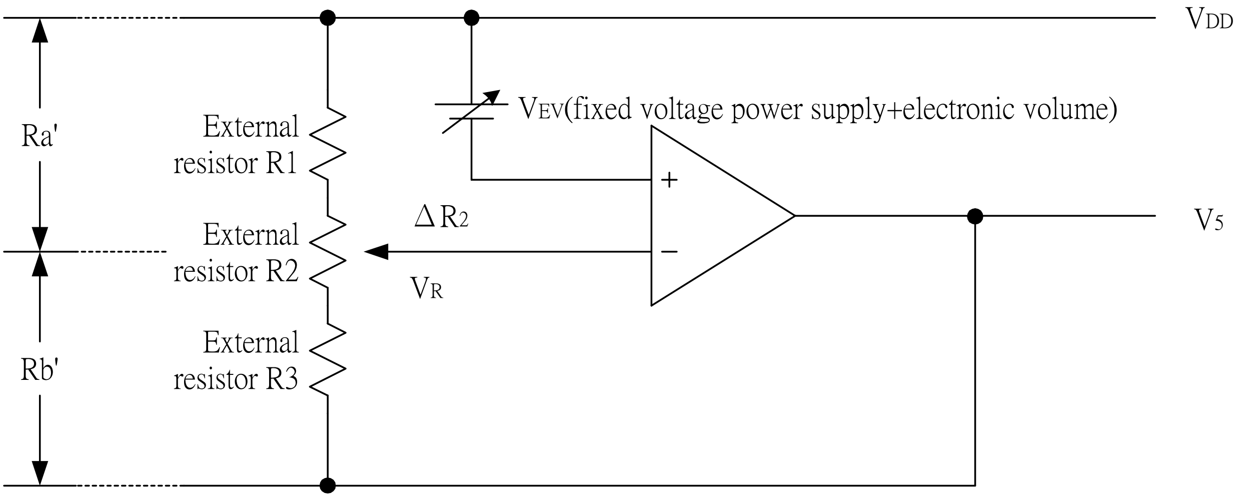


Figure 12

Setup example: When selecting Ta = 25°C and V_5 = –5 to –9 V (using R2) for an ST7533 the temperature gradient = –0.15%/°C.

When the central value for the electronic volume register is set at (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0), then α = 31 and V_{REG} = –2.1 V so, according to equation C-1, when $\Delta R_2 = 0\ \Omega$, in order to make V_5 = –9 V,

$$-9V = \left(1 + \frac{R3+R2}{R1}\right) \bullet \left(1 - \frac{31}{162}\right) \bullet (-2.1)$$

When $\Delta R_2 = R_2$, in order to make V = –5 V,

$$-5V = \left(1 + \frac{R3}{R1+R2}\right) \bullet \left(1 - \frac{31}{162}\right) \bullet (-2.1)$$

When the current flowing V_{DD} and V_5 is set to 5 uA,

$$R_1 + R_2 + R_3 = 1.4M\Omega \qquad \text{(Equation C-4)}$$

With this, according to equation C-2, C-3 and C-4,

$$R1 = 264k\Omega$$

$$R2 = 211k\Omega$$

$$R3 = 925k\Omega$$

The V_5 voltage variable range and notch width based on the electron volume function is as shown in Table 15.

Table 15

V5	Min	Typ	Max	Units
Variable Range	–8.7 (63 levels)	–7.0 (central value)	–5.3 (0 level)	[V]
Notch width		53		[mV]

* When the V_5 voltage regulator internal resistors or the electronic volume function is used, it is necessary to at least set the voltage regulator circuit and the voltage follower circuit to an operating mode using the power control set commands. Moreover, it is necessary to provide a voltage from V_{OUT} when the Booster circuit is OFF.
* The V_R terminal is enabled only when the V_5 voltage regulator internal resistors are not used (i.e. the IRS terminal = "L"). When the V_5 voltage regulator internal resistors are used (i.e. when the IRS terminal = "H"), then the V_R terminal is left open.
* Because the input impedance of the VR terminal is high, it is necessary to take into consideration short leads, shield cables, etc. to handle noise.

The LCD Voltage Generator Circuit

The V_5 voltage is produced by a resistive voltage divider within the IC, and can be produced at the V_1, V_2, V_3, and V_4 voltage levels required for liquid crystal driving. Moreover, when the voltage follower changes the impedance, it provides V_1, V_2, V_3 and V_4 to the liquid crystal drive circuit.

High Power Mode

The power supply circuit equipped in the ST7533 chips has very low power consumption (normal mode: HPM = "H"). However, for LCDs or panels with large loads, this low-power power supply may cause display quality to degrade. When this occurs, setting the HPM terminal to "L" (high power mode) can improve the quality of the display. We recommend that the display be checked on actual equipment to determine whether or not to use this mode. Moreover, if the improvement to the display is inadequate even after high power mode has been set, then it is necessary to add a liquid crystal drive power supply externally.

The Internal Power Supply Shutdown Command Sequence

The sequence shown in Figure 13 is recommended for shutting down the internal power supply, first placing the power supply in power saver mode and then turning the power supply OFF.

Sequence	Details (Command, status)	D7	D6	D5	D4	D3	D2	D1	D0	
		Command address								
Step1	Display OFF	1	0	1	0	1	1	1	0	Power saver
Step2	Display all points ON	1	0	1	0	0	1	0	1	commands
End	Internal power supply OFF									(compound)

Figure 13

The temperature grade of the Internal Power Supply for ST7533 (-0.15%/°C) :

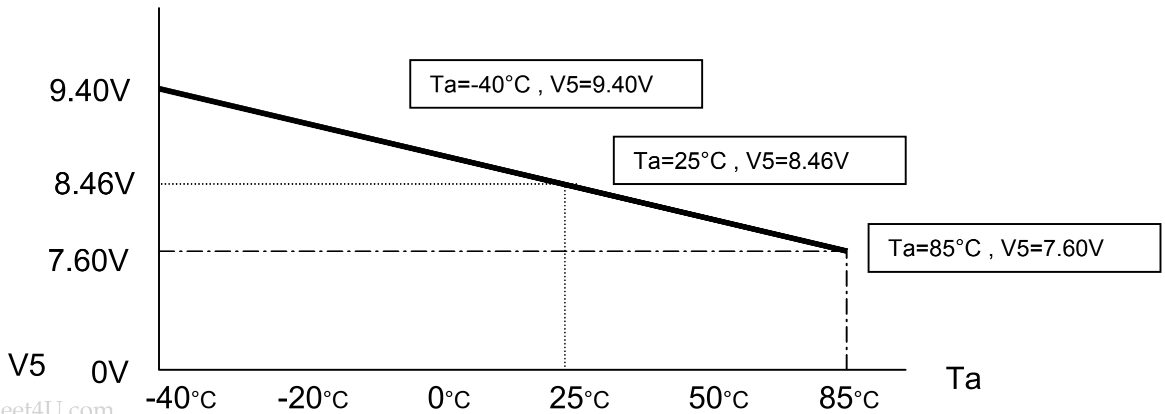


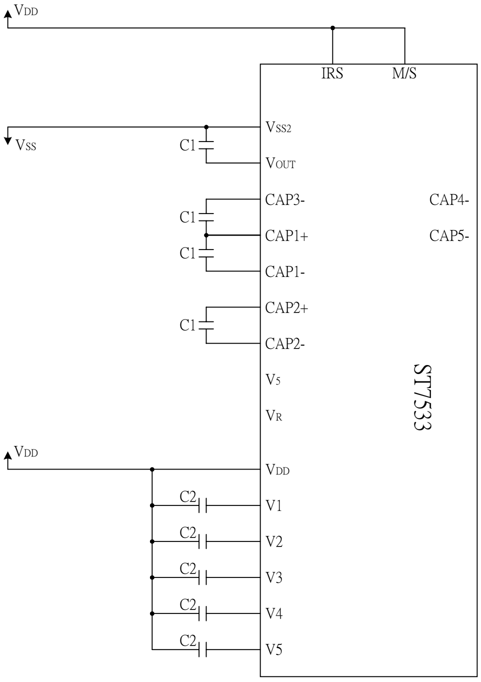
Figure 14

Reference Circuit Examples

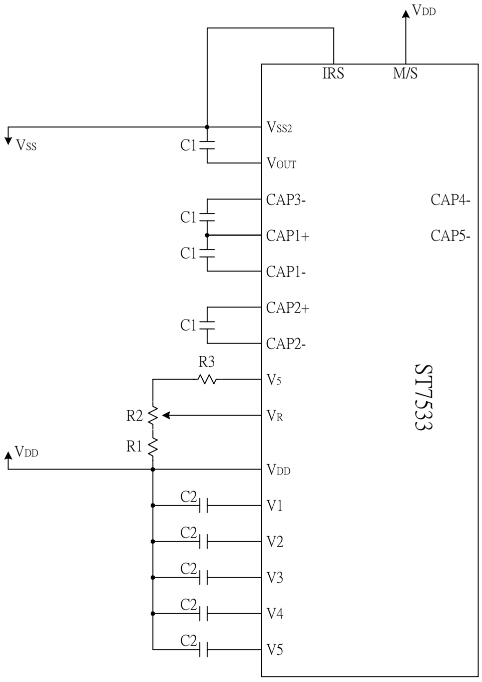
Figure 15 shows reference circuit examples.

1. When used all of the step-up circuit, voltage regulating circuit and V/F circuit

(1) When the voltage regulator internal resistor is used.
(Example where VSS2 = VSS, with 4x step-up)

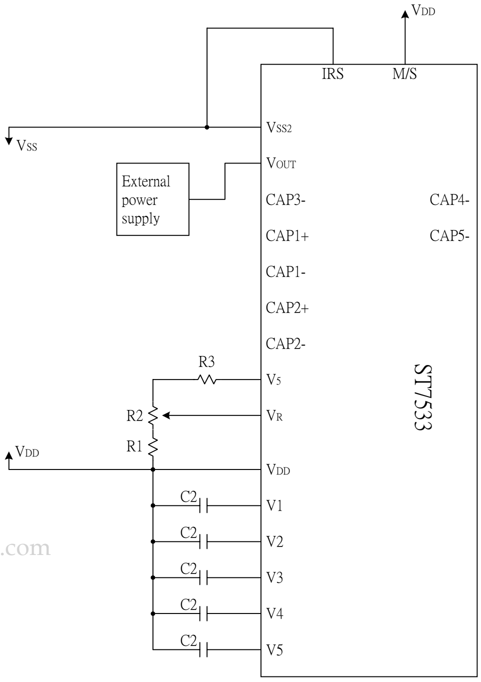


(2) When the voltage regulator internal resistor is not used.
(Example where VSS2 = VSS, with 4x step-up)

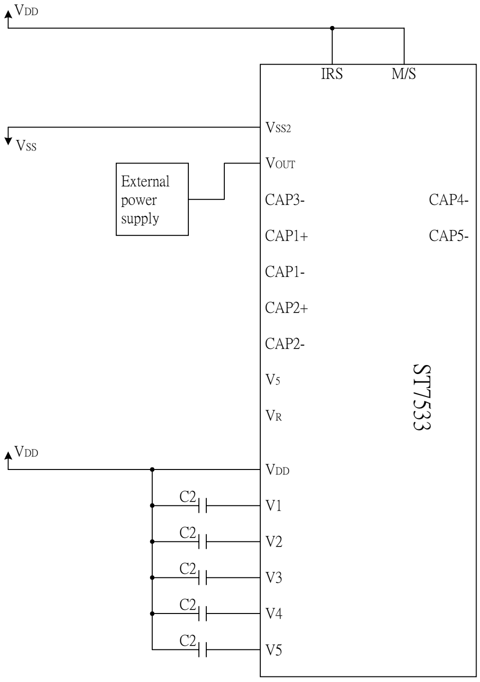


2. When the voltage regulator circuit and V/F circuit alone are used

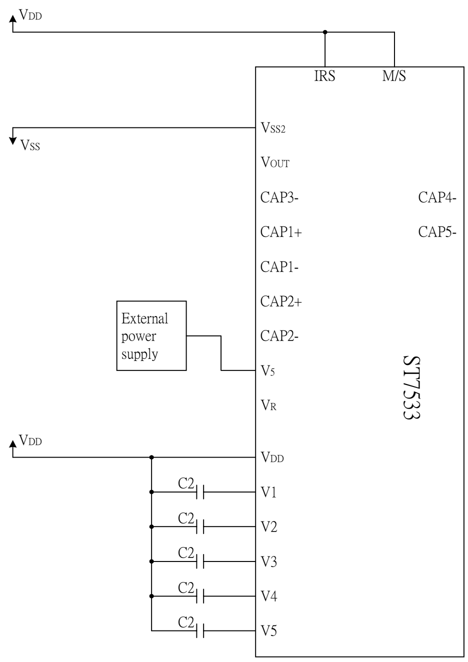
(1) When the V5 voltage regulator internal resistor is not used.



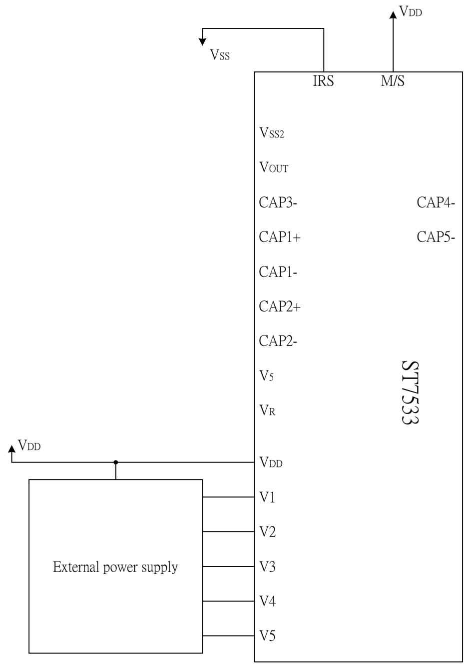
(2) When the V5 voltage regulator internal resistor is used.



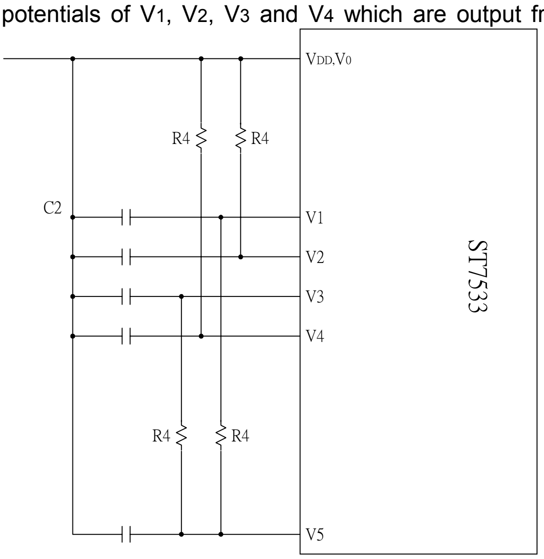
3. When the V/F circuit alone is used



4. When the built-in power is not used



5. When the built-in power circuit is used to drive a liquid crystal panel heavily loaded with AC or DC, it is recommended to connect an external resistor to stabilize potentials of V_1, V_2, V_3 and V_4 which are output from the built-in voltage follower.



Reference set value R4: 100KΩ ~ 1MΩ It is recommended to set an optimum resistance value R4 taking the liquid crystal display and the drive waveform.

Examples of shared reference settings When V_5 can vary between –8 and 12 V

Item	Set value	units
c1 c2	1.0 to 4.7 0.1 to 4.7	uF uF

C1 and C2 are determined by the size of the LCD being driven

Figure 15

* 1. Because the VR terminal input impedance is high, use short leads and shielded lines.

* 2. C1 and C2 are determined by the size of the LCD being driven. Select a value that will stabilize the liquid crystal drive voltage.

Example of the Process by which to Determine the Settings:

- Turn the voltage regulator circuit and voltage follower circuit ON and supply a voltage to VOUT from the outside.
- Determine C2 by displaying an LCD pattern with a heavy load (such as horizontal stripes) and selecting a C2 that stabilizes the liquid crystal drive voltages (V_1 to V_5). Note that all C2 capacitors must have the same capacitance value.
- Next turn all the power supplies ON and determine C1.

The Reset Circuit

When the /RES input comes to the "L" level, these LSIs return to the default state. Their default states are as follows:

1. Display OFF
2. Normal display
3. ADC select: Normal (ADC command D0 = "L")
4. Power control register: (D2, D1, D0) = (0, 0, 0)
5. Serial interface internal register data clear
6. LCD power supply bias rate:
   1/33 DUTY = 1/6 bias
   1/17 DUTY = 1/5 bias
7. All-indicator lamps-on OFF (All-indicator lamps ON/OFF command D0 = "L")
8. Power saving clear
9. V_5 voltage regulator internal resistors Ra and Rb separation
10. Output conditions of SEG and COM terminals SEG=VDD , COM=VDD
11. Read modify write OFF
12. Static indicator OFF Static indicator register : (D1, D2) = (0, 0)
13. Display start line set to first line
14. Column address set to Address 0
15. Page address set to Page 0
16. Common output status normal
17. V_5 voltage regulator internal resistor ratio set mode clear
18. Electronic volume register set mode clear Electronic volume register :
    (D5, D4, D3, D2, D1, D0) = (1, 0. 0, 0, 0,0)
19. Test mode clear

On the other hand, when the reset command is used, the above default settings from 11 to 19 are only executed. When the power is turned on, the IC internal state becomes unstable, and it is necessary to initialize it using the /RES terminal. After the initialization, each input terminal should be controlled normally.
Moreover, when the control signal from the MPU is in the high impedance, an over current may flow to the IC. After applying a current, it is necessary to take proper measures to prevent the input terminal from getting into the high impedance state.
If the internal liquid crystal power supply circuit is not used on ST7533,it is necessary that /RES is "H" when the external liquid crystal power supply is turned on. This IC has the function to discharge V_5 when /RES is "L," and the external power supply short-circuits to V_{DD} when /RES is "L." While /RES is "L," the oscillator and the display timing generator stop, and the CL, FR, FRS and /DOF terminals are fixed to "H." The terminals D0 to D7 are not affected. The V_{DD} level is output from the SEG and COM output terminals. This means that an internal resistor is connected between V_{DD} and V_5.
When the internal liquid crystal power supply circuit is not used on other models of ST7533 series, it is necessary that /RES is "L" when the external liquid crystal power supply is turned on.
While /RES is "L," the oscillator works but the display timing generator stops, and the CL, FR, FRS and /DOF terminals are fixed to "H." The terminals D0 to D7 are not affected.

COMMANDS

The ST7533 identify the data bus signals by a combination of A0, /RD (E), /WR(R/W) signals. Command interpretation and execution does not depend on the external clock, but rather is performed through internal timing only, and thus the processing is fast enough that normally a busy check is not required.
In the 8080 MPU interface, commands are launched by inputting a low pulse to the /RD terminal for reading, and inputting a low pulse to the WR terminal for writing. In the 6800 Series MPU interface, the interface is placed in a read mode when an “H” signal is input to the R/W terminal and placed in a write mode when a “L” signal is input to the R/W terminal and then the command is launched by inputting a high pulse to the E terminal. Consequently, the 6800 Series MPU interface is different than the 80x86 Series MPU interface in that in the explanation of commands and the display commands the status read and display data read /RD (E) becomes “1(H)”. In the explanations below the commands are explained using the 8080 Series MPU interface as the example.
When the serial interface is selected, the data is input in sequence starting with D7.
<Explanation of Commands>

Display ON/OFF

This command turns the display ON and OFF.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	1	1	1	1	Display ON
										0	Display OFF

When the display OFF command is executed when in the display all points ON mode, power saver mode is entered. See the section on the power saver for details.

Display Start Line Set

This command is used to specify the display start line address of the display data RAM shown in Figure 4. For further details see the explanation of this function in “The Line Address Circuit”.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Line address
0	1	0	0	1	0	0	0	0	0	0	0
						0	0	0	0	1	1
						0	0	0	1	0	2
							↓				↓
						1	1	1	1	0	30
						1	1	1	1	1	31

Page Address Set

This command specifies the page address corresponding to the low address when the MPU accesses the display data RAM (see Figure 4). Specifying the page address and column address enables to access a desired bit of the display data RAM. Changing the page address does not accompany a change in the status display.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Page address
0	1	0	1	0	1	1	0	0	0	0	0
								0	0	1	1
								0	1	0	2
								0	1	1	3
								1	0	0	4

Column Address Set

This command specifies the column address of the display data RAM shown in Figure 4. The column address is split into two sections (the higher 4 bits and the lower 4 bits) when it is set (fundamentally, set continuously). Each time the display data RAM is accessed, the column address automatically increments (+1), making it possible for the MPU to continuously read from/write to the display data. The column address increment is topped at 5FH. This does not change the page address continuously. See the function explanation in "The Column Address Circuit," for details.

	A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	A7	A6	A5	A4	A3	A2	A1	A0	Column address
High bits →	0	1	0	0	0	0	1	A7	A6	A5	A4	0	0	0	0	0	0	0	0	0
Low bits →							0	A3	A2	A1	A0	0	0	0	0	0	0	0	1	1
												0	0	0	0	0	0	1	0	2
																↓				↓
												0	1	0	1	1	1	1	0	94
												0	1	0	1	1	1	1	1	95

Status Read

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY	BUSY = 1: it indicates that either processing is occurring internally or a reset condition is in process. BUSY = 0: A new command can be accepted . if the cycle time can be satisfied, there is no need to check for BUSY conditions.
ADC	This shows the relationship between the column address and the segment driver. 0: Normal (column address n ↔ SEG n) 1: Reverse (column address 95-n ↔ SEG n) (The ADC command switches the polarity.)
ON/OFF	ON/OFF: indicates the display ON/OFF state. 0: Display ON 1: Display OFF (This display ON/OFF command switches the polarity.)
RESET	This indicates that the chip is in the process of initialization either because of a /RES signal or because of a reset command. 0: Operating state 1: Reset in progress

Display Data Write

This command writes 8-bit data to the specified display data RAM address. Since the column address is automatically incremented by "1" after the write, the MPU can write the display data.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7 D6 D5 D4 D3 D2 D1 D0
1	1	0	Write data

Display Data Read

This command reads 8-bit data from the specified display data RAM address. Since the column address is automatically incremented by “1” after the read, the CPU can continuously read multiple-word data. One dummy read is required immediately after the column address has been set. See the function explanation in “Display Data RAM” for the explanation of accessing the internal registers. When the serial interface is used, reading of the display data becomes unavailable.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7 D6 D5 D4 D3 D2 D1 D0
1	0	1	Read data

ADC Select (Segment Driver Direction Select)

This command can reverse the correspondence between the display RAM data column address and the segment driver output. Thus, sequence of the segment driver output pins may be reversed by the command. See the column address circuit (Figure 4) for the detail. Increment of the column address (by “1”) accompanying the reading or writing the display data is done according to the column address indicated in Figure 4.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	0	0	0 1	Normal Reverse

Display Normal/Reverse

This command can reverse the lit and unlit display without overwriting the contents of the display data RAM. When this is done the display data RAM contents are maintained.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	1	0 1	RAM Data “H” LCD ON voltage (normal) RAM Data “L” LCD ON voltage (reverse)

Display All Points ON/OFF

This command makes it possible to force all display points ON regardless of the content of the display data RAM. The contents of the display data RAM are maintained when this is done. This command takes priority over the display normal/reverse command.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	0	0 1	Normal display mode Display all points ON

When the display is in an OFF mode, executing the display all points ON command will place the display in power save mode. For details, see the Power Save section.

LCD Bias Set

This command selects the voltage bias ratio required for the liquid crystal display.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Select Status 1/33duty	 1/17duty
0	1	0	1	0	1	0	0	0	1	0	1/6 bias	1/6 bias
										1	1/5 bias	1/5 bias

Read/Modify/Write

This command is used paired with the “END” command. Once this command has been input, the display data read command does not change the column address, but only the display data write command increments (+1) the column address. This mode is maintained until the END command is input. When the END command is input, the column address returns to the address it was at when the read/modify/write command was entered. This function makes it possible to reduce the load on the MPU when there are repeating data changes in a specified display region, such as when there is a blanking cursor.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

* Even in read/modify/write mode, other commands aside from display data read/write commands can also be used.

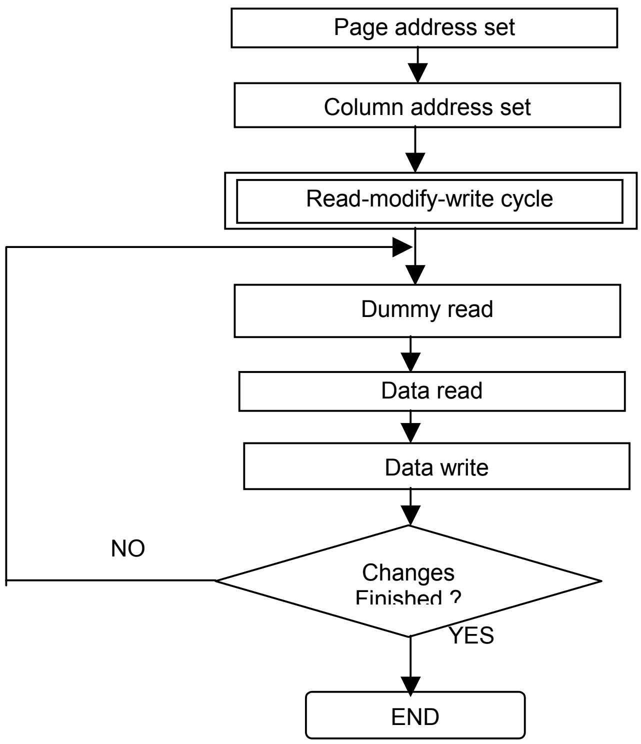


Figure 24 Command Sequence For read modify write

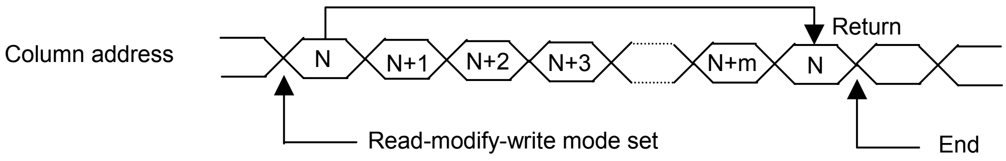


Figure 25

End

This command releases the read/modify/write mode, and returns the column address to the address it was at when the mode was entered.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

Reset

This command initializes the display start line, the column address, the page address, the common output mode, the V_5 voltage regulator internal resistor ratio, the electronic volume, and the static indicator are reset, and the read/modify/write mode and test mode are released. There is no impact on the display data RAM. See the function explanation in "Reset" for details.
The reset operation is performed after the reset command is entered.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The initialization when the power supply is applied must be done through applying a reset signal to the /RES terminal. The reset command must not be used instead.

Common Output Mode Select

This command can select the scan direction of the COM output terminal. For details, see the function explanation in "Common Output Mode Select Circuit."

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	Selected Mode	1/33duty	1/17duty
0	1	0	1	1	0	0	0	*	*	*	Normal	COM0→COM31	COM0→COM15
							1				Reverse	COM31→COM0	COM15→COM0

* Disabled bit

Power Controller Set

This command sets the power supply circuit functions. See the function explanation in “The Power Supply Circuit,” for details

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Selected Mode
0	1	0	0	0	1	0	1	0			Booster circuit: OFF
								1			Booster circuit: ON
									0		Voltage regulator circuit: OFF
									1		Voltage regulator circuit: ON
										0	Voltage follower circuit: OFF
										1	Voltage follower circuit: ON

V5 Voltage Regulator Internal Resistor Ratio Set

This command sets the V_5 voltage regulator internal resistor ratio. For details, see the function explanation is “The Voltage Regulator circuit " and table 11 .

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Rb/Ra Ratio
0	1	0	0	0	1	0	0	0	0	0	Small
								0	0	1	
								0	1	0	
									↓		↓
								1	1	1	
								1	1	1	Large

The Electronic Volume (Double Byte Command)

This command makes it possible to adjust the brightness of the liquid crystal display by controlling the LCD drive voltage V5 through the output from the voltage regulator circuits of the internal liquid crystal power supply. This command is a two byte command used as a pair with the electronic volume mode set command and the electronic volume register set command, and both commands must be issued one after the other.

The Electronic Volume Mode Set

When this command is input, the electronic volume register set command becomes enabled. Once the electronic volume mode has been set, no other command except for the electronic volume register command can be used. Once the electronic volume register set command has been used to set data into the register, then the electronic volume mode is released.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

Electronic Volume Register Set

By using this command to set six bits of data to the electronic volume register, the liquid crystal drive voltage V_5 assumes one of the 64 voltage levels.
When this command is input, the electronic volume mode is released after the electronic volume register has been set.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	$\lvert V_5 \rvert$
0	1	0	*	*	0	0	0	0	0	1	Small
			*	*	0	0	0	0	1	0	
			*	*	0	0	0	0	1	1	
							↓				↓
			*	*	1	1	1	1	1	0	
			*	*	1	1	1	1	1	1	Large

* Inactive bit (set “0”)
When the electronic volume function is not used, set this to (1, 0, 0, 0, 0, 0)

The Electronic Volume Register Set Sequence

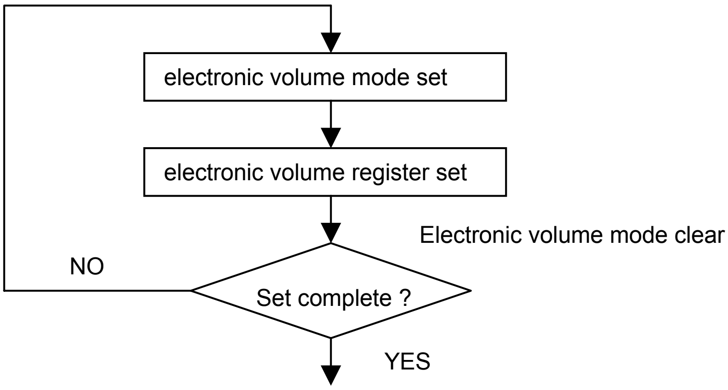


Figure 26

Static Indicator (Double Byte Command)

This command controls the static drive system indicator display. The static indicator display is controlled by this command only, and is independent of other display control commands.
This is used when one of the static indicator liquid crystal drive electrodes is connected to the FR terminal, and the other is connected to the FRS terminal. A different pattern is recommended for the static indicator electrodes than for the dynamic drive electrodes. If the pattern is too close, it can result in deterioration of the liquid crystal and of the electrodes.
The static indicator ON command is a double byte command paired with the static indicator register set command, and thus one must execute one after the other. (The static indicator OFF command is a single byte command.)

Static Indicator ON/OFF

When the static indicator ON command is entered, the static indicator register set command is enabled. Once the static indicator ON command has been entered, no other command aside from the static indicator register set command can be used. This mode is cleared when data is set in the register by the static indicator register set command.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Static Indicator
0	1	0	1	0	1	0	1	1	0	0	OFF
										1	ON

Static Indicator Register Set

This command sets two bits of data into the static indicator register, and is used to set the static indicator into a blinking mode.

A0	E / $\overline{RD}$	$R/\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Indicator Display State
0	1	0	*	*	*	*	*	*	0	0	OFF
									0	1	ON (blinking at approximately one second intervals)
									1	0	ON (blinking at approximately 0.5 second intervals)
									1	1	ON (constantly on)

* Disabled bit (set "0")

Static Indicator Register Set Sequence

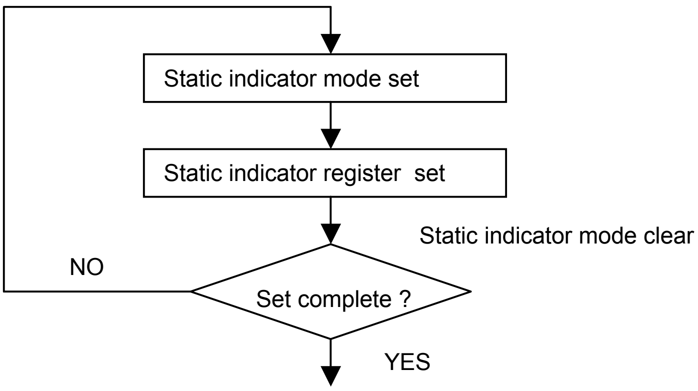


Figure 27

Power Save (Compound Command)

When the display all points ON is performed while the display is in the OFF mode, the power saver mode is entered, thus greatly reducing power consumption.
The power saver mode has two different modes: the sleep mode and the standby mode. When the static indicator is OFF, it is the sleep mode that is entered. When the static indicator is ON, it is the standby mode that is entered.
In the sleep mode and in the standby mode, the display data is saved as is the operating mode that was in effect before the power saver mode was initiated, and the MPU is still able to access the display data RAM.
Refer to figure 28 for power save off sequence.

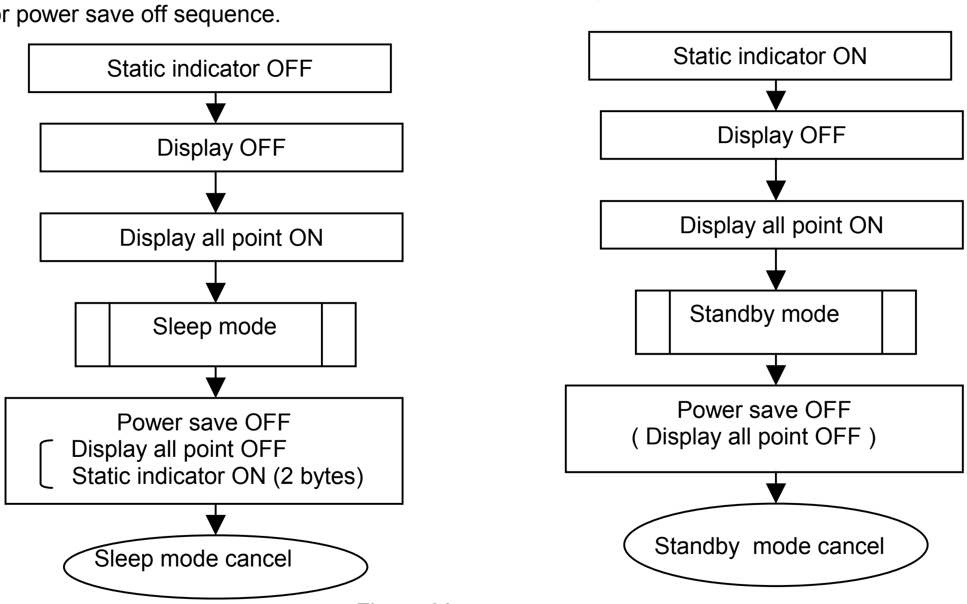


Figure 28

Sleep Mode

This stops all operations in the LCD display system, and as long as there are no accesses from the MPU, the consumption current is reduced to a value near the static current. The internal modes during sleep mode are as follows:
1. The oscillator circuit and the LCD power supply circuit are halted.
2. All liquid crystal drive circuits are halted, and the segment in common drive outputs output a V_{DD} level.

Standby Mode

The duty LCD display system operations are halted and only the static drive system for the indicator continues to operate, providing the minimum required consumption current for the static drive. The internal modes are in the following states during standby mode.
1 The LCD power supply circuits are halted. The oscillator circuit continues to operate.
2 The duty drive system liquid crystal drive circuits are halted and the segment and common driver outputs output a V_{DD} level. The static drive system does not operate.
When a reset command is performed while in standby mode, the system enters sleep mode.
* When an external power supply is used, it is recommended that the functions of the external power supply circuit be stopped when the power saver mode is started. For example, when the various levels of liquid crystal drive voltage are provided by external resistive voltage dividers, it is recommended that a circuit be added in order to cut the electrical current flowing through the resistive voltage divider circuit when the power saver mode is in effect. The ST7533 series chips have a liquid crystal display blanking control terminal /DOF. This terminal enters an "L" state when the power saver mode is launched. Using the output of /DOF, it is possible to stop the function of an external power supply circuit.

NOP

Non-OPeration Command

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

Test

This is a command for IC chip testing. Please do not use it. If the test command is used by accident, it can be cleared by applying a "L" signal to the /RES input by the reset command or by using an NOP.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	1	1	*	*

* Inactive bit

Note: The ST7533 maintain their operating modes until something happens to change them. Consequently, excessive external noise, etc., can change the internal modes of the ST7533 . Thus in the packaging and system design it is necessary to suppress the noise or take measure to prevent the noise from influencing the chip. Moreover, it is recommended that the operating modes be refreshed periodically to prevent the effects of unanticipated noise.

Table 16: Table of ST7533 Commands

(Note) *: disabled data

Command	Command Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF 0: OFF, 1: ON
(2) Display start line set	0	1	0	0	1	Display start address						Sets the display RAM display start line address
(3) Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address
(4) Column address set upper bit Column address set lower bit	0 0	1 1	0 0	0 0	0 0	0 0	1 0	Most significant column address Least significant column address				Sets the most significant 4 bits of the display RAM column address. Sets the least significant 4 bits of the display RAM column address.
(5) Status read	0	0	1	Status				0	0	0	0	Reads the status data
(6) Display data write	1	1	0	Write data								Writes to the display RAM
(7) Display data read	1	0	1	Read data								Reads from the display RAM
(8) ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
(9) Display normal/ reverse	0	1	0	1	0	1	0	0	1	1	0 1	Sets the LCD display normal/ reverse 0: normal, 1: reverse
(10) Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display all points 0: normal display 1: all points ON
(11) LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD drive voltage bias ratio 0: 1/6 bias, 1: 1/5 bias (ST7533)
(12) Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0
(13) End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(15) Common output mode select	0	1	0	1	1	0	0	0 1	*	*	*	Select COM output scan direction 0: normal direction 1: reverse direction
(16) Power control set	0	1	0	0	0	1	0	1	Operating mode			Select internal power supply operating mode
(17) V_5 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio(Rb/Ra) mode
(18) Electronic volume mode set Electronic volume register set	0	1	0	1 0	0 0	0 Electronic volume value	0	0	0	0	1	Set the V_5 output voltage electronic volume register
(19) Static indicator ON/OFF Static indicator register set	0	1	0	1 0	0 0	1 0	0 0	1 0	1 0	0 0	0 1 Mode	0: OFF, 1: ON Set the flashing mode
(20) Power saver												Display OFF and display all points ON compound command
(21) NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(22) Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Do not use this command

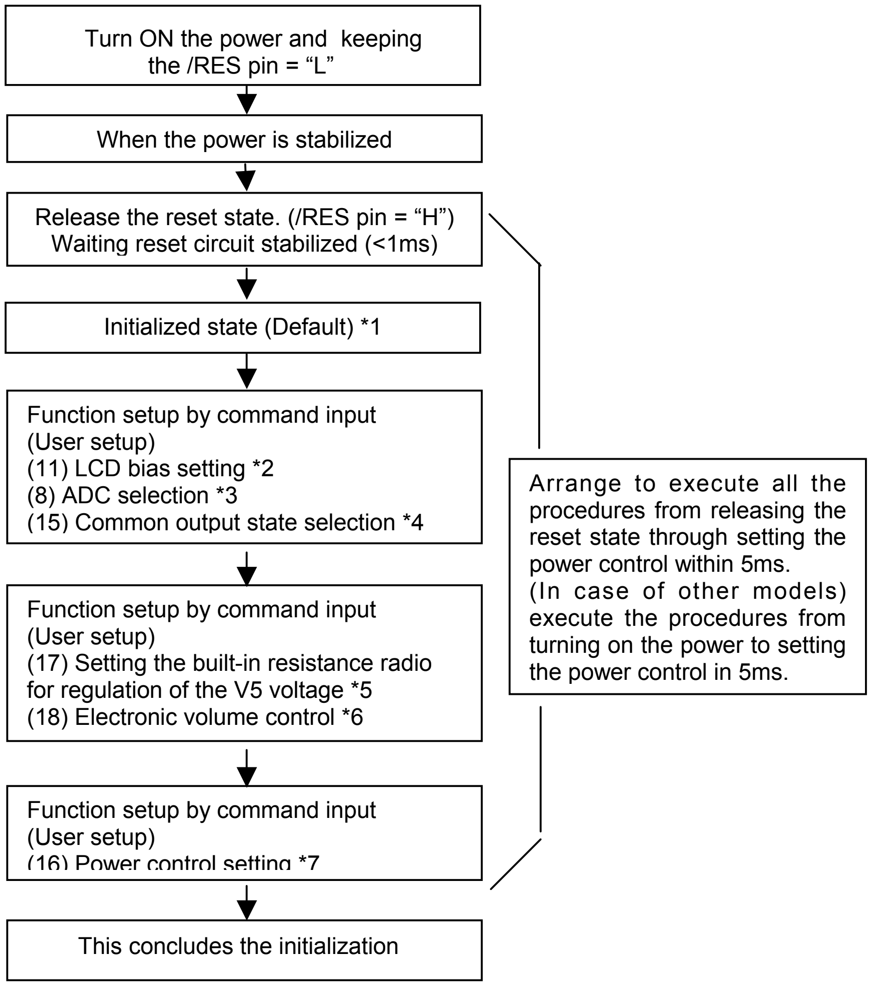
COMMAND DESCRIPTION

Instruction Setup: Reference

(1) Initialization

Note: With this IC, when the power is applied, LCD driving non-selective potentials V_2 and V_3 (SEG pin) and V_1 and V_4 (COM pin) are output through the LCD driving output pins SEG and COM. When electric charge is remaining in the smoothing capacitor connecting between the LCD driving voltage output pins (V_1 ~ V_5) and the V_{DD} pin, the picture on the display may become totally dark instantaneously when the power is turned on. To avoid occurrence of such a failure, we recommend the following flow when turning on the power.

1. When the built-in power is being used immediately after turning on the power:

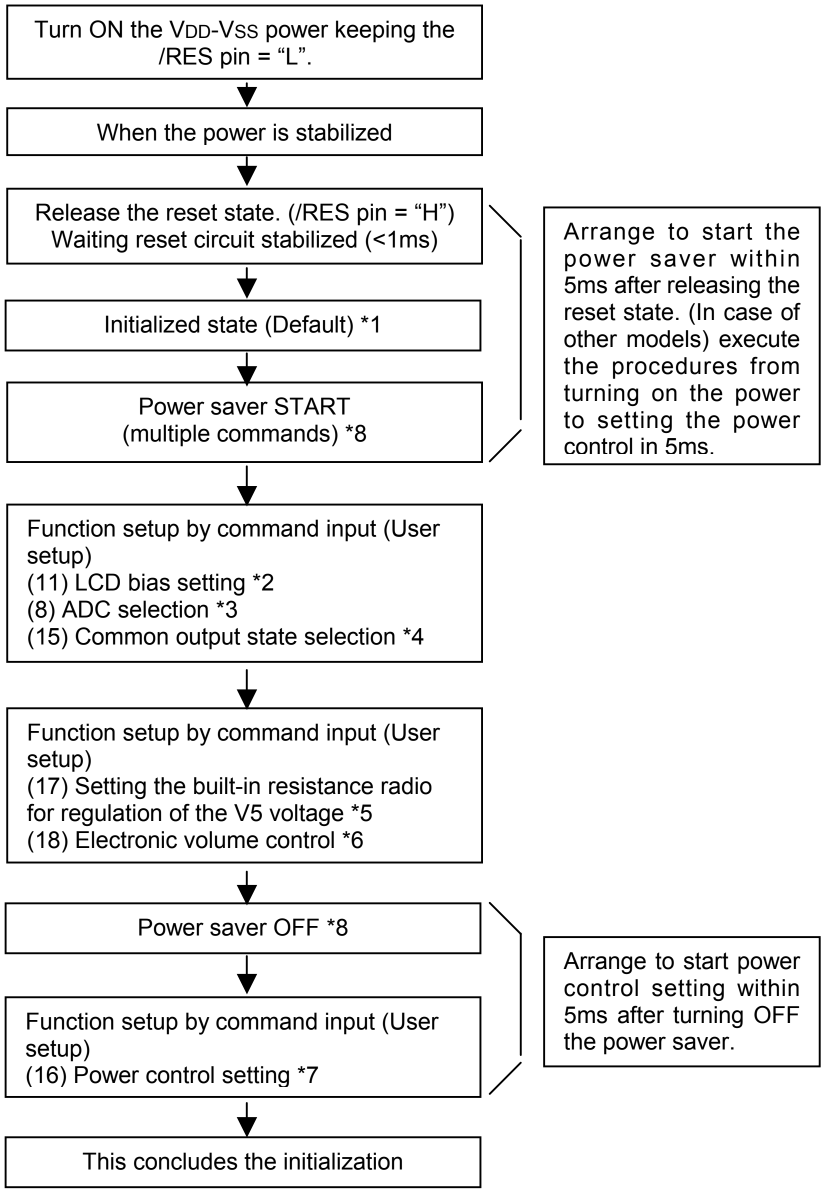


* The target time of 5ms will result to vary depending on the panel characteristics and the capacitance of the smoothing capacitor. Therefore, we suggest you to conduct an operation check using the actual equipment.

Notes: Refer to respective sections or paragraphs listed below.

*1: Description of functions; Resetting circuit
*2: Command description; LCD bias setting
*3: Command description; ADC selection
*4: Command description; Common output state selection
*5: Description of functions; Power circuit & Command description; Setting the built-in resistance radio for regulation of the V5 voltage
*6: Description of functions; Power circuit & Command description; Electronic volume control
*7: Description of functions; Power circuit & Command description; Power control setting

2. When the built-in power is not being used immediately after turning on the power:



* The target time of 5ms will result to vary depending on the panel characteristics and the capacitance of the smoothing capacitor. Therefore, we suggest you to conduct an operation check using the actual equipment.

Notes: Refer to respective sections or paragraphs listed below.
*1: Description of functions; Resetting circuit
*2: Command description; LCD bias setting
*3: Command description; ADC selection
*4: Command description; Common output state selection
*5: Description of functions; Power circuit & Command description; Setting the built-in resistance radio for regulation of the V5 voltage
*6: Description of functions; Power circuit & Command description; Electronic volume control
*7: Description of functions; Power circuit & Command description; Power control setting
*8: The power saver ON state can either be in sleep state or stand-by state.
Command description; Power saver START (multiple commands)

(2) Data Display

End of initialization

↓

Function setup by command input (User setup)
(2) Display start line set *9
(3) Page address set *10
(4) Column address set *11

↓

Function setup by command input (User setup)
(6) Display data write *12

↓

Function setup by command input (User setup)
(1) Display ON/OFF *13

↓

End of data display

Notes: Reference items
*9: Command Description; Display start line set
*10: Command Description; Page address set
*11: Command Description; Column address set
*12: Command Description; Display data write
*13: Command Description; Display ON/OFF
Avoid displaying all the data at the data display start (when the display is ON) in white.

(3) Power OFF *14

Optional status

↓

Function setup by command input (User setup)
(20) Power save *15

↓

Reset active ($\overline{RES}$ pin = "L")

↓

V_{DD} – V_{SS} power OFF

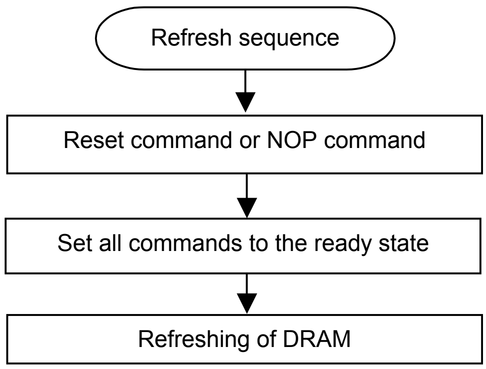
Set the time (t_L) from reset active to turning off the V_{DD} - V_{SS} power (V_{DD} - V_{SS} = 1.8V) longer than the time (t_H) when the potential of V_5 ~ V_1 becomes below the threshold voltage (approximately 1V) of the LCD panel. For t_H, refer to the <Reference Data> of this event. When t_H is too long, insert a resistor between V_5 and V_{DD} to reduce it.

Notes: Reference items
*14: The logic circuit of this IC's power supply V_{DD} - V_{SS} controls the driver of the LCD power supply V_{DD} - V_5. So, if the power supply V_{DD} - V_{SS} is cut off when the LCD power supply V_{DD} - V_5 has still any residual voltage, the driver (COM. SEG) may output any uncontrolled voltage. When turning off the power, observe the following basic procedures:
• After turning off the internal power supply, make sure that the potential V_5 ~ V_1 has become below the threshold voltage of the LCD panel, and then turn off this IC's power supply (V_{DD} - V_{SS}). 6. Description of Function, 6.7 Power Circuit

*15: After inputting the power save command, be sure to reset the function using the /RES terminal until the power supply V_{DD} - V_{SS} is turned off. 7. Command Description (20) Power Save
*16: After inputting the power save command, do not reset the function using the /RES terminal until the power supply V_{DD} - V_{SS} is turned off. 7. Command Description (20) Power Save

Refresh

It is recommended to turn on the refresh sequence regularly at a specified interval.



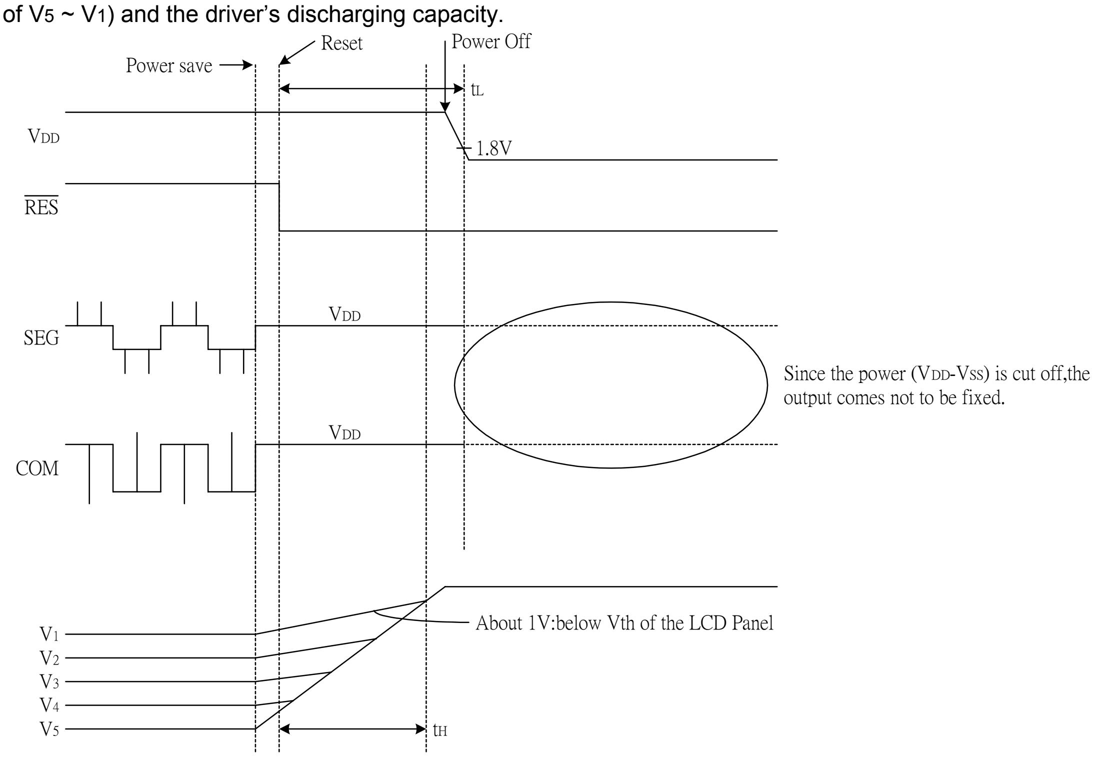
Precautions on Turning off the power

<Turning the power (V_{DD} - V_{SS}) off>

1) Power Save (The LCD powers (V_{DD} - V_5) are off.) → Reset input → Power (V_{DD} - V_{SS}) OFF

- Observe $t_L > t_H$.
- When $t_L < t_H$, an irregular display may occur.

Set t_L on the MPU according to the software. t_H is determined according to the external capacity C2 (smoothing capacity of V_5 ~ V_1) and the driver's discharging capacity.

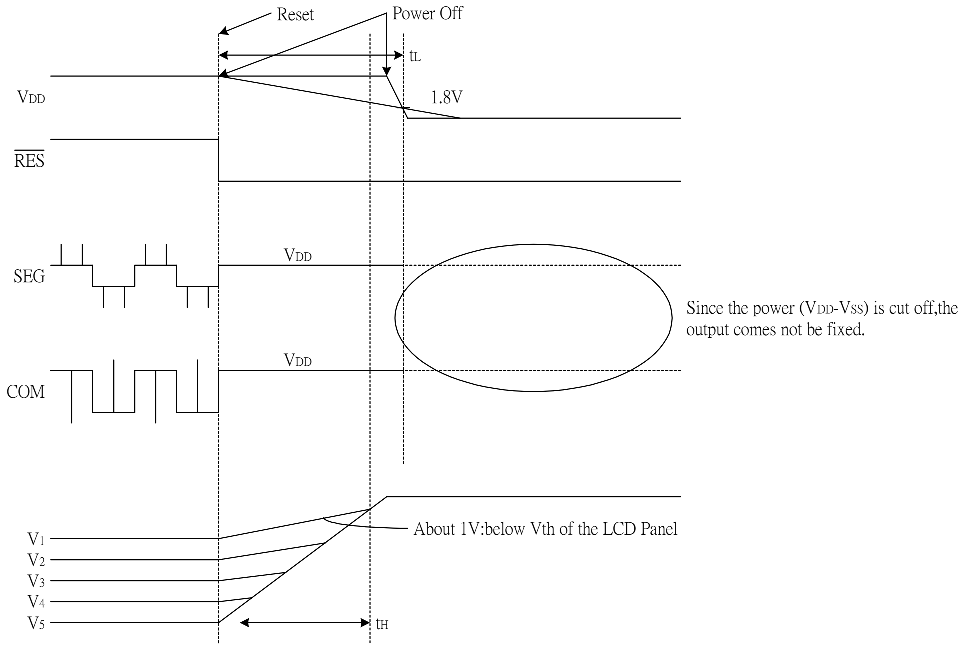


<Turning the power (V_{DD} - V_{SS}) off : When command control is not possible.>
2) Reset (The LCD powers (V_{DD} - V_{SS}) are off.) → Power (V_{DD} - V_{SS}) OFF

• Observe $t_L > t_H$.

• When $t_L < t_H$, an irregular display may occur.

For t_L, make the power (V_{DD} - V_{SS}) falling characteristics longer or consider any other method. t_H is determined according to the external capacity C2 (smoothing capacity of V_5 to V_1) and the driver's discharging capacity.



<Reference Data>

V_5 voltage falling (discharge) time (t_H) after the process of operation → power save → reset.

V_5 voltage falling (discharge) time (t_H) after the process of operation → reset.

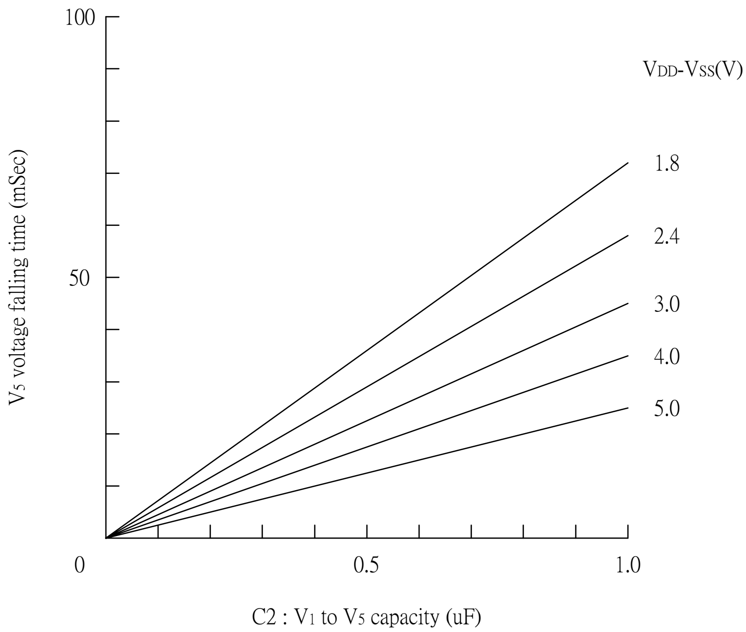


Figure 31

ABSOLUTE MAXIMUM RATINGS

Unless otherwise noted, V_{SS} = 0V

Table 17

Parameter		Symbol	Conditions	Unit
Power Supply Voltage		V_{DD}	–0.3 ~ +5.0	V
Power supply voltage (V_{DD} standard)		V_{SS2}	–4.0 ~ -1.8	V
Power supply voltage (V_{DD} standard)		V_5, V_{OUT}	–16.0 ~ +0.3	V
Power supply voltage (V_{DD} standard)		V_1, V_2, V_3, V_4	V_5 to +0.3	V
Input voltage		V_{IN}	–0.3 to V_{DD} + 0.3	V
Output voltage		V_O	–0.3 to V_{DD} + 0.3	V
Operating temperature		T_{OPR}	–40 to +85	°C
Storage temperature	Bare chip	T_{STR}	–55 to +125	°C

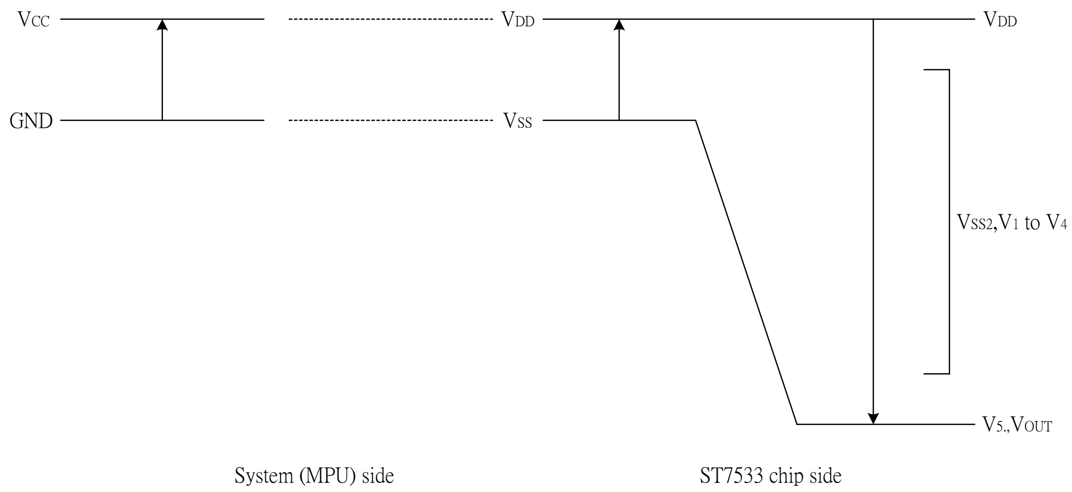


Figure 30

Notes and Cautions

1. The V_{SS2}, V_1 to V_5 and V_{OUT} are relative to the V_{DD} = 0V reference.
2. Insure that the voltage levels of V_1, V_2, V_3, and V_4 are always such that $V_{DD} \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_5$.
3. Permanent damage to the LSI may result if the LSI is used outside of the absolute maximum ratings. Moreover, it is recommended that in normal operation the chip be used at the electrical characteristic conditions, and use of the LSI outside of these conditions may not only result in malfunctions of the LSI, but may have a negative impact on the LSI reliability as well.

DC CHARACTERISTICS

Unless otherwise specified, V_{SS} = 0 V, V_{DD} = 3.0 V ± 10%, Ta = –40 to 85°C

Table 18

Item	Symbol	Condition	Rating			Units	Applicable Pin
			Min.	Typ.	Max.		
Operating Voltage (1)	Vss		-3.3	—	-1.8	V	Vss*1
Operating Voltage (2)	V_{SS2}	(Relative to V_{DD})	–3.3	—	–1.8	V	V_{SS2}
Operating Voltage (3)	V_{SS2}	(Relative to V_{DD})	–13.0	—	–4.0	V	V_5 *2
			0.4 x V_5	—	V_{DD}		V_1, V_2
			V_5	—	0.6 x V_5		V_3, V_4
High-level Input Voltage	V_{IHC}		0.8 x V_{DD}	—	V_{DD}	V	*3
Low-level Input Voltage	V_{ILC}		V_{SS}	—	0.2 x V_{DD}	V	*3
High-level Output Voltage	V_{OHC}	I_{OH} = –0.5 Ma	0.8 x V_{DD}	—	V_{DD}	V	*4
Low-level Output Voltage	V_{OLC}	I_{OL} = 0.5 mA	V_{SS}	—	0.2 x V_{DD}	V	*4
Input leakage current	I_{LI}	V_{IN} = V_{DD} or V_{SS}	–1.0	—	1.0	μA	*5
Output leakage current	I_{LO}	V_{IN} = V_{DD} or V_{SS}	–3.0	—	3.0	μA	*6
Liquid Crystal Driver ON Resistance	R_{ON}	Ta = 25°C (Relative To V_{DD}) V_5 = –13.0 V	—	2.0	3.5	KΩ	SEGn COMn *7
		V_5 = –8.0 V	—	3.2	5.4		
Static Consumption Current	I_{SSQ}	V_5 = –13.0 V(Relative To V_{DD})	—	0.01	2	μA	V_{SS}, V_{SS2}
Output Leakage Current	I_{5Q}		—	0.01	10	μA	V5
Input Terminal Capacitance	C_{IN}	Ta = 25°C , f = 1 MHz	—	5.0	8.0	pF	
Oscillator Frequency — Internal Oscillator	f_{OSC}	1/33 duty , Ta = 25°C	17	24	27	kHz	*8
Oscillator Frequency — External Input	f_{CL}		17	24	27	kHz	CL

Table 19

	Item	Symbol	Condition	Rating			Units	Applicable Pin
				Min.	Typ.	Max.		
Internal Power	Input voltage	V_{SS2}	(Relative To V_{DD})	–3.3	—	–1.8	V	V_{SS2}
	Supply Step-up output voltage Circuit	V_{OUT}	(Relative To V_{DD})	–13.0	—	—	V	V_{OUT}
	Voltage regulator Circuit Operating Voltage	V_{OUT}	(Relative To V_{DD})	–13.0	—	–6.0	V	V_{OUT}
	Voltage Follower Circuit Operating Voltage	V_5	(Relative To V_{DD})	–13.0	—	–4.0	V	V_5 * 9
	Base Voltage	V_{RS}	Ta = 25°C , (Relative To V_{DD}) –0.15%/°C	–2.07	–2.10	–2.13	V	*10

• Dynamic Consumption Current : During Display, with the Internal Power Supply OFF Current consumed by total ICs when an external power supply is used .

Table 20

Test pattern	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
Display Pattern OFF	I_{DD}	VDD = 3.0 V, V5 – VDD = –11.0 V	—	4	12	μA	*11
Display Pattern Checker	I_{DD}	VDD = 3.0 V, V5 – VDD = –11.0 V	—	7	21	μA	*11

• Dynamic Consumption Current : During Display, with the Internal Power Supply ON

Table 21

Test pattern	Symbol	Condition		Rating			Units	Notes
				Min.	Typ.	Max.		
Display Pattern OFF	I_{DD}	VDD = 3.0 V, Quad step-up voltage. V5 – VDD = –11.0 V	Normal Mode	—	70	110	μA	*12
			High-Power Mode	—	90	150		
Display Pattern Checker	I_{DD}	VDD = 3.0 V, Quad step-up voltage. V5 – VDD = –11.0 V	Normal Mode	—	95	130	μA	*12
			High-Power Mode	—	130	180		

• Consumption Current at Time of Power Saver Mode : VSS = -3.0 V ± 10%

Table 22

Item	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
Sleep mode	I_{DD}	Ta = 25°C	—	0.1	4	μA	
Standby Mode	I_{DD}	Ta = 25°C	—	5	10		

• The Relationship Between Oscillator Frequency f_{OSC}, Display Clock Frequency f_{CL} and the Liquid Crystal Frame Rate Frequency f_{FR}

Table 23

Item		f_{CL}	f_{FR}
1/33 DUTY	Used internal oscillator circuit	fOSC / 8	fOSC / (8*33)
	Used **external** display clock	External input (f_{CL})	fCL / 264
1/17 DUTY	Used internal oscillator circuit	fOSC / 16	fOSC / (16*17)
	Used **external** display clock	External input (f_{CL})	fCL / 272

(f_{FR} is the liquid crystal alternating current period, and not the FR signal period.)

References for items market with *

*1 While a broad range of operating voltages is guaranteed, performance cannot be guaranteed if there are sudden fluctuations to the voltage while the MPU is being accessed.

*2 The operating voltage range for the V_{DD} system and the V_5 system is. This applies when the external power supply is being used.

*3 The A0, D0 to D5, D6 (SCL), D7 (SI), RD (E), /WR (R/W), /CS1, CS2, CLS, CL, FR, M/S and C86, P/S, /DOF, /RES, IRS, and /HPM terminals.

*4 The D0 to D7, FR, FRS, /DOF, and CL terminals.

*5 The A0, /RD (E), /WR (R/W), /CS1, CS2, CLS, M/S, C86, P/S, /RES, IRS, and /HPM terminals.

*6 Applies when the D0 to D5, D6 (SCL), D7 (SI), CL, FR, and /DOF terminals are in a high impedance state.

*7 These are the resistance values for when a 0.1 V voltage is applied between the output terminal SEGn or COMn and the various power supply terminals (V_1, V_2, V_3, and V_4). These are specified for the operating voltage (3) range. R_{ON} = 0.1 V / △I (Where △I is the current that flows when 0.1 V is applied while the power supply is ON.)

*8 See Table 23 for the relationship between the oscillator frequency and the frame rate frequency.

*9 The V_5 voltage regulator circuit regulates within the operating voltage range of the voltage follower.

*10 This is the internal voltage reference supply for the V_5 voltage regulator circuit. In the ST7533 , the temperature range approximately –0.15%/°C.

*11, 12 It indicates the current consumed on ICs alone when the internal oscillator circuit and display are turned on. The ST7533 is 1/5 biased. Does not include the current due to the LCD panel capacity and wiring capacity. Applicable only when there is no access from the MPU.

*12 It is the value on a ST7533 having the V_{REG} temperature gradient is –0.15%/°C when the V_5 voltage regulator internal resistor is used.

TIMING CHARACTERISTICS

System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)

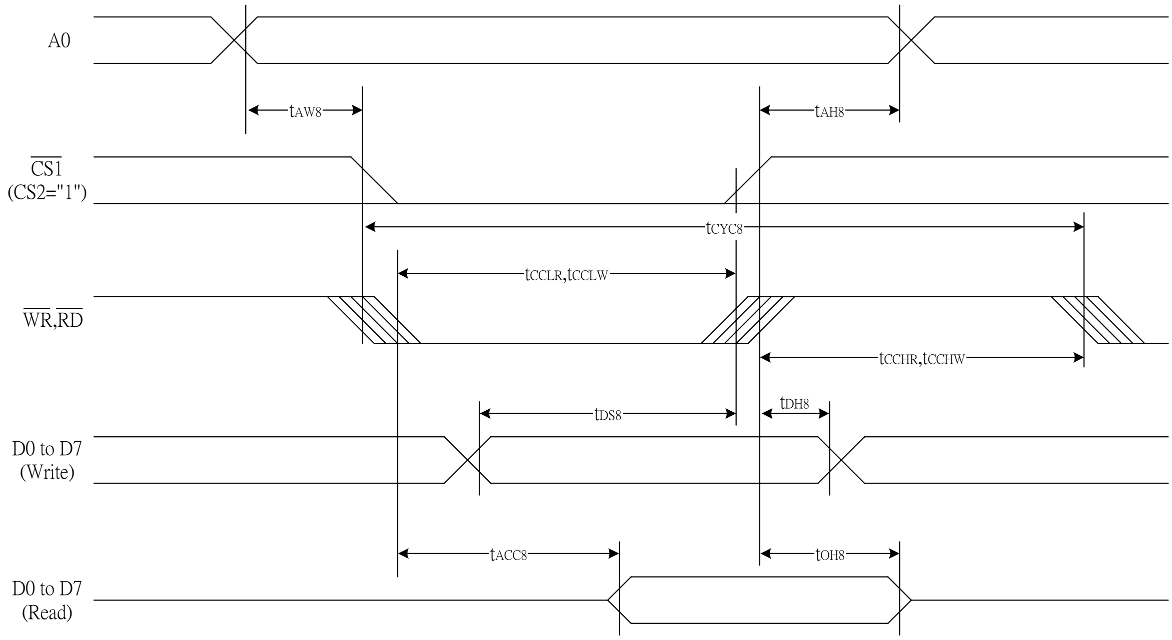


Figure 37

Table 24

(V_{DD} = 3.3V , Ta =25°C)

Item	Signal	Symbol	Condition	Rating Min.	Rating Max.	Units
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System cycle time		t_{CYC8}		240	—	
Enable L pulse width (WRITE)	WR	t_{CCLW}		80	—	
Enable H pulse width (WRITE)		t_{CCHW}		80	—	
Enable L pulse width (READ)	RD	t_{CCLR}		140	—	
Enable H pulse width (READ)		t_{CCHR}		80		
WRITE Data setup time	D0 to D7	t_{DS8}		40	—	
WRITE Data hold time		t_{DH8}		10	—	
READ access time		t_{ACC8}	C_L = 100 pF	—	70	
READ Output disable time		t_{OH8}	C_L = 100 pF	5	50	

Table 25

(V_{DD} = 2.7 V , Ta = 25°C)

Item	Signal	Symbol	Condition	Rating Min.	Rating Max.	Units
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System cycle time		t_{CYC8}		400	—	
Enable L pulse width (WRITE)	WR	t_{CCLW}		220	—	
Enable H pulse width (WRITE)		t_{CCHW}		180	—	
Enable L pulse width (READ)	RD	t_{CCLR}		220	—	
Enable H pulse width (READ)		t_{CCHR}		180	—	
WRITE Data setup time	D0 to D7	t_{DS8}		40	—	
WRITE Data hold time		t_{DH8}		15	—	
READ access time		t_{ACC8}	C_L = 100 pF	—	140	
READ Output disable time		t_{OH8}	C_L = 100 pF	10	100	

Table 26

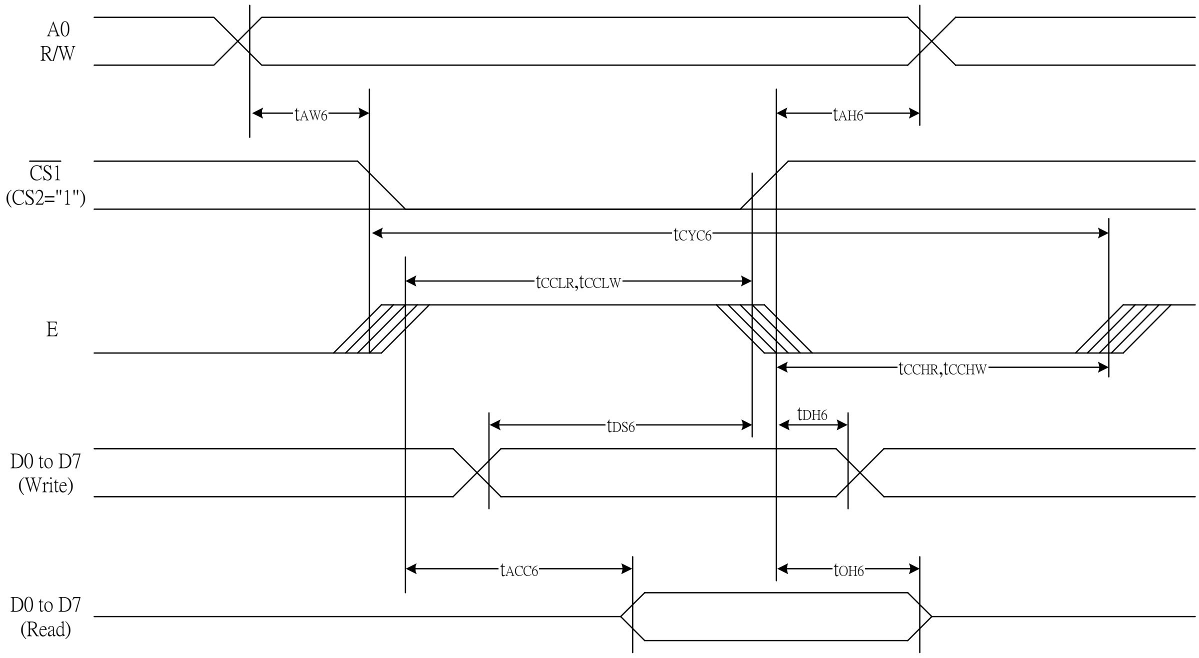
(V_{DD} = 1.8V , Ta = 25°C)

Item	Signal	Symbol	Condition	Rating Min.	Rating Max.	Units
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System cycle time		t_{CYC8}		640	—	
Enable L pulse width (WRITE)	WR	t_{CCLW}		360	—	
Enable H pulse width (WRITE)		t_{CCHW}		280	—	
Enable L pulse width (READ)	RD	t_{CCLR}		360	—	
Enable H pulse width (READ)		t_{CCHR}		280		
WRITE Data setup time	D0 to D7	t_{DS8}		80	—	
WRITE Data hold time		t_{DH8}		30	—	
READ access time		t_{ACC8}	C_L = 100 pF	—	240	
READ Output disable time		t_{OH8}	C_L = 100 pF	10	200	

*1 The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) ≦ ($t_{CYC8} – t_{CCLW} – t_{CCHW}$) for ($t_r + t_f$) ≦ ($t_{CYC8} – t_{CCLR} – t_{CCHR}$) are specified.

*2 All timing is specified using 20% and 80% of V_{DD} as the reference.

*3 t_{CCLW} and t_{CCLR} are specified as the overlap between $\overline{CS1}$ being “L” (CS2 = “H”) and $\overline{WR}$ and $\overline{RD}$ being at the “L” level.



System Bus Read/Write Characteristics 2 (For the 6800 Series MPU)

Figure 38

Table 27

(V_{DD} = 3.3 V , Ta = 25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH6}		0	—	ns
Address setup time		t_{AW6}		0	—	
System cycle time		t_{CYC6}		240	—	
Enable L pulse width (WRITE)	WR	t_{EWLW}		80	—	
Enable H pulse width (WRITE)		t_{EWHW}		80	—	
Enable L pulse width (READ)	RD	t_{EWLR}		80	—	
Enable H pulse width (READ)		t_{EWHR}		140		
WRITE Data setup time	D0 to D7	t_{DS6}		40	—	
WRITE Data hold time		t_{DH6}		10	—	
READ access time		t_{ACC6}	C_L = 100 pF	—	70	
READ Output disable time		t_{OH6}	C_L = 100 pF	5	50	

Table 28

(V_{DD} = 2.7V , Ta =25°C)

Item	Signal	Symbol	Condition	Rating Min.	Rating Max.	Units
Address hold time	A0	t_{AH6}		0	—	ns
Address setup time		t_{AW6}		0	—	
System cycle time		t_{CYC6}		400	—	
Enable L pulse width (WRITE)	WR	t_{EWLW}		220	—	
Enable H pulse width (WRITE)		t_{EWHW}		180	—	
Enable L pulse width (READ)	RD	t_{EWLR}		220	—	
Enable H pulse width (READ)		t_{EWHR}		180	—	
WRITE Data setup time	D0 to D7	t_{DS6}		40	—	
WRITE Data hold time		t_{DH6}		15	—	
READ access time		t_{ACC6}	C_L = 100 pF	—	140	
READ Output disable time		t_{OH6}	C_L = 100 pF	10	100	

Table 29

(V_{DD} =1.8V , Ta =25°C)

Item	Signal	Symbol	Condition	Rating Min.	Rating Max.	Units
Address hold time	A0	t_{AH6}		0	—	ns
Address setup time		t_{AW6}		0	—	
System cycle time		t_{CYC6}		640	—	
Enable L pulse width (WRITE)	WR	t_{EWLW}		360	—	
Enable H pulse width (WRITE)		t_{EWHW}		280	—	
Enable L pulse width (READ)	RD	t_{EWLR}		360	—	
Enable H pulse width (READ)		t_{EWHR}		280	—	
WRITE Data setup time	D0 to D7	t_{DS6}		80	—	
WRITE Data hold time		t_{DH6}		30	—	
READ access time		t_{ACC6}	C_L = 100 pF	—	240	
READ Output disable time		t_{OH6}	C_L = 100 pF	10	200	

*1 The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) ≦ ($t_{CYC6} - t_{EWLW} - t_{EWHW}$) for ($t_r + t_f$) ≦ ($t_{CYC6} - t_{EWLR} - t_{EWHR}$) are specified.
*2 All timing is specified using 20% and 80% of V_{DD} as the reference.
*3 t_{EWLW} and t_{EWLR} are specified as the overlap between $\overline{CS1}$ being “L” (CS2 = “H”) and E.

The Serial Interface

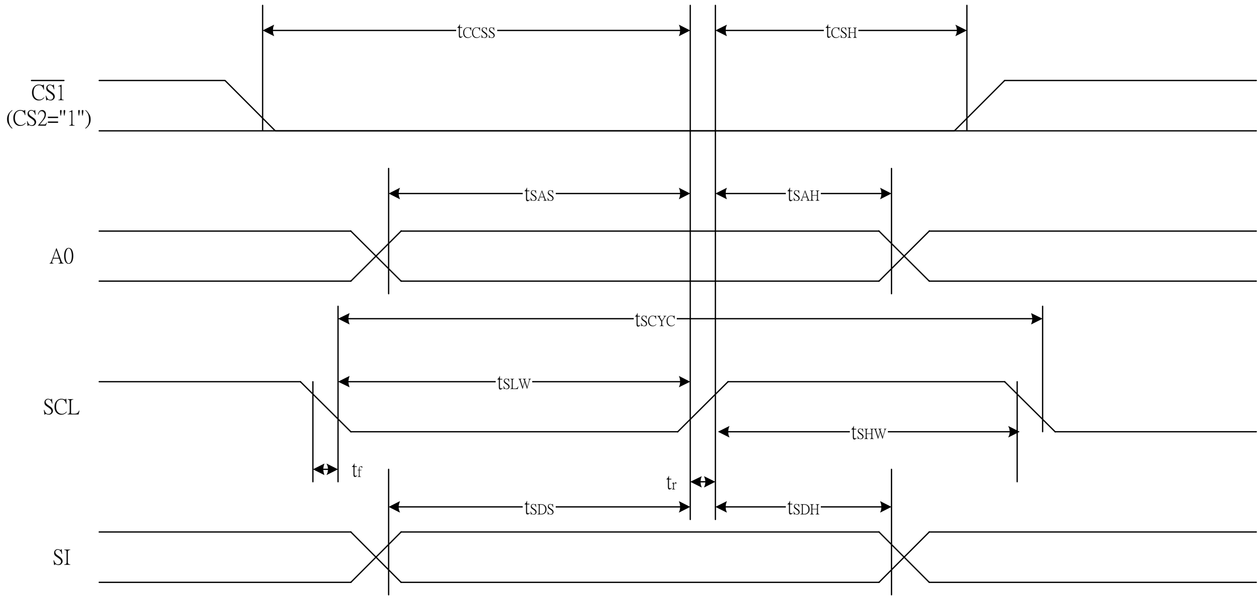


Figure 39

Table 30

(VDD = 3.3V, Ta =25°C)

Item	Signal	Symbol	Condition	Rating Min.	Rating Max.	Units
Serial Clock Period	SCL	tSCYC		50	—	ns
SCL “H” pulse width		tSHW		25	—	
SCL “L” pulse width		tSLW		25	—	
Address setup time	A0	tSAS		20	—	
Address hold time		tSAH		10	—	
Data setup time	SI	tSDS		20	—	
Data hold time		tSDH		10	—	
CS-SCL time	CS	tCSS		20	—	
CS-SCL time		tCSH		40	—	

Table 31

(VDD =2.7V , Ta =25°C)

Item	Signal	Symbol	Condition	Rating Min.	Rating Max.	Units
Serial Clock Period	SCL	tSCYC		100	—	ns
SCL “H” pulse width		tSHW		50	—	
SCL “L” pulse width		tSLW		50	—	
Address setup time	A0	tSAS		30	—	
Address hold time		tSAH		20	—	
Data setup time	SI	tSDS		30	—	
Data hold time		tSDH		20	—	
CS-SCL time	CS	tCSS		30	—	
CS-SCL time		tCSH		60	—	

Table 32

(V_{DD} = 1.8V , Ta = 25°C)

Item	Signal	Symbol	Condition	Rating Min.	Rating Max.	Units
Serial Clock Period	SCL	T_{SCYC}		200	—	ns
SCL "H" pulse width		T_{SHW}		80	—	
SCL "L" pulse width		T_{SLW}		80	—	
Address setup time	A0	T_{SAS}		60	—	
Address hold time		T_{SAH}		30	—	
Data setup time	SI	T_{SDS}		60	—	
Data hold time		T_{SDH}		30	—	
CS-SCL time	CS	T_{CSS}		40	—	
CS-SCL time		t_{CSH}		100	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
*2 All timing is specified using 20% and 80% of V_{DD} as the standard.

Reset Timing

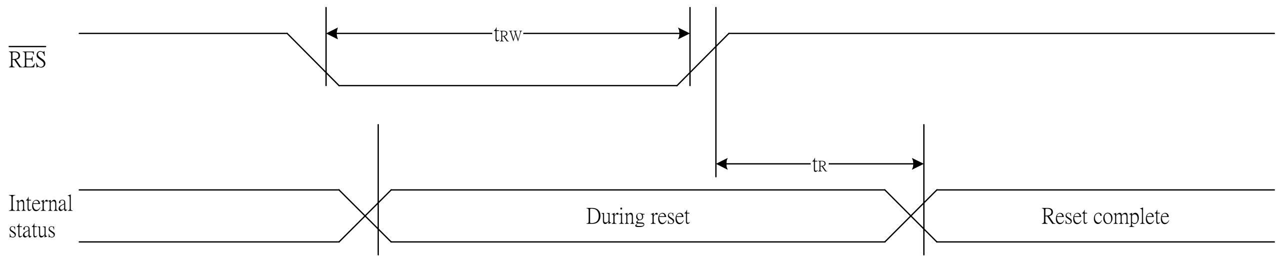


Figure 41

Table 36

(VDD = 3.3V , Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	1.0	us
Reset "L" pulse width	RES	tRW		1.0	—	—	us

Table 37

(VDD = 2.7V , Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	2.0	us
Reset "L" pulse width	RES	tRW		2.0		—	us

Table 38

(VDD = 1.8V , Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	3.0	us
Reset "L" pulse width	RES	tRW		3.0	—	—	us

*1 All timing is specified with 20% and 80% of VDD as the standard.

THE MPU INTERFACE (REFERENCE EXAMPLES)

The ST7533 Series can be connected to either 80X86 Series MPUs or to 68000 Series MPUs. Moreover, using the serial interface it is possible to operate the ST7533 series chips with fewer signal lines.
The display area can be enlarged by using multiple ST7533 Series chips. When this is done, the chip select signal can be used to select the individual ICs to access.

(1) 8080 Series MPUs

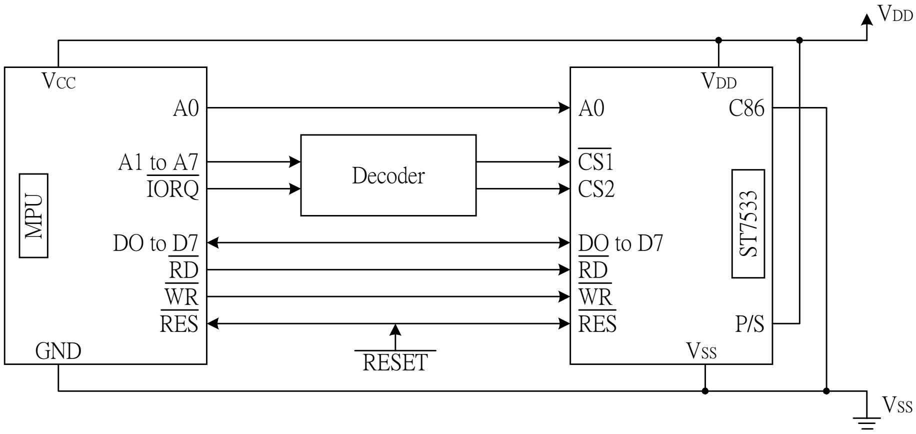


Figure 42-1

(2) 6800 Series MPUs

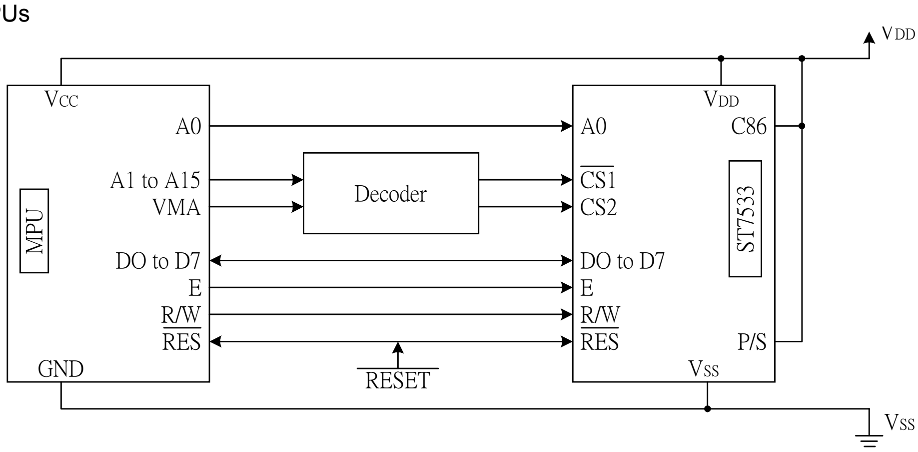


Figure 42-2

(3) Using the Serial Interface

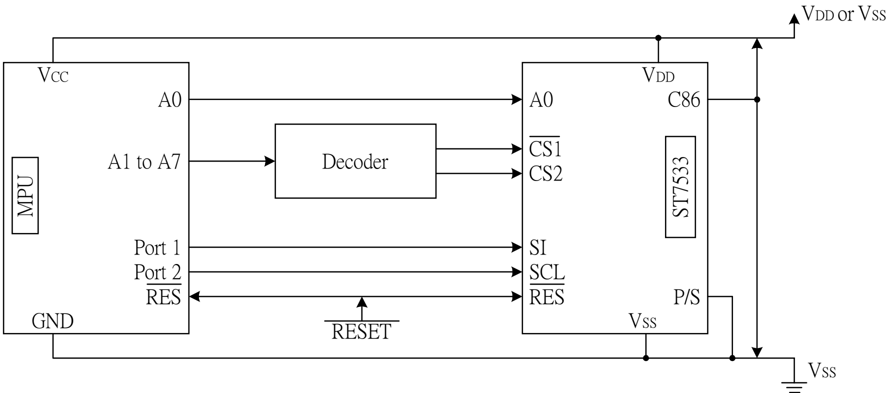


Figure 42-3

CONNECTIONS BETWEEN LCD DRIVERS (REFERENCE EXAMPLE)

The liquid crystal display area can be enlarged with ease through the use of multiple ST7533 Series chips. Use a same equipment type.

(1) ST7533 (master) ↔ ST7533 (slave)

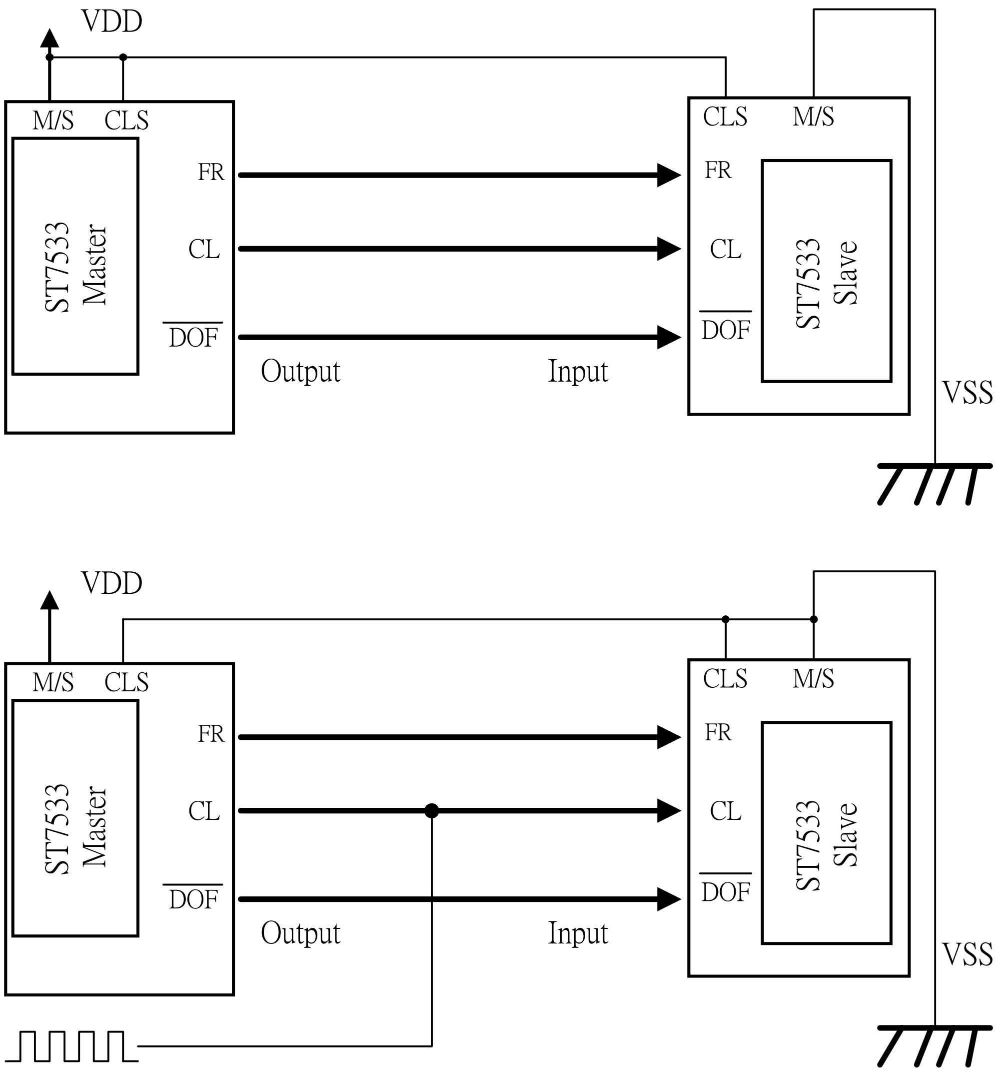


Figure 43-1

(2) Single-chip Structure

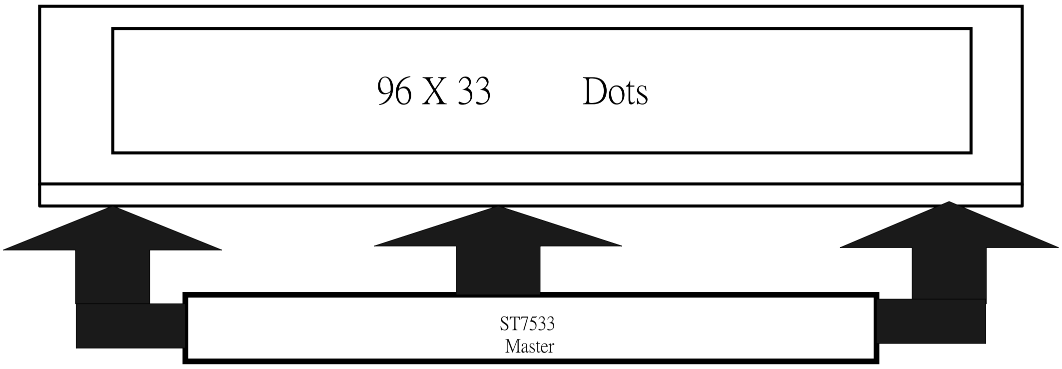


Figure 43-2

(3) Double-chip Structure

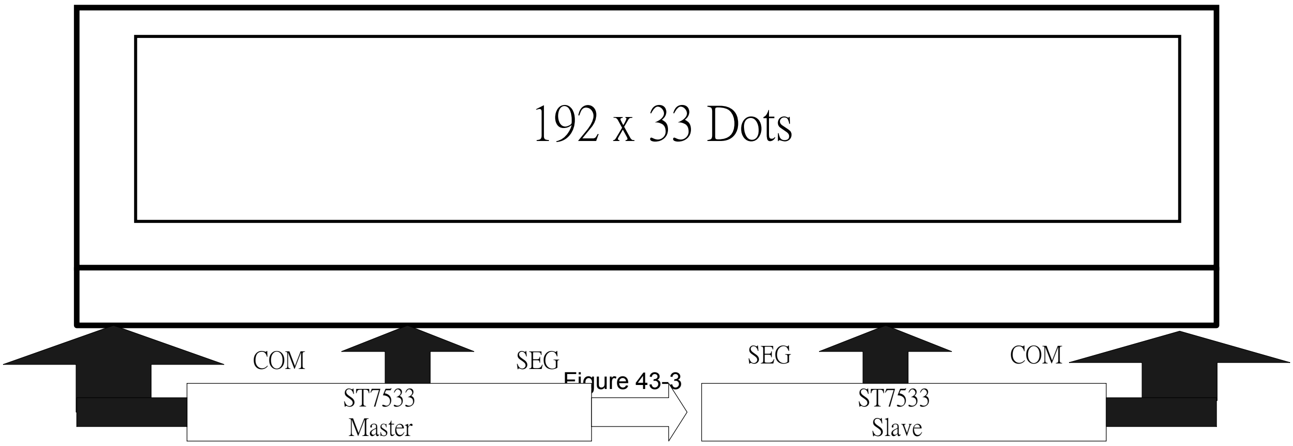


Figure 43-3

Revisions

Version 0.1 - Preliminary.

Version 0.2 - update Pad Center Coordinates page 2,3,4.

Version 0.2a - update PIN DESCRIPTIONS M/S.

Version 0.2b - update ABSOLUTE MAXIMUM RATINGS & DC CHARACTERISTICS.

Version 0.2c - update Master and Slave reference example.

Version 0.3 - update Pad Center Coordinates (1/33 , 1/17 Duty) page 3,4,5,6 and page-18.

Version 0.3a - update Pad diagram page2 and v5 regulator voltage diagram page24

Version 0.3b - Logic power supply $V_{DD} – V_{SS}$ = 1.8V to 3.3V (+10% Range) , V_{OUT}= -13V (+10% Range)

Version 0.3c - Modify page-27 The temperature grade of the Internal Power Supply for ST7533 (-0.05%/°C) Figure 14

Version 0.3d - Delete page-40 Figure 29

Version 0.4 - Modify V_{RS} temperature gradient (-0.15%/°C) and Reset “L” pulse width

Version 0.5 - Delete shipping forms include bare chip and TCP

Version 0.6 - Modify page-10 The TEST0(PAD No.65) must connect VDD

Version 1.0 - Modify Tdh (data hold time) and page41,42 initial flow , datasheet version change version 1.0