ST7554

V.90 USB WORLD MODEM CONTROLLER

SUMMARY DATA

GENERAL

- USB HOT PLUG & PLAY INTERFACE
- DIRECT INTERFACE TO ST MAFE+DAA CHIP-SET ST75951/ST952 FOR WORLD-WIDE DAA DESIGN OR TO STLC7550 FOR TRADITIONAL DAA DESIGN
- WINDOWS® 98 AND NT 5.0 SUPPORT
- TAPI 2.0 COMPLIANT
- SOFTWARE UPGRADABLE
- MINIMUM SYSTEM REQUIREMENTS:
- USB MOTHERBOARD, 166MHz PENTIUM® PROCESSOR WITH MMX™ TECHNOLOGY, WINDOWS® 98 AND 16MBYTES RAM OR WINDOWS® NT 5.0 AND 32MBYTES RAM

DEVICE FEATURES

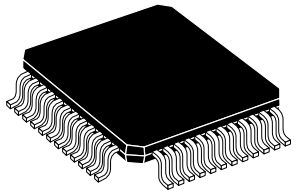
- SINGLE 9.216MHz CRYSTAL OSCILLATOR
- INTEGRATED ANALOG AND DIGITAL 3.3V REGULATORS
- DEDICATED PINS FOR RING, OFF-HOOK, CLID, LOOP CURRENT SENSE
- 0.5µm CMOS PROCESS
- TQFP48 (7 x 7 mm) PACKAGE

DATA MODEM / FAX / VOICE

- V.90
- V.34BIS, V.34, V.32BIS, V.32, V.22BIS, V.22, V.23, V.21
- BELL 103 AND BELL 212A
- V.17, V.27TER, V.29, FAX CLASS 1 SUPPORT
- V.42, V.42BIS, MNP 2, 3, 4, 5
- V.80
- V.8 AND AUTO MODE
- VOICE / FAX / MODEM DISTINCTION
- ADPCM VOICE COMPRESSION/DECOM-PRESSION
- VOICE DETECTION (SILENCE DETECTION)

OTHER FEATURES

- VIRTUAL UART (460.8Kbps)
- AT HAYES COMMAND COMPATIBLE
- TIME INDEPENDENT ESCAPE SEQUENCE (TIES) COMMAND
- CALLER ID



TQFP48 (7 x 7 x 1.40mm)
(Full Plastic Quad Flat Pack)

ORDER CODE : ST7554TQF7

- DTMF DETECTION AND GENERATION
- WAKE UP ON RING
- WORLD-WIDE PROGRAMMABLE SILICON DAA SUPPORT FOR ST75951/ST952 MAFE+DAA CHIP-SET

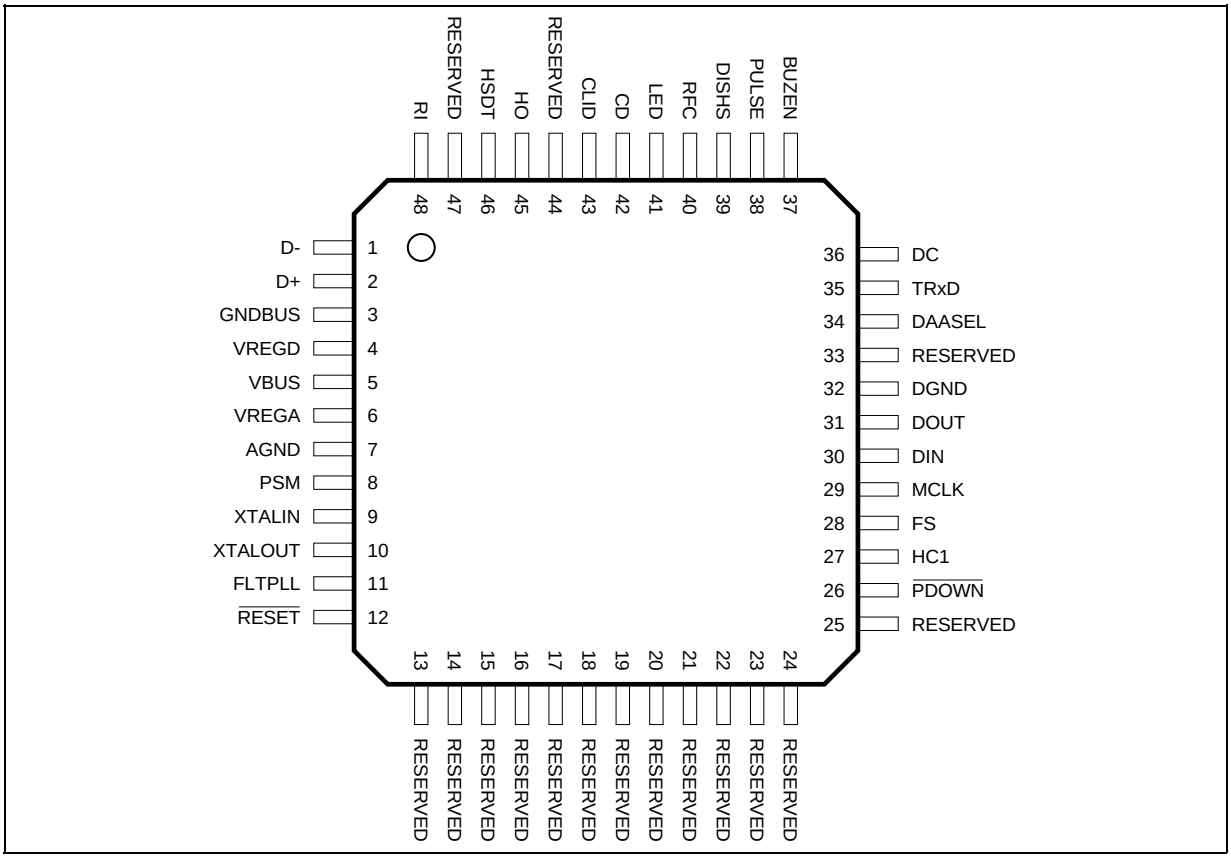
UNIVERSAL SERIAL BUS

- SPECIFICATION 1.0, 12MBps FULL SPEED
- ON-CHIP USB TRANSCEIVER WITH DIGITAL PLL
- COMMUNICATION DEVICE CLASS AND VENDOR REQUESTS
- BUS OR SELF POWERED APPLICATION (PIN-PROGRAMMABLE)
- ONNOW POWER MANAGEMENT (D0, D2, D3)
- LOW POWER CONSUMPTION (SUSPEND MODE D2), WHOLE APPLICATION BELOW 500µA

DESCRIPTION

The ST7554 is a single chip host signal processing Modem/fax/voice controller that supports data rates up to 56Kbps. All data pump and protocol functions are executed on the host PC's processor. This product has been developed in cooperation with Smart Link Ltd, who ported "USB-Modio", its host based Modem and system software into ST system and hardware platform. The ST7554 directly connects to ST high performance Modem analog front-end (MAFE) STLC7550 or to the highly integrated MAFE+DAA chip-set ST75951/ST952. The ST7554 also features an Universal Serial Bus (USB) interface for direct connection to the host PC for maximum flexibility and real plug & play operation.

PIN CONNECTIONS



PIN LIST

Name	Pin	Type	Description
XTALIN	9	I	Crystal Input
XTALOUT	10	O	Crystal Output
$\overline{\text{RESET}}$	12	I	Reset Function to initialise the device (active low)
VBUS	5	I	Positive Voltage Regulator Input, connected to USB VBUS
GNDBUS	3	I	Regulator Ground, connected to USB Ground (0V) (see Note 1)
VREGA	6	I/O	Positive Regulated Analog Input/Output Power Supply
VREGD	4	I/O	Positive Regulated Digital Input/Output Power Supply
PSM	8	I	Power Supply Mode (Bus-powered or Self-powered)
D+	2	I/O	Positive Data Signal of Differential Data Bus conforming to USB Standard Specification 1.0
D-	1	I/O	Negative Data Signal of Differential Data Bus conforming to USB Standard Specification 1.0
TRxD	35	I/O	Transmit/Receive Data Led
DC	36	I/O	DC mask
BUZEN	37	I/O	Buzzer Amplifier Enable/Mute
PULSE	38	I/O	Pulse dialing
DISHS	39	I/O	Disconnect external phone
RFC	40	I/O	Refresh
LED	41	I/O	LED control
CD	42	I/O	Carrier Detect Led
CLID	43	I/O	Caller ID
HO	45	I/O	Hook Control
HSDT	46	I/O	Current sense
RI	48	I/O	Ring Indicator
HC1	27	O	Modem Codec Hardware Control mode selection
$\overline{\text{PDOWN}}$	26	O	SSI Powerdown bit output (active low)
MCLK	29	O	SSI Master Clock Output
DAASEL	34	I	Select Silicon or Discrete DAA Configuration Mode
FS	28	I	SSI Frame Synchronisation Input
DOUT	31	O	SSI Serial Data Output
DIN	30	I	SSI Serial Data Input
FLTPLL	11	OA	PLL filter analog output. Must be connected to analog ground AGND with 33pF capacitor
DGND	32	I	Digital Ground (0V) (see Note 1)
AGND	7	I	Analog Ground (0V) (see Note 1)
RESERVED	13 to 25-33-44	-	Not connected
RESERVED	47	-	Connect to digital ground DGND

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Note 1 : Analog and digital ground pins must be tied together to USB ground GNDBUS.

PIN DESCRIPTION

1 - Power Supply (7 pins)

1.1 - Regulator Input Power Supply (VBUS)

This pin must be connected to USB VBUS (+5V). It supplies the integrated analog USB transceiver.

It is also the positive regulator power supply input (5V) when ST7554 is in bus-powered mode (PSM = 1) and it is used to internally generate the 3.3V supply for the digital and analog circuitry.

1.2 - Regulated Analog V_{DD} Supply (VREGA)

This pin is the analog power supply input (PSM = 0) or analog 3.3V power supply output (PSM = 1).
This pin is the positive analog power supply for the external Codec and DAA.
It is recommended to add a 1µF capacitor between VREGA and GNDA as close as possible to the IC pins.

1.3 - Regulated V_{DD} Supply (VREGD)

This pin is the digital power supply input (PSM = 0) or digital 3.3V power supply output (PSM = 1).
This pin is the positive digital power supply for the external Codec and DAA.
It is recommended to add a 1µF capacitor between VREGA and GNDA as close as possible to the IC pins.

1.4 - Power Supply Mode (PSM)

This pin controls the VREGD and VREGA power supply mode.

When PSM = 1, the application is bus-powered. The 3.3V power supply is generated internally from VBUS. In this case VREGD and VREGA are outputs which can be used to supply 3.3V to external devices (see Figure 1).
When PSM = 0, the application is self-powered. VBUS must be still connected to the VBUS Pin of the USB connector in order to supply the integrated USB transceiver. Anyway in this case VREGD and VREGA must be fed by a 3.3V externally regulated digital and analog power supplies (see Figure 2).

1.5 - Ground (DGND, AGND and GNDBUS)

DGND, AGND and GNDBUS are the digital, analog and USB ground return pins respectively. They should be connected together outside the chip to the GND pin of the USB plug.

Figure 1 : ST7554 in Bus-Powered mode (PSM = 1)

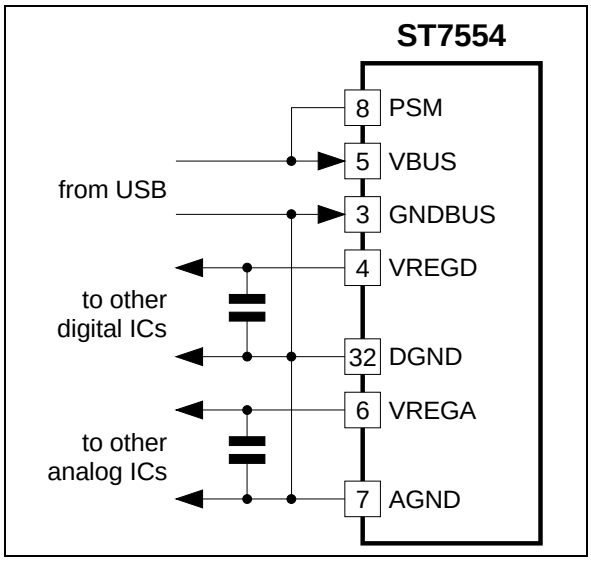
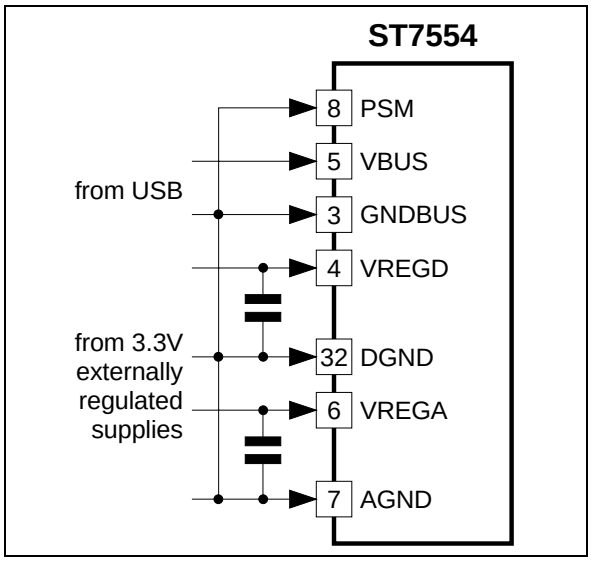


Figure 2 : ST7554 in Self Powered mode (PSM = 0)



2 - USB Interface (D+ , D-)

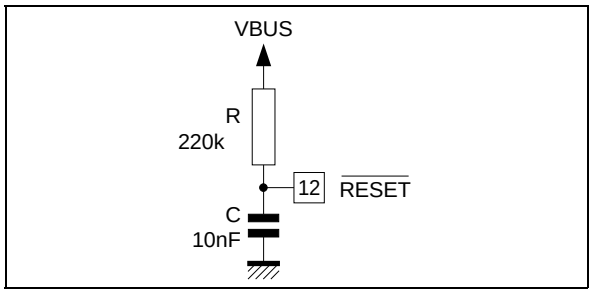
These pins are the positive and negative USB differential data lines. They shall be both connected to the USB plug or USB protection circuit via 27Ω series resistors for line impedance matching.

PIN DESCRIPTION (continued)

3 - Reset, Powerdown ($\overline{\text{RESET}}$, $\overline{\text{PDOWN}}$)

$\overline{\text{RESET}}$ Pin initialises the internal counters and control registers to their default value. A minimum low pulse of 1ms is required to reset the chip.
In a typical application $\overline{\text{RESET}}$ is connected to VBUS through a R, C network. This ensures that the chip is reset at each connection / disconnection to the USB bus (see Figure 3).
$\overline{\text{PDOWN}}$ Pin shall be connected to the powerdown inputs of the external codec used on the SSI.
When ST7554 is in Suspend mode, $\overline{\text{PDOWN}}$ is forced low so that the external codec is in powerdown.

Figure 3 : RC network for $\overline{\text{RESET}}$



4 - Serial Synchronous Interface

ST7554 has a Serial Syncronous Interface (SSI) dedicated to the connection of the STLC7550 or ST75951, ST high performance Modem Analog Front-End (MAFE).

4.1 - Data (DIN, DOUT)

Digital data word input/output of SSI, to be connected to the data word pins of STLC7550 or ST75951.

4.2 - Master Clock (MCLK)

This pin is the master clock output.

4.3 - Frame Synchronization (FS)

The frame synchronization is used to synchronize data transfer between ST7554 and the external Codec.

4.4 - Hardware Control (HC1)

HC1 must be connected to the corresponding pin of STLC7550 or ST75951, while their HC0 Pin shall be tied to the 3.3V VREGD digital supply. This pin selects data or control modes for the Modem Codec.

4.5 - DAA Selection (DAASEL)

Connect to VREGD when using silicon DAA chipset based on ST75951 + ST952. Connect to DGND when using STLC7550 with discrete interface.

5 - DAA Control Pins (IMP, DC, BUZEN, PULSE, DISHS, RFC, LED, CLID, HO, HSDT, RI)

These pins control the World Wide software programmable DAA through ST75951/ST952.

6 - Crystal (XTALIN, XTALOUT)

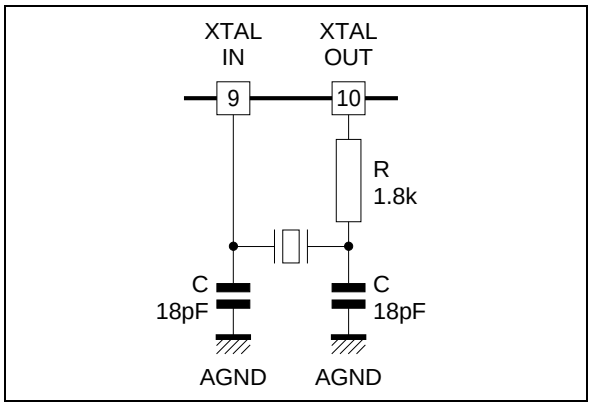
These pins must be tied to the 9.216MHz external crystal.

It is recommended to use a ±50ppm fundamental parallel resonator crystal. It is recommended to insert a 1.8kΩ resistor between XTALOUT and the crystal to limit its energy to 100µW for a 20Ω resonator (see Figure 4).

For a SMD crystal the load capacitor is typically C_{LOAD} = 12pF and this leads to an ideal value of C = 24pF for the capacitors between the crystal and analog ground (AGND). Anyway, in practice these capacitors shall be reduced down to C = 18pF each by considering parasitic capacitors on PCB and package (see Figure 4).

After a reset or when leaving the suspend state, the 9.216MHz is asserted inside ST7554 only 3.5ms later in order to wait for it to be stable.

Figure 4 : Application schematic for the 9.216MHz external crystal



7 - PLL Output Filter (FLTPLL)

This pin must be connected to the analog ground (AGND) through a 33pF capacitor.

8 - Reserved Pins (18 pins)

These pins must be left not connected except Pin 47 which should be connected to the digital ground DGND.

ELECTRICAL SPECIFICATIONS

Unless otherwise stated, electrical characteristics are specified over the operating range.
Typical values are given for V_{BUS} = +5V, V_{REGA} = 3.3V, V_{REGD} = 3.3V, T_{amb} = 25°C.

Absolute Maximum Rating (AGND = DGND = USB GND = 0V, all voltages with respect to 0V)

Symbol	Parameter	Value	Unit
DV_{DD}	Digital Power Supply	-0.3, 6.0	V
I_I	Input Current per Pin	-10, +10	mA
I_O	Output Current per Pin	-20, +20	mA
V_{IA}	Analog Input Voltage	-0.3, AV_{DD} + 0.3	V
V_{ID}	Digital Input Voltage	-0.3, DV_{DD} + 0.3	V
T_{oper}	Operating Temperature	0, +70	°C
T_{stg}	Storage Temperature	-55, +150	°C
P_{tot}	Maximum Power Dissipation	200	mW

Warning : Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranted at these extremes.

Nominal DC Characteristics (T_{amb} = 0 to 70°C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
POWER SUPPLY AND COMMON MODE VOLTAGE					
V_{BUS}	Supply Voltage	4	5	5.25	V
I_{VBUS}	Supply Current		TBD		mA
I_{VBUSS}	Supply Current in Suspend Mode (PSM = 1)		TBD		µA
V_{REGA}	Analog regulated Output Power Supply (PSM =1) Analog regulated Input Power Supply (PSM =0)	3.4-10% 3.3-10%	3.4 3.3	3.4+10% 3.3+10%	V V
V_{REGD}	Digital regulated Output Power Supply (PSM =1) Digital regulated Input Power Supply (PSM =0)	3.4-10% 3.3-10%	3.4 3.3	3.4+10% 3.3+10%	V V
I_{VREGA}	Analog regulated Output Current (PSM =1) Analog regulated Input Current (PSM =0)		 TBD	40	mA mA
I_{VREGD}	Digital regulated Output Current (PSM =1) Digital regulated Input Current (PSM =0)		20 20		mA mA
P_{DLP}	Low Power Mode (Suspend mode D2, wake-up on ring enabled)		TBD		mW
P_D	Operating Power (SSI in power-down)		TBD		mW
P_D	Operating Power (D0 power state)		TBD		mW
DIGITAL INTERFACE (except XTALIN, XTALOUT, PSM and $\overline{RESET}$) (these inputs have hysteresis)					
V_{IH} V_{IL}	High Level Input Voltage Low Level Input Voltage	0.8 x V_{REGD}		 0.2 x V_{REGD}	V V
V_{OH} V_{OL}	High Level Output Voltage Low Level Output Voltage	0.85 x V_{REGD}		 0.4	V V
I_{LEAK}	Input Leakage Current			± 1	µA
I_{OL} I_{OH}	High Level Output Current (0 < V_{OL} < $V_{OLMax.}$) Low Level Output Current ($V_{OHMin.}$ < V_{OH} < V_{REGD})	 -2		2	mA mA
V_{HYST}	Schmitt Trigger Hysteresis	0.8			V
C_{IN}	Input Capacitance		3		pF
PSM, $\overline{RESET}$ (these inputs have hysteresis)					
V_{IH} V_{IL}	High Level Input Voltage Low Level Input Voltage	0.7 x V_{BUS}		 0.3 x V_{BUS}	V V
I_{LEAK}	Input Leakage Current			± 1	µA
V_{HYST}	Schmitt Trigger Hysteresis	1	1.3		V
CRYSTAL OSCILLATOR (XTALIN, XTALOUT)					
V_{IH} V_{IL}	High Level Input Voltage Low Level Input Voltage		0.8 x V_{REGA} 0.2 x V_{REGA}		V V
I_{IH} I_{IL}	High Level Input Current Low Level Input Current	 -20		20	µA µA

UNIVERSAL SERIAL BUS INTERFACE

(see Chapter 7 of USB rev 1.0 for complete Electrical Specification)

Nominal DC Characteristics (D+, D-)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DI}	Differential Input Sensitivity [(D+) - (D-)]	0.2			V
V_{CM}	Differential Common Mode Range	0.8		2.5	V
V_{SE}	Single Ended Receiver Threshold	0.8		2	V
V_{OH} V_{OL}	High Level Output Static Voltage (RL of 15kΩ to GND) Low Level Output Static Voltage (RL of 1.5kΩ to 3.6V)	2.8		3.6 0.3	V V
I_{LO}	Hi-Z State Data Line Leakage Current (0V < V_{IN} < 3.3V)			±10	µA
C_{IN}	Transceiver Capacitance (Pin to GND)			20	pF
R_D (2)	Driver Output Resistance (steady state drive)	TBD		TBD	Ω

Note 2 : Excludes external resistor. In order to comply with USB Specifications 1.0, external series resistors of 27Ω ±1% each on D+ and D- are recommended

AC Characteristics (D+, D-) (see Figure 5 for test scheme)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{DR}	Average bit rate (12 M/s ± 0.05%)	11.97		12.03	Mbps
t_R	Rise Time between 10% and 90% (see Figure 6)	4		20	ns
t_F	Fall Time 10% and 90% (see Figure 6)	4		20	ns
V_{CRS}	Output Signal Crossover Voltage	1.3		2	V

Figure 5 : Test Scheme for D+/D-

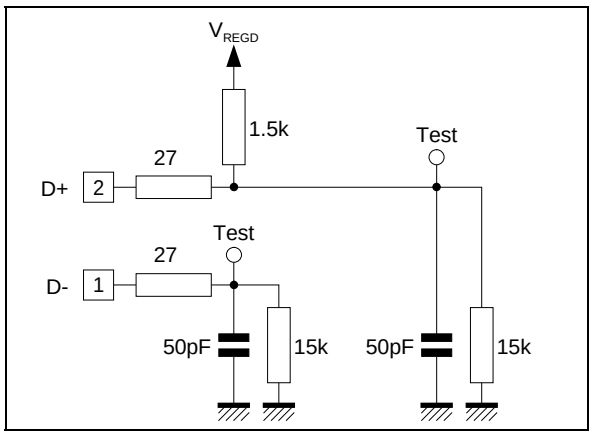
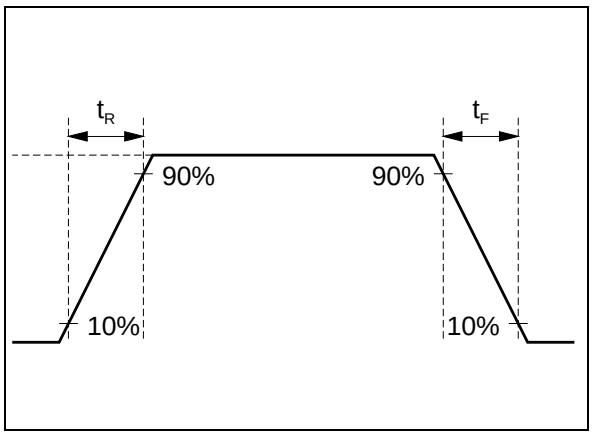


Figure 6 : Rise and Fall Time Measures



TYPICAL APPLICATIONS

Figure 7 : ST7554 Typical Application Diagram with ST75951/ST952

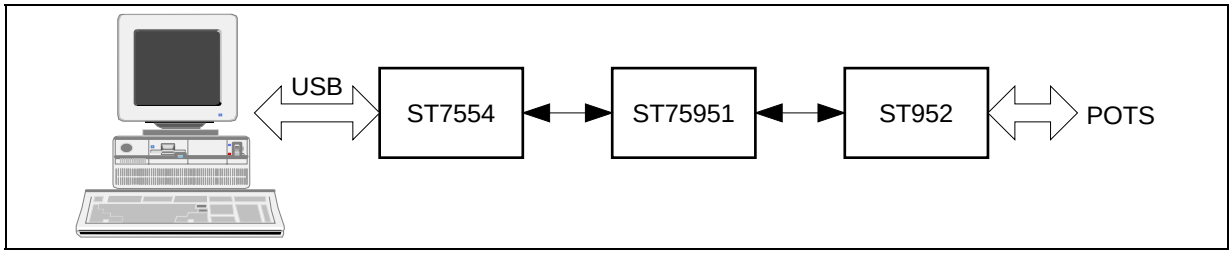
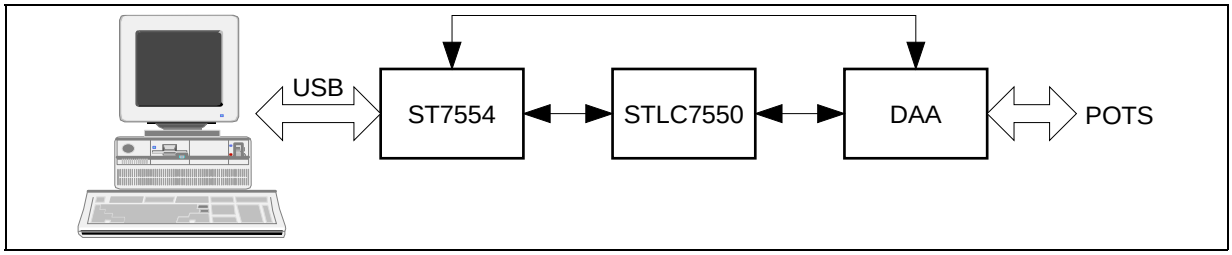
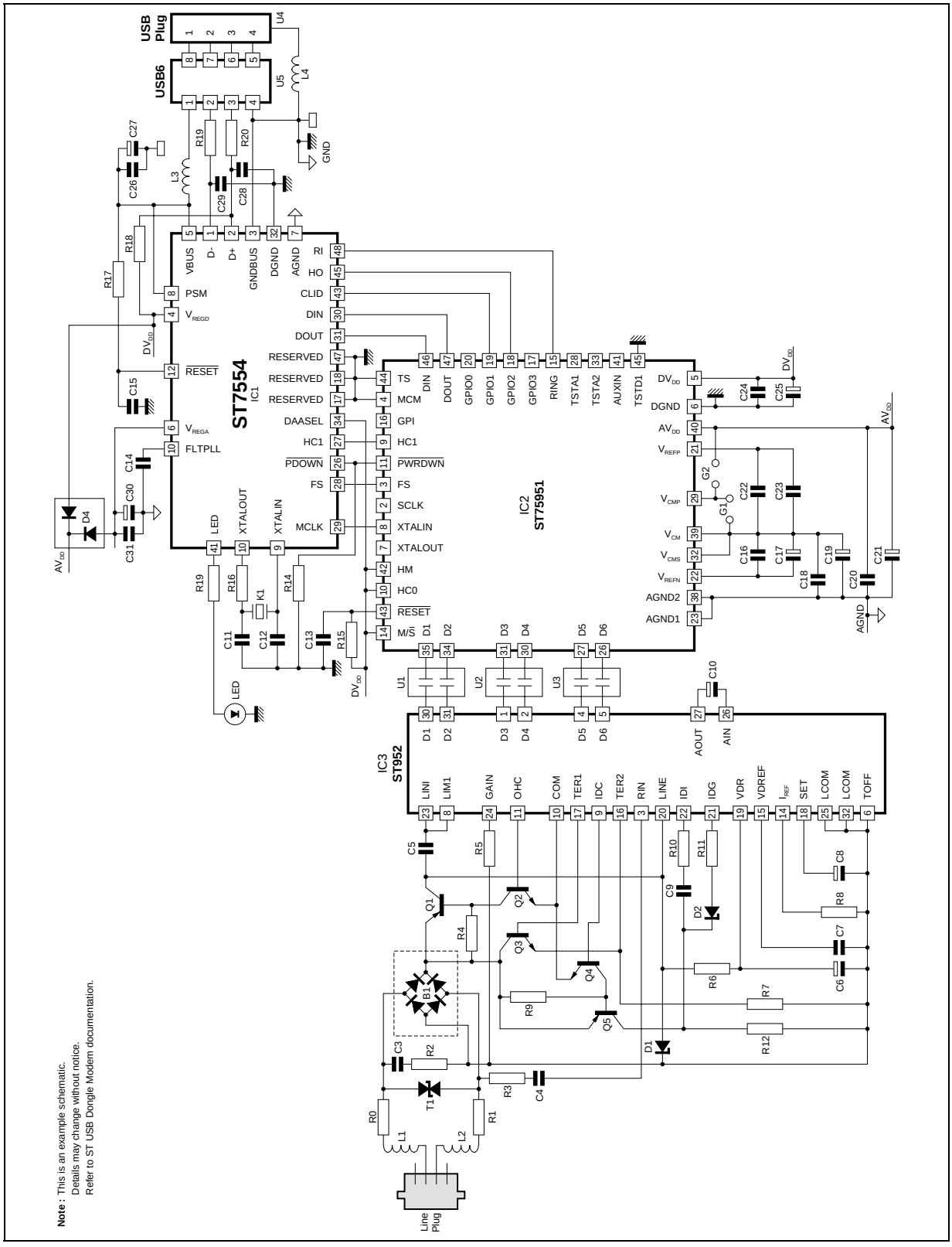


Figure 8 : ST7554 Typical Application Diagram with STLC7550



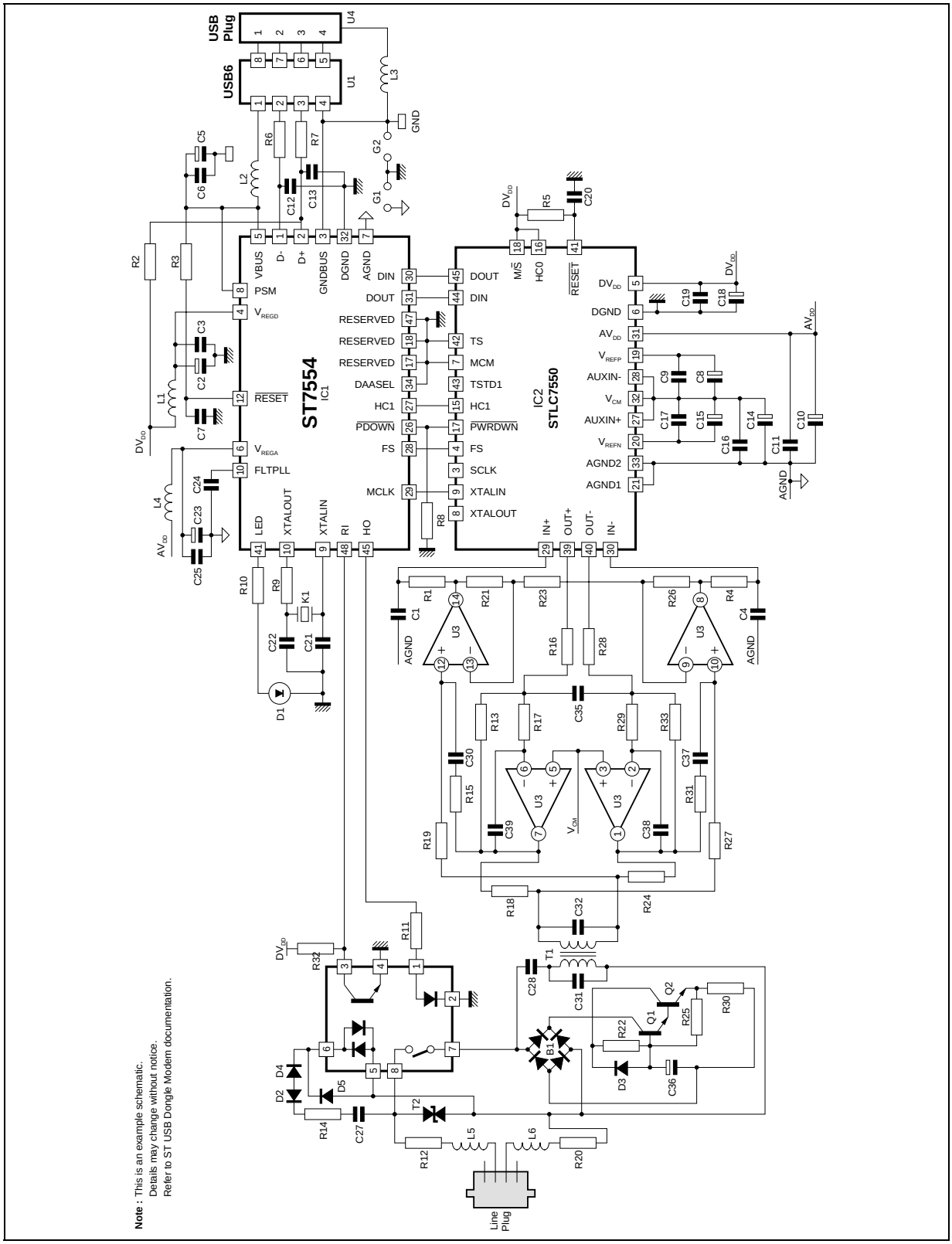
TYPICAL APPLICATIONS (continued)

Figure 9 : ST7554 Schematic Diagram with ST75951/ST952



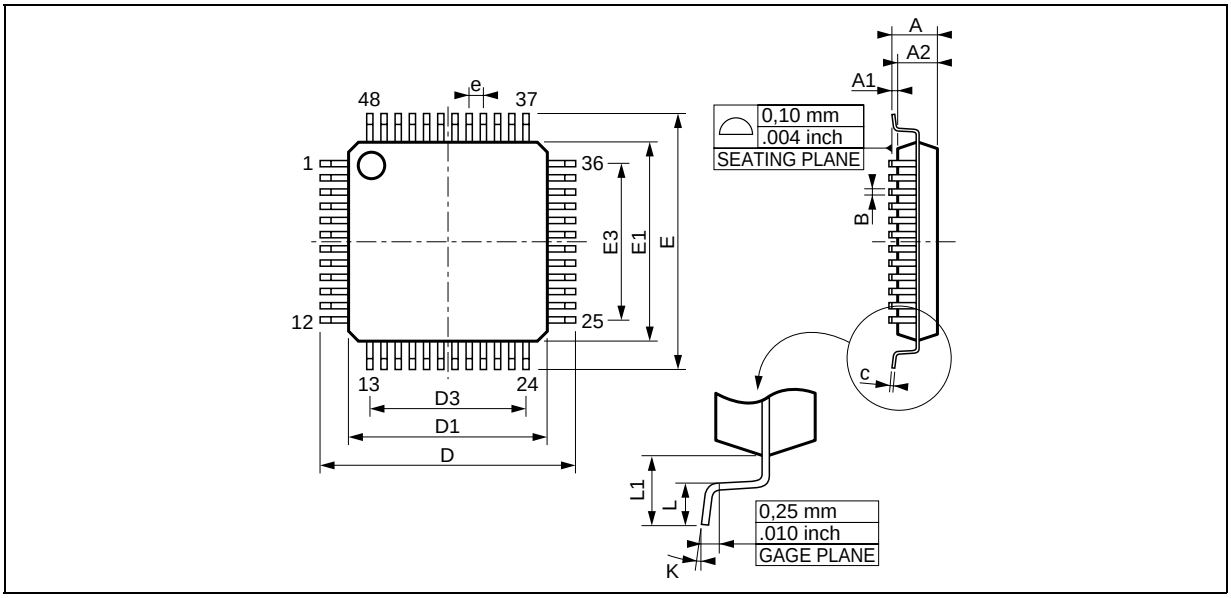
TYPICAL APPLICATIONS (continued)

Figure 10 : ST7554 Schematic Diagram with STLC7550 (in TQFP48 package)



PACKAGE MECHANICAL DATA

48 PINS - THIN PLASTIC QUAD FLAT PACK (TQFP)



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09		0.20	0.004		0.008
D		9.00			0.354	
D1		7.00			0.276	
D3		5.50			0.216	
e		0.50			0.0197	
E		9.00			0.354	
E1		7.00			0.276	
E3		5.50			0.216	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0^o (Min.), 7^o (Max.)					

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