

Sitronix

ST7598

344 x 88 Dot Matrix LCD Controller/Driver

INTRODUCTION

ST7598 is a single-chip LSI for graphic dot-matrix LCD systems. It incorporates power system, LCD controller and drivers for common/segment outputs. ST7598 can be connected directly to a microprocessor with 8-bit parallel interface or 4-line serial interface (SPI-4) or 3-line serial interface (SPI-3). Display data sent from MCU is stored into internal Display Data RAM (DDRAM) of 344x88 bits. ST7598 contains 344 segment-output and 88 common-output. The display data bits in DDRAM are directly related to the pixels on LCD panel. With built-in oscillation circuit and low power consumption power circuits, ST7598 can drive LCD panel without external clock or power, so that it is possible to make a display system with the fewest components and minimal power consumption.

FEATURES

Single-chip LCD controller/driver

Driver Output Circuits

- ◆ 344 segment outputs / 88 common outputs

On-chip Display Data RAM

- ◆ Capacity: $344 \times 88 = 30,272$ bits

Microprocessor Interface

- ◆ 8-bit bi-directional parallel interface supports 6800-series or 8080-series MCU
- ◆ 4-Line (8-bit) and 3-Line (9-bit) serial interfaces support write-operation and register-read (status/temperature...)
- ◆ All interfaces can read temperature (when sensor is ON), IC status and PROM data (register value)

External RSTB (Hardware Reset) Pin

On-chip Oscillator Circuit

- ◆ Internal oscillator requires no external component (external clock input is also supported)

On-chip Low Power Analog Circuit

- ◆ V3 generator with built-in boost-capacitors
- ◆ Built-in voltage regulator with programmable contrast
- ◆ Built-in PROM (Programmable Read-Only Memory) to

optimize Vop for LCD panel (3 times programmable)

- ◆ Built-in voltage follower for LCD bias voltages
- ◆ Support external power supply

Display Function

- ◆ Programmable display duty: $1/88 \sim 1/8$ (in 4-line basis)
Scan duty: $1/88 \sim 1/64$ (in 4-line basis)
- ◆ Support interlace-scanning method
- ◆ N-lines inversion

Built-in Temperature Sensor

- ◆ Temperature compensation with built-in thermal sensor
- ◆ Programmable Vop thermal gradient (19 slopes) and frame frequencies

Operating Voltage Range

- ◆ Digital Power (VDD1, VDD3): 3.3V ~ 5.0V (TYP.)
- ◆ Analog Power (VDD2): 3.3V ~ 5.0V (TYP.)

LCD Operating Voltage Range

- ◆ Maximum Vop: 22.2V ($V_{op}=V3-MV3$, i.e. $V3=11.1V$)

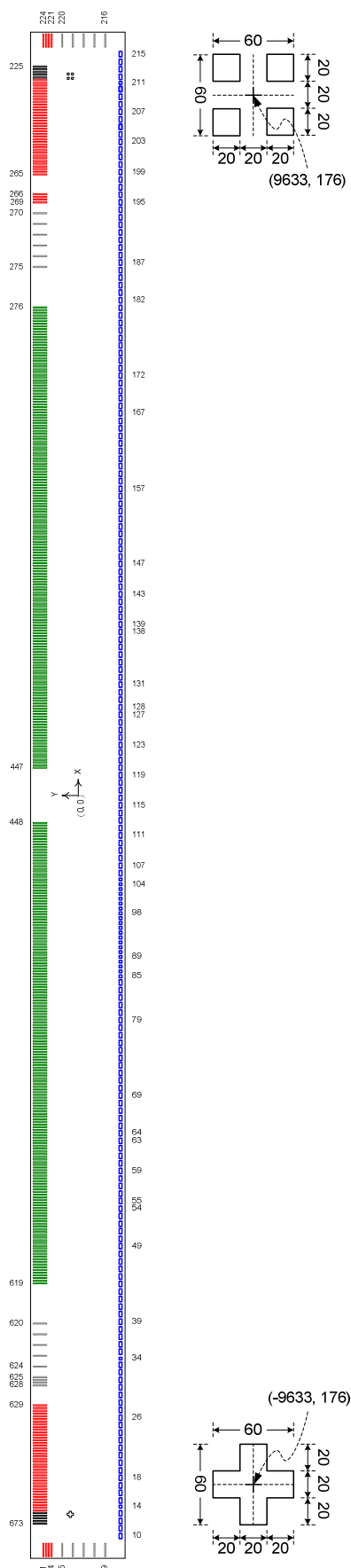
Operating Temperature Range : -40 ~ 95 °C

Package Type: COG

- ◆ Part Number : ST7598-G2-B1

AEC-Q100 Compliant for Automotive Applications

PAD ARRANGEMENT



Chip Size: 20706 x 1276 (+/- 15) Unit: um

Chip Thickness	480	Bump Height	15
PAD		Bump Size	
1~9, 216~224		96 x 26	
10~13, 15~33, 35~84, 106~210, 212~215		80 x 45	
14, 34, 85~105, 211		30 x 45	
225~673		26 x 96	
PAD		Minimal Pitch	
1~9, 216~224, 225~673		40	
10~215		52.5	
* Refer to “PAD CENTER COORDINATES” for ITO layout			

PAD CENTER COORDINATES

PAD	NAME	X	Y
1	COM[3]	-10273.5	540
2	COM[2]	-10273.5	500
3	COM[1]	-10273.5	460
4	COM[0]	-10273.5	420
5	Reserve	-10273.5	260
6	Reserve	-10273.5	100
7	Reserve	-10273.5	-60
8	Reserve	-10273.5	-220
9	Reserve	-10273.5	-380
10	Dummy	-10132.5	-584
11	Dummy	-10027.5	-584
12	Dummy	-9922.5	-584
13	Dummy	-9817.5	-584
14	Dummy	-9738.75	-584
15	VPP	-9660	-584
16	VPP	-9555	-584
17	EXTB	-9450	-584
18	T19	-9345	-584
19	CL	-9240	-584
20	T18	-9135	-584
21	CSB	-9030	-584
22	RSTB	-8925	-584
23	A0	-8820	-584
24	RWR	-8715	-584
25	ERD	-8610	-584
26	D0	-8505	-584
27	D1	-8400	-584
28	D2	-8295	-584
29	D3	-8190	-584
30	D4	-8085	-584
31	D5	-7980	-584
32	D6	-7875	-584
33	D7	-7770	-584
34	VSS1	-7691.25	-584
35	MODE	-7612.5	-584
36	CLS	-7507.5	-584
37	IF2	-7402.5	-584
38	IF1	-7297.5	-584
39	VDD2	-7192.5	-584
40	VDD2	-7087.5	-584
41	VDD2	-6982.5	-584
42	VDD2	-6877.5	-584
43	VDD2	-6772.5	-584
44	VDD2	-6667.5	-584
45	VDD2	-6562.5	-584
46	VDD2	-6457.5	-584

PAD	NAME	X	Y
47	VDD2	-6352.5	-584
48	VDD2	-6247.5	-584
49	VDD1	-6142.5	-584
50	VDD1	-6037.5	-584
51	VDD1	-5932.5	-584
52	VDD1	-5827.5	-584
53	VDD1	-5722.5	-584
54	VDD3	-5617.5	-584
55	VD1O	-5512.5	-584
56	VD1O	-5407.5	-584
57	VD1O	-5302.5	-584
58	VD1O	-5197.5	-584
59	VD1I	-5092.5	-584
60	VD1I	-4987.5	-584
61	VD1I	-4882.5	-584
62	VD1I	-4777.5	-584
63	VSS3	-4672.5	-584
64	VSS1	-4567.5	-584
65	VSS1	-4462.5	-584
66	VSS1	-4357.5	-584
67	VSS1	-4252.5	-584
68	VSS1	-4147.5	-584
69	VSS2	-4042.5	-584
70	VSS2	-3937.5	-584
71	VSS2	-3832.5	-584
72	VSS2	-3727.5	-584
73	VSS2	-3622.5	-584
74	VSS2	-3517.5	-584
75	VSS2	-3412.5	-584
76	VSS2	-3307.5	-584
77	VSS2	-3202.5	-584
78	VSS2	-3097.5	-584
79	VC	-2992.5	-584
80	VC	-2887.5	-584
81	VC	-2782.5	-584
82	VC	-2677.5	-584
83	VC	-2572.5	-584
84	VC	-2467.5	-584
85	T17	-2388.75	-584
86	T16	-2336.25	-584
87	T15	-2283.75	-584
88	T14	-2231.25	-584
89	TFCOM0	-2178.75	-584
90	T13	-2126.25	-584
91	T12	-2073.75	-584
92	T11	-2021.25	-584

PAD	NAME	X	Y
93	T10	-1968.75	-584
94	T9	-1916.25	-584
95	T8	-1863.75	-584
96	T7	-1811.25	-584
97	T6	-1758.75	-584
98	TFCOM1	-1706.25	-584
99	T5	-1653.75	-584
100	T4	-1601.25	-584
101	T3	-1548.75	-584
102	T2	-1496.25	-584
103	T1	-1443.75	-584
104	T0	-1391.25	-584
105	VREF	-1338.75	-584
106	TCAP	-1260	-584
107	V2	-1155	-584
108	V2	-1050	-584
109	V2	-945	-584
110	V2	-840	-584
111	V1	-735	-584
112	V1	-630	-584
113	V1	-525	-584
114	V1	-420	-584
115	MV1	-315	-584
116	MV1	-210	-584
117	MV1	-105	-584
118	MV1	0	-584
119	MV2	105	-584
120	MV2	210	-584
121	MV2	315	-584
122	MV2	420	-584
123	V3I	525	-584
124	V3I	630	-584
125	V3I	735	-584
126	V3I	840	-584
127	V3S	945	-584
128	V3O	1050	-584
129	V3O	1155	-584
130	V3O	1260	-584
131	MV3OI	1365	-584
132	MV3OI	1470	-584
133	MV3OI	1575	-584
134	MV3OI	1680	-584
135	MV3OI	1785	-584
136	MV3OI	1890	-584
137	MV3OI	1995	-584
138	MV3S	2100	-584
139	CB1P	2205	-584
140	CB1P	2310	-584

PAD	NAME	X	Y
141	CB1P	2415	-584
142	CB1P	2520	-584
143	CB1N	2625	-584
144	CB1N	2730	-584
145	CB1N	2835	-584
146	CB1N	2940	-584
147	AVDD	3045	-584
148	AVDD	3150	-584
149	AVDD	3255	-584
150	AVDD	3360	-584
151	AVDD	3465	-584
152	AVDD	3570	-584
153	AVDD	3675	-584
154	AVDD	3780	-584
155	AVDD	3885	-584
156	AVDD	3990	-584
157	CA1P	4095	-584
158	CA1P	4200	-584
159	CA1P	4305	-584
160	CA1P	4410	-584
161	CA1P	4515	-584
162	CA1P	4620	-584
163	CA1P	4725	-584
164	CA1P	4830	-584
165	CA1P	4935	-584
166	CA1P	5040	-584
167	CA1N	5145	-584
168	CA1N	5250	-584
169	CA1N	5355	-584
170	CA1N	5460	-584
171	CA1N	5565	-584
172	CA2P	5670	-584
173	CA2P	5775	-584
174	CA2P	5880	-584
175	CA2P	5985	-584
176	CA2P	6090	-584
177	CA2P	6195	-584
178	CA2P	6300	-584
179	CA2P	6405	-584
180	CA2P	6510	-584
181	CA2P	6615	-584
182	CA2N	6720	-584
183	CA2N	6825	-584
184	CA2N	6930	-584
185	CA2N	7035	-584
186	CA2N	7140	-584
187	NAVDD	7245	-584
188	NAVDD	7350	-584

PAD	NAME	X	Y
189	NAVDD	7455	-584
190	NAVDD	7560	-584
191	NAVDD	7665	-584
192	NAVDD	7770	-584
193	NAVDD	7875	-584
194	NAVDD	7980	-584
195	CD1P	8085	-584
196	CD1P	8190	-584
197	CD1P	8295	-584
198	CD1P	8400	-584
199	CD1N	8505	-584
200	CD1N	8610	-584
201	CD1N	8715	-584
202	CD1N	8820	-584
203	CD2P	8925	-584
204	CD2P	9030	-584
205	CD2P	9135	-584
206	CD2P	9240	-584
207	CD2N	9345	-584
208	CD2N	9450	-584
209	CD2N	9555	-584
210	CD2N	9660	-584
211	Dummy	9738.75	-584
212	Dummy	9817.5	-584
213	Dummy	9922.5	-584
214	Dummy	10027.5	-584
215	Dummy	10132.5	-584
216	Reserve	10273.5	-380
217	Reserve	10273.5	-220
218	Reserve	10273.5	-60
219	Reserve	10273.5	100
220	Reserve	10273.5	260
221	COM[4]	10273.5	420
222	COM[5]	10273.5	460
223	COM[6]	10273.5	500
224	COM[7]	10273.5	540
225	Dummy	10026.49	558.5
226	Dummy	9986.49	558.5
227	Dummy	9946.49	558.5
228	Dummy	9906.49	558.5
229	Dummy	9866.49	558.5
230	COM[12]	9826.49	558.5
231	COM[13]	9786.49	558.5
232	COM[14]	9746.49	558.5
233	COM[15]	9706.49	558.5
234	COM[20]	9666.49	558.5
235	COM[21]	9626.49	558.5
236	COM[22]	9586.49	558.5

PAD	NAME	X	Y
237	COM[23]	9546.49	558.5
238	COM[28]	9506.49	558.5
239	COM[29]	9466.49	558.5
240	COM[30]	9426.49	558.5
241	COM[31]	9386.49	558.5
242	COM[36]	9346.49	558.5
243	COM[37]	9306.49	558.5
244	COM[38]	9266.49	558.5
245	COM[39]	9226.49	558.5
246	COM[44]	9186.49	558.5
247	COM[45]	9146.49	558.5
248	COM[46]	9106.49	558.5
249	COM[47]	9066.49	558.5
250	COM[52]	9026.49	558.5
251	COM[53]	8986.49	558.5
252	COM[54]	8946.49	558.5
253	COM[55]	8906.49	558.5
254	COM[60]	8866.49	558.5
255	COM[61]	8826.49	558.5
256	COM[62]	8786.49	558.5
257	COM[63]	8746.49	558.5
258	COM[68]	8706.49	558.5
259	COM[69]	8666.49	558.5
260	COM[70]	8626.49	558.5
261	COM[71]	8586.49	558.5
262	COM[76]	8546.49	558.5
263	COM[77]	8506.49	558.5
264	COM[78]	8466.49	558.5
265	COM[79]	8426.49	558.5
266	COM[84]	8306.24	558.5
267	COM[85]	8266.24	558.5
268	COM[86]	8226.24	558.5
269	COM[87]	8186.24	558.5
270	Reserve	8026.24	558.5
271	Reserve	7866.24	558.5
272	Reserve	7706.24	558.5
273	Reserve	7546.24	558.5
274	Reserve	7386.24	558.5
275	Reserve	7226.24	558.5
276	SEG[343]	6963.57	558.5
277	SEG[342]	6923.57	558.5
278	SEG[341]	6883.57	558.5
279	SEG[340]	6843.57	558.5
280	SEG[339]	6803.57	558.5
281	SEG[338]	6763.57	558.5
282	SEG[337]	6723.57	558.5
283	SEG[336]	6683.57	558.5
284	SEG[335]	6643.57	558.5

PAD	NAME	X	Y
285	SEG[334]	6603.57	558.5
286	SEG[333]	6563.57	558.5
287	SEG[332]	6523.57	558.5
288	SEG[331]	6483.57	558.5
289	SEG[330]	6443.57	558.5
290	SEG[329]	6403.57	558.5
291	SEG[328]	6363.57	558.5
292	SEG[327]	6323.57	558.5
293	SEG[326]	6283.57	558.5
294	SEG[325]	6243.57	558.5
295	SEG[324]	6203.57	558.5
296	SEG[323]	6163.57	558.5
297	SEG[322]	6123.57	558.5
298	SEG[321]	6083.57	558.5
299	SEG[320]	6043.57	558.5
300	SEG[319]	6003.57	558.5
301	SEG[318]	5963.57	558.5
302	SEG[317]	5923.57	558.5
303	SEG[316]	5883.57	558.5
304	SEG[315]	5843.57	558.5
305	SEG[314]	5803.57	558.5
306	SEG[313]	5763.57	558.5
307	SEG[312]	5723.57	558.5
308	SEG[311]	5683.57	558.5
309	SEG[310]	5643.57	558.5
310	SEG[309]	5603.57	558.5
311	SEG[308]	5563.57	558.5
312	SEG[307]	5523.57	558.5
313	SEG[306]	5483.57	558.5
314	SEG[305]	5443.57	558.5
315	SEG[304]	5403.57	558.5
316	SEG[303]	5363.57	558.5
317	SEG[302]	5323.57	558.5
318	SEG[301]	5283.57	558.5
319	SEG[300]	5243.57	558.5
320	SEG[299]	5203.57	558.5
321	SEG[298]	5163.57	558.5
322	SEG[297]	5123.57	558.5
323	SEG[296]	5083.57	558.5
324	SEG[295]	5043.57	558.5
325	SEG[294]	5003.57	558.5
326	SEG[293]	4963.57	558.5
327	SEG[292]	4923.57	558.5
328	SEG[291]	4883.57	558.5
329	SEG[290]	4843.57	558.5
330	SEG[289]	4803.57	558.5
331	SEG[288]	4763.57	558.5
332	SEG[287]	4723.57	558.5

PAD	NAME	X	Y
333	SEG[286]	4683.57	558.5
334	SEG[285]	4643.57	558.5
335	SEG[284]	4603.57	558.5
336	SEG[283]	4563.57	558.5
337	SEG[282]	4523.57	558.5
338	SEG[281]	4483.57	558.5
339	SEG[280]	4443.57	558.5
340	SEG[279]	4403.57	558.5
341	SEG[278]	4363.57	558.5
342	SEG[277]	4323.57	558.5
343	SEG[276]	4283.57	558.5
344	SEG[275]	4243.57	558.5
345	SEG[274]	4203.57	558.5
346	SEG[273]	4163.57	558.5
347	SEG[272]	4123.57	558.5
348	SEG[271]	4083.57	558.5
349	SEG[270]	4043.57	558.5
350	SEG[269]	4003.57	558.5
351	SEG[268]	3963.57	558.5
352	SEG[267]	3923.57	558.5
353	SEG[266]	3883.57	558.5
354	SEG[265]	3843.57	558.5
355	SEG[264]	3803.57	558.5
356	SEG[263]	3763.57	558.5
357	SEG[262]	3723.57	558.5
358	SEG[261]	3683.57	558.5
359	SEG[260]	3643.57	558.5
360	SEG[259]	3603.57	558.5
361	SEG[258]	3563.57	558.5
362	SEG[257]	3523.57	558.5
363	SEG[256]	3483.57	558.5
364	SEG[255]	3443.57	558.5
365	SEG[254]	3403.57	558.5
366	SEG[253]	3363.57	558.5
367	SEG[252]	3323.57	558.5
368	SEG[251]	3283.57	558.5
369	SEG[250]	3243.57	558.5
370	SEG[249]	3203.57	558.5
371	SEG[248]	3163.57	558.5
372	SEG[247]	3123.57	558.5
373	SEG[246]	3083.57	558.5
374	SEG[245]	3043.57	558.5
375	SEG[244]	3003.57	558.5
376	SEG[243]	2963.57	558.5
377	SEG[242]	2923.57	558.5
378	SEG[241]	2883.57	558.5
379	SEG[240]	2843.57	558.5
380	SEG[239]	2803.57	558.5

PAD	NAME	X	Y
381	SEG[238]	2763.57	558.5
382	SEG[237]	2723.57	558.5
383	SEG[236]	2683.57	558.5
384	SEG[235]	2643.57	558.5
385	SEG[234]	2603.57	558.5
386	SEG[233]	2563.57	558.5
387	SEG[232]	2523.57	558.5
388	SEG[231]	2483.57	558.5
389	SEG[230]	2443.57	558.5
390	SEG[229]	2403.57	558.5
391	SEG[228]	2363.57	558.5
392	SEG[227]	2323.57	558.5
393	SEG[226]	2283.57	558.5
394	SEG[225]	2243.57	558.5
395	SEG[224]	2203.57	558.5
396	SEG[223]	2163.57	558.5
397	SEG[222]	2123.57	558.5
398	SEG[221]	2083.57	558.5
399	SEG[220]	2043.57	558.5
400	SEG[219]	2003.57	558.5
401	SEG[218]	1963.57	558.5
402	SEG[217]	1923.57	558.5
403	SEG[216]	1883.57	558.5
404	SEG[215]	1843.57	558.5
405	SEG[214]	1803.57	558.5
406	SEG[213]	1763.57	558.5
407	SEG[212]	1723.57	558.5
408	SEG[211]	1683.57	558.5
409	SEG[210]	1643.57	558.5
410	SEG[209]	1603.57	558.5
411	SEG[208]	1563.57	558.5
412	SEG[207]	1523.57	558.5
413	SEG[206]	1483.57	558.5
414	SEG[205]	1443.57	558.5
415	SEG[204]	1403.57	558.5
416	SEG[203]	1363.57	558.5
417	SEG[202]	1323.57	558.5
418	SEG[201]	1283.57	558.5
419	SEG[200]	1243.57	558.5
420	SEG[199]	1203.57	558.5
421	SEG[198]	1163.57	558.5
422	SEG[197]	1123.57	558.5
423	SEG[196]	1083.57	558.5
424	SEG[195]	1043.57	558.5
425	SEG[194]	1003.57	558.5
426	SEG[193]	963.57	558.5
427	SEG[192]	923.57	558.5
428	SEG[191]	883.57	558.5

PAD	NAME	X	Y
429	SEG[190]	843.57	558.5
430	SEG[189]	803.57	558.5
431	SEG[188]	763.57	558.5
432	SEG[187]	723.57	558.5
433	SEG[186]	683.57	558.5
434	SEG[185]	643.57	558.5
435	SEG[184]	603.57	558.5
436	SEG[183]	563.57	558.5
437	SEG[182]	523.57	558.5
438	SEG[181]	483.57	558.5
439	SEG[180]	443.57	558.5
440	SEG[179]	403.57	558.5
441	SEG[178]	363.57	558.5
442	SEG[177]	323.57	558.5
443	SEG[176]	283.57	558.5
444	SEG[175]	243.57	558.5
445	SEG[174]	203.57	558.5
446	SEG[173]	163.57	558.5
447	SEG[172]	123.57	558.5
448	SEG[171]	-123.57	558.5
449	SEG[170]	-163.57	558.5
450	SEG[169]	-203.57	558.5
451	SEG[168]	-243.57	558.5
452	SEG[167]	-283.57	558.5
453	SEG[166]	-323.57	558.5
454	SEG[165]	-363.57	558.5
455	SEG[164]	-403.57	558.5
456	SEG[163]	-443.57	558.5
457	SEG[162]	-483.57	558.5
458	SEG[161]	-523.57	558.5
459	SEG[160]	-563.57	558.5
460	SEG[159]	-603.57	558.5
461	SEG[158]	-643.57	558.5
462	SEG[157]	-683.57	558.5
463	SEG[156]	-723.57	558.5
464	SEG[155]	-763.57	558.5
465	SEG[154]	-803.57	558.5
466	SEG[153]	-843.57	558.5
467	SEG[152]	-883.57	558.5
468	SEG[151]	-923.57	558.5
469	SEG[150]	-963.57	558.5
470	SEG[149]	-1003.57	558.5
471	SEG[148]	-1043.57	558.5
472	SEG[147]	-1083.57	558.5
473	SEG[146]	-1123.57	558.5
474	SEG[145]	-1163.57	558.5
475	SEG[144]	-1203.57	558.5
476	SEG[143]	-1243.57	558.5

PAD	NAME	X	Y
477	SEG[142]	-1283.57	558.5
478	SEG[141]	-1323.57	558.5
479	SEG[140]	-1363.57	558.5
480	SEG[139]	-1403.57	558.5
481	SEG[138]	-1443.57	558.5
482	SEG[137]	-1483.57	558.5
483	SEG[136]	-1523.57	558.5
484	SEG[135]	-1563.57	558.5
485	SEG[134]	-1603.57	558.5
486	SEG[133]	-1643.57	558.5
487	SEG[132]	-1683.57	558.5
488	SEG[131]	-1723.57	558.5
489	SEG[130]	-1763.57	558.5
490	SEG[129]	-1803.57	558.5
491	SEG[128]	-1843.57	558.5
492	SEG[127]	-1883.57	558.5
493	SEG[126]	-1923.57	558.5
494	SEG[125]	-1963.57	558.5
495	SEG[124]	-2003.57	558.5
496	SEG[123]	-2043.57	558.5
497	SEG[122]	-2083.57	558.5
498	SEG[121]	-2123.57	558.5
499	SEG[120]	-2163.57	558.5
500	SEG[119]	-2203.57	558.5
501	SEG[118]	-2243.57	558.5
502	SEG[117]	-2283.57	558.5
503	SEG[116]	-2323.57	558.5
504	SEG[115]	-2363.57	558.5
505	SEG[114]	-2403.57	558.5
506	SEG[113]	-2443.57	558.5
507	SEG[112]	-2483.57	558.5
508	SEG[111]	-2523.57	558.5
509	SEG[110]	-2563.57	558.5
510	SEG[109]	-2603.57	558.5
511	SEG[108]	-2643.57	558.5
512	SEG[107]	-2683.57	558.5
513	SEG[106]	-2723.57	558.5
514	SEG[105]	-2763.57	558.5
515	SEG[104]	-2803.57	558.5
516	SEG[103]	-2843.57	558.5
517	SEG[102]	-2883.57	558.5
518	SEG[101]	-2923.57	558.5
519	SEG[100]	-2963.57	558.5
520	SEG[99]	-3003.57	558.5
521	SEG[98]	-3043.57	558.5
522	SEG[97]	-3083.57	558.5
523	SEG[96]	-3123.57	558.5
524	SEG[95]	-3163.57	558.5

PAD	NAME	X	Y
525	SEG[94]	-3203.57	558.5
526	SEG[93]	-3243.57	558.5
527	SEG[92]	-3283.57	558.5
528	SEG[91]	-3323.57	558.5
529	SEG[90]	-3363.57	558.5
530	SEG[89]	-3403.57	558.5
531	SEG[88]	-3443.57	558.5
532	SEG[87]	-3483.57	558.5
533	SEG[86]	-3523.57	558.5
534	SEG[85]	-3563.57	558.5
535	SEG[84]	-3603.57	558.5
536	SEG[83]	-3643.57	558.5
537	SEG[82]	-3683.57	558.5
538	SEG[81]	-3723.57	558.5
539	SEG[80]	-3763.57	558.5
540	SEG[79]	-3803.57	558.5
541	SEG[78]	-3843.57	558.5
542	SEG[77]	-3883.57	558.5
543	SEG[76]	-3923.57	558.5
544	SEG[75]	-3963.57	558.5
545	SEG[74]	-4003.57	558.5
546	SEG[73]	-4043.57	558.5
547	SEG[72]	-4083.57	558.5
548	SEG[71]	-4123.57	558.5
549	SEG[70]	-4163.57	558.5
550	SEG[69]	-4203.57	558.5
551	SEG[68]	-4243.57	558.5
552	SEG[67]	-4283.57	558.5
553	SEG[66]	-4323.57	558.5
554	SEG[65]	-4363.57	558.5
555	SEG[64]	-4403.57	558.5
556	SEG[63]	-4443.57	558.5
557	SEG[62]	-4483.57	558.5
558	SEG[61]	-4523.57	558.5
559	SEG[60]	-4563.57	558.5
560	SEG[59]	-4603.57	558.5
561	SEG[58]	-4643.57	558.5
562	SEG[57]	-4683.57	558.5
563	SEG[56]	-4723.57	558.5
564	SEG[55]	-4763.57	558.5
565	SEG[54]	-4803.57	558.5
566	SEG[53]	-4843.57	558.5
567	SEG[52]	-4883.57	558.5
568	SEG[51]	-4923.57	558.5
569	SEG[50]	-4963.57	558.5
570	SEG[49]	-5003.57	558.5
571	SEG[48]	-5043.57	558.5
572	SEG[47]	-5083.57	558.5

PAD	NAME	X	Y
573	SEG[46]	-5123.57	558.5
574	SEG[45]	-5163.57	558.5
575	SEG[44]	-5203.57	558.5
576	SEG[43]	-5243.57	558.5
577	SEG[42]	-5283.57	558.5
578	SEG[41]	-5323.57	558.5
579	SEG[40]	-5363.57	558.5
580	SEG[39]	-5403.57	558.5
581	SEG[38]	-5443.57	558.5
582	SEG[37]	-5483.57	558.5
583	SEG[36]	-5523.57	558.5
584	SEG[35]	-5563.57	558.5
585	SEG[34]	-5603.57	558.5
586	SEG[33]	-5643.57	558.5
587	SEG[32]	-5683.57	558.5
588	SEG[31]	-5723.57	558.5
589	SEG[30]	-5763.57	558.5
590	SEG[29]	-5803.57	558.5
591	SEG[28]	-5843.57	558.5
592	SEG[27]	-5883.57	558.5
593	SEG[26]	-5923.57	558.5
594	SEG[25]	-5963.57	558.5
595	SEG[24]	-6003.57	558.5
596	SEG[23]	-6043.57	558.5
597	SEG[22]	-6083.57	558.5
598	SEG[21]	-6123.57	558.5
599	SEG[20]	-6163.57	558.5
600	SEG[19]	-6203.57	558.5
601	SEG[18]	-6243.57	558.5
602	SEG[17]	-6283.57	558.5
603	SEG[16]	-6323.57	558.5
604	SEG[15]	-6363.57	558.5
605	SEG[14]	-6403.57	558.5
606	SEG[13]	-6443.57	558.5
607	SEG[12]	-6483.57	558.5
608	SEG[11]	-6523.57	558.5
609	SEG[10]	-6563.57	558.5
610	SEG[9]	-6603.57	558.5
611	SEG[8]	-6643.57	558.5
612	SEG[7]	-6683.57	558.5
613	SEG[6]	-6723.57	558.5
614	SEG[5]	-6763.57	558.5
615	SEG[4]	-6803.57	558.5
616	SEG[3]	-6843.57	558.5
617	SEG[2]	-6883.57	558.5
618	SEG[1]	-6923.57	558.5
619	SEG[0]	-6963.57	558.5
620	Reserve	-7226.24	558.5

PAD	NAME	X	Y
621	Reserve	-7386.24	558.5
622	Reserve	-7546.24	558.5
623	Reserve	-7706.24	558.5
624	Reserve	-7866.24	558.5
625	Reserve	-8026.24	558.5
626	Reserve	-8066.24	558.5
627	Reserve	-8106.24	558.5
628	Reserve	-8146.24	558.5
629	COM[83]	-8266.49	558.5
630	COM[82]	-8306.49	558.5
631	COM[81]	-8346.49	558.5
632	COM[80]	-8386.49	558.5
633	COM[75]	-8426.49	558.5
634	COM[74]	-8466.49	558.5
635	COM[73]	-8506.49	558.5
636	COM[72]	-8546.49	558.5
637	COM[67]	-8586.49	558.5
638	COM[66]	-8626.49	558.5
639	COM[65]	-8666.49	558.5
640	COM[64]	-8706.49	558.5
641	COM[59]	-8746.49	558.5
642	COM[58]	-8786.49	558.5
643	COM[57]	-8826.49	558.5
644	COM[56]	-8866.49	558.5
645	COM[51]	-8906.49	558.5
646	COM[50]	-8946.49	558.5
647	COM[49]	-8986.49	558.5
648	COM[48]	-9026.49	558.5
649	COM[43]	-9066.49	558.5
650	COM[42]	-9106.49	558.5
651	COM[41]	-9146.49	558.5
652	COM[40]	-9186.49	558.5
653	COM[35]	-9226.49	558.5
654	COM[34]	-9266.49	558.5
655	COM[33]	-9306.49	558.5
656	COM[32]	-9346.49	558.5
657	COM[27]	-9386.49	558.5
658	COM[26]	-9426.49	558.5
659	COM[25]	-9466.49	558.5
660	COM[24]	-9506.49	558.5
661	COM[19]	-9546.49	558.5
662	COM[18]	-9586.49	558.5
663	COM[17]	-9626.49	558.5
664	COM[16]	-9666.49	558.5
665	COM[11]	-9706.49	558.5
666	COM[10]	-9746.49	558.5
667	COM[9]	-9786.49	558.5
668	COM[8]	-9826.49	558.5

ST7598

PAD	NAME	X	Y
669	Dummy	-9866.49	558.5
670	Dummy	-9906.49	558.5
671	Dummy	-9946.49	558.5
672	Dummy	-9986.49	558.5
673	Dummy	-10026.49	558.5

Unit : um

Note:

- Please refer to the instructions “COM Scan Direction” and “Enable DDRAM” to decide COM layout sequence.

BLOCK DIAGRAM

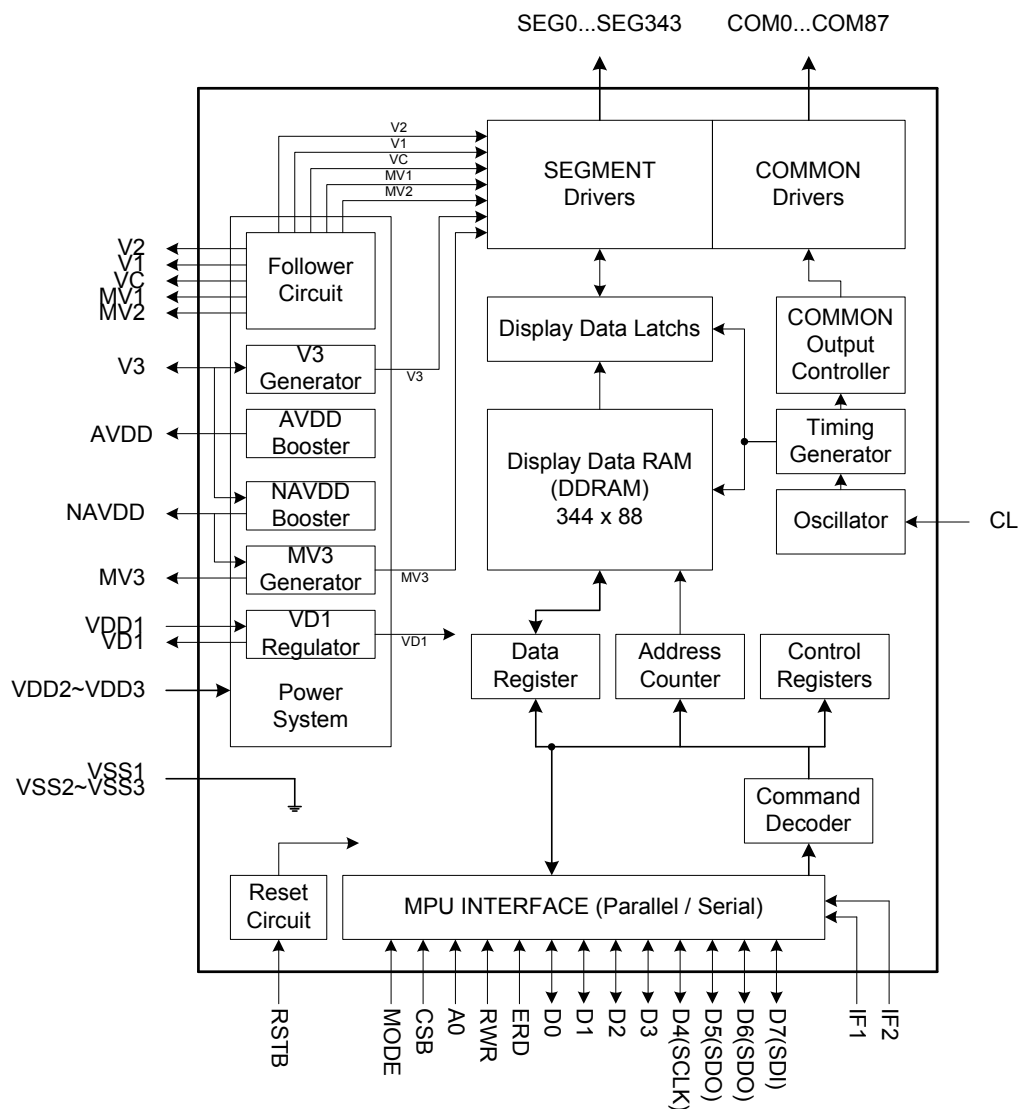


Fig. 1 Block Diagram

PIN DESCRIPTION

Power System

Name	Type	Description																
VDD1	Power	VDD1 is the power of interface I/O circuit and OSC circuit. VDD1 and VDD3 are separated in ITO and connected together by FPC or PCB.																
VDD2	Power	VDD2 is the analog power for booster circuit and OP.																
VDD3	Power	VDD3 is the power of VREF circuit. VDD1 and VDD3 are separated in ITO and connected together by FPC or PCB.																
VSS1	Power	Ground of interface, logic and OSC circuit. Ground system should be connected by FPC or PCB.																
VSS2	Power	Ground of booster circuit and OP. Ground system should be connected by FPC or PCB.																
VSS3	Power	Ground of VREF circuit. Ground system should be connected by FPC or PCB.																
VD1I VD1O	Power	VD1 is the power of internal digital circuit. It's generated by VD1 regulator (typical 1.8V). VD1I is the power source of digital circuit. VD1O is the output of VD1 regulator. VD1I and VD1O should be connected together by FPC or PCB. Those pins can not connect with VDD power (VDD1, VDD2 and VDD3).																
V3O V3I V3S	Power	LCD driver supply. V3O is the output voltage of V3 generated by ST7598. V3I is the V3 supply of LCD drivers. V3S is the sensor of the V3 generator. V3O, V3I and V3S should be connected together by FPC. The relation of the LCD dirver supply voltages are : <table><tr><td>Output</td><td>V3</td><td>V2</td><td>V1</td><td>VC</td><td>MV1</td><td>MV2</td><td>MV3</td></tr><tr><td>Voltage</td><td>Vop / 2</td><td>V3 * Bias</td><td>V2 / 2</td><td>GND</td><td>MV2 / 2</td><td>MV3 * Bias</td><td>- V3</td></tr></table>	Output	V3	V2	V1	VC	MV1	MV2	MV3	Voltage	Vop / 2	V3 * Bias	V2 / 2	GND	MV2 / 2	MV3 * Bias	- V3
Output	V3	V2	V1	VC	MV1	MV2	MV3											
Voltage	Vop / 2	V3 * Bias	V2 / 2	GND	MV2 / 2	MV3 * Bias	- V3											
V2	Power	LCD driver supply.																
V1	Power	LCD driver supply.																
VC	Power	LCD driver supply for center level. VC should be connected with ground system by FPC or PCB.																
MV1	Power	LCD driver supply.																
MV2	Power	LCD driver supply.																
MV3OI MV3S	Power	LCD driver supply. MV3OI is the output voltage of MV3 generated by ST7598 for supply LCD drivers. MV3S is the sensor of the MV3 generator. MV3OI and MV3S should be connected together by FPC.																

Name	Type	Description
AVDD	Power	AVDD is the supply power of positive analog circuits, such as V2, V1 and the power source of V3 generator. Connect a capacitor between AVDD pin and VSS2.
NAVDD	Power	NAVDD is the supply power of negative analog circuits, such as MV2, MV1 and the power source of MV3 generator. Connect a capacitor between NAVDD pin and VSS2.
CA1P CA1N CA2P CA2N	Power	DC/DC converter for AVDD power circuit. Connect a non-polar capacitor between CA1P pin and CA1N pin. Connect a non-polar capacitor between CA2P pin and CA2N pin.
CB1P CB1N	Power	DC/DC converter for MV3 power circuit. Connect a non-polar capacitor between CB1P pin and CB1N pin.
CD1P CD1N CD2P CD2N	Power	DC/DC converter for NAVDD power circuit. Connect a non-polar capacitor between CD1P pin and CD1N pin. Connect a non-polar capacitor between CD2P pin and CD2N pin.

LCD Driver Outputs

Name	Type	Description
SEG0 to SEG343	Output	LCD SEG-driver outputs. One voltage level of V2, V1, VC, MV1 and MV2 is selected by combining display DDRAM.
COM0 to COM87	Output	LCD COM-driver outputs. One voltage level of V3, VC and MV3 is selected by combining display DDRAM.

Microprocessor Interface

Name	Type	Description															
RSTB	Input	Reset input pin. When RSTB is "L", internal initialization procedure is executed.															
IF[2:1]	Input	These pins select interface operation mode. <table> <tr> <th>IF2</th><th>IF1</th><th>MCU interface type</th></tr> <tr> <td>H</td><td>H</td><td>80 series 8-bit parallel</td></tr> <tr> <td>H</td><td>L</td><td>68 series 8-bit parallel</td></tr> <tr> <td>L</td><td>H</td><td>8-bit serial (4-Line)</td></tr> <tr> <td>L</td><td>L</td><td>9-bit serial (3-Line)</td></tr> </table> Note: Refer to "Interface Selection" for detailed information.	IF2	IF1	MCU interface type	H	H	80 series 8-bit parallel	H	L	68 series 8-bit parallel	L	H	8-bit serial (4-Line)	L	L	9-bit serial (3-Line)
IF2	IF1	MCU interface type															
H	H	80 series 8-bit parallel															
H	L	68 series 8-bit parallel															
L	H	8-bit serial (4-Line)															
L	L	9-bit serial (3-Line)															
CSB	Input	Chip select input pin. CSB="L": This chip is selected and the MCU interface is active. CSB="H": This chip is not selected and the MCU interface is disabled (D[7:0] are high impedance).															
A0	Input	A0 determines whether the access is related data or command. - In parallel interface and 4-Line SPI: A0 is register selection input. A0 = "H": inputs on data bus are display data; A0 = "L": inputs on data bus are command. - A0 is not used in 3-Line SPI. Please fix to "H" by VDD1.															
RWR	Input	Read / Write execution control pin. (This pin is only used in parallel interface) <table> <tr> <th>MCU Type</th><th>RWR</th><th>Description</th></tr> <tr> <td>6800-series</td><td>R/W</td><td>Read / Write control input pin R/W = "H" : read R/W = "L" : write</td></tr> <tr> <td>8080-series</td><td>/WR</td><td>Write enable clock input pin. The data are latched at the rising edge of the /WR signal.</td></tr> </table> This pin is not used in serial interfaces and should be connected to "H" by VDD1.	MCU Type	RWR	Description	6800-series	R/W	Read / Write control input pin R/W = "H" : read R/W = "L" : write	8080-series	/WR	Write enable clock input pin. The data are latched at the rising edge of the /WR signal.						
MCU Type	RWR	Description															
6800-series	R/W	Read / Write control input pin R/W = "H" : read R/W = "L" : write															
8080-series	/WR	Write enable clock input pin. The data are latched at the rising edge of the /WR signal.															
ERD	Input	Read / Write execution control pin. (This pin is only used in parallel interface) <table> <tr> <th>MCU Type</th><th>ERD</th><th>Description</th></tr> <tr> <td>6800-series</td><td>E</td><td>Read / Write control input pin. R/W = "H": When E is "H", data bus is in output status. R/W = "L": The data are latched at the falling edge of the E signal.</td></tr> <tr> <td>8080-series</td><td>/RD</td><td>Read enable input pin. When /RD is "L", data bus is in output status.</td></tr> </table> This pin is not used in serial interfaces and should be connected to "H" by VDD1.	MCU Type	ERD	Description	6800-series	E	Read / Write control input pin. R/W = "H": When E is "H", data bus is in output status. R/W = "L": The data are latched at the falling edge of the E signal.	8080-series	/RD	Read enable input pin. When /RD is "L", data bus is in output status.						
MCU Type	ERD	Description															
6800-series	E	Read / Write control input pin. R/W = "H": When E is "H", data bus is in output status. R/W = "L": The data are latched at the falling edge of the E signal.															
8080-series	/RD	Read enable input pin. When /RD is "L", data bus is in output status.															
D[7:0]	I/O	The bi-directional data bus of the MCU interface. When CSB is "H", they are high impedance. If using serial interface: SDI: D7 SDO: D5, D6 SCL: D4 D0~D3 must connected to "H" by VDD1.															

Note:

- After VDD1 is turned ON, all MCU interface pins should not be left OPEN.
- The un-used pins should be connected to VDD1.

PROM Pins

Name	Type	Description
VPP	Power	The programming power supply of the built-in PROM. Apply external power (VPP=7.25~7.75V, VPP _{TYP} =7.5V) here when programming (> 4mA for successful programming).
EXTB	Input	EXTB="L": Enable the extension operation mode for PROM operation. When programming PROM, connect EXTB to VSS1 externally. This pin has an internal pull-high resistor. Please leave this pin OPEN after special operation.

System Pins

Name	Type	Description
MODE	Input	Must fix to "H" by VDD1.
CLS	Input	When using internal clock oscillator, please connect this pin to "H" by VDD1. When using external clock oscillator, please connect this pin to "L" by VSS1.
CL	I/O	When using internal clock oscillator, this pin is oscillator output. When using external clock oscillator, this pin is oscillator input.

Test Pins

Name	Type	Description
TCAP	Test	Reserved for testing only. Leave this pin open.
VREF	Test	Reserved for testing only. Leave this pin open.
T0~T19	Test	Reserved for testing only. Leave those pins open.
TFCOM0 TFCOM1	Test	Reserved for testing only. Leave those pins open.

Note: Please refer to LCD LAYOUT GUIDE for Application Circuit, ITO Layout Suggestion and ITO Resistance.

FUNCTION DESCRIPTION

Microprocessor Interface

Chip Select Input

CSB pin is used for chip selection. ST7598 can interface with a MCU when CSB is “L”. If CSB is “H”, the inputs of A0, ERD and RWR with any combination will be ignored and D[7:0] are high impedance. In 3-Line and 4-Line serial interfaces, the internal shift register and serial counter are reset when CSB is “H”.

Interface Selection

The interface selection is controlled by IF[2:1] pins. Please refer to the table below:

Table 1

Setting		MCU Type	Interface Pin Function				
IF2	IF1		CSB	A0	RWR	ERD	D[7:0]
H	H	Parallel 8080 series MCU	CSB	A0	/WR	/RD	D[7:0]
H	L	Parallel 6800 series MCU			R/W	E	
L	H	Serial 4-Line series MCU			-	-	
L	L	Serial 3-Line series MCU		-	-	-	D7=SDI, D[5:6]=SDO, D4=SCL, D[0:3] are not used

Note: The un-used pins are marked as “-” and should be connected to “H” by VDD1.

Parallel Interface

When parallel interface is selected, the interface transmission type will be determined by the combination of the control signals. Please refer to the table below:

Table 2

8080 series MCU		6800 series MCU		A0	CSB	Interface Transmission Type
/WR	/RD	R/W	E			
↑	H	L	↓	L	L	Write Command
↑	H	L	↓	H		Write Display Data or Parameter
H	↓	H	↑	H		Read Display Data or Parameter Start
H	↑	H	↓	H		Read Display Data or Parameter Stop

Note:

1. Reading Display Data or Parameter is specified by the instruction before the read operation.
2. When reading Display Data (DDRAM contents), the first output byte is dummy byte.
3. When reading Parameter (temperature, status and PROM data), the first output byte is valid.

Serial Interface

In serial interface (4-Line or 3-Line), IC is active and the control signals (SDI, SDO, SCL and A0 for 4-Line) are enabled when CSB is “L”. When CSB is “H”, the MCU interface is not active and the internal shift-register and serial-counter are reset.

If CSB is set to “H” before all data bits (8 bits) are entered completely, the data concerned is invalidated. Before entering succeeding sets of data, you must input the data concerned again. In order to avoid transfer error due to incoming noise when write command or data, it is recommended to set CSB at “H” on byte basis, so that the serial-to-parallel counter and the shift-register can be cleared after each byte of transmission.

The serial interface can read: temperature, status and PROM parameter, except Display Data. Please note that:

1. A read transfer will be stopped if CSB is set to “H”.
2. When reading IC status, the first output bit is dummy bit.
3. When reading temperature and PROM content, the first output bit is valid (without dummy bit).

4-Line Serial Interface

In 4-Line serial interface, A0 signal is latched at the 8th rising edge of the SCL signal (refer to Fig. 2).

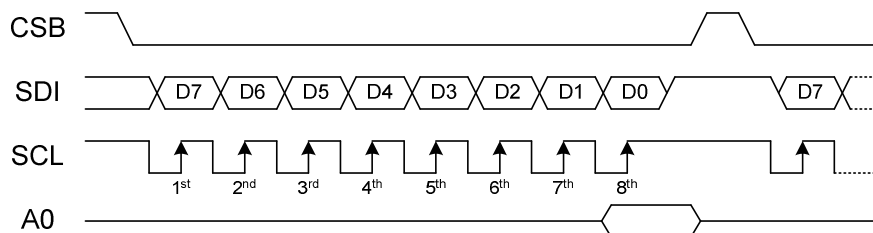


Fig. 2 Write-Operation of 4-Line Serial Interface

After entering the Read Status instruction to read IC status, the information is shifted out as shown below. CSB signal must be kept at "L" during this period. The 1st read out data (1st Data) is 9 bits, which includes a dummy bit at the 1st bit. After 1st Data, all read out data (2nd Data) will be 8 bits.

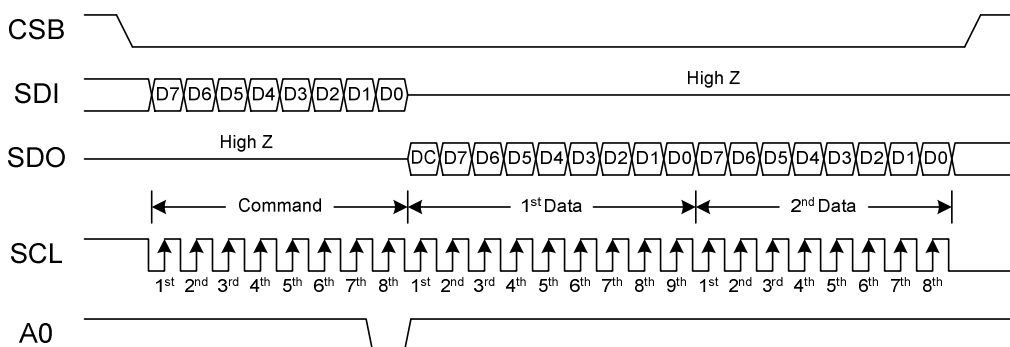


Fig. 3 Read-Operation of 4-Line Serial Interface

3-Line Serial Interface

In 3-Line interface, A0 signal is not available. The 1st output bit defines command byte or parameter byte (refer to Fig. 4).

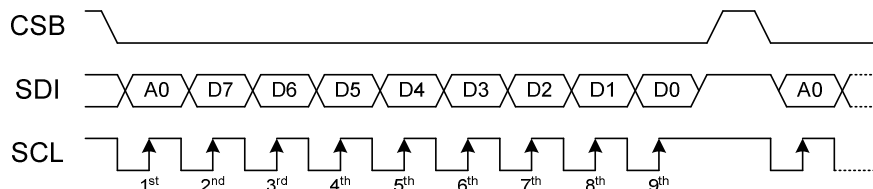


Fig. 4 Write-Operation of 3-Line Serial Interface

After entering the Read Status instruction to read IC status, the information is shifted out as shown below. CSB signal must be kept at "L" during this period. The 1st read out data (1st Data) is 9 bits, which includes a dummy bit at the 1st bit. After 1st Data, all read out data (2nd Data) will be 8 bits.

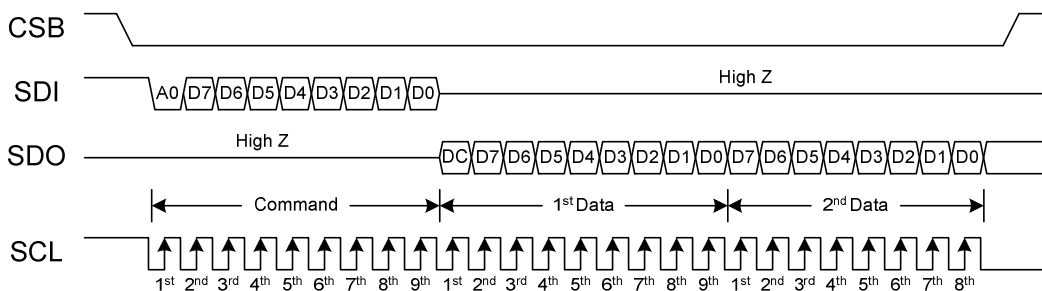


Fig. 5 Read-Operation of 3-Line Serial Interface

Display Data RAM (DDRAM)

ST7598 containing a 344x88 bits static RAM stores the display data. The display data RAM (DDRAM) stores the pixel data of the LCD. The built-in DDRAM is an addressable memory array with 344 columns by 88 rows. When the data bit in DDRAM is “1”, the segment driver will output “ON” voltage. If it is “0”, the segment driver will output “OFF” voltage. The LCD controller reads the pixel data in DDRAM, and then it outputs to COM/SEG pad. While the LCD controller operates independently, display data can be written into DDRAM at the same time and data is also being displayed on LCD panel without causing the abnormal display.

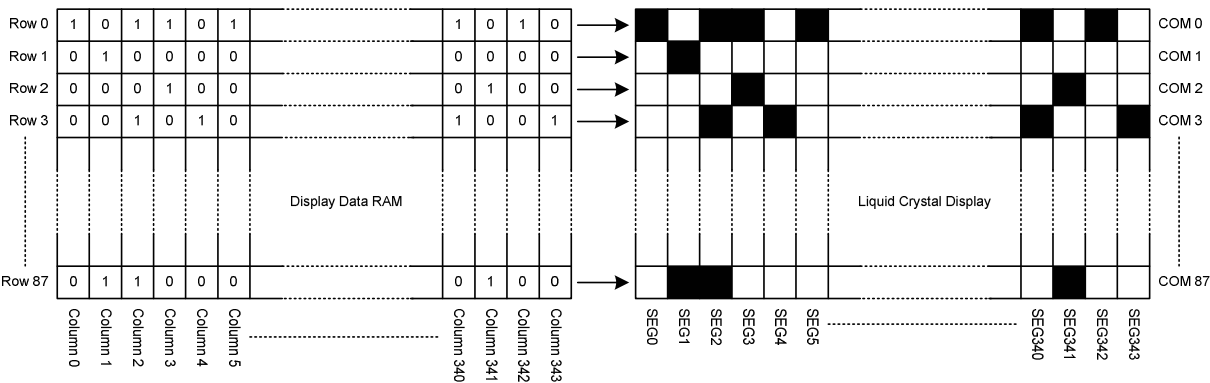


Fig. 6 DDRAM Mapping

Page Address Circuit

This circuit provides the page address of DDRAM. It incorporates a 4-bit Page Address Register which can be modified by the instruction of Page Address Set only. As shown in Fig. 7, the 88 rows are configured as 11 pages with 8-bit (for COM0~COM87 while row address direction is normal). The page address must be set before accessing DDRAM content.

Column Address Circuit

This circuit provides the column address of DDRAM. It incorporates a 9-bit Column Address Register which can be modified by the instruction of “Column Address” only. The column address must be set before accessing DDRAM content.

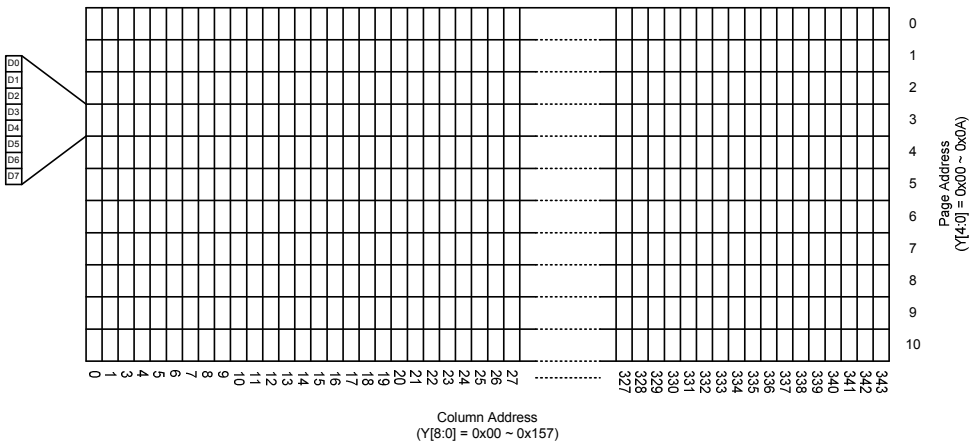


Fig. 7 DDRAM Format

Addressing

Data is downloaded into the Display Data RAM matrix in ST7598 as byte-format. The Display Data RAM has a matrix of 344 by 88 bits. The address ranges are: X=0~343 (column address), Y=0~10 (page address). Address outside these ranges is not allowed.

Addressing the target DDRAM of access is specified with Page Address Set and Column Address Set commands. Using the Display Data Input/Output Direction command allows user to increase the address either in the page or column direction. In both case, the address is increased by one (+1) after one byte write (or read) operation.

When Display Data Input/Output Direction command setting is column direction, the column address counter is increased by 1 (+1) after the write or read operation as shown in Fig. 8. If column address counter is over 157h after data accessed, the page address is increased by one (+1) and the column address is returned to 00h respectively.

When Display Data Input/Output Direction command setting is page direction, the page address counter is increase by 1 (+1) after the write or read operation as shown in Fig. 9. Unlike the column direction, the page address counter doesn't return to 0 if the page address exceeds 0Ah in page direction; and the application system should set page address to 0 and increase column address by one (+1) manually by Page Address Set and Column Address Set commands.

Whichever direction is selected, the page address and column address counters will NOT returned to 00h and 00h, after the last DDRAM byte of column address 157h and page address 0Ah is accessed.

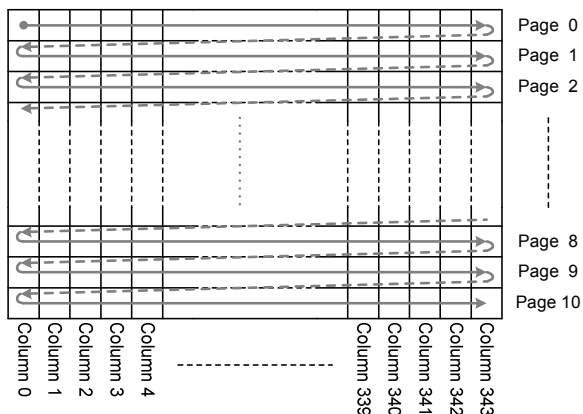


Fig. 8 Display Data Input Direction (DIR=0 & MX=0)

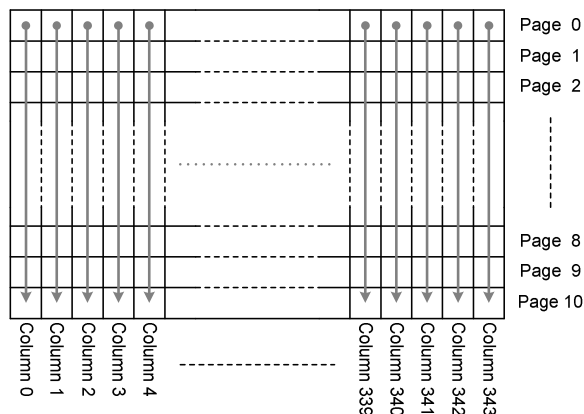


Fig. 9 Display Data Input Direction (DIR=1 & MX=0)

LCD Display Function
DDRAM Map to LCD Driver Output

The internal relation between DDRAM and LCD driver circuit (SEG/COM output path) with different MX or MY setting is illustrated below. Please refer to the instructions “COM Scan Direction” and “Enable DDRAM” to decide COM layout sequence.

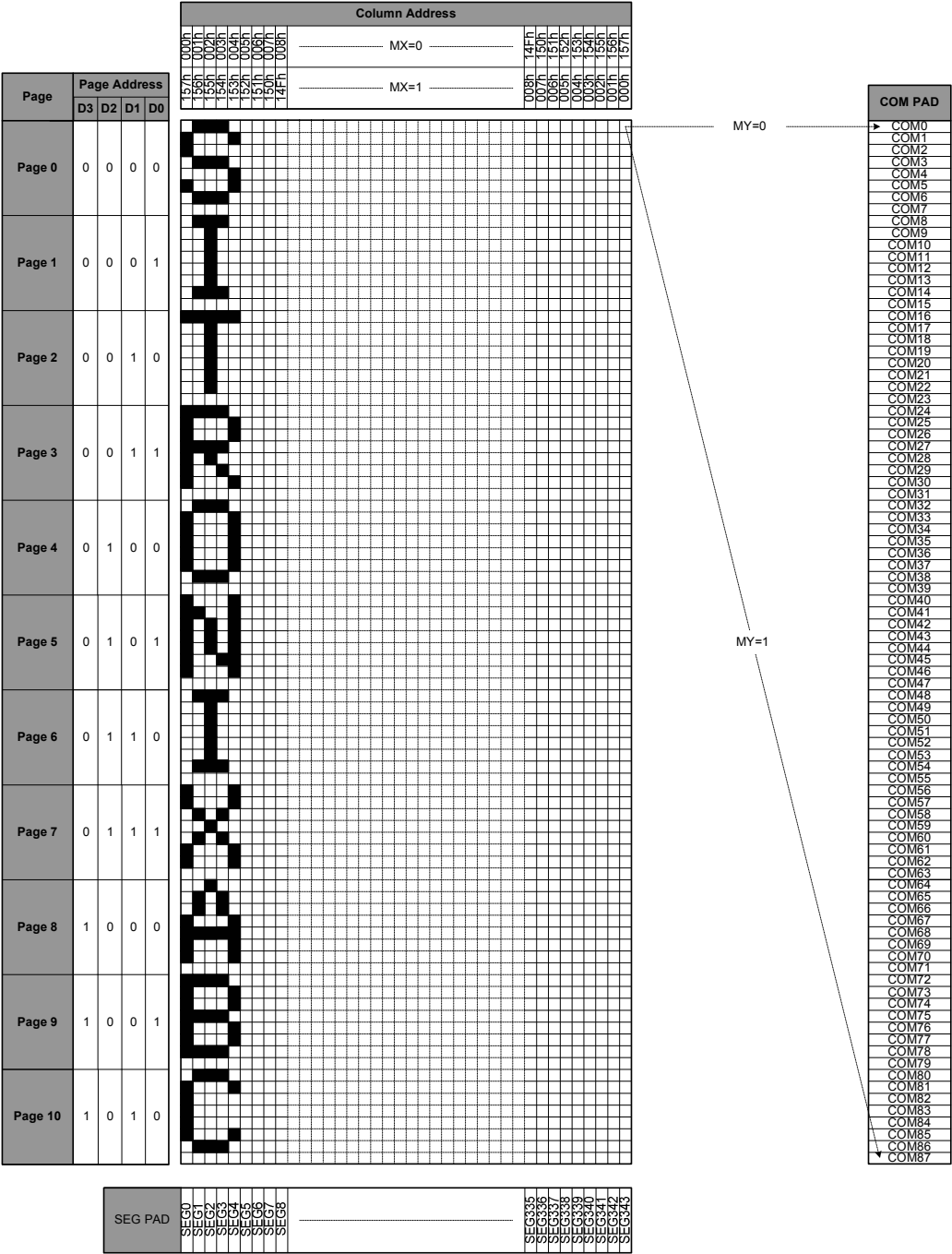


Fig. 10 DDRAM Display Direction

Liquid Crystal Driver Power Circuit

The built-in power circuits generate the voltage levels which are necessary to drive the liquid crystal. The built-in power system has voltage booster, voltage regulator and voltage follower circuits. Before power ST7598 is OFF, a Power OFF procedure is needed. Please refer to the OPERATION FLOW section.

Internal Analog Power Circuits and External Connection

The maximum external components are 13 capacitors. The detailed values of these capacitors are determined by panel size and panel loading. By increasing internal schottky diodes, 2 external schottky diodes are reserved for heavy loading.

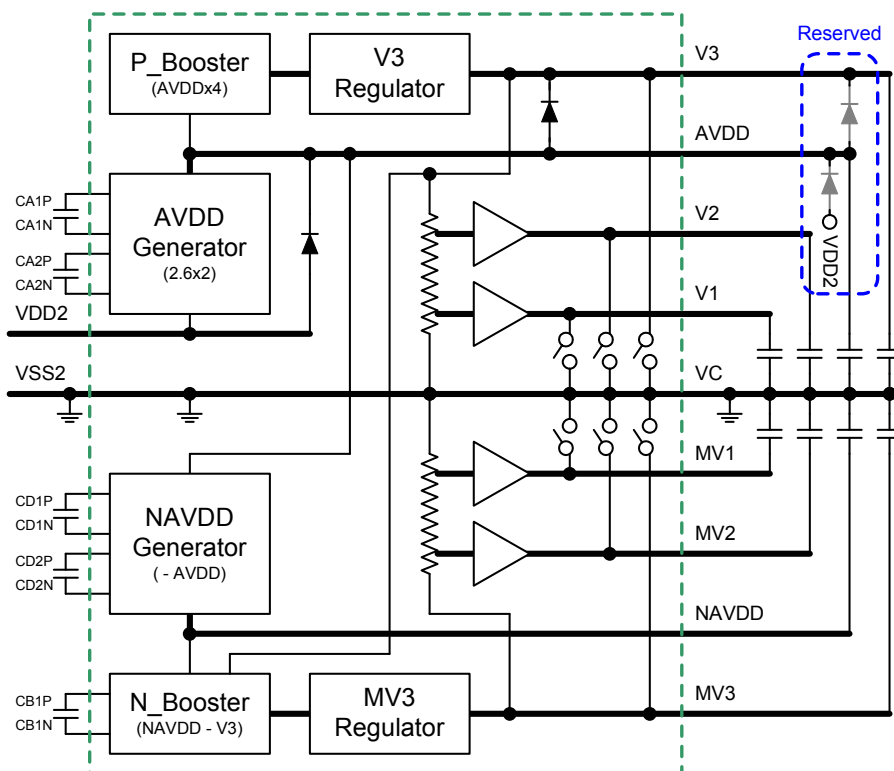
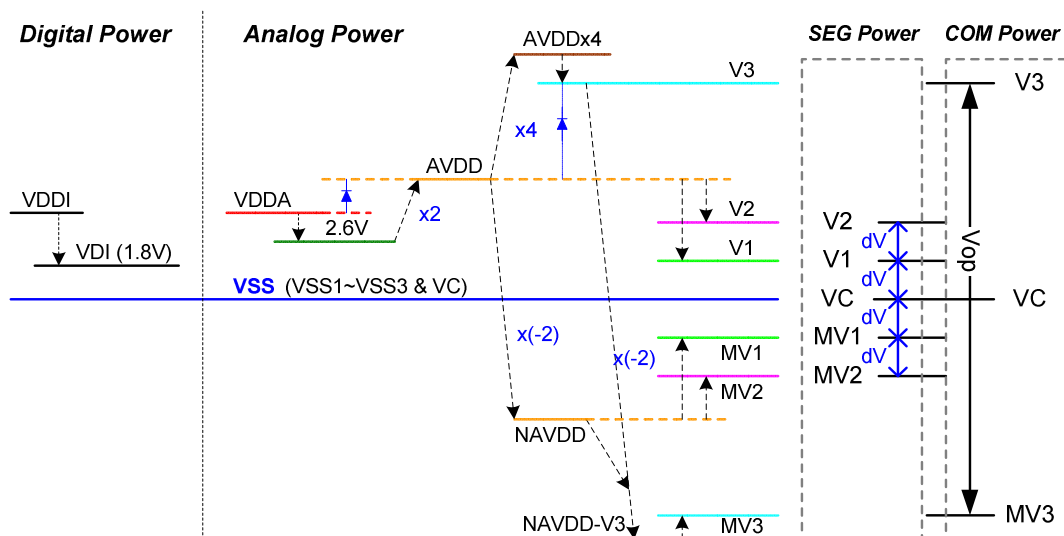


Fig. 11 Internal Power Circuits & External Connection

The relationship of internal power circuits is shown below.



V3/MV3 Voltage Regulator

The built-in regulator regulates a stable voltage V3 and MV3. The voltage level of V3/MV3 can be programmed by software instruction. Besides software instruction, ST7598 also provide extra function to adjust the voltage level of V3/MV3, such as Voltage Offset and Temperature Component. The voltage level of V3/MV3 is controlled through the parameters of EV[7:0] and VOF[7:0]. EV[7:0] is set by software instruction and the VOF[7:0] is downloaded from PROM.

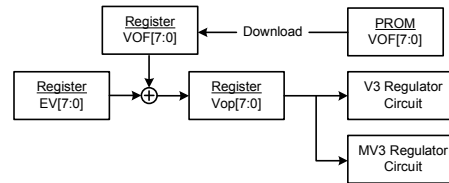


Fig. 12 V3/MV3 Generation

The V3/MV3 calculation formula is shown below. The default value of VOF[7:0] is 00h that download from PROM.

$$Vop[7:0] = EV[7:0] + VOF[7:0]$$

$$V3 = 6.0 + 0.02 \times Vop[7:0] = 6.0 + 0.02 \times (EV[7:0] + VOF[7:0])$$

$$MV3 = -6.0 - 0.02 \times Vop[7:0] = -6.0 - 0.02 \times (EV[7:0] + VOF[7:0])$$

$$LCD\ Vop = V3 - MV3$$

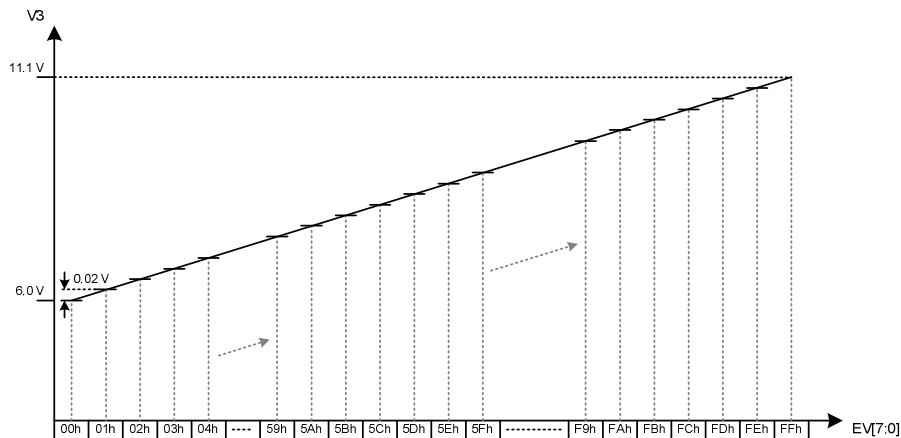


Fig. 13 V3 Programmable Range

The maximum voltage level of V3 or minimum voltage level of MV3 that can be generated is dependent on the VDD2 voltage and the loading of LCD module. VOF[7:0] is 2's complement, so that VOF[7:0] can increase or decrease V3 and MV3 respectively. The value of Vop[8:0] will return to 000h while the value of Vop[8:0] add one step (+1) is over 1FFh.

VOF7	VOF6	VOF5	VOF4	VOF3	VOF2	VOF1	VOF0	V3 Offset	MV3 Offset	Vop Offset
0	1	1	1	1	1	1	1	+2540 mV	-2540 mV	+5080 mV
	1	1	1	1	1	1	0	+2520 mV	-2520 mV	+5040 mV
	:	:	:	:	:	:	:	:	:	:
	0	0	0	0	0	1	0	+40 mV	-40 mV	+80 mV
	0	0	0	0	0	0	1	+20 mV	-20 mV	+40 mV
	0	0	0	0	0	0	0	0 mV	0mV	0 mV
1	1	1	1	1	1	1	1	-20 mV	+20 mV	-40 mV
	1	1	1	1	1	1	0	-40 mV	+40 mV	-80 mV
	:	:	:	:	:	:	:	:	:	:
	0	0	0	0	0	0	1	-2540 mV	+2540 mV	-5080 mV
	0	0	0	0	0	0	0	-2560 mV	+2560 mV	-5120 mV

BIAS Voltage Follower

The internal bias ratio resistors divide V3 and MV3 into four reference levels for V2, V1, MV1 and MV2. The BIAS Voltage Follower generates V2, V1, MV1 and MV2 according to these four reference levels. This circuit is operated in AVDD and NAVDD voltage system as the power source. The idea BIAS ratio is shown in below formula:

$$\text{Idea BIAS ratio: } \text{BIAS} = (\text{Duty})^{0.5}$$

The available range for V2, V1, MV1 and MV2 is shown in below table.

Symbol	Available Range
V2	$2.0V < V2 < AVDD - 0.7V$
V1	$1.0V < V1 < V2$
MV1	$MV2 < MV1 < -1.0V$
MV2	$NAVDD + 0.7V < MV2 < -2.0V$

The bias ratio and available V3, MV3 and Vop are shown in below table.

BIAS	Available V3 Range	Available MV3 Range	Available Vop Range
1/6	6.0V ~ 6.45V	-6.45V ~ -6.0V	12.0V ~ 12.9V
1/7	6.0V ~ 7.525V	-7.525V ~ -6.0V	12.0V ~ 15.05V
1/8	6.0V ~ 8.6V	-8.6V ~ -6.0V	12.0V ~ 17.2V
1/9	6.0V ~ 9.675V	-9.675V ~ -6.0V	12.0V ~ 19.35V
1/10	6.0V ~ 10.75V	-10.75V ~ -6.0V	12.0V ~ 21.5V
1/11	6.0V ~ 11.1V	-11.1V ~ -6.0V	12.0V ~ 22.2V
1/12	6.0V ~ 11.1V	-11.1V ~ -6.0V	12.0V ~ 22.2V
1/13	6.5V ~ 11.1V	-11.1V ~ -6.5V	13.0V ~ 22.2V

Note:

1. The maximum voltage level of V3 or minimum voltage level of MV3 that can be generated is dependent on the VDD2 voltage and the loading of LCD module.
2. The upper limit of the available Vop is absolutely voltage level without consider temperature compensation for V3 and MV3. The voltage level of Vop must be within "Available Vop Range" after considering temperature compensation for V3 and MV3.

For example, if we reserved -1V ~ +2.2V (Vop) for temperature compensation, the recommended power parameters are:

BIAS	Available V3 Range	Available MV3 Range	Available Vop Range
1/6 ~ 1/7			
1/8	6.5V ~ 7.5V	-7.5V ~ -6.5V	13V ~ 15V
1/9	6.5V ~ 8.575V	-8.575V ~ -6.5V	13V ~ 17.15V
1/10	6.5V ~ 9.65V	-9.65V ~ -6.5V	13V ~ 19.3V
1/11	6.5V ~ 10V	-10V ~ -6.5V	13V ~ 20V
1/12	6.5V ~ 10V	-10V ~ -6.5V	13V ~ 20V
1/13	7.0V ~ 10V	-10V ~ -7.0V	14V ~ 20V

Power System Setup

The power system of ST7598 can be constructed in different ways. The power system can use internal power circuits or external positive level power supplies. The combination of the internal power circuits or external positive level power supplies is also allowed. The power supplies of negative voltage level for negative power system are disallowed. The following table describes how to use the power system (internal or external). Be sure both of the hardware connection and software setting must be correct.

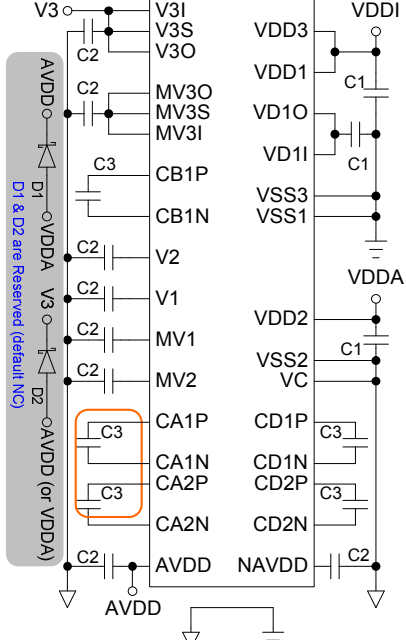
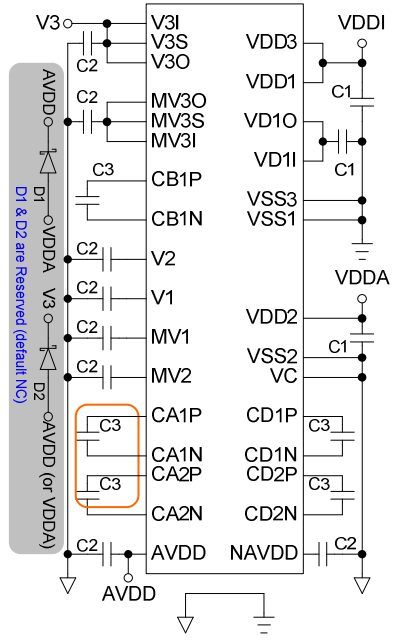
Software Setting for Power Control						Hardware Setting
VAD	V3	VPF	VMV3	VNAD	VNF	
1	-	-	-	-	-	<u>Internal AVDD</u> 1. Connect booster capacitor between CA1P and CA1N. 2. Connect booster capacitor between CA2P and CA2N. 3. Connect storage capacitor between AVDD and VSS2.
0	-	-	-	-	-	<u>External AVDD</u> 1. Connect storage capacitor between AVDD and VSS2. 2. Apply external voltage level to AVDD.
-	1	-	-	-	-	<u>Internal V3</u> 1. Connect storage capacitor between V3 and VSS2.
-	0	-	-	-	-	<u>External V3</u> 1. Connect storage capacitor between V3 and VSS2. 2. Apply external voltage level to V3.
-	-	1	-	-	-	<u>Internal Positive Follower</u> 1. Connect storage capacitor between V2 and VSS2. 2. Connect storage capacitor between V1 and VSS2.
-	-	0	-	-	-	<u>External Positive Follower</u> 1. Connect storage capacitor between V2 and VSS2. 2. Connect storage capacitor between V1 and VSS2. 3. Apply external voltage levels to V2 and V1.
-	-	-	1	1	1	<u>Internal NAVDD, MV3 and Negative Follower</u> 1. Connect booster capacitor between CD1P and CD1N. 2. Connect booster capacitor between CD2P and CD2N. 3. Connect storage capacitor between NAVDD and VSS2. 4. Connect booster capacitor between CB1P and CB1N. 5. Connect storage capacitor between MV3 and VSS2. 6. Connect storage capacitor between MV2 and VSS2. 7. Connect storage capacitor between MV1 and VSS2.

Note:

- Whether power on or power off sequence must according to section of System Power ON or Power OFF to avoid abnormal phenomenon.

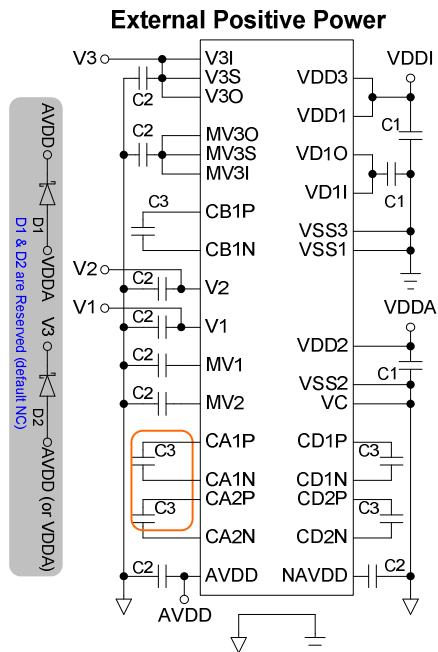
The following figures illustrate the connection of typical power applications.

Case 1: All Internal LCD Power Circuits

[Hardware Connection]	[Hardware Connection]
All Internal Powers 	External Regulator 
[Software Setting] Power Control: V3=VPF=VMV3=VNAD=VNF=1 [Optional Setting] - External AVDD: VAD=0 Remove 2 CAPs at CA1P/N, CA2P/N (recommend for 5V system) - Internal AVDD: VAD=1 Connect 2 CAPs at CA1P/N, CA2P/N (recommend for 3.3V system) [Related Features] <u>Contrast Control</u>: Software Control <u>Vop Adjustment</u>: Adjust by Internal PROM <u>BIAS Control</u>: Software Control <u>Vop Temperature Compensation</u>: Software Defined <u>fFR Temperature Compensation</u>: Software Defined <u>The Schottky diodes (D1 & D2) are reserved.</u>	[Software Setting] Power Control: V3=0, VPF=VMV3=VNAD=VNF=1 [Optional Setting] - External AVDD: VAD=0 Remove 2 CAPs at CA1P/N, CA2P/N (recommend for 5V system) - Internal AVDD: VAD=1 Connect 2 CAPs at CA1P/N, CA2P/N (recommend for 3.3V system) [Related Features] <u>Contrast Control</u>: External Circuit <u>Vop Adjustment</u>: External Circuit <u>BIAS Control</u>: Software Control <u>Vop Temperature Compensation</u>: External Circuit <u>fFR Temperature Compensation</u>: Software Defined <u>The Schottky diodes (D1 & D2) are reserved.</u>
➤ The Schottky diode is used to isolate the AVDD noise and it also keeps AVDD power quality.	➤ The Schottky diode is used to isolate the AVDD noise and it also keeps AVDD power quality.

Case 3: External Regulator & Follower (V3 & VPF)

[Hardware Connection]



[Software Setting]

Power Control: V3=VPF=0, VMV3=VNAD=VNF=1

[Optional Setting]

- External AVDD: VAD=0
Remove 2 CAPs at CA1P/N, CA2P/N
(recommend for 5V system)
- Internal AVDD: VAD=1
Connect 2 CAPs at CA1P/N, CA2P/N
(recommend for 3.3V system)

[Related Features]

Contrast Control: External Circuit

Vop Adjustment: External Circuit

BIAS Control: External Circuit (Fixed)

Vop Temperature Compensation: External Circuit

fFR Temperature Compensation: Software Defined

The Schottky diodes (D1 & D2) are reserved.

This case uses only external positive power circuits.

- The Schottky diode is used to isolate the AVDD noise and it also keeps AVDD power quality.

External Components of Power Circuit

The optimum values of C1, C2 and C3 depend on the loading of LCD panel. The value should be determined by customer. When determining the capacitor value, customer can display a pattern with large loading and than check if the capacitor makes the voltage stable or not. The following table is a quick reference for the initial setting.

Symbol	Type	Reference Value (uF)
C1	Capacitor for supply voltage regulation	0.1 ~ 4.7
C2	Capacitor for LCD voltage stabilization	1.0 ~ 4.7
C3	Capacitor for booster	1.0 ~ 4.7

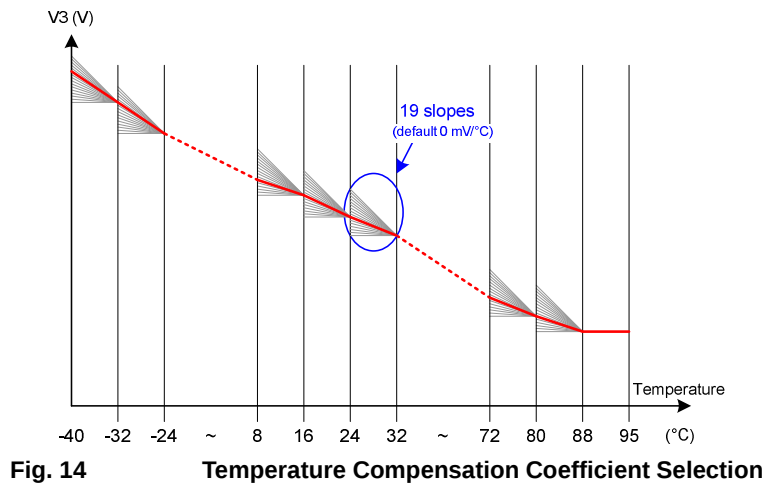
Note:

1. Please place all these capacitors close to the related pin of IC.
2. If the LCD panel is large or the ITO resistance is not good, the capacitor value maybe larger than the reference value. If the value is more than 10uF, customer should consider the following suggestion.
3. When the LCD panel size is large and desired display quality is unavailable by increasing the value of capacitor, it is recommended to use the LCD related power externally.
4. The acceptable voltage level of each capacitor as shown in Application Circuit.

Temperature Gradient Selection Circuit

Set V3 with Temperature Compensation (Temperature ≠ 24°C)

There are 19-line slopes in each temperature step, and customer can select one line slope of temperature compensation coefficient for each temperature step. Each temperature step is 8°C. Please see Fig. 14 as below.



The temperature compensation circuit includes negative and positive temperature gradient slope coefficient. If the temperature gradient slope coefficient is negative (FMTx=0), the available gradient Mx is 0mV/°C, -5mV/°C, -10mV/°C, ... and -75mV/°C. The parameter (MTx) of Temperature Gradient Set instruction (where x=0, 1, 2, ..., E, F) has a setting value between 0 and 15. MTx=0 results in Mx=0mV/°C increment on V3, MTx=1 results in Mx=-5mV/°C increment, ..., MTx=15 results in Mx=-15x5mV/°C increment. If the temperature gradient slope coefficient is positive (FMTx=1), the available gradient Mx is 0mV/°C, 5mV/°C, 10mV/°C and 15mV/°C. The parameter (MTx) of Temperature Gradient Set instruction (where x=0, 1, 2, ..., E, F) has a setting value between 0 and 3. MTx=0 results in Mx=0mV/°C increment on V3, MTx=1 results in Mx=5mV/°C increment, MTx=2 results in Mx=10mV/°C increment and MTx=3 results in Mx=15mV/°C increment.

Note that each MTx individually corresponds to a temperature interval; the Mx means temperature gradient slope coefficient. The relations between Mx and V3 quantity due to temperature V3(T) are described in the equation shown in Table 3.

Temperature Range	V3(T) Equation (Ta=T°C)	Simplified V3(T) Equation
-40°C ≤ T < -32°C	$V3(T) = V3(Tn32) - (-32-T) * M0$	$= V3(T24) - 8 * (M7+M6+M5+M4+M3+M2+M1) - (-32-T) * M0$
-32°C ≤ T < -24°C	$V3(T) = V3(Tn24) - (-24-T) * M1$	$= V3(T24) - 8 * (M7+M6+M5+M4+M3+M2) - (-24-T) * M1$
-24°C ≤ T < -16°C	$V3(T) = V3(Tn16) - (-16-T) * M2$	$= V3(T24) - 8 * (M7+M6+M5+M4+M3) - (-16-T) * M2$
-16°C ≤ T < -8°C	$V3(T) = V3(Tn8) - (-8-T) * M3$	$= V3(T24) - 8 * (M7+M6+M5+M4) - (-8-T) * M3$
-8°C ≤ T < 0°C	$V3(T) = V3(T0) - (0-T) * M4$	$= V3(T24) - 8 * (M7+M6+M5) - (0-T) * M4$
0°C ≤ T < 8°C	$V3(T) = V3(T8) - (8-T) * M5$	$= V3(T24) - 8 * (M7+M6) - (8-T) * M5$
8°C ≤ T < 16°C	$V3(T) = V3(T16) - (16-T) * M6$	$= V3(T24) - 8 * M7 - (16-T) * M6$
16°C ≤ T < 24°C	$V3(T) = V3(T24) - (24-T) * M7$	$= V3(T24) - (24-T) * M7$
24°C ≤ T < 32°C	$V3(T) = V3(T24) + (T-24) * M8$	$= V3(T24) + (T-24) * M8$
32°C ≤ T < 40°C	$V3(T) = V3(T32) + (T-32) * M9$	$= V3(T24) + 8 * M8 + (T-32) * M9$
40°C ≤ T < 48°C	$V3(T) = V3(T40) + (T-40) * MA$	$= V3(T24) + 8 * (M8+M9) + (T-40) * MA$
48°C ≤ T < 56°C	$V3(T) = V3(T48) + (T-48) * MB$	$= V3(T24) + 8 * (M8+M9+MA) + (T-48) * MB$
56°C ≤ T < 64°C	$V3(T) = V3(T56) + (T-56) * MC$	$= V3(T24) + 8 * (M8+M9+MA+MB) + (T-56) * MC$
64°C ≤ T < 72°C	$V3(T) = V3(T64) + (T-64) * MD$	$= V3(T24) + 8 * (M8+M9+MA+MB+MC) + (T-64) * MD$
72°C ≤ T < 80°C	$V3(T) = V3(T72) + (T-72) * ME$	$= V3(T24) + 8 * (M8+M9+MA+MB+MC+MD) + (T-72) * ME$
80°C ≤ T < 88°C	$V3(T) = V3(T80) + (T-80) * MF$	$= V3(T24) + 8 * (M8+M9+MA+MB+MC+MD+ME) + (T-80) * MF$
88°C ≤ T < 95°C	$V3(T) = V3(T88)$	$= V3(T24) + 8 * (M8+M9+MA+MB+MC+MD+ME+MF)$

* Mn (M[0:F]) refers to the slope of each Vop curve, which is the combination of MTx and FMTx (don't forget +/-).

Table 3

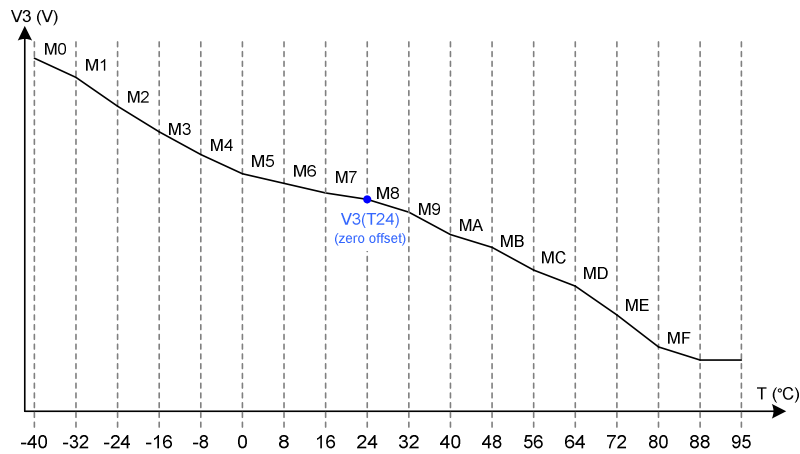


Fig. 15 Temperature Gradient Compensation

Note:

- Please make sure to avoid any kind of heating source near ST7598 such as back light, to prevent V3 is not anticipative because of temperature compensation circuit is working.

For example, $V_{op}=18.6V$, $TC=-15mV/^{\circ}C$, the V3 (Vop) in 8~39 $^{\circ}C$ are listed below:

Range (Mx)	Parameter (MTn)	Flag (FMTn)	Slope (mV/ $^{\circ}C$)	Ta ($^{\circ}C$)	V3 (V)	Vop (V)
⋮	⋮	⋮	⋮	⋮	⋮	⋮
M6	3	0	-15	8	9.540	19.08
				9	9.525	19.05
				10	9.510	19.02
				11	9.495	18.99
				12	9.480	18.96
				13	9.465	18.93
				14	9.450	18.90
				15	9.435	18.87
M7	3	0	-15	16	9.420	18.84
				17	9.405	18.81
				18	9.390	18.78
				19	9.375	18.75
				20	9.360	18.72
				21	9.345	18.69
				22	9.330	18.66
				23	9.315	18.63
M8	3	0	-15	24	9.300	18.60
				25	9.285	18.57
				26	9.270	18.54
				27	9.255	18.51
				28	9.240	18.48
				29	9.225	18.45
				30	9.210	18.42
				31	9.195	18.39
M9	3	0	-15	32	9.180	18.36
				33	9.165	18.33
				34	9.150	18.30
				35	9.135	18.27
				36	9.120	18.24
				37	9.105	18.21
				38	9.090	18.18
				39	9.075	18.15
⋮	⋮	⋮	⋮	⋮	⋮	⋮

Frequency Temperature Gradient Compensation Coefficient

ST7598 will auto-switch frame rate in different temperature such as Fig. 16. TA, TB and TC are frame rate switching temperature which can be defined by customer with instruction Set Frequency Compensation Temperature Range. FRA, FRB, FRC and FRD are switched frame rate which also can be defined by customer with instruction Operation Clock Frequency Select. The temperature hysteresis "THF" in the Fig. 16 that defines the sensitivity of internal temperature sensor and the value can be altered by instruction Temperature Hysteresis Value Set.

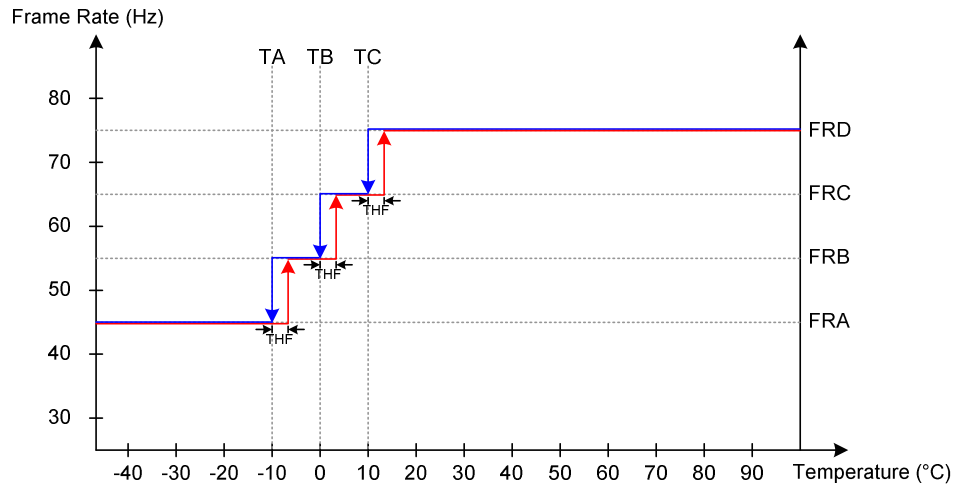


Fig. 16 Frame Rate

RESET CIRCUIT

Setting RSTB pin to "L" (hardware reset) can initialize internal function. Generally, VDD1 is not stable at the time that the system power is just turned ON. The hardware reset is required to initialize internal registers after VDD1 is stable. Initialization by RSTB pin is essential before operating. The default values of registers are listed below:

Procedure	After Hardware Reset
Content of DDRAM	No Change
Display ON/OFF	Display OFF
Display Inverse	Normal
Display All Pixel ON	Normal
COM Scan Direction	COM0→COM87
Page Address	Y[3:0]=00h
Column Address	X[8:0]=00h
Display Data Input/Output Direction	Column Direction
Column Address Direction	COL-0→COL-343
N-Line Inversion	NL[4:0]=00h
N-Line Inversion ON/FF	OFF
Read Modify Write	Disable
Built-in Oscillator Circuit ON/OFF	OFF
Power Control	All Power OFF
Booster Level	Booster Level1
BIAS	BS[2:0]=00h
Electronic Volume	EV[7:0]=00h
Power Discharge	All Discharge OFF
Power Save	Non-Standby Mode (Normal Mode)
Temperature Gradient Compensation	MTx[3:0]=00h
Temperature Gradient Compensation Flag	FMTx=00h
Temperature Detection	OFF
LCD Driving Method	NLFR=1
Frequency Compensation Temperature Range	Tx[6:0]=00h
Temperature Hysteresis Value	THV[3:0]=04h, THF[3:0]=02h
Test	Disable

Table 4

INSTRUCTION TABLE

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Display ON/OFF	0	0	1	0	1	0	1	1	1	D	Set LCD display mode D=0: display off D=1: display on
Display Inverse	0	0	1	0	1	0	0	1	1	INV	Set inverse display mode INV=0: normal display INV=1: inverse display
Display All Pixel ON	0	0	1	0	1	0	0	1	0	AP	Set all pixel on mode AP=0: normal display AP=1: all pixel on
COM Scan Direction	0	0	1	1	0	0	0	1	0	0	MY=0: COM0→COM87
	1	0	0	0	0	0	0	0	1	MY	MY=1: COM87→COM0
Page Address	0	0	1	0	1	1	0	0	0	1	Set the page address of DDRAM
	1	0	0	0	0	0	Y3	Y2	Y1	Y0	
Column Address	0	0	0	0	0	1	0	0	1	1	Set the column address of DDRAM
	1	0	-	-	-	-	-	-	-	X8	
	1	0	X7	X6	X5	X4	X3	X2	X1	X0	
Display Data Write	0	0	0	0	0	1	1	1	0	1	Write display data to DDRAM
	1	0	D7	D6	D5	D4	D3	D2	D1	D0	
Display Data Read	0	0	0	0	0	1	1	1	0	0	Read display data from DDRAM
	1	1	D7	D6	D5	D4	D3	D2	D1	D0	
Display Data Input/Output Direction	0	0	1	0	0	0	0	1	0	DIR	Set DDRAM data input direction DIR=0: column direction DIR=1 : page direction
Column Address Direction	0	0	1	0	1	0	0	0	0	MX	Set column addressing direction MX=0: COL-0→COL-343 MX=1: COL-343→COL-0
N-Line Inversion	0	0	0	0	1	1	0	1	1	0	Set N-Line inversion
	1	0	0	0	0	NL4	NL3	NL2	NL1	NL0	
N-Line Inversion ON/OFF	0	0	1	1	1	0	0	1	0	NL	Set N-Line inversion mode NL=0: N-Line inversion off NL=1: N-Line inversion on
Enable DDRAM	0	0	0	1	1	0	1	1	0	1	Enable DDRAM 1/88 Duty: ED[7:0]=15h ED[15:8]=0Ch 1/72 Duty: ED[7:0]=11h ED[15:8]=0Eh 1/64 Duty: ED[7:0]=0Fh ED[15:8]=0Fh
	1	0	ED[7:0]								
	1	0	ED[15:8]								
Read Modify Write	0	0	1	1	1	0	0	0	0	0	Enable Read Modify Write mode
Read Modify Write End	0	0	1	1	1	0	1	1	1	0	Disable Read Modify Write mode
Built-in Oscillator Circuit ON/OFF	0	0	1	0	1	0	1	0	1	OSC	Set built-in oscillator mode OSC=0: built-in oscillator off OSC=1: built-in oscillator on

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Operation Clock Frequency	0	0	0	1	0	1	1	1	1	1	Set frame rate in different temperature range
	1	0	FRB3	FRB2	FRB1	FRB0	FRA3	FRA2	FRA1	FRA0	
	1	0	FRD3	FRD2	FRD1	FRD0	FRC3	FRC2	FRC1	FRC0	
Power Control	0	0	0	0	1	0	0	1	0	1	Set built-in power circuits on/off
	1	0	-	-	VAD	V3	VPF	VMV3	VNAD	VNF	
Booster Level	0	0	0	0	1	0	1	0	1	1	Set the level of built-in booster circuit
	1	0	-	-	-	-	-	-	0	BL	
BIAS	0	0	1	0	1	0	0	0	1	0	Set the bias ratio of liquid crystal driving voltage
	1	0	0	0	0	0	0	BS2	BS1	BS0	
Electronic Volume	0	0	1	0	0	0	0	0	0	1	Set the V3 level for liquid crystal driving voltage
	1	0	EV7	EV6	EV5	EV4	EV3	EV2	EV1	EV0	
	1	0	0	0	0	0	0	0	0	0	
Power Discharge	0	0	1	1	1	0	1	0	1	0	Set power circuits discharge
	1	0	-	-	-	-	DV3	DVPF	DVNF	DVMV3	
Power Save	0	0	1	0	1	0	1	0	0	PD	Set power save mode PD=0 : normal mode PD=1 : standby mode
Temperature Gradient Compensation	0	0	0	1	0	0	1	1	1	0	Set temperature gradient compensation coefficient
	1	0	MT1[3 :0]				MT0[3 :0]				
	1	0	MT3[3 :0]				MT2[3 :0]				
	1	0	MT5[3 :0]				MT4[3 :0]				
	1	0	MT7[3 :0]				MT6[3 :0]				
	1	0	MT9[3 :0]				MT8[3 :0]				
	1	0	MTB[3 :0]				MTA[3 :0]				
	1	0	MTD[3 :0]				MTC[3 :0]				
	1	0	MTF[3 :0]				MTE[3 :0]				
Temperature Gradient Compensation Flag	0	0	0	0	1	1	1	0	0	1	Set the slope of temperature gradient is positive or negative
	1	0	FMT7	FMT6	FMT5	FMT4	FMT3	FMT2	FMT1	FMT0	
	1	0	FMTF	FMTE	FMTD	FMTC	FMTB	FMTA	FMT9	FMT8	
Read Status	0	0	1	0	0	0	1	1	1	0	Read IC status
	1	1	D	OSC	AVD	V3	VPF	VMV3	VNAD	VNF	
	1	1	DISV	-	MY	PD	TD	NLFR	-	-	
Temperature Detection	0	0	0	1	1	0	1	0	0	TD	Set temperature detection mode TD=0: disable mode TD=1: enable mode
LCD Driving Method	0	0	1	1	1	0	0	1	1	1	Set LCD driving method
	1	0	-	-	-	NLFR	1	-	-	1	
NOP	0	0	1	1	1	0	0	0	1	1	No operation
Frequency Compensation Temperature Range	0	0	1	1	1	0	1	1	0	0	Set temperature range for frequency compensation
	1	0	-	TA6	TA5	TA4	TA3	TA2	TA1	TA0	
	1	0	-	TB6	TB5	TB4	TB3	TB2	TB1	TB0	
	1	0	-	TC6	TC5	TC4	TC3	TC2	TC1	TC0	

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Temperature Hysteresis Value	0	0	1	1	1	0	1	1	0	1	Set temperature hysteresis value
	1	0	-	-	0	0	THV3	THV2	THV1	THV0	
	1	0	-	-	-	-	THF3	THF2	THF1	THD0	
Current Temperature	0	0	1	1	1	0	1	1	1	1	Monitor current temperature
	1	1	T7	T6	T5	T4	T3	T2	T1	T0	
Test	0	0	1	1	1	1	1	1	TE	T	Set test command mode TE=0 : normal command mode TE=1 : test command mode T : select test command mode

INSTRUCTION DESCRIPTION

Display ON/OFF

This instruction turns the display ON or OFF. When ST7598 enters display off, the display output is blank regardless of the content of DDRAM. When ST7598 enters display on (exit display off), the display output is according to content of DDRAM.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	1	1	1	D	D=0: Display off (Default) D=1: Display on

Display Inverse

This instruction would inverse the scanned data without recover the content of DDRAM. As the result, the ON and OFF status of all pixels are interchanged.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	0	1	1	INV	INV=0: Normal display (Default) INV=1: Inverse display

Display All Pixel ON

When ST7598 enters all pixels on mode, all display pixels are turned on regardless of the content of DDRAM. The content of DDRAM is not changed by setting Display All Pixel ON.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	0	1	0	AP	AP=0: Normal display (Default) AP=1: All pixel on

COM Scan Direction

This instruction defines the COM direction of scan read from DDRAM.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	0	0	0	1	0	0	MY=0: COM0→COM87 MY=1: COM87→COM0
1	0	0	0	0	0	0	0	1	MY	

Note: “-” is disable bit. It can be either logic 0 or 1.

Page Address

This instruction defines the page address corresponding to line address of DDRAM when MCU access to the DDRAM shown in Fig. 10. The detail description is showed in the section of Page Address Circuit.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	1	0	0	0	1	Y[3:0]=0h~Ah
1	0	0	0	0	0	Y3	Y2	Y1	Y0	

Note: “-” is disable bit. It can be either logic 0 or 1.

Y3	Y2	Y1	Y0	Page Address
0	0	0	0	Page 0
0	0	0	1	Page 1
0	0	1	0	Page 2
:	:	:	:	:
1	0	0	0	Page 8
1	0	0	1	Page 9
1	0	1	0	Page 10

Column Address

This instruction defines the column address of DDRAM. The detail description is showed in the section of Column Address Circuit.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	0	1	0	0	1	1	X[8:0]=00h~157h
1	0	-	-	-	-	-	-	-	X8	
1	0	X7	X6	X5	X4	X3	X2	X1	X0	

Note: “-” is disable bit. It can be either logic 0 or 1.

X8	X7	X6	X5	X4	X3	X2	X1	X0	Column Address
0	0	0	0	0	0	0	0	0	Column 0
0	0	0	0	0	0	0	0	1	Column 1
0	0	0	0	0	0	0	1	0	Column 2
:	:	:	:	:	:	:	:	:	:
1	0	1	0	1	0	1	0	1	Column 341
1	0	1	0	1	0	1	1	0	Column 342
1	0	1	0	1	0	1	1	1	Column 343

Display Data Write

This instruction is used to transfer data from MCU to DDRAM without changing status of ST7598. The page address and column address will be reset to customer setting when this instruction is accepted. The pre-instruction is defined to enter write DDRAM mode. The following continuously data means content of DDRAM without pre-instruction. After each access, column address counter or page address counter is automatically increased by one (+1). The increment method of page address counter or column address counter is depending on instruction Display Data Input Direction. Display Data Write would be stopped when any other instruction is accepted.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	0	1	1	1	0	1	
1	0	D7	D6	D5	D4	D3	D2	D1	D0	

Display Data Read

The instruction is used to transfer data from DDRAM to MCU without changing status of ST7598. The page address and column address will be reset to customer setting when this instruction is accepted. The pre-instruction is defined to enter read DDRAM mode. The following continuously data means content of DDRAM without pre-instruction. After each access, column address counter or page address counter is automatically increased by one (+1). The increment method of page address counter or column address counter is depending on instruction Display Data Input Direction. Read Display Data would be stopped when any other instruction is accepted. Read Display Data is only available via the parallel interface.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	0	1	1	1	0	0	
1	1	D7	D6	D5	D4	D3	D2	D1	D0	

Display Data Input/Output Direction

This instruction defines the direction where the address counter of DDRAM is automatically increment. The detail description is showed in the section of Addressing.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	0	0	1	0	DIR	DIR=0 : Column direction (Default) DIR=1 : Page direction

Column Address Direction

This instruction defines the addressing direction of column address as shown in Fig. 10.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	0	0	0	MX	MX=0: COL-0→COL-343 (Default) MX=1: COL-343→COL-0

N-Line Inversion

This instruction defines the liquid crystal alternating line number which alters the driving signal phase (in 4-line basis).

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	1	0	1	1	0	NL[4:0]=00h~14h
1	0	0	0-	0	NL4	NL3	NL2	NL1	NL0	

Note: “-” is disable bit. It can be either logic 0 or 1.

The relationship between the parameter NL[4:0] and the number of inverted lines is shown below.

NL4	NL3	NL2	NL1	NL0	N-Line Inversion
0	0	0	0	0	8 (4x2)
0	0	0	0	1	8 (4x2)
0	0	0	1	0	12 (4x3)
:	:	:	:	:	:
1	0	0	1	0	76 (4x19)
1	0	0	1	1	80 (4x20)
1	0	1	0	0	84 (4x21)

N-Line Inversion ON/OFF

This instruction defines the function of N-Line inversion is disable or enable. If the N-Line inversion is turning off, the liquid crystal is alternated by frame inversion.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	0	1	0	NL	NL=0: N-Line inversion off (Default) NL=1: N-Line inversion on

Enable DDRAM

This instruction is used to initial DDRAM and DDRAM interface for write to DDRAM or read from DDRAM. This instruction should be set in the initial flow. ED[7:0] and ED[15:8] should be set according to different duty setting. The following table determines COM layouy sequence.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	1	0	1	1	0	1	Enable DDRAM
1	0	ED[7:0]								ED[7:0] : Set Display Duty
1	0	ED[15:8]								ED[15:8] : Select First COM Group

ED[7:0] is calculated according to the Display Duty.

Dusplay Duty	1/88	1/84	1/80	...	1/68	1/64	1/60	1/56	...	1/8	1/8
Scan Duty	1/88	1/84	1/80	...	1/68	Fix at 1/64					
Calculation	88/4-1	84/4-1	80/4-1	...	68/4-1	64/4-1	60/4-1	56/4-1	...	8/4-1	---
ED[7:0] (Hex)	15h	14h	13h	...	10h	0Fh	0Eh	0Dh	...	01h	00h

ED[15:8] is the ID of each COM output group. By assigning an ID into ED[15:8], the first scan COM group is selected.

ED[15:8] (Hex)		0Ch				0Dh				0Eh				0Fh				10h			
Group		1				2				3				4				5			
MY	0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
	1	87	86	85	84	83	82	81	80	79	78	77	76	75	74	73	72	71	70	69	68

11h				12h				13h				14h				15h				16h			
6				7				8				9				10				11			
20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43
67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44

17h				18h				19h				1Ah				1Bh				1Ch			
12				13				14				15				16				17			
44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67
43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20

1Dh				1Eh				1Fh				20h				21h			
18				19				20				21				22			
68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87
19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Read Modify Write

This instruction is used to enter Read Modify Write mode. When entering Read Modify Write mode, the display data read will not increase address counter. Only the display data write will increase the address counter. This mode is maintained until the instruction Read Modify Write End is accepted.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	0	0	0	0	

* Because the serial interfaces (SPI-4 and SPI-3) can't read display data, the Read-Modify-Write function is not available.

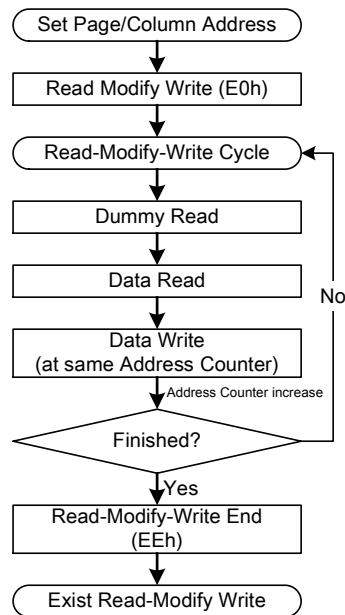


Fig. 17 Read Modify Write Flow

Read Modify Write End

This instruction is used to release the Read Modify Write mode. The page address and column address will return to initial address while the instruction Read Modify Write End is accepted.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	1	1	1	0	

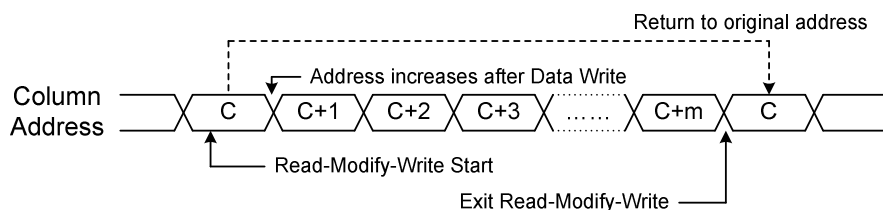


Fig. 18 Address Relationship of Read Modify Write

Built-in Oscillator Circuit ON/OFF

This instruction is used to turn on or off the built-in oscillator circuit. When the built-in power supply is used, the Built-in Oscillator Circuit ON must be executed before the instruction Power Control. If the built-in oscillator circuit is turned off while the built-in power supply is used, abnormal display may occur.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	1	0	1	OSC	OSC=0: Built-in oscillator off OSC=1: Built-in oscillator on

Operation Clock Frequency

This instruction defines the temperature compensation gradient of frequency which automatically adjusts the frame frequency according to the current temperature.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	0	1	1	1	1	1	FRA[3:0]: FR for -40℃~TA
1	0	FRB3	FRB2	FRB1	FRB0	FRA3	FRA2	FRA1	FRA0	FRB[3:0]: FR for TA~TB
1	0	FRD3	FRD2	FRD1	FRD0	FRC3	FRC2	FRC1	FRC0	FRC[3:0]: FR for TB~TC FRD[3:0]: FR for TC~95℃

This instruction is used to specify the divide-ratio of the internal operation clock (PWMCK) to the built-in oscillator frequency (fOSC). This instruction is enable only when built-in oscillator clock is turned on. If the built-in oscillator circuit is turned off, the external clock entered to CL pin is used as the internal operation clock. The below table shows the relation between the divide-ratio and the register value which is set by the parameter (FRx[3:0]). This table also illustrates the relation between the internal operation clock (PWMCK) and the display operation clock (fDCLK).

FRx[3:0]	DIV	PWMCK (kHz) fOSC/DIV	fDCLK (kHz) PWMCK/15	fFR (Hz)		
				88 Lines	72 Lines	64~8 Lines
0000	5	326.0	21.7	236	286	319
0001	6	271.7	18.1	197	238	266
0010	7	232.9	15.5	168	204	228
0011	8	203.8	13.6	148	179	200
0100	9	181.1	12.1	132	159	178
0101	10	163.0	10.9	118	143	160
0110	12	135.8	9.1	99	120	134
0111	14	116.4	7.8	85	103	115
1000	15	108.7	7.2	78	95	106
1001	16	101.9	6.8	74	89	100
1010	18	90.6	6.0	65	79	88
1011	20	81.5	5.4	59	71	79
1100	21	77.6	5.2	57	68	76
1101	24	67.9	4.5	49	59	66
1110	25	65.2	4.3	47	57	63
1111	28	58.2	3.9	42	51	57

Note:

fOSC: Oscillator frequency of the built-in oscillator circuit.

PWMCK: Internal operation clock. It is the basic clock used by the synchronous circuit of ST7598. PWMCK is obtained by dividing fOSC.

fDCLK: Display Operation Clock. It is used to specify a single duration in the sequential drive of liquid crystal. It constantly meets the relation of PWMCK/15 independent of the value of the operation clock frequency select command. The relationship will not change even when the external clock is used.

fFR: The frequency of Frame Rate.

Power Control

This instruction used to control the status of built-in power circuit.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	0	0	1	0	1	
1	0	-	-	VAD	V3	VPF	VMV3	VNAD	VNF	

Note: “-” is disable bit. It can be either logic 0 or 1.

ST7598 provides built-in power supply for LCD driving voltage. ST7598 allows using some part(s) of the built-in power circuit(s) with some external voltage(s). The following table shows how these circuits can be controlled through this command. The detail description of power circuit setup is showed in Power System Setup. The power on/off flow please refers to the sections of System Power ON and Power OFF to avoid abnormal display.

Flag	Status of Built-in Power Circuit
VAD	VAD=0: Built-in AVDD Booster Circuit OFF VAD=1: Built-in AVDD Booster Circuit ON
V3	V3=0: Built-in V3 Regulator Circuit OFF V3=1: Built-in V3 Regulator Circuit ON
VPF	VPF=0: Built-in Positive Follower Circuit OFF VPF=1: Built-in Positive Follower Circuit ON
VMV3	VMV3=0: Built-in MV3 Regulator Circuit OFF VMV3=1: Built-in MV3 Regulator Circuit ON
VNAD	VNAD=0: Built-in NAVDD Booster Circuit OFF VNAD=1: Built-in NAVDD Booster Circuit ON
VNF	VNF=0: Built-in Negative Follower Circuit OFF VNF=1: Built-in Negative Follower Circuit ON

The internal clock is required to operate the built-in power supply circuit. During the operation of the built-in power supply circuit, be sure that the internal clock is present inside. If the built-in oscillator circuit is used, please execute the built-in oscillator circuit turning on before the power circuit turning on. If the external oscillator is used, must operate the external oscillator before the power circuit turning on. If the internal clock is cut off during the operation of the built-in power circuit, abnormal display mat occur.

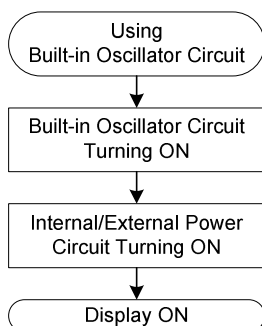


Fig. 19 Power Control (Using Built-in Oscillator)

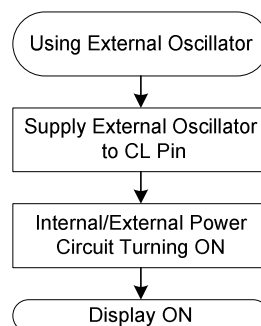


Fig. 20 Power Control (Using External Oscillator)

Booster Level

This instruction defines the booster level without change any hardware connection.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	0	1	0	1	1	BL=0: Booster Level 1
1	0	-	-	-	-	-	-	0	BL	BL=1: Reserved for testing

Note: “-” is disable bit. It can be either logic 0 or 1.

BIAS

This instruction defines the bias ratio of voltage requirement for liquid crystal.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	0	0	1	0	
1	0	0	0	0	0	0	BS2	BS1	BS0	

Note: “-” is disable bit. It can be either logic 0 or 1.

The relationship between the parameter BS[2:0] and the bias ratio is shown below.

BS2	BS1	BS0	BIAS Ratio
0	0	0	1/6
0	0	1	1/7
0	1	0	1/8
0	1	1	1/9
1	0	0	1/10
1	0	1	1/11
1	1	0	1/12
1	1	1	1/13

The relationship between the bias ratio and the analog voltage level is shown below.

Symbol	Voltage Level
V3	$V3 = V_{op}/2$
V2	$V2 = 2 \times \text{BIAS} \times V_{op}$
V1	$V1 = \text{BIAS} \times V_{op}$
VC	$VC = V_{SS2}$
MV1	$MV1 = -\text{BIAS} \times V_{op}$
MV2	$MV2 = -2 \times \text{BIAS} \times V_{op}$
MV3	$MV3 = -V_{op}/2$

Note: The limitation of analog voltage is shown in section of BIAS Voltage Follower.

Electronic Volume

This instruction defines the liquid crystal driving voltage V3 that issued from built-in analog power circuit. The maximum voltage level of Vop that can be generated is dependent on the VDD2 voltage and the loading of LCD module. The detail description is showed in section of V3/MV3 Voltage Regulator.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	0	0	0	0	1	EV[7:0]=00h~FFh
1	0	EV7	EV6	EV5	EV4	EV3	EV2	EV1	EV0	
1	0	0	0	0	0	0	0	0	0	

Note: "-" is disable bit. It can be either logic 0 or 1.

The relationship between the parameter EV[7:0] and the voltage level of V3/MV3/Vop is shown below.

EV7	EV6	EV5	EV4	EV3	EV2	EV1	EV0	V3	MV3	Vop
0	0	0	0	0	0	0	0	6.00	-6.00	12
0	0	0	0	0	0	0	1	6.02	-6.02	12.04
0	0	0	0	0	0	1	0	6.04	-6.04	12.08
:	:	:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	0	11.04	-11.04	22.08
1	1	1	1	1	1	0	1	11.06	-11.06	22.12
1	1	1	1	1	1	1	0	11.08	-11.08	22.16
1	1	1	1	1	1	1	1	11.10	-11.10	22.20

Note: The formula of idea Vop is shown in section of V3/MV3 Voltage Regulator.

Power Discharge

This instruction used to discharge the capacitor connected to the analog power supply circuit. The discharge flow please refers to the section of Power OFF to avoid abnormal display.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	1	0	1	0	
1	0	-	-	-	-	DV3	DVPF	DVNF	DVMV3	

Flag	Status of Built-in Power Circuit
DV3	DV3=0: Disable discharge V3 DV3=1: Enable discharge V3
DVPF	DVPF=0: Disable discharge positive follower (V2 & V1) DVPF=1: Enable discharge positive follower (V2 & V1)
DVNF	DVNF=0: Disable discharge negative follower (MV1 & MV2) and NAVDD DVNF=1: Enable discharge negative follower (MV1 & MV2) and NAVDD
DVMV3	DVMV3=0: Disable discharge MV3 DVMV3=1: Enable discharge MV3

Note:

1. Do not discharge before related power is turned off while using internal power system.
2. Do not discharge before related power is turned off while using external power system.

Power Save

This instruction defines the status of chip is normal mode or standby mode. When ST7598 enters the standby mode, the mode causes the LCD module entering the minimum power consumption. Besides, the internal analog circuit will be turned off without discharge power and the display will turn off.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	1	0	0	PD	PD=0 : Normal mode PD=1 : Standby mode

Temperature Gradient Compensation

This instruction defines the temperature gradient compensation coefficient. Depend on the instruction of Temperature Gradient Compensation Flag, the temperature gradient slope can be set either positive or negative. The detail description is showed in the section of Temperature Gradient Selection Circuit.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	0	0	1	1	1	0	MTx[3:0]=0h~Fh (Negative TC) MTx[3:0]=0h~3h (Positive TC)
1	0	MT1[3:0]				MT0[3:0]				
1	0	MT3[3:0]				MT2[3:0]				
1	0	MT5[3:0]				MT4[3:0]				
1	0	MT7[3:0]				MT6[3:0]				
1	0	MT9[3:0]				MT8[3:0]				
1	0	MTB[3:0]				MTA[3:0]				
1	0	MTD[3:0]				MTC[3:0]				
1	0	MTF[3:0]				MTE[3:0]				

The related temperature range and available setting value of MTx[3:0] is shown below.

MTx Parameter	Temperature Range	Negative TC Value (for FMTx=0)	Positive TC Value (for FMTx=1)
MT0[3:0]	-40℃ ≤ T < -32℃	0h~Fh	0h~3h
MT1[3:0]	-32℃ ≤ T < -24℃	0h~Fh	0h~3h
MT2[3:0]	-24℃ ≤ T < -16℃	0h~Fh	0h~3h
MT3[3:0]	-16℃ ≤ T < -8℃	0h~Fh	0h~3h
MT4[3:0]	-8℃ ≤ T < 0℃	0h~Fh	0h~3h
MT5[3:0]	0℃ ≤ T < 8℃	0h~Fh	0h~3h
MT6[3:0]	8℃ ≤ T < 16℃	0h~Fh	0h~3h
MT7[3:0]	16℃ ≤ T < 24℃	0h~Fh	0h~3h
MT8[3:0]	24℃ ≤ T < 32℃	0h~Fh	0h~3h
MT9[3:0]	32℃ ≤ T < 40℃	0h~Fh	0h~3h
MTA[3:0]	40℃ ≤ T < 48℃	0h~Fh	0h~3h
MTB[3:0]	48℃ ≤ T < 56℃	0h~Fh	0h~3h
MTC[3:0]	56℃ ≤ T < 64℃	0h~Fh	0h~3h
MTD[3:0]	64℃ ≤ T < 72℃	0h~Fh	0h~3h
MTE[3:0]	72℃ ≤ T < 80℃	0h~Fh	0h~3h
MTF[3:0]	80℃ ≤ T < 88℃	0h~Fh	0h~3h

* The slope from 88℃ to 95℃ is 0mV/℃.

The relationship between the parameters FMTx/MTx[3:0] and the voltage level of V3/MV3/Vop is shown below. The FMTx is set by instruction of Temperature Gradient Compensation Flag.

FMTx	MTx3	MTx2	MTx1	MTx0	V3(mV/°C)	MV3(mV/°C)	Vop(mV/°C)
0	0	0	0	0	0	0	0
	0	0	0	1	-5	5	-10
	0	0	1	0	-10	10	-20
	0	0	1	1	-15	15	-30
	0	1	0	0	-20	20	-40
	0	1	0	1	-25	25	-50
	0	1	1	0	-30	30	-60
	0	1	1	1	-35	35	-70
	1	0	0	0	-40	40	-80
	1	0	0	1	-45	45	-90
	1	0	1	0	-50	50	-100
	1	0	1	1	-55	55	-110
	1	1	0	0	-60	60	-120
	1	1	0	1	-65	65	-130
	1	1	1	0	-70	70	-140
	1	1	1	1	-75	75	-150
1	0	0	0	0	0	0	0
	0	0	0	1	5	-5	10
	0	0	1	0	10	-10	20
	0	0	1	1	15	-15	30

Temperature Gradient Compensation Flag

This instruction defines the temperature gradient compensation coefficient is negative or positive temperature gradient compensation coefficient.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	1	1	0	0	1	FMTx=0: Negative TC FMTx=1: Positive TC
1	0	FMT7	FMT6	FMT5	FMT4	FMT3	FMT2	FMT1	FMT0	
1	0	FMTF	FMTE	FMTD	FMTC	FMTB	FMTA	FMT9	FMT8	

Read Status

This instruction can read out the status of ST7598.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	0	1	1	1	0	
1	1	D	OSC	AVD	V3	VPF	VMV3	VNAD	VNF	
1	1	DISV	-	MY	PD	TD	NLFR	-	-	

Note: “-” is disable bit. It can be either logic 0 or 1.

The relationship between the flag and the status of IC is shown below.

Flag	Function	0	1
D	Display ON/OFF	OFF	ON
OSC	Built-in OSC Circuit ON/OFF	OFF	ON
AVD	AVDD ON/OFF	OFF	ON
V3	V3 ON/OFF	OFF	ON
VPF	Positive Follower ON/OFF	OFF	ON
VMV3	MV3 ON/OFF	OFF	ON
VNAD	NAVDD ON/OFF	OFF	ON
VNF	Negative Follower ON/OFF	OFF	ON
DISV	Power Discharge ON/OFF	OFF	ON
MY	COM Output Direction	Normal	Reverse
PD	Power Save	Normal	Standby
TD	Temperature Detection ON/OFF	OFF	ON
NLFR	N-Line Inversion Reset by Frame ON/OFF	ON	OFF

Temperature Detection

This instruction defines the status of temperature detection. All temperature related functions will be disabled if TD=0. If temperature detection and compensation is not used, please set TD=0, MTn[3:0]=0 and FRA=FRB=FRC=FRD=0.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	1	0	1	0	0	TD	TD=0 : Disable mode TD=1 : Enable mode

LCD Driving Method

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	0	1	1	1	
1	0	-	-	-	NLFR	1	-	-	1	

Note: “-” is disable bit. It can be either logic 0 or 1.

Flag	Status
NLFR	NLFR=0: N-Line Inversion Reset by Frame Inversion ON NLFR=1: N-Line Inversion Reset by Frame Inversion OFF

The relationship between parameters (NL & NLFR) and COM output method is shown below.

A. 20 lines display without N-Line inversion (NL=0, NLFR=x)

COM	Positive Frame					Negative Frame				
COM[3:0]	+	+	+	+		-	-	-	-	
COM[7:4]		+	+	+	+		-	-	-	-
COM[11:8]			+	+	+	+		-	-	-
COM[15:12]				+	+	+	+		-	-
COM[19:16]					+	+	+	+		-

B. 12-Line inversion in 20 lines display without frame inversion (NL=1, NLFR=1)

COM	Positive Frame					Negative Frame				
COM[3:0]	+	+	+	+		-	-	-	-	
COM[7:4]		+	+	+	+		+	+	+	+
COM[11:8]			+	+	+	+		+	+	+
COM[15:12]				-	-	-			+	+
COM[19:16]					-	-	-			-

C. 8-Line inversion in 20 lines display without frame inversion (NL=1, NLFR=1)

COM	Positive Frame					Negative Frame				
COM[3:0]	+	+	+	+		+	+	+	+	
COM[7:4]		+	+	+	+		-	-	-	-
COM[11:8]			-	-	-			-	-	-
COM[15:12]				-	-	-			+	+
COM[19:16]					+	+	+	+		+

D. 12-Line inversion in 20 lines display with frame inversion (NL=1, NLFR=0)

COM	Positive Frame					Negative Frame				
COM[3:0]	+	+	+	+		-	-	-	-	
COM[7:4]		+	+	+	+		-	-	-	-
COM[11:8]			+	+	+			-	-	-
COM[15:12]				-	-	-			+	+
COM[19:16]					-	-	-			+

E. 8-Line inversion in 20 lines display with frame inversion (NL=1, NLFR=0)

COM	Positive Frame					Negative Frame				
COM[3:0]	+	+	+	+		-	-	-	-	
COM[7:4]		+	+	+	+		-	-	-	-
COM[11:8]			-	-	-			+	+	+
COM[15:12]				-	-	-			+	+
COM[19:16]					+	+	+	+		-

NOP

“No Operation” instruction. ST7598 will do nothing when receiving this instruction.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	0	0	1	1	No operation

Frequency Compensation Temperature Range

This instruction defines the temperature range for automatic frame rate adjustment according to current temperature as shown in Fig. 16.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	1	1	0	0	TA[6:0]=09h~76h
1	0	-	TA6	TA5	TA4	TA3	TA2	TA1	TA0	TB[6:0]=09h~76h
1	0	-	TB6	TB5	TB4	TB3	TB2	TB1	TB0	TC[6:0]=09h~76h
1	0	-	TC6	TC5	TC4	TC3	TC2	TC1	TC0	TA<TB-8 and TB<TC-8

Note: “-” is disable bit. It can be either logic 0 or 1.

The target temperature add 40 will become the decimal value of register TA[6:0]/TB[6:0]/TC[6:0].

Temp. Range Value	Temp. Rising State (°C)	Temp. Falling State (°C)	Restriction
Freq. Changing Point A (TA)	(TA[6:0]-40)+THF[3:0]	TA[6:0]-40	TB[6:0]>TA[6:0]+THF[3:0]
Freq. Changing Point B (TB)	(TB[6:0]-40)+THF[3:0]	TB[6:0]-40	TC[6:0]>TB[6:0]+THF[3:0]
Freq. Changing Point C (TC)	(TC[6:0]-40)+THF[3:0]	TC[6:0]-40	87°C ≥TC[6:0]+THF[3:0]

Example:

If TA wants to be set at -10°C, TA[6:0]=-10+40=30=1Eh

If TB wants to be set at 0°C, TB[6:0]=0+40=40=28h

If TC wants to be set at 10°C, TC[6:0]=10+40=50=32h

Temperature Hysteresis Value

This instruction defines the temperature compensation threshold. THV[3:0] is used to set the threshold (hysteresis) value for Vop while THF[3:0] is used to set the threshold (hysteresis) value for frame frequency (fFR). The threshold values (THV & THF) can avoid the Vop/fFR switching up and down, when the ambient temperature changes around the junction of two temperature ranges. When the ambient temperature is decreasing, the Vop/fFR is changed at the junction temperature between two temperature ranges. But if the temperature is increasing, the Vop/fFR is not changed until the temperature exceeds the “junction+hysteresis”.

For example,

- THV[3:0]=4 (2°C) and the ambient temperature is increasing from 27°C to 35°C. Vop slope is MT8 in 27.0 °C ~33.5°C, and it changes to MT9 if Ta is 34°C or higher.
- Similarly, if we set THF[3:0]=3 (3°C) and TA at -20 °C as a point to change fFR. fFR changes from FRB[3:0] to FRA[3:0] when temperature decreases from -19.5°C to -20.0°C. But fFR changes from FRA[3:0] to FRB[3:0] when temperature increases from -17.5°C to -17.0°C.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	1	1	0	1	THV[3:0]=00h~0Fh
1	0	-	-	0	0	THV3	THV2	THV1	THV0	THF[3:0]=00h~0Fh
1	0	-	-	-	-	THF3	THF2	THF1	THF0	

Note: “-” is disable bit. It can be either logic 0 or 1.

The relationship between the parameter THV[3:0] and the temperature hysteresis for Vop is shown below.

THV3	THV2	THV1	THV0	Temp. Hysteresis for Vop
0	0	0	0	0°C (stop TC auto-adjust of Vop)
0	0	0	1	0.5°C
0	0	1	0	1.0°C
:	:	:	:	:
1	1	0	1	6.5°C
1	1	1	0	7.0°C
1	1	1	1	7.5°C

The relationship between the parameter THF[3:0] and the temperature hysteresis for frame rate is shown below.

THF3	THF2	THF1	THF0	Temp. Hysteresis for FR
0	0	0	0	0°C (stop TC auto-adjust of fFR)
0	0	0	1	1°C
0	0	1	0	2°C
:	:	:	:	:
1	1	0	1	13°C
1	1	1	0	14°C
1	1	1	1	15°C

Current Temperature

This instruction used to detect current temperature. If the value of T[7:0] is 00h means the internal detected temperature is -40°C and the current temperature is: **Temperature=T[7:0]x0.5-40** (°C). The ambient temperature maybe varies in a small range and the temperature compensation function will adjust Vop (or fFR) up-and-down. As the result, the display looks like flickering. To prevent this kind of problem, THV[3:0] and THF[3:0] are used to reduce the sensitivity of ambient temperature.

- The accuracy of temperature detection will not be affected by THV/THF.
- The built-in thermal sensor is designed for temperature compensation of Vop and fFR. It can't be used to replace a real thermal meter.
- When the ambient temperature (Ta) is higher than 87.5°C (i.e. 88~95°C), the reading parameter is always 0xFF.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	1	1	1	1	Ta=T[7:0]x0.5-40 (°C)
1	1	T7	T6	T5	T4	T3	T2	T1	T0	

Test

This instruction is reserved for IC testing.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	1	1	1	TE	T	TE=0: Normal command mode TE=1: Test command mode T: Select test command mode

INSTRUCTION TABLE (PROM Function)

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Test	0	0	1	1	1	1	1	1	TE	T	Set test command mode
TE=1 & T=1											
Vop Increase	0	0	1	1	0	1	0	1	1	0	Vop increase one step
Vop Decrease	0	0	1	1	0	1	0	1	1	1	Vop decrease one step
Vop Offset	0	0	1	1	0	1	0	0	1	1	Vop offset
	1	0	VOF7	VOF6	VOF5	VOF4	VOF3	VOF2	VOF1	VOF0	
PROM WR/RD Control	0	0	1	0	0	1	0	0	0	1	PROM WR/RD control
	1	0	0	0	WR/RD	0	0	0	0	0	WR/RD=0: enable PROM read WR/RD=1: enable PROM write
PROM Control Out	0	0	1	0	0	1	0	0	1	0	Cancel PROM control function
PROM Write	0	0	1	0	0	1	0	0	1	1	PROM programming procedure
PROM Read	0	0	1	0	0	1	0	1	0	0	PROM up-load procedure
PROM Auto Read Control	0	0	1	0	0	1	0	1	1	0	PROM Auto Read Control
	1	0	0	0	0	XARD	0	0	0	0	XARD=0: enable auto read XARD=1: disable auto read

INSTRUCTION DESCRIPTION (PROM Function)

Vop Increase

This instruction is used to increase Vop step by one (VOF[7:0]+1).

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	0	1	0	1	1	0	

Vop Decrease

This instruction is used to decrease Vop step by one (VOF[7:0]-1).

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	0	1	0	1	1	1	

Vop Offset

This instruction is changes VopOffset directly. It is not recommended to set VopOffset directly with this instruction.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	0	1	0	0	1	1	
1	0	VOF7	VOF6	VOF5	VOF4	VOF3	VOF2	VOF1	VOF0	

PROM WR/RD Control

This instruction is used to set the status of PROM that write to PROM or read from PROM.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	1	0	0	0	1	WR/RD=0: Enable PROM read RW/RD=1: Enable PROM write
1	0	0	0	WR /RD	0	0	0	0	0	

PROM Control Out

This instruction is used to cancel PROM control function.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	1	0	0	1	0	

PROM Write

This instruction is used to trigger PROM programming procedure.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	1	0	0	1	1	

PROM Read

This instruction is used to trigger PROM up-load procedure.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	1	0	1	0	0	

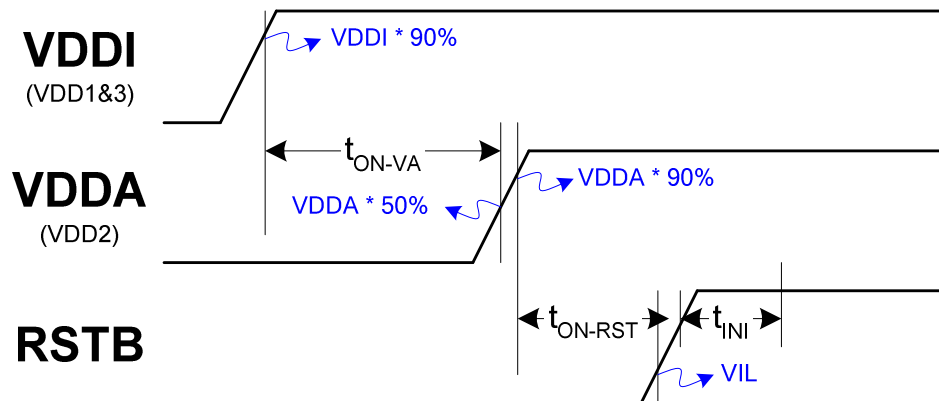
PROM Auto Read Control

This instruction is used to set status of PROM auto read function is enable or disable.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	1	0	1	1	0	
1	0	0	0	0	XARD	0	0	0	0	

OPERATION FLOW

System Power ON Sequence



Timing Requirement:

Item	Symbol	Requirement	Note
VDDA power delay	t_{ON-VA}	$0 \leq t_{ON-VA}$	- If VDDI and VDDA are separated, turn ON VDDI first and then VDDA. - The hardware reset must be kept LOW until the last power is stable (higher than 90% of the rated value). - Applying VDDI and VDDA in any order will not damage IC.
RSTB wait time	t_{ON-RST}	$0 \leq t_{ON-RST}$	- Keep "$t_{ON-VA} + t_{ON-RST}$" $\geq t_{RW}$. - Increasing t_{ON-RST} can cover the power stable time difference in customer's system.
Initial wait time	t_{INI}	$t_R \leq t_{INI}$	- The initial procedure starts after t_{INI}. - It is recommended to keep t_{INI} larger than t_R.

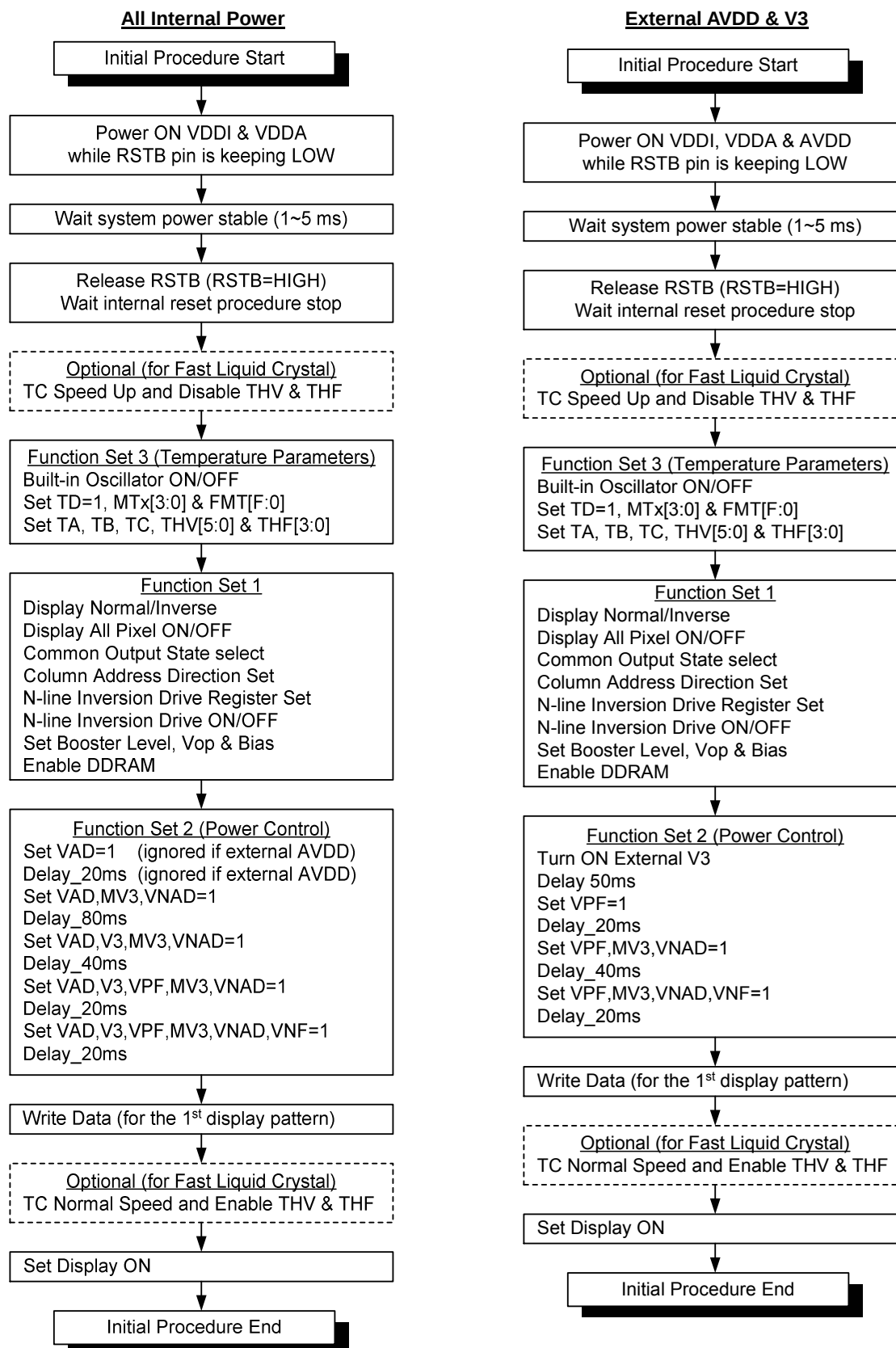
Note:

- IC will NOT be damaged if either VDDI or VDDA is OFF while another is ON.
The specification listed below just wants to prevent abnormal display on LCD module.
- Power stable is defined as the time that the later power (VDDI or VDDA) reaches 90% of its rated voltage. The power stable-time depends on system and the time is not included in this specification (customer should consider this factor).

Initial Flow

Referential Flow

After the system power ON, the initial flow should set the driver IC for the first display ON.



Referential Initial Code

The following codes are listed for quick reference. Customer should fine tune parameters according to LCD performance.

```
void initial(void)
{
    Reset_ms(1);
    Delay_ms(5);
    Write(COMMAND, 0xAE);    // Display OFF
    Write(COMMAND, 0xEA);    // Power Discharge Control
    Write(DATA, 0x00);       // Discharge OFF
    // Optional : TC speed-up for critical case with fast liquid crystal
    Write(COMMAND, 0xFE);    // Enable Test Mode
    Write(COMMAND, 0xF8);    // TC Speed Control
    Write(DATA, 0x2D);       // TC Speed Up
    Write(COMMAND, 0xF9);    // TC Test Function
    Write(DATA, 0x20);       // Disable THV & THF
    Write(COMMAND, 0xFC);    // Exit Test Mode
    // Start TC & OSC earlier for critical case with fast liquid crystal
    Write(COMMAND, 0xAB);    // OSC ON
    Write(COMMAND, 0x69);    // Temperature Detection ON
    Write(COMMAND, 0x4E);    // TC Setting
    Write(DATA, 0x00);       // 0mV/°C, should be adjusted by customer
    Write(DATA, 0x00);       // 0mV/°C, should be adjusted by customer
    Write(DATA, 0x00);       // 0mV/°C, should be adjusted by customer
    Write(DATA, 0x00);       // 0mV/°C, should be adjusted by customer
    Write(DATA, 0x00);       // 0mV/°C, should be adjusted by customer
    Write(DATA, 0x00);       // 0mV/°C, should be adjusted by customer
    Write(DATA, 0x00);       // 0mV/°C, should be adjusted by customer
    Write(COMMAND, 0x39);    // TC Flag
    Write(DATA, 0x00);
    Write(DATA, 0x00);
    Write(COMMAND, 0x5F);    // Set Frame Frequency
    Write(DATA, 0x77);       // fFR=85Hz in all temperature range
    Write(DATA, 0x77);       // should be adjusted by customer
    Write(COMMAND, 0xEC);    // FR Compensation Temp. Range
    Write(DATA, 0x19);       // TA = -15 degree
    Write(DATA, 0x2D);       // TB = 5 degree
    Write(DATA, 0x55);       // TC = 45 degree
    Write(COMMAND, 0xED);    // Temp. Hysteresis Value (thermal sensitivity)
    Write(DATA, 0x04);       // Vop threshold: +2°C
    Write(DATA, 0x04);       // fFR threshold: +4°C

    Write(COMMAND, 0xA6);    // Display Inverse OFF
    Write(COMMAND, 0xA4);    // Disable Display All Pixel ON
    Write(COMMAND, 0xC4);    // COM Output Status
    Write(DATA, 0x02);       // Interlace mode, MY=0
    Write(COMMAND, 0x36);    // Set N-Line
    Write(DATA, 0x05);       // N-Line=(5+1)x4=24
    Write(COMMAND, 0xE4);    // N-Line OFF
    Write(COMMAND, 0xE7);    // LCD Drive Method
    Write(DATA, 0x19);       // NLFR=1
    Write(COMMAND, 0x81);    // Set EV=32h
    Write(DATA, 0x32);       // VOP=14V
    Write(DATA, 0x00);
    Write(COMMAND, 0xA2);    // BIAS
    Write(DATA, 0x03);       // 1/9 BIAS
    Write(COMMAND, 0xA0);    // Column Address Direction: MX=0
    Write(COMMAND, 0x84);    // Display Data Input Direction: Column
    Write(COMMAND, 0x6D);    // Enable DDRAM
    Write(DATA, 0x15);       // Duty = 1/88 duty
    Write(DATA, 0x0C);

    Write(COMMAND, 0x25);    // Power Control
    Write(DATA, 0x20);       // AVDD ON
    Delay_ms(20);
    Write(COMMAND, 0x25);    // Power Control
```

```

Write(DATA, 0x26);           // AVDD, MV3 & NAVDD ON
Delay_ms(80);
Write(COMMAND, 0x25);        // Power Control
Write(DATA, 0x36);           // AVDD, MV3, NAVDD & V3 ON
Delay_ms(40);
Write(COMMAND, 0x25);        // Power Control
Write(DATA, 0x3E);           // AVDD, MV3, NAVDD, V3 & VPF ON
Delay_ms(20);
Write(COMMAND, 0x25);        // Power Control
Write(DATA, 0x3F);           // AVDD, MV3, NAVDD, V3, VPF & VNF ON
Delay_ms(20);

Write(COMMAND, 0xB1);        // Page Address
Write(DATA, 0x00);           // Page 0
Write(COMMAND, 0x13);        // Column Address
Write(DATA, 0x00);           // Start Column = 0
Write(DATA, 0x00);
Write(COMMAND, 0x1D);        // Write Data 3784bytes to all DDRAM
for(init i=0; i<3784; i++)
Write(DATA, 0x00);           // Write Data 0x00 for 1st Display pattern
// Optional : if TC is set speed-up, reset TC to normal mode
Write(COMMAND, 0xFE);        // Enable Test Mode
Write(COMMAND, 0xF8);        // TC Speed Control
Write(DATA, 0x21);           // TC Speed Normal
Write(COMMAND, 0xF9);        // TC Test Function
Write(DATA, 0x00);           // Enable THV & THF
Write(COMMAND, 0xFC);        // Exit Test Mode

Write(COMMAND, 0xAF);        // Display ON
}

```

This initial code is used for the applications with all internal power circuits. The internal power sequence is shown below:

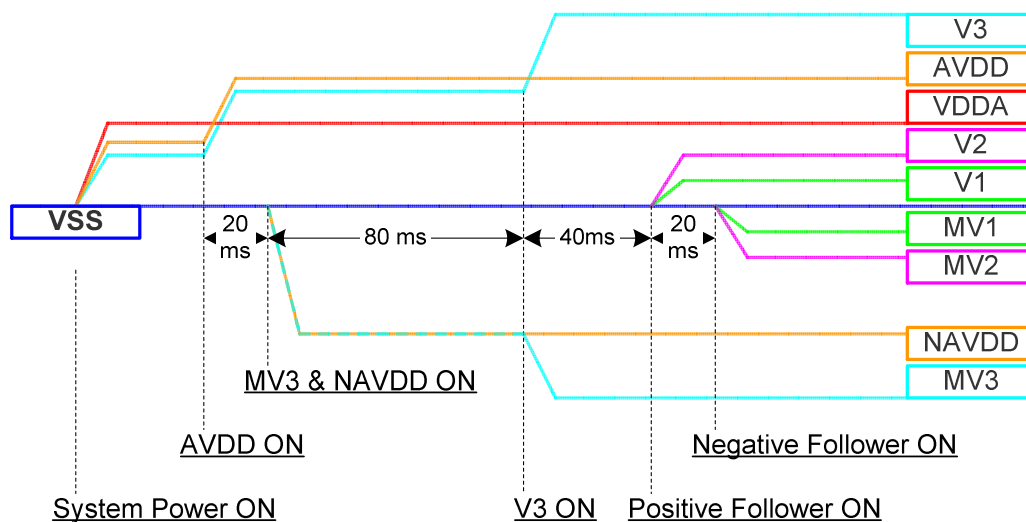
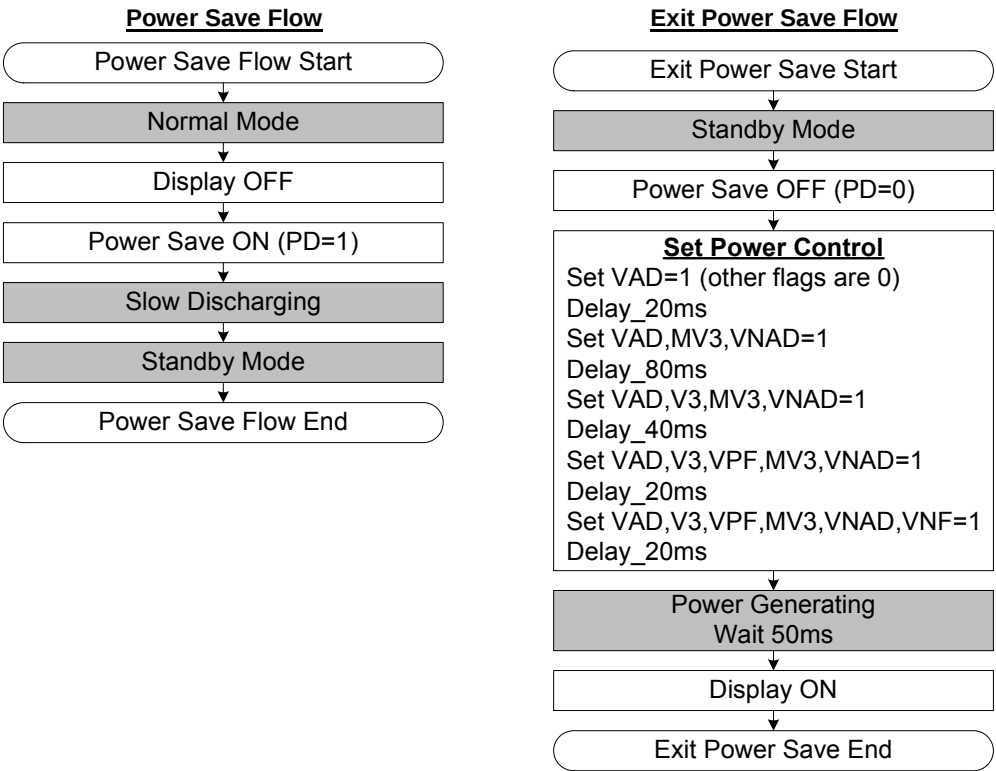


Fig. 21 Internal Analog Power ON Sequence

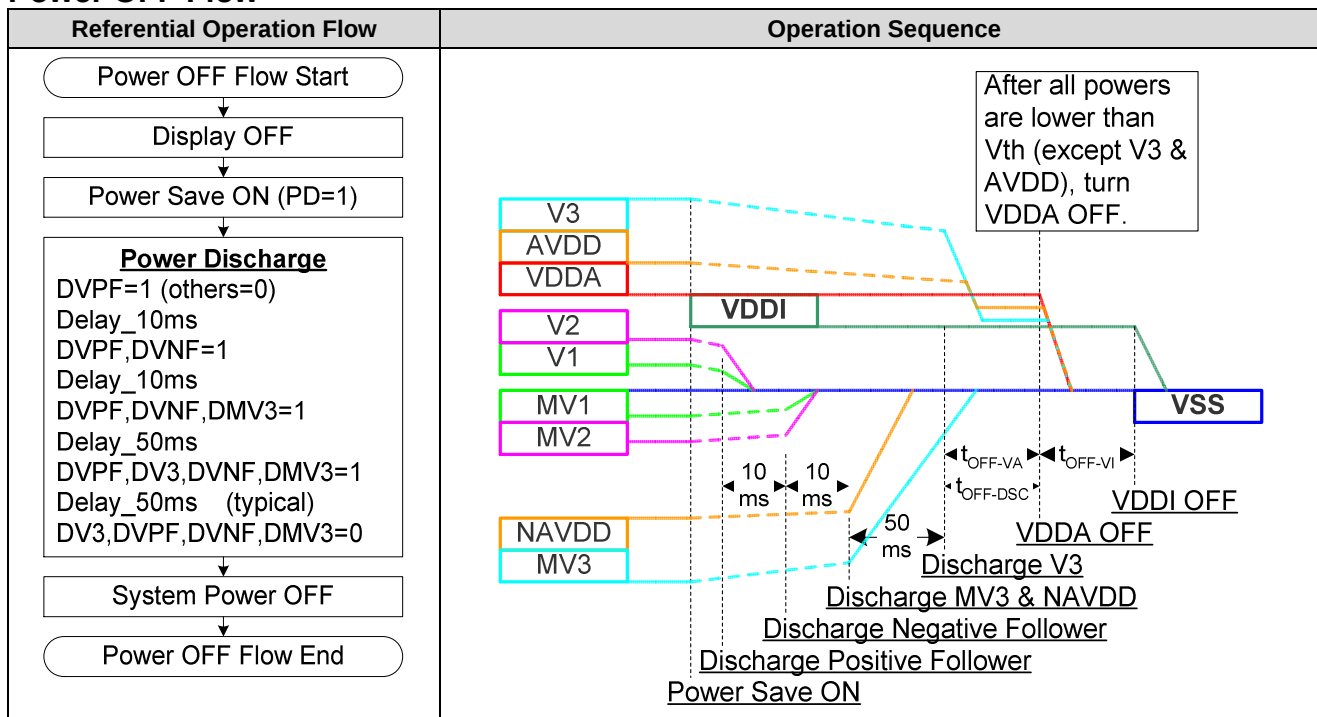
Power Saving Flow

Referential Flow



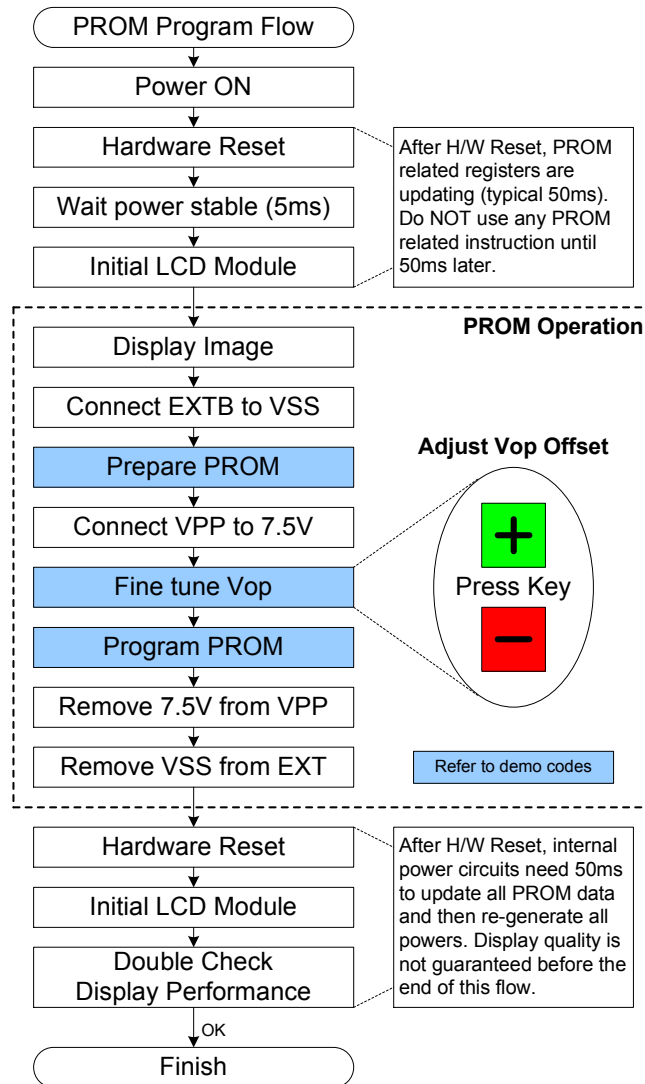
Note: For external power application, please refer to the initial flow for the correct Power Control sequence.

Power OFF Flow



Item	Symbol	Requirement	Description
Analog circuit discharge off delay	$t_{OFF-DSC}$	$30ms \leq t_{OFF-DSC}$	- It is recommended to turn OFF analog discharge after the discharge procedure is finished. - The discharge process is finished when: V2, V1, MV1 & MV2 are lower than V_{th} of liquid crystal; $VDDA > AVDD > V3$. - The time will be different from LCD modules, since the panel loading & ITO resistance are different. And the system power and external capacitors will also influence it. - The typical value is 50ms. And it is recommended to measure the time by real LCD module and application system.
VDDA power off delay	t_{OFF-VA}	$t_{OFF-DSC} \leq t_{OFF-VA}$	- Turn VDDA off after discharge procedure is finished. - AVDD and V3 fall as VDDA falling.
VDDI power off delay	t_{OFF-VI}	$0 \leq t_{OFF-VI}$	- If VDDI and VDDA are separated, turn VDDI off after VDDA. - The AVDD falling time depends on the LCD module and power circuit on the application system.

PROM Operation Referential PROM Program Flow



Referential PROM Operation Code

```
void PreparePROM (void)
{
    //----- Preset PROM mode before Programming PROM -----
    Write(COMMAND, 0xFF);           // Enter PROM Test Mode
    Write(COMMAND, 0x96);           // Disable Auto-Load
    Write(DATA, 0x10);
    Write(COMMAND, 0x94);           // Load Programmed data into Register
    Delay_ms(50);
    PROM_LED(ON);                  // GPIO control LED ON
                                   // Reserved for PROM indicator of 7.5V switch (ON)
}

void FineTuneVop (void)
{
    //----- Fine tune Vop with "+" & "-" buttons -----
    Write(COMMAND, 0xD6);           // Write command 0xD6 if "+" button is pressed
    or                               // Vop increase 1 step (VopOffset+1)
    Write(COMMAND, 0xD7);           // Write command 0xD7 if "-" button is pressed
                                   // Vop decrease 1 step (VopOffset-1)
}

void ProgramPROM (void)
{
    //----- Program PROM after VopOffset is adjusted -----
    Write(COMMAND, 0x95);           // Program mode parameter
    Write(DATA, 0x08);
    Write(COMMAND, 0x91);           // Change PROM Control into Program mode
    Write(DATA, 0x20);
    Delay_ms(50);
    Write(COMMAND, 0x93);           // Program Start
    Delay_ms(50);
    Write(COMMAND, 0x92);           // Exit PROM control
    Write(COMMAND, 0x94);           // Load Programmed data into Register
    Delay_ms(50);
    Write(COMMAND, 0xFC);           // Exit PROM Test Mode
    PROM_LED(OFF);                 // GPIO control LED OFF. Confirm display quality.
                                   // Reserved for PROM indicator of 7.5V switch (OFF)
}
```

Note:

1. If Vop is incorrect and display performance is not accepted after PROM programmed, please redo this flow again to fine tune Vop again.
2. Each press on the "+" or "-" key should execute one command 0xD6 (0xD7) to adjust VopOffset one step up (down).
3. Do not have the backlight closed to IC, because the temperature compensation is turned ON during the burning process. The backlight may heat IC and influence the altitude of Vop.
4. This flow (Burning Flow) is used for LCM assembler.
5. PROM can be written 3 times.

The programmed VopOffset parameter can be read out by the following codes.

```
void ReadVopOffset (void)
{
    //----- Read VopOffset from PROM Register -----
    byte VopOffset; // Allocate 1 byte for VopOffset
    Write(COMMAND, 0xFF); // Enter Test mode
    Write(COMMAND, 0x91); // Set PROM Control to Download mode
    Write(DATA, 0x00);
    Delay_ms(50);
    Write(COMMAND, 0x94); // Load Programmed data into Register
    Delay_ms(50);
    Write(COMMAND, 0x92); // Exit PROM control
    Write(COMMAND, 0x34); // Set PROM Read to byte mode (VopOffset)
    Write(DATA, 0x03);
    Write(COMMAND, 0x35); // Execute PROM Read (byte read)
    VopOffset = Read_LCD(1,PROM); // LCD interface read 1-byte without dummy read
    DisplayPROM(VopOffset); // Display VopOffset to screen
    Write(COMMAND, 0x92); // Exit PROM control
    Write(COMMAND, 0xFC); // Exit Test mode
}
```

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

ABSOLUTE MAXIMUM RATINGS

VSS1 = VSS2 = VSS3 = 0V

Parameter	Symbol	Conditions	Unit
Digital Power Supply Voltage	VDDI (VDD1 & VDD3)	-0.3 ~ 6.0	V
Analog Power supply voltage	VDDA (VDD2)	-0.3 ~ 6.0	V
LCD Power supply voltage	V3	-0.3 ~ 12.21	V
LCD Power supply voltage	V2, V1	-0.3 ~ 6.0	V
LCD Power supply voltage	AVDD	-0.3 ~ 6.0	V
LCD Power supply voltage	NAVDD	-6.0 ~ 0.3	V
LCD Power supply voltage	MV1, MV2	-6.0 ~ 0.3	V
LCD Power supply voltage	MV3	-12.21 ~ 0.3	V
MCU Interface Input Voltage	VIN	-0.3 ~ VDDI+0.3	V
Operating temperature	TOPR	-40 ~ +95	°C
Storage temperature	TSTR	-55 ~ +125	°C

Note:

1. All voltages are respect to VSS1 unless otherwise noted (VSS1=VSS2=VSS3).
2. Stresses exceed the ranges listed above may cause permanent damage to IC.
3. Parameters are valid over operating temperature range unless otherwise specified.
4. Insure the voltage levels always match the correct relation (except Power ON and Power OFF sequence):
V3 > AVDD > V2 > V1 > VSS2 > MV1 > MV2 > NAVDD > MV3
5. Stresses exceed the ABSOLUTE MAXIMUM RATINGS listed above may cause permanent damage to IC. These ratings are stress only. IC should be operated under DC/AC Characteristics condition for normal operation. If this condition is not met. IC operation may be error and the reliability may be deteriorated.

DC CHARACTERISTICS

VSS1=VSS2=VSS3 =0V and Ta = -40 ~ 95 °C, unless otherwise specified.

Item	Symbol	Condition	Related Pin	Rating			Unit
				Min.	Typ.	Max.	
Digital Operating Voltage	VDDI		VDD1, VDD3	3.0	–	5.5	V
Analog Operating Voltage	VDDA		VDD2	3.0	–	5.5	V
Input High-level Voltage	V _{IH}		MCU Interface	0.8*VDD1	–	VDD1	V
Input Low-level Voltage	V _{IL}		MCU Interface	VSS1	–	0.2*VDD1	V
Output High-level Voltage	V _{OH}	I _{OH} =1.0mA, VDD1=3.0V	D[7:0] TSYNC	0.8*VDD1	–	VDD1	V
Output Low-level Voltage	V _{OL}	I _{OL} =-1.0mA, VDD1=3.0V	D[7:0] TSYNC	VSS1	–	0.2*VDD1	V
V3 Accuracy	ΔV3	Ta=25°C, VDD=3.0V V3=10V, Bias=1/12	V3	-0.12	–	0.12	V
Input Leakage Current	I _{IL}	Vin = VDD1 or VSS1	MCU Interface	-1.0	–	1.0	μA
ON Resistance of LCD Drivers	R _{ON}	Ta=25°C	Vop=18.0V, BIAS=1/11 ΔV=10% COM Drivers	–	1.8	–	KΩ
			Vop=18.0V, BIAS=1/11 ΔV=10% SEG Drivers	–	1.8	–	KΩ
Read Temperature Offset	ΔT _{RD}	VDD=3.3V, Ta=25°C	–	-2	–	2	°C
		VDD=3.3V, Ta=-40~95°C	–	-4 *	–	4 *	
Operation Clock	f _{OSC}	Internal Oscillator	–	1467	1630	1793	KHz

Note:

- The detected temperature is IC working temperature, which maybe a little bit higher than ambient temperature.

The current consumed by whole IC (bare die) with internal power system:

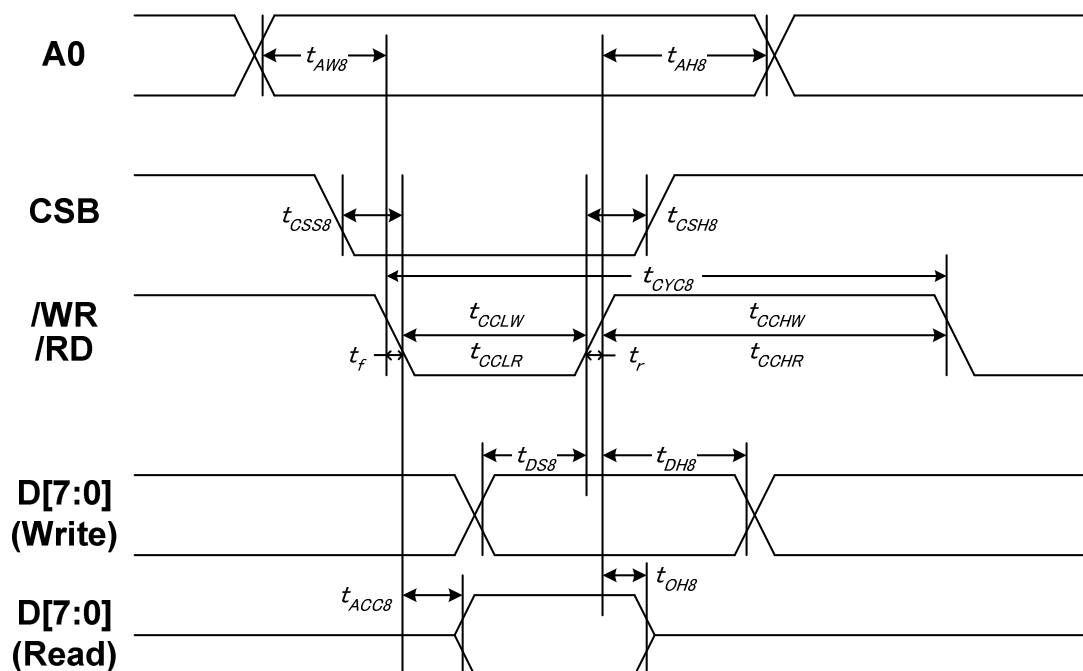
Item	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Display Current (Digital)	IDDI	Display ON, Pattern: SNOW (Static), VDDI=VDDA=3.3V, Internal AVDD, Booster Level1, Vop = 15V, Bias=1/10 N-Line OFF, fFR= 85Hz, Ta=25°C	–	150	–	μA
Display Current (Analog)	IDDA			1000		
Standby	ISS	VDDI=VDDA=3.3V, Internal AVDD, Ta=25°C	–	80	–	μA

Note:

- The current is DC characteristic of a "Bare Chip".

TIMING CHARACTERISTIC

System Bus Timing for 8080 MCU Interface



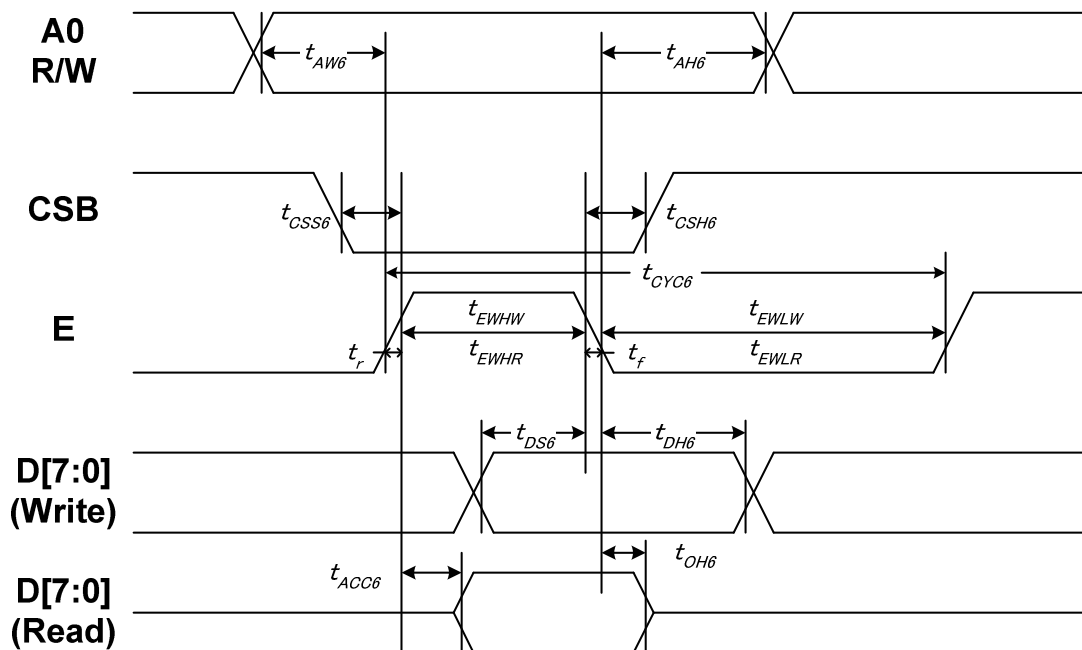
VDD1 = 3.0V~5.5V , Ta = -40°C ~ 95°C

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	t_{AW8}		10	—	ns
Address hold time		t_{AH8}		0	—	
System cycle time	/WR	t_{CYC8}		320	—	
/WR L pulse width (WRITE)		t_{CCLW}		150	—	
/WR H pulse width (WRITE)		t_{CCHW}		150	—	
/RD L pulse width (READ)	/RD	t_{CCLR}		150	—	
/RD H pulse width (READ)		t_{CCHR}		150	—	
CSB setup time	CSB	t_{CSS8}		75	—	
CSB hold time		t_{CSH8}		50	—	
WRITE Data setup time	D[7:0]	t_{DS8}		50	—	
WRITE Data hold time		t_{DH8}		50	—	
READ access time		t_{ACC8}	CL = 100 pF	—	100	
READ Output disable time		t_{OH8}	CL = 100 pF	0	80	

Note:

- The input signal rise time and fall time (t_r , t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, $(t_r + t_f) \leq (t_{CYC8} - t_{CCLW} - t_{CCHW})$ for $(t_r + t_f) \leq (t_{CYC8} - t_{CCLR} - t_{CCHR})$ are specified.
- All timing is specified using 20% and 80% of VDD1 as the reference.
- t_{CCLW} and t_{CCLR} are specified as the overlap between CSB being "L" and /WR (or /RD) being at the "L" level. CSB and /WR (or /RD) cannot act at the same time and CSB should be 100ns wider than /WR (or /RD).
- The system voltage apply to IC will be decreased by ITO resistance. For example, a system using 3V for VDD1, the voltage apply to IC will be lower than 3.0V. Therefore, the AC timing maybe a little bit larger than the value listed above.

System Bus Timing for 6800 MCU Interface



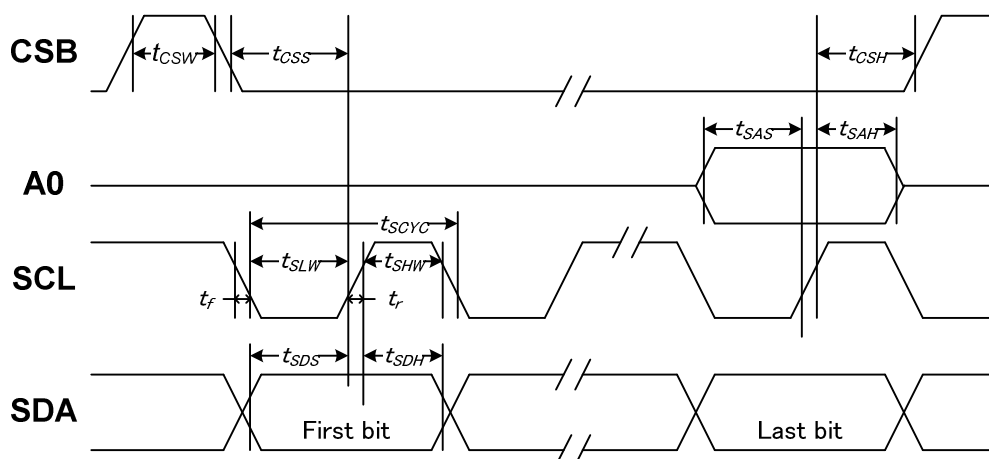
VDD1 = 3.0V~5.5V, Ta = -40°C ~ 95°C

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	t_{AW6}		10	—	ns
Address hold time		t_{AH6}		0	—	
System cycle time	E	t_{CYC6}		320	—	
Enable L pulse width (WRITE)		t_{EWLW}		150	—	
Enable H pulse width (WRITE)		t_{EWHW}		150	—	
Enable L pulse width (READ)		t_{EWLR}		150	—	
Enable H pulse width (READ)		t_{EWHR}		150	—	
CSB setup time	CSB	t_{CSS6}		75	—	
CSB hold time		t_{CSH6}		50	—	
Write data setup time	D[7:0]	t_{DS6}		50	—	
Write data hold time		t_{DH6}		50	—	
Read data access time		t_{ACC6}	CL = 100 pF	—	100	
Read data output disable time		t_{OH6}	CL = 100 pF	0	90	

Note:

- The input signal rise time and fall time (t_r , t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) $\leq$ ($t_{CYC6} - t_{EWLW} - t_{EWHW}$) for ($t_r + t_f$) $\leq$ ($t_{CYC6} - t_{EWLR} - t_{EWHR}$) are specified.
- All timing is specified using 20% and 80% of VDD1 as the reference.
- t_{EWLW} and t_{EWLR} are specified as the overlap between CSB being "L" and E. CSB and E cannot act at the same time and CSB should be 100ns wider than E.
- The system voltage apply to IC will be decreased by ITO resistance. For example, a system using 3V for VDDI, the voltage apply to IC will be lower than 3.0V. Therefore, the AC timing maybe a little bit larger than the value listed above.

System Bus Timing for 4-Line SPI MCU Interface



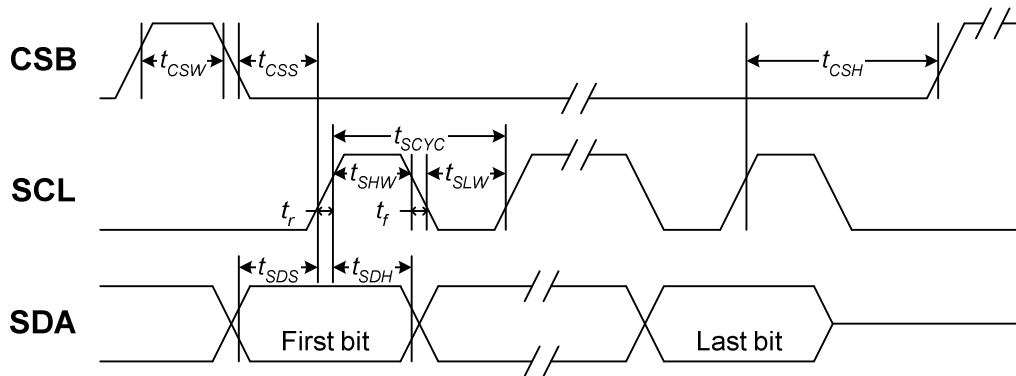
VDD1 = 3.0V~5.5V , Ta = -40°C ~ 95°C

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCL	tSCYC		140	—	ns
SCL "H" pulse width		tSHW		70	—	
SCL "L" pulse width		tSLW		60	—	
Address setup time	A0	tSAS		20	—	
Address hold time		tSAH		20	—	
Data setup time	SDA	tSDS		40	—	
Data hold time		tSDH		40	—	
CSB setup time	CSB	tCSS		60	—	
CSB hold time		tCSH		70	—	
CSB "H" pulse width		tCSW		15	—	

Note:

1. The input signal rise and fall time (t_r , t_f) are specified at 15 ns or less.
2. All timing is specified using 20% and 80% of VDD1 as the standard.
3. The system voltage apply to IC will be decreased by ITO resistance. For example, a system using 3V for VDDI, the voltage apply to IC will be lower than 3.0V. Therefore, the AC timing maybe a little bit larger than the value listed above.

System Bus Timing for 3-Line SPI MCU Interface



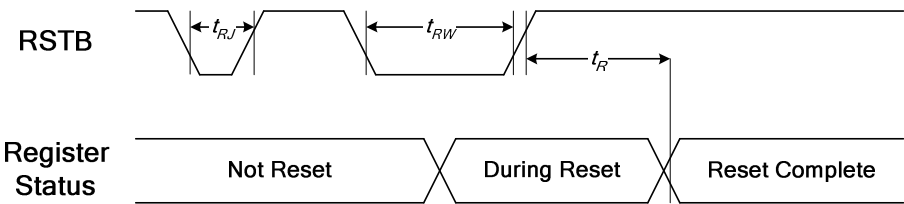
VDD1 = 3.0V~5.5V , Ta = -40°C ~ 95°C

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial Clock Period	SCL	tSCYC		140	—	ns
SCL "H" pulse width		tSHW		70	—	
SCL "L" pulse width		tSLW		60	—	
Data setup time	SDA	tSDS		40	—	
Data hold time		tSDH		40	—	
CSB setup time	CSB	tCSS		60	—	
CSB hold time		tCSH		70	—	
CSB "H" pulse width		tCSW		15	—	

Note:

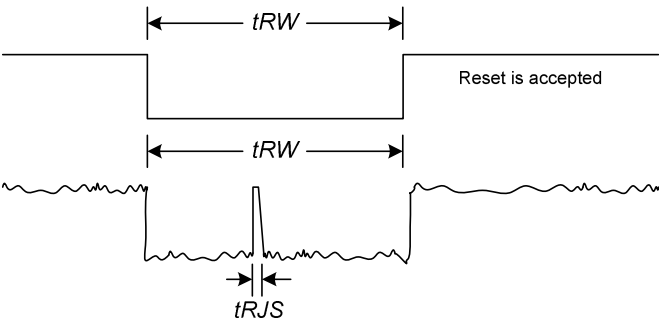
1. The input signal rise and fall time (t_r , t_f) are specified at 15 ns or less.
2. All timing is specified using 20% and 80% of VDD1 as the standard.
3. The system voltage apply to IC will be decreased by ITO resistance. For example, a system using 3V for VDDI, the voltage apply to IC will be lower than 3.0V. Therefore, the AC timing maybe a little bit larger than the value listed above.
4. For general speed AC timing, tCSW is 10ns. For extremely fast AC timing, please set tCSW to be 15ns.

Reset Timing



VDD1 = 3.0V~5.5V , Ta = -40℃ ~ 95℃

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Reset time	RSTB	tR		—	5 ^{*1}	us
Reset “L” pulse width		tRW		15	—	
Reset rejection		tRJ		—	5	
Reset rejection (for noise spike)		tRJS		—	10	ns



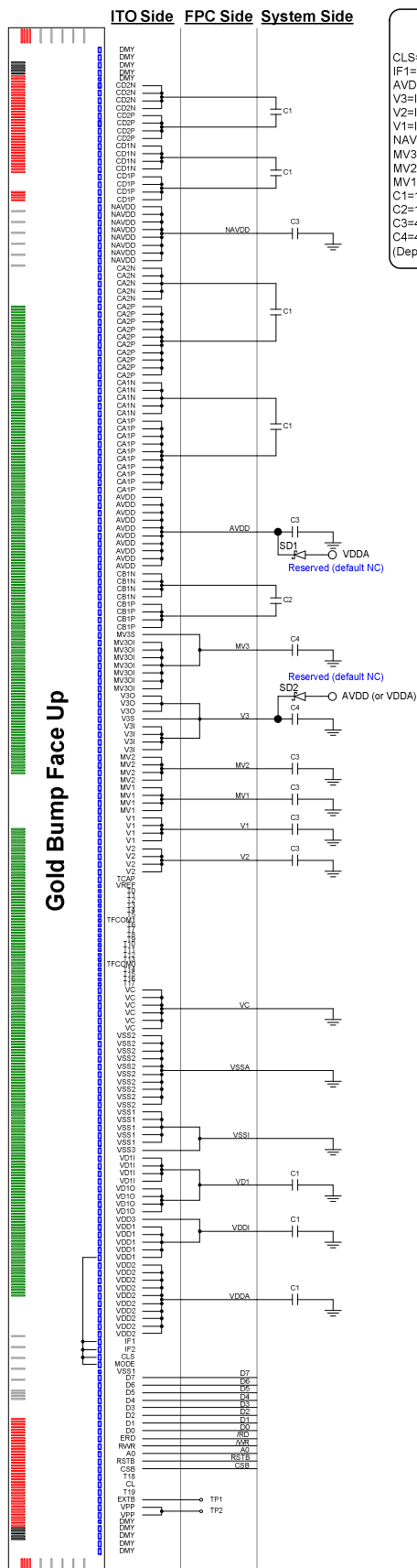
Note:

1. For PROM related operation, it takes 50ms at least for PROM Registers to load PROM contents.
Do NOT use any PROM related command during this period.
2. When the system issues a RSTB LOW pulse, the reset procedure of IC will start if the LOW pulse is longer than t_{RW} specified above. If the LOW pulse is less than t_{RJ} specified above, the reset procedure of IC will not start.
If the LOW pulse is longer than t_{RJ} and less than t_{RW} , the reset procedure of IC is not guaranteed.

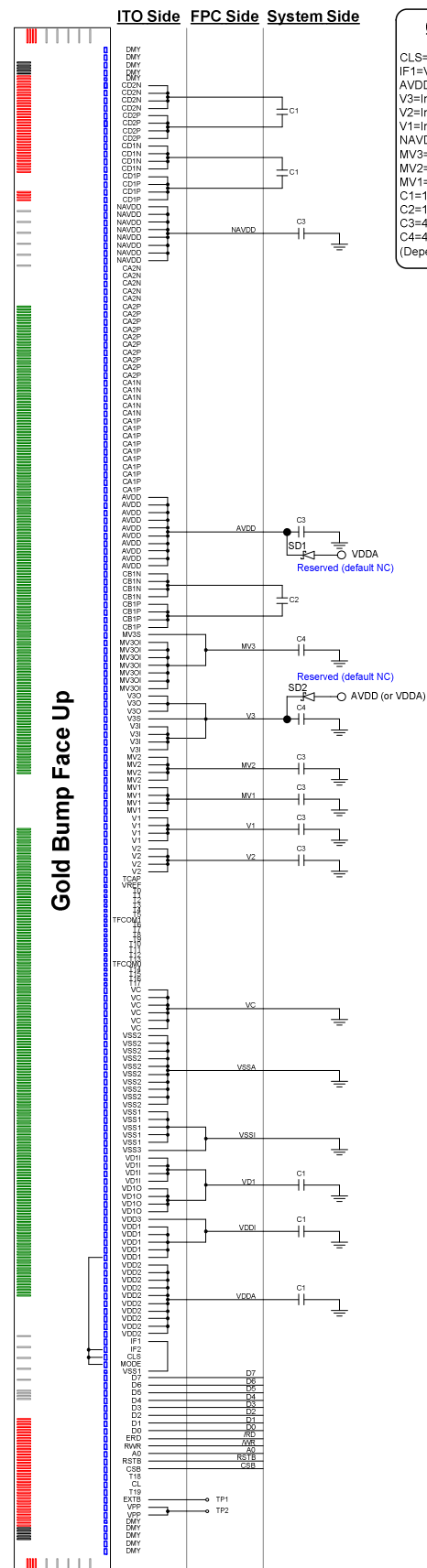
LCD LAYOUT GUIDE

Application Circuit

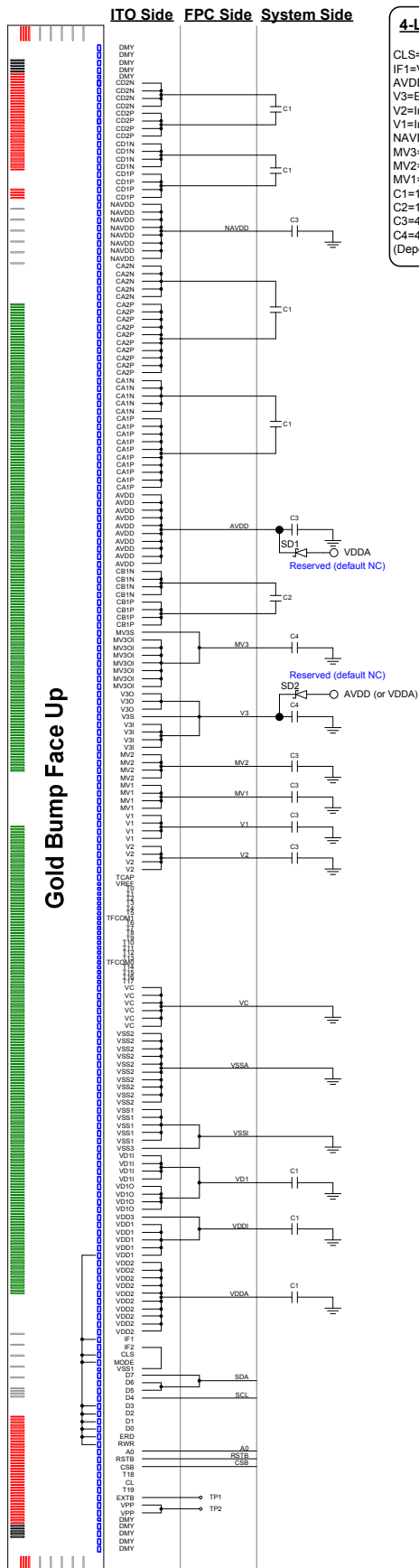
Parallel 8080 Interface



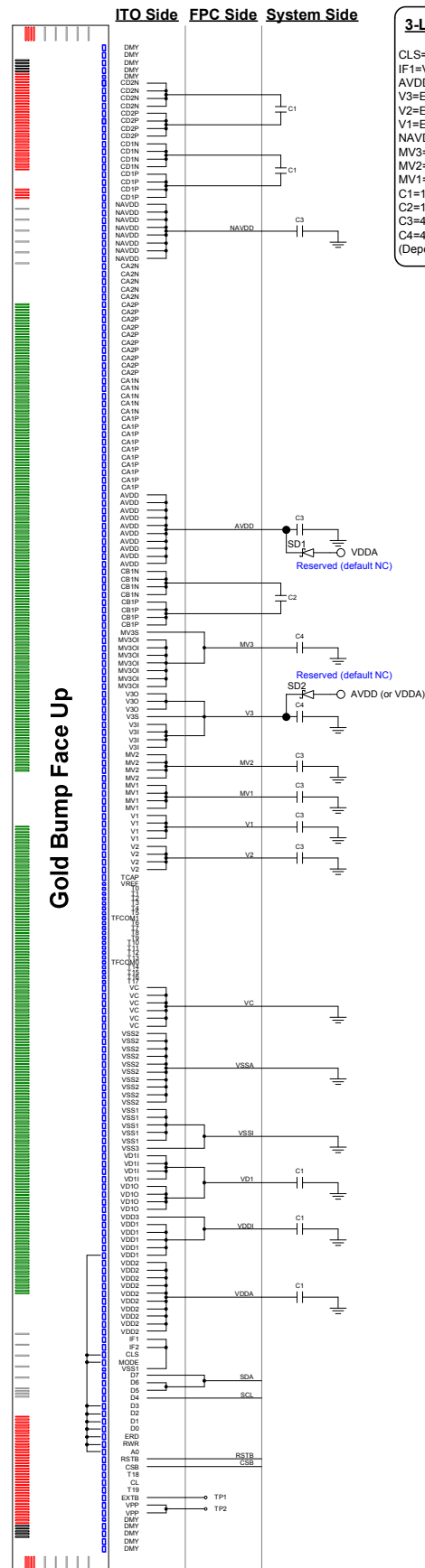
Parallel 6800 Interface



Serial 4-Line SPI



Serial 3-Line SPI



ITO Layout Suggestion

The ITO layout suggestion is shown as below:

- For V3, MV3, VD1, VSS and VDD

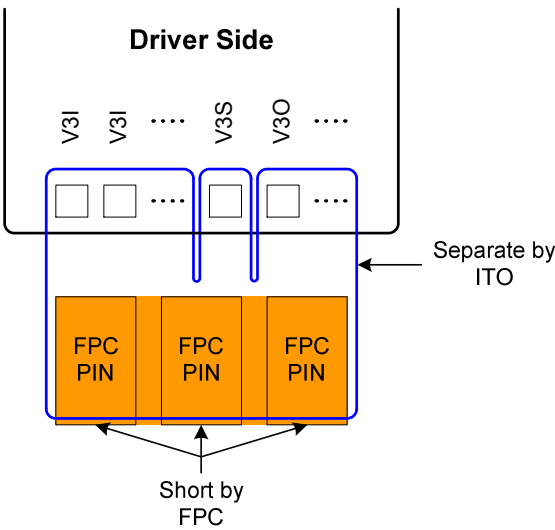


Fig. 22 V3 ITO Layout

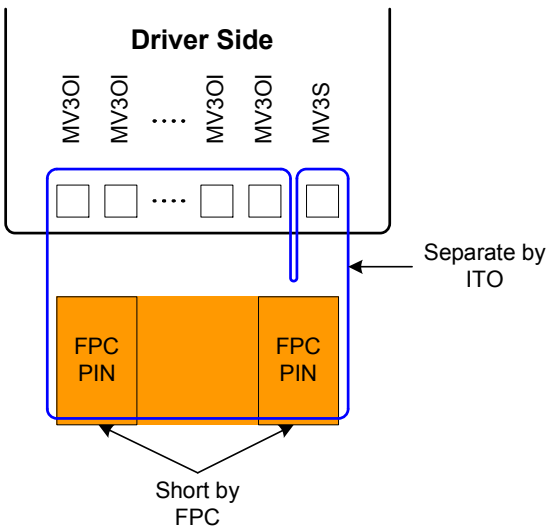


Fig. 23 MV3 ITO Layout

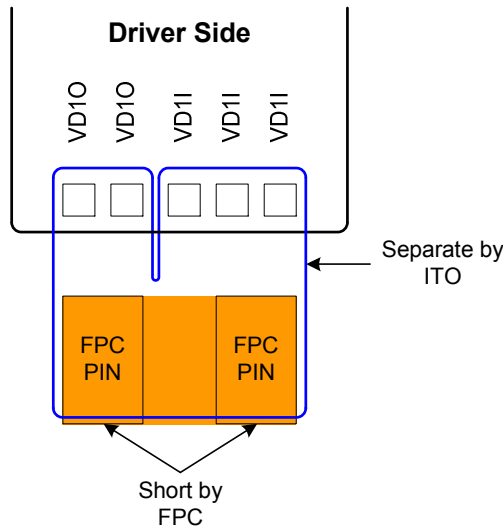


Fig. 24 VD1 ITO Layout

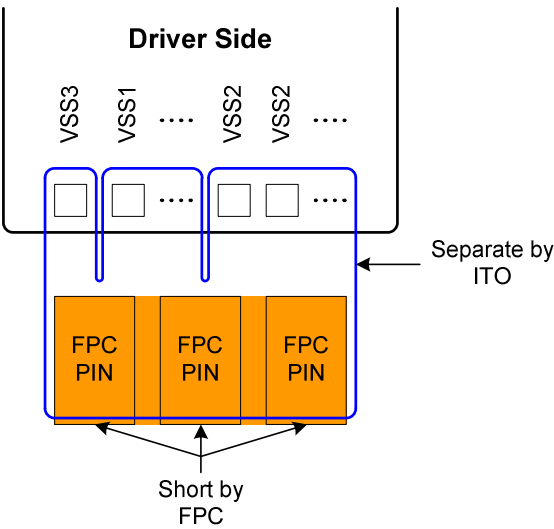


Fig. 25 VSS ITO Layout

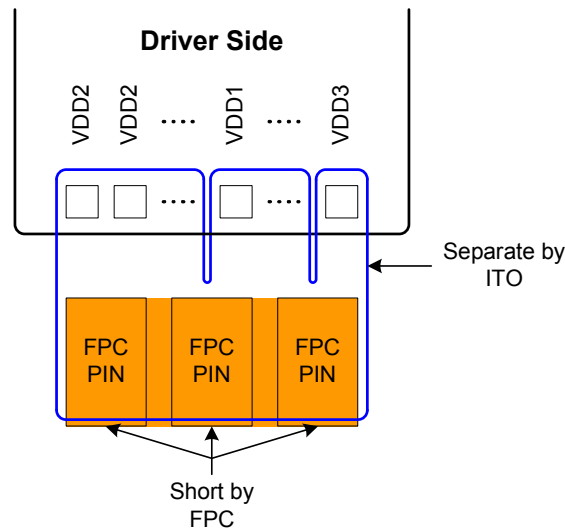


Fig. 26 VDD ITO Layout

● For VPP and EXTB

1. VPP is the power source which programs the internal PROM. If the ITO resistance is too high, the operation current will cause voltage drop while programming. Please try to keep the ITO resistance as low as possible.
2. It is recommended to design VPP and EXTB pins to be "Test Points" (instead of regular pins on FPC).

ITO Resistance

Pin Name	ITO Resister
VPP	<50Ω
VDD1, VDD2, VDD3, VSS1, VSS2, VSS3, VD1I, VD1O, V3O, V3I, V3S, V2, V1, VC, MV1, MV2, MV3OI, MV3S, AVDD, NAVDD, CA1P, CA1N, CA2P, CA2N, CB1P, CB1N, CD1P, CD1N, CD2P, CD2N	<100Ω
A0, ERD, RWR, CSB, D[7:0]	<700Ω
IF[2:1], CLS, MODE, EXTB	<1KΩ
RSTB	<5KΩ
TCAP, CL, VREF, T0~T19, TFCOM0, TFCOM1	Floating

Note:

1. Make sure that the ITO resistance of COM0 ~ COM87 is equal, and so is it of SEG0 ~ SEG343.
2. These Limitations include the bottleneck of ITO layout.
3. The ITO layout suggestions are listed above.
4. The resistance of RSTB is 1KΩ~3KΩ generally. It can be the combination of ITO and external resistor.

REVISION HISTORY

Version	Date	Description
1.0	2011/11/8	● Change Version to V1.0 for mass production. ● Part Number : ST7598-G2.
1.1	2012/5/25	● Release ST7598-G2-B1 (smaller current) ● Fix description of TA~TC restriction: “-”THF[3:0] => “+”THF[3:0] (Page 48)
1.2	2012/9/25	● Fix Addressing description and related drawing.
1.3	2012/12/12	● Add AEC-Q100 description : “AEC-Q100 compliant for automotive applications”. ● Modify internal analog power circuits, add the internal analog power circuit relationship and rename this section as “Internal Analog Power Circuits and External Connection”. ● Reserve external schottky diodes in power circuits and application circuits. ● Modify initial flow and initial code for fast liquid crystal. ● Modify PROM flow to prevent data transfer noise. ● Reduce RSTB ITO Limitation for easy LCD layout. ● Remove reversion history before version 1.0.
1.4	2013/5/17	● Modify the initial code according to the initial flow.
1.5	2013/11/26	● Fix figure and typo.
1.6	2014/10/29	● Release linear display duty (1/88 ~ 1/8 display duty). ● Increase operating temperature range up to 95℃. ● Increase storage temperature range up to 125℃. ● Release fest AC timing for all temperature range. ● Add maximum and minimum value of fOSC (Page 62). ● [Power System Setup] Rewrite the description of Case 1~3 : External AVDD is recommend for 5V system and Internal AVDD is recommend for 3.3V system. ● Rewrite temperature compensation table with detail formula. ● Modify some instruction descriptions to prevent misunderstanding.

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