ST7689

128RGB x 160 dot 65K Color with Frame Memory Single-Chip CSTN Controller/Driver

Datasheet

Version 1.0

2009/10

Sitronix Technology Corporation

LIST OF CONTENT

LIST OF FIGURES

LIST OF TABLES

1. INTRODUCTION

The ST7689 is a driver & controller LSI for 65K color graphic dot-matrix liquid crystal display systems. It generates 384 segments and 160 commons driver circuits. This chip is connected directly to a microprocessor, accepts Serial Peripheral Interface or 8-bit/16-bit parallel display data and stores in an on-chip display data RAM. It performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

2. FEATURES

Driver Output Circuits

- 384 segment outputs / 160 common outputs

Applicable Duty Ratios

- Various partial display
- Partial window moving & data scrolling

Gray-Scale Display

- 4FRC & 31 PWM function circuit to display 64 gray-scale display
- Support 8 color mode (Idle mode)

On-chip Display Data RAM

- Capacity: 128 x 160 x 16 = 327,680 bits

Color support by Interface

- 256 color mode(RGB)=(332) mode
- 4k colors (RGB)=(444) mode
- 65K colors (RGB)=(565) mode
- 262K colors (RGB)=(666) mode (truncate)

Microprocessor Interface

- 8/16-bit parallel bi-directional interface with 6800-series or 8080-series
- 3-line (9-bits) , 4-line(8-bits) serial interface

On-chip Low Power Analog Circuit

- On-chip oscillator circuit and voltage regulator
- Voltage converter (x5, x6, x7, x8) with internal booster capacitors.
- Extremely few outsider components. (Required outsider components: 4 Capacitors)
- On-chip electronic contrast control function
- Voltage follower

(LCD bias: 1/9, 1/10, 1/11, 1/12, 1/13, 1/14)

Operating Voltage Range

- Supply Digital Voltage →VDDI (VDD) = 1.65~3.3V
- Supply Analog Voltage → VDDA (VDD1, VDD2, VDD3, VDD4, VDD5) = 2.4~3.3V
- LCD driving voltage (VOP = V0 - VSS): Max: 18V

LCD Driving Voltage (PROM)

- Contrast Adjustment Value is stored in the built-in PROM (Programmable ROM) for better display quality

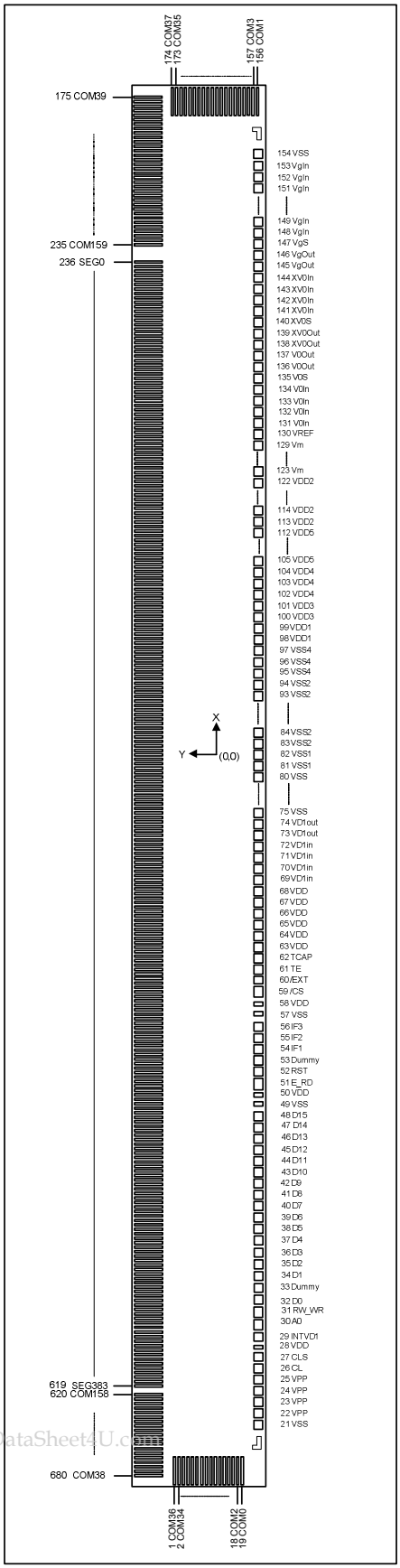
LCD Driving Setting Suggestion

- Vop=15~16V, Bias=1/9~1/11

Package Type

- Application for COG

3. PAD ARRANGEMENT (COG)



Chip Size : 11434 um x 701 um

Bump Pitch :

PAD1~19, 156~174, 175~235 pitch= 22um(min, com/seg)

PAD 236 ~ 619, 620~ 680 pitch= 22um(min, com/seg)

PAD 235 ~ 236, 619~620 pitch=116.33um (min, com/seg)

PAD 21~27,32~48, 50~51, 52~56, 58~59, 60~154 pitch= 80um(I/O)

PAD 27~29, 48~49, 56~57 pitch= 60um(I/O)

PAD 29~30, 31~32, 51~52, 59~60 pitch= 100um(I/O)

PAD 30~31 pitch= 120um(I/O)

PAD 49~50, 57~58 pitch= 40um(I/O)

Bump Size :

PAD30~31, 51, 59	PAD28, 49~50, 57~58
Bump width=105um (min, I/O)	Bump width=25um (min, I/O)
Bump space=15um (min, I/O)	Bump space=15um (min, I/O)
Bump length=63um(min, I/O)	Bump length=63um(min, I/O)
Bump area=6615um^2(I/O)	Bump area=1575um^2(I/O)
PAD21~27, 29, 32~48, 52~56, 60~154	PAD1~19, 156~174, 175~235, 236~619, 620~680
Bump width=65um (min, I/O)	Bump width=10.5um (min, com/seg)
Bump space=15um (min, I/O)	Bump space=11.5um (min, com/seg)
Bump length=63um(min, I/O)	Bump length=149.4um(min, com/seg)
Bump area=4095um^2(I/O)	Bump area=1568.7um^2(com/seg)

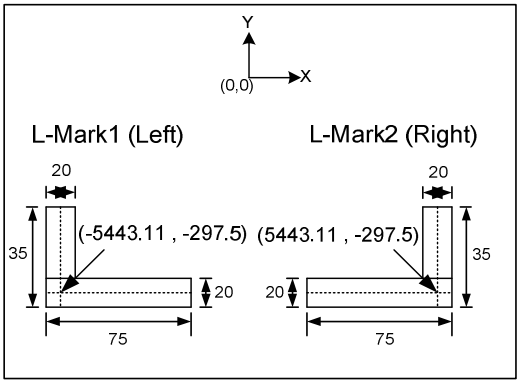
ST7689-G4 (Bump Height: 15um, Hardness: 75HV)

ST7689-G4-1 (Bump Height: 12um, Hardness: 90HV)

Chip Thickness: 300um

Alignment mark

The center of alignment mark: see bellow Table



4. PAD CENTER COORDINATES

PAD	NAME	X	Y
1	COM36	-5606.5	111.5
2	COM34	-5606.5	89.5
3	COM32	-5606.5	67.5
4	COM30	-5606.5	45.5
5	COM28	-5606.5	23.5
6	COM26	-5606.5	1.5
7	COM24	-5606.5	-20.5
8	COM22	-5606.5	-42.5
9	COM20	-5606.5	-64.5
10	COM18	-5606.5	-86.5
11	COM16	-5606.5	-108.5
12	COM14	-5606.5	-130.5
13	COM12	-5606.5	-152.5
14	COM10	-5606.5	-174.5
15	COM8	-5606.5	-196.5
16	COM6	-5606.5	-218.5
17	COM4	-5606.5	-240.5
18	COM2	-5606.5	-262.5
19	COM0	-5606.5	-284.5
20	L-Mark	-5443.11	-297.5
21	VSS	-5300	-283
22	VPP	-5220	-283
23	VPP	-5140	-283
24	VPP	-5060	-283
25	VPP	-4980	-283
26	CL	-4900	-283
27	CLS	-4820	-283
28	VDD	-4760	-283
29	INTVD1	-4700	-283
30	A0	-4600	-283
31	RW_WR	-4480	-283
32	D0	-4380	-283
33	DUMMY	-4300	-283
34	D1	-4220	-283

PAD	NAME	X	Y
35	D2	-4140	-283
36	D3	-4060	-283
37	D4	-3980	-283
38	D5	-3900	-283
39	D6	-3820	-283
40	D7	-3740	-283
41	D8	-3660	-283
42	D9	-3580	-283
43	D10	-3500	-283
44	D11	-3420	-283
45	D12	-3340	-283
46	D13	-3260	-283
47	D14	-3180	-283
48	D15	-3100	-283
49	VSS	-3040	-283
50	VDD	-3000	-283
51	E_RD	-2920	-283
52	/RST	-2820	-283
53	DUMMY	-2740	-283
54	IF1	-2660	-283
55	IF2	-2580	-283
56	IF3	-2500	-283
57	VSS	-2440	-283
58	VDD	-2400	-283
59	/CS	-2320	-283
60	/EXT	-2220	-283
61	TE	-2140	-283
62	TCAP	-2060	-283
63	VDD	-1980	-283
64	VDD	-1900	-283
65	VDD	-1820	-283
66	VDD	-1740	-283
67	VDD	-1660	-283
68	VDD	-1580	-283

PAD	NAME	X	Y
69	VD1in	-1500	-283
70	VD1in	-1420	-283
71	VD1in	-1340	-283
72	VD1in	-1260	-283
73	VD1out	-1180	-283
74	VD1out	-1100	-283
75	VSS	-1020	-283
76	VSS	-940	-283
77	VSS	-860	-283
78	VSS	-780	-283
79	VSS	-700	-283
80	VSS	-620	-283
81	VSS1	-540	-283
82	VSS1	-460	-283
83	VSS2	-380	-283
84	VSS2	-300	-283
85	VSS2	-220	-283
86	VSS2	-140	-283
87	VSS2	-60	-283
88	VSS2	20	-283
89	VSS2	100	-283
90	VSS2	180	-283
91	VSS2	260	-283
92	VSS2	340	-283
93	VSS2	420	-283
94	VSS2	500	-283
95	VSS4	580	-283
96	VSS4	660	-283
97	VSS4	740	-283
98	VDD1	820	-283
99	VDD1	900	-283
100	VDD3	980	-283
101	VDD3	1060	-283
102	VDD4	1140	-283
103	VDD4	1220	-283
104	VDD4	1300	-283

PAD	NAME	X	Y
105	VDD5	1380	-283
106	VDD5	1460	-283
107	VDD5	1540	-283
108	VDD5	1620	-283
109	VDD5	1700	-283
110	VDD5	1780	-283
111	VDD5	1860	-283
112	VDD5	1940	-283
113	VDD2	2020	-283
114	VDD2	2100	-283
115	VDD2	2180	-283
116	VDD2	2260	-283
117	VDD2	2340	-283
118	VDD2	2420	-283
119	VDD2	2500	-283
120	VDD2	2580	-283
121	VDD2	2660	-283
122	VDD2	2740	-283
123	Vm	2820	-283
124	Vm	2900	-283
125	Vm	2980	-283
126	Vm	3060	-283
127	Vm	3140	-283
128	Vm	3220	-283
129	Vm	3300	-283
130	VREF	3380	-283
131	V0in	3460	-283
132	V0in	3540	-283
133	V0in	3620	-283
134	V0in	3700	-283
135	V0s	3780	-283
136	V0out	3860	-283
137	V0out	3940	-283
138	XV0out	4020	-283
139	XV0out	4100	-283
140	XV0s	4180	-283

PAD	NAME	X	Y
141	XV0in	4260	-283
142	XV0in	4340	-283
143	XV0in	4420	-283
144	XV0in	4500	-283
145	Vgout	4580	-283
146	Vgout	4660	-283
147	Vgs	4740	-283
148	Vgin	4820	-283
149	Vgin	4900	-283
150	Vgin	4980	-283
151	Vgin	5060	-283
152	Vgin	5140	-283
153	Vgin	5220	-283
154	VSS	5300	-283
155	L-Mark	5443.11	-297.5
156	COM1	5606.5	-284.5
157	COM3	5606.5	-262.5
158	COM5	5606.5	-240.5
159	COM7	5606.5	-218.5
160	COM9	5606.5	-196.5
161	COM11	5606.5	-174.5
162	COM13	5606.5	-152.5
163	COM15	5606.5	-130.5
164	COM17	5606.5	-108.5
165	COM19	5606.5	-86.5
166	COM21	5606.5	-64.5
167	COM23	5606.5	-42.5
168	COM25	5606.5	-20.5
169	COM27	5606.5	1.5
170	COM29	5606.5	23.5
171	COM31	5606.5	45.5
172	COM33	5606.5	67.5
173	COM35	5606.5	89.5
174	COM37	5606.5	111.5
175	COM39	5649.33	240
176	COM41	5627.33	240

PAD	NAME	X	Y
177	COM43	5605.33	240
178	COM45	5583.33	240
179	COM47	5561.33	240
180	COM49	5539.33	240
181	COM51	5517.33	240
182	COM53	5495.33	240
183	COM55	5473.33	240
184	COM57	5451.33	240
185	COM59	5429.33	240
186	COM61	5407.33	240
187	COM63	5385.33	240
188	COM65	5363.33	240
189	COM67	5341.33	240
190	COM69	5319.33	240
191	COM71	5297.33	240
192	COM73	5275.33	240
193	COM75	5253.33	240
194	COM77	5231.33	240
195	COM79	5209.33	240
196	COM81	5187.33	240
197	COM83	5165.33	240
198	COM85	5143.33	240
199	COM87	5121.33	240
200	COM89	5099.33	240
201	COM91	5077.33	240
202	COM93	5055.33	240
203	COM95	5033.33	240
204	COM97	5011.33	240
205	COM99	4989.33	240
206	COM101	4967.33	240
207	COM103	4945.33	240
208	COM105	4923.33	240
209	COM107	4901.33	240
210	COM109	4879.33	240
211	COM111	4857.33	240
212	COM113	4835.33	240

PAD	NAME	X	Y
213	COM115	4813.33	240
214	COM117	4791.33	240
215	COM119	4769.33	240
216	COM121	4747.33	240
217	COM123	4725.33	240
218	COM125	4703.33	240
219	COM127	4681.33	240
220	COM129	4659.33	240
221	COM131	4637.33	240
222	COM133	4615.33	240
223	COM135	4593.33	240
224	COM137	4571.33	240
225	COM139	4549.33	240
226	COM141	4527.33	240
227	COM143	4505.33	240
228	COM145	4483.33	240
229	COM147	4461.33	240
230	COM149	4439.33	240
231	COM151	4417.33	240
232	COM153	4395.33	240
233	COM155	4373.33	240
234	COM157	4351.33	240
235	COM159	4329.33	240
236	SEG0	4213	240
237	SEG1	4191	240
238	SEG2	4169	240
239	SEG3	4147	240
240	SEG4	4125	240
241	SEG5	4103	240
242	SEG6	4081	240
243	SEG7	4059	240
244	SEG8	4037	240
245	SEG9	4015	240
246	SEG10	3993	240
247	SEG11	3971	240
248	SEG12	3949	240

PAD	NAME	X	Y
249	SEG13	3927	240
250	SEG14	3905	240
251	SEG15	3883	240
252	SEG16	3861	240
253	SEG17	3839	240
254	SEG18	3817	240
255	SEG19	3795	240
256	SEG20	3773	240
257	SEG21	3751	240
258	SEG22	3729	240
259	SEG23	3707	240
260	SEG24	3685	240
261	SEG25	3663	240
262	SEG26	3641	240
263	SEG27	3619	240
264	SEG28	3597	240
265	SEG29	3575	240
266	SEG30	3553	240
267	SEG31	3531	240
268	SEG32	3509	240
269	SEG33	3487	240
270	SEG34	3465	240
271	SEG35	3443	240
272	SEG36	3421	240
273	SEG37	3399	240
274	SEG38	3377	240
275	SEG39	3355	240
276	SEG40	3333	240
277	SEG41	3311	240
278	SEG42	3289	240
279	SEG43	3267	240
280	SEG44	3245	240
281	SEG45	3223	240
282	SEG46	3201	240
283	SEG47	3179	240
284	SEG48	3157	240

PAD	NAME	X	Y
285	SEG49	3135	240
286	SEG50	3113	240
287	SEG51	3091	240
288	SEG52	3069	240
289	SEG53	3047	240
290	SEG54	3025	240
291	SEG55	3003	240
292	SEG56	2981	240
293	SEG57	2959	240
294	SEG58	2937	240
295	SEG59	2915	240
296	SEG60	2893	240
297	SEG61	2871	240
298	SEG62	2849	240
299	SEG63	2827	240
300	SEG64	2805	240
301	SEG65	2783	240
302	SEG66	2761	240
303	SEG67	2739	240
304	SEG68	2717	240
305	SEG69	2695	240
306	SEG70	2673	240
307	SEG71	2651	240
308	SEG72	2629	240
309	SEG73	2607	240
310	SEG74	2585	240
311	SEG75	2563	240
312	SEG76	2541	240
313	SEG77	2519	240
314	SEG78	2497	240
315	SEG79	2475	240
316	SEG80	2453	240
317	SEG81	2431	240
318	SEG82	2409	240
319	SEG83	2387	240
320	SEG84	2365	240

PAD	NAME	X	Y
321	SEG85	2343	240
322	SEG86	2321	240
323	SEG87	2299	240
324	SEG88	2277	240
325	SEG89	2255	240
326	SEG90	2233	240
327	SEG91	2211	240
328	SEG92	2189	240
329	SEG93	2167	240
330	SEG94	2145	240
331	SEG95	2123	240
332	SEG96	2101	240
333	SEG97	2079	240
334	SEG98	2057	240
335	SEG99	2035	240
336	SEG100	2013	240
337	SEG101	1991	240
338	SEG102	1969	240
339	SEG103	1947	240
340	SEG104	1925	240
341	SEG105	1903	240
342	SEG106	1881	240
343	SEG107	1859	240
344	SEG108	1837	240
345	SEG109	1815	240
346	SEG110	1793	240
347	SEG111	1771	240
348	SEG112	1749	240
349	SEG113	1727	240
350	SEG114	1705	240
351	SEG115	1683	240
352	SEG116	1661	240
353	SEG117	1639	240
354	SEG118	1617	240
355	SEG119	1595	240
356	SEG120	1573	240

PAD	NAME	X	Y
357	SEG121	1551	240
358	SEG122	1529	240
359	SEG123	1507	240
360	SEG124	1485	240
361	SEG125	1463	240
362	SEG126	1441	240
363	SEG127	1419	240
364	SEG128	1397	240
365	SEG129	1375	240
366	SEG130	1353	240
367	SEG131	1331	240
368	SEG132	1309	240
369	SEG133	1287	240
370	SEG134	1265	240
371	SEG135	1243	240
372	SEG136	1221	240
373	SEG137	1199	240
374	SEG138	1177	240
375	SEG139	1155	240
376	SEG140	1133	240
377	SEG141	1111	240
378	SEG142	1089	240
379	SEG143	1067	240
380	SEG144	1045	240
381	SEG145	1023	240
382	SEG146	1001	240
383	SEG147	979	240
384	SEG148	957	240
385	SEG149	935	240
386	SEG150	913	240
387	SEG151	891	240
388	SEG152	869	240
389	SEG153	847	240
390	SEG154	825	240
391	SEG155	803	240
392	SEG156	781	240

PAD	NAME	X	Y
393	SEG157	759	240
394	SEG158	737	240
395	SEG159	715	240
396	SEG160	693	240
397	SEG161	671	240
398	SEG162	649	240
399	SEG163	627	240
400	SEG164	605	240
401	SEG165	583	240
402	SEG166	561	240
403	SEG167	539	240
404	SEG168	517	240
405	SEG169	495	240
406	SEG170	473	240
407	SEG171	451	240
408	SEG172	429	240
409	SEG173	407	240
410	SEG174	385	240
411	SEG175	363	240
412	SEG176	341	240
413	SEG177	319	240
414	SEG178	297	240
415	SEG179	275	240
416	SEG180	253	240
417	SEG181	231	240
418	SEG182	209	240
419	SEG183	187	240
420	SEG184	165	240
421	SEG185	143	240
422	SEG186	121	240
423	SEG187	99	240
424	SEG188	77	240
425	SEG189	55	240
426	SEG190	33	240
427	SEG191	11	240
428	SEG192	-11	240

PAD	NAME	X	Y
429	SEG193	-33	240
430	SEG194	-55	240
431	SEG195	-77	240
432	SEG196	-99	240
433	SEG197	-121	240
434	SEG198	-143	240
435	SEG199	-165	240
436	SEG200	-187	240
437	SEG201	-209	240
438	SEG202	-231	240
439	SEG203	-253	240
440	SEG204	-275	240
441	SEG205	-297	240
442	SEG206	-319	240
443	SEG207	-341	240
444	SEG208	-363	240
445	SEG209	-385	240
446	SEG210	-407	240
447	SEG211	-429	240
448	SEG212	-451	240
449	SEG213	-473	240
450	SEG214	-495	240
451	SEG215	-517	240
452	SEG216	-539	240
453	SEG217	-561	240
454	SEG218	-583	240
455	SEG219	-605	240
456	SEG220	-627	240
457	SEG221	-649	240
458	SEG222	-671	240
459	SEG223	-693	240
460	SEG224	-715	240
461	SEG225	-737	240
462	SEG226	-759	240
463	SEG227	-781	240
464	SEG228	-803	240

PAD	NAME	X	Y
465	SEG229	-825	240
466	SEG230	-847	240
467	SEG231	-869	240
468	SEG232	-891	240
469	SEG233	-913	240
470	SEG234	-935	240
471	SEG235	-957	240
472	SEG236	-979	240
473	SEG237	-1001	240
474	SEG238	-1023	240
475	SEG239	-1045	240
476	SEG240	-1067	240
477	SEG241	-1089	240
478	SEG242	-1111	240
479	SEG243	-1133	240
480	SEG244	-1155	240
481	SEG245	-1177	240
482	SEG246	-1199	240
483	SEG247	-1221	240
484	SEG248	-1243	240
485	SEG249	-1265	240
486	SEG250	-1287	240
487	SEG251	-1309	240
488	SEG252	-1331	240
489	SEG253	-1353	240
490	SEG254	-1375	240
491	SEG255	-1397	240
492	SEG256	-1419	240
493	SEG257	-1441	240
494	SEG258	-1463	240
495	SEG259	-1485	240
496	SEG260	-1507	240
497	SEG261	-1529	240
498	SEG262	-1551	240
499	SEG263	-1573	240
500	SEG264	-1595	240

PAD	NAME	X	Y
501	SEG265	-1617	240
502	SEG266	-1639	240
503	SEG267	-1661	240
504	SEG268	-1683	240
505	SEG269	-1705	240
506	SEG270	-1727	240
507	SEG271	-1749	240
508	SEG272	-1771	240
509	SEG273	-1793	240
510	SEG274	-1815	240
511	SEG275	-1837	240
512	SEG276	-1859	240
513	SEG277	-1881	240
514	SEG278	-1903	240
515	SEG279	-1925	240
516	SEG280	-1947	240
517	SEG281	-1969	240
518	SEG282	-1991	240
519	SEG283	-2013	240
520	SEG284	-2035	240
521	SEG285	-2057	240
522	SEG286	-2079	240
523	SEG287	-2101	240
524	SEG288	-2123	240
525	SEG289	-2145	240
526	SEG290	-2167	240
527	SEG291	-2189	240
528	SEG292	-2211	240
529	SEG293	-2233	240
530	SEG294	-2255	240
531	SEG295	-2277	240
532	SEG296	-2299	240
533	SEG297	-2321	240
534	SEG298	-2343	240
535	SEG299	-2365	240
536	SEG300	-2387	240

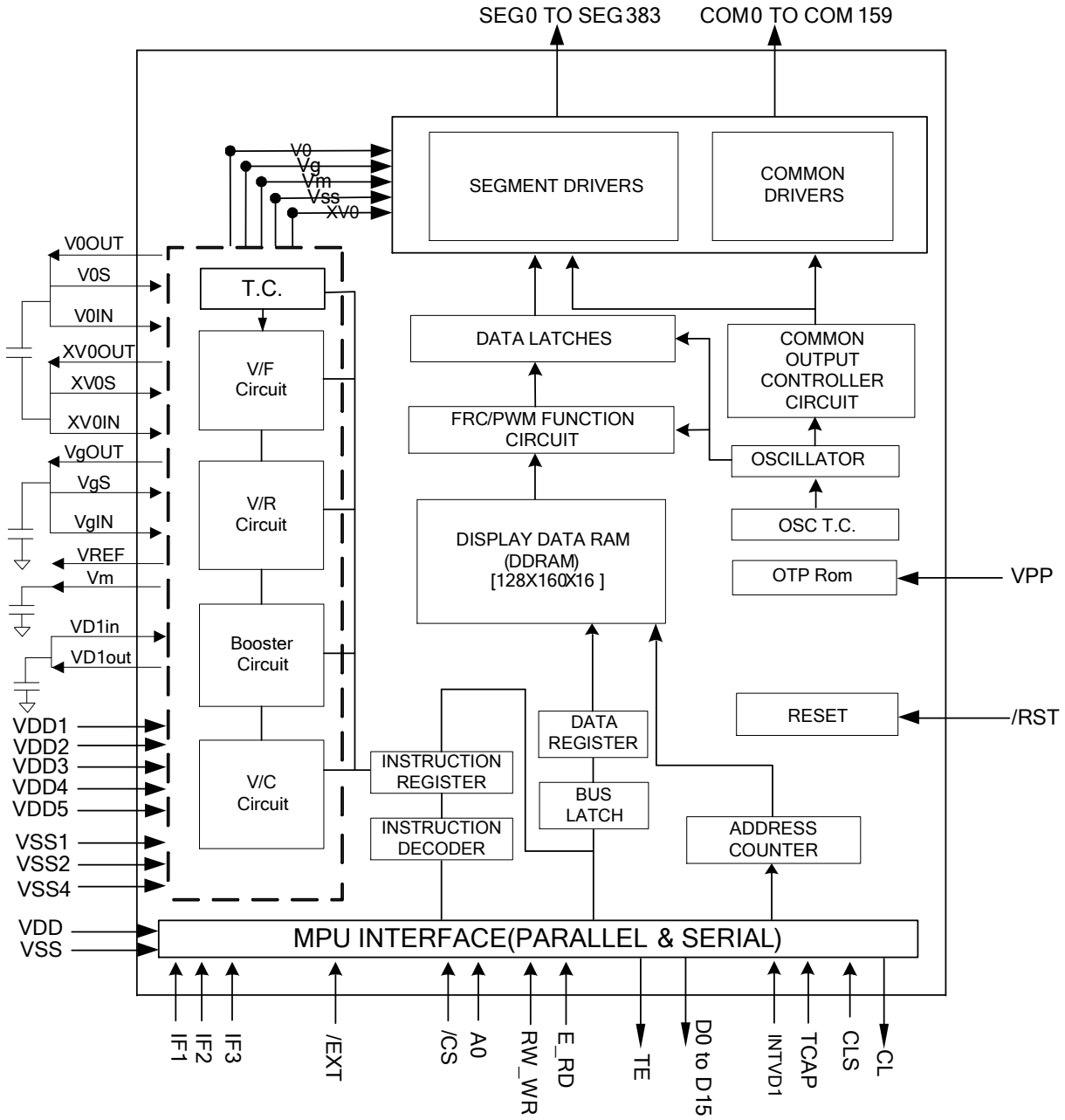
PAD	NAME	X	Y
537	SEG301	-2409	240
538	SEG302	-2431	240
539	SEG303	-2453	240
540	SEG304	-2475	240
541	SEG305	-2497	240
542	SEG306	-2519	240
543	SEG307	-2541	240
544	SEG308	-2563	240
545	SEG309	-2585	240
546	SEG310	-2607	240
547	SEG311	-2629	240
548	SEG312	-2651	240
549	SEG313	-2673	240
550	SEG314	-2695	240
551	SEG315	-2717	240
552	SEG316	-2739	240
553	SEG317	-2761	240
554	SEG318	-2783	240
555	SEG319	-2805	240
556	SEG320	-2827	240
557	SEG321	-2849	240
558	SEG322	-2871	240
559	SEG323	-2893	240
560	SEG324	-2915	240
561	SEG325	-2937	240
562	SEG326	-2959	240
563	SEG327	-2981	240
564	SEG328	-3003	240
565	SEG329	-3025	240
566	SEG330	-3047	240
567	SEG331	-3069	240
568	SEG332	-3091	240
569	SEG333	-3113	240
570	SEG334	-3135	240
571	SEG335	-3157	240
572	SEG336	-3179	240

PAD	NAME	X	Y
573	SEG337	-3201	240
574	SEG338	-3223	240
575	SEG339	-3245	240
576	SEG340	-3267	240
577	SEG341	-3289	240
578	SEG342	-3311	240
579	SEG343	-3333	240
580	SEG344	-3355	240
581	SEG345	-3377	240
582	SEG346	-3399	240
583	SEG347	-3421	240
584	SEG348	-3443	240
585	SEG349	-3465	240
586	SEG350	-3487	240
587	SEG351	-3509	240
588	SEG352	-3531	240
589	SEG353	-3553	240
590	SEG354	-3575	240
591	SEG355	-3597	240
592	SEG356	-3619	240
593	SEG357	-3641	240
594	SEG358	-3663	240
595	SEG359	-3685	240
596	SEG360	-3707	240
597	SEG361	-3729	240
598	SEG362	-3751	240
599	SEG363	-3773	240
600	SEG364	-3795	240
601	SEG365	-3817	240
602	SEG366	-3839	240
603	SEG367	-3861	240
604	SEG368	-3883	240
605	SEG369	-3905	240
606	SEG370	-3927	240
607	SEG371	-3949	240
608	SEG372	-3971	240

PAD	NAME	X	Y
609	SEG373	-3993	240
610	SEG374	-4015	240
611	SEG375	-4037	240
612	SEG376	-4059	240
613	SEG377	-4081	240
614	SEG378	-4103	240
615	SEG379	-4125	240
616	SEG380	-4147	240
617	SEG381	-4169	240
618	SEG382	-4191	240
619	SEG383	-4213	240
620	COM158	-4329.33	240
621	COM156	-4351.33	240
622	COM154	-4373.33	240
623	COM152	-4395.33	240
624	COM150	-4417.33	240
625	COM148	-4439.33	240
626	COM146	-4461.33	240
627	COM144	-4483.33	240
628	COM142	-4505.33	240
629	COM140	-4527.33	240
630	COM138	-4549.33	240
631	COM136	-4571.33	240
632	COM134	-4593.33	240
633	COM132	-4615.33	240
634	COM130	-4637.33	240
635	COM128	-4659.33	240
636	COM126	-4681.33	240
637	COM124	-4703.33	240
638	COM122	-4725.33	240
639	COM120	-4747.33	240
640	COM118	-4769.33	240
641	COM116	-4791.33	240
642	COM114	-4813.33	240
643	COM112	-4835.33	240
644	COM110	-4857.33	240

PAD	NAME	X	Y
645	COM108	-4879.33	240
646	COM106	-4901.33	240
647	COM104	-4923.33	240
648	COM102	-4945.33	240
649	COM100	-4967.33	240
650	COM98	-4989.33	240
651	COM96	-5011.33	240
652	COM94	-5033.33	240
653	COM92	-5055.33	240
654	COM90	-5077.33	240
655	COM88	-5099.33	240
656	COM86	-5121.33	240
657	COM84	-5143.33	240
658	COM82	-5165.33	240
659	COM80	-5187.33	240
660	COM78	-5209.33	240
661	COM76	-5231.33	240
662	COM74	-5253.33	240
663	COM72	-5275.33	240
664	COM70	-5297.33	240
665	COM68	-5319.33	240
666	COM66	-5341.33	240
667	COM64	-5363.33	240
668	COM62	-5385.33	240
669	COM60	-5407.33	240
670	COM58	-5429.33	240
671	COM56	-5451.33	240
672	COM54	-5473.33	240
673	COM52	-5495.33	240
674	COM50	-5517.33	240
675	COM48	-5539.33	240
676	COM46	-5561.33	240
677	COM44	-5583.33	240
678	COM42	-5605.33	240
679	COM40	-5627.33	240
680	COM38	-5649.33	240

5. BLOCK DIAGRAM



6. PIN DESCRIPTION

6.1. Power Supply

Name	I/O	Description
VDD	Supply	Power supply for logic circuit.
VDD1	Supply	Power supply for OSC circuit.
VDD2	Supply	Power supply for booster circuit.
VDD3	Supply	Power supply for LCD.
VDD4	Supply	Power supply for LCD.
VDD5	Supply	Power supply for LCD.
VSS	Supply	Ground for logic circuit. Ground system should be connected together.
VSS1	Supply	Ground for OSC circuit. Ground system should be connected together.
VSS2	Supply	Ground for Booster Circuit. Ground system should be connected together.
VSS4	Supply	Ground for LCD. Ground system should be connected together.

6.2. LCD Power Supply Pins

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>$V0_{OUT}$
$V0_{IN}$
$V0_S$</td><td>I/O</td><td>Positive LCD driver supply voltages.
$V0_{OUT}$ is the output voltage of V0 generated by ST7689.
$V0_{IN}$ is the input pin of power supply to generate V0 voltage for LCD.
$V0_S$ is the input pin of power supply to sense the V0 voltage.
$V0_{OUT}$, $V0_{IN}$ & $V0_S$ should be connected together in FPC.</td></tr>
<tr><td>$XV0_{OUT}$
$XV0_{IN}$
$XV0_S$</td><td>I/O</td><td>Negative LCD driver supply voltages.
$XV0_{OUT}$ is the output voltage of XV0 generated by ST7689.
$XV0_{IN}$ is the input pin of power supply to generate XV0 voltage for LCD.
$XV0_S$ is the input pin of power supply to sense the XV0 voltage.
$XV0_{OUT}$, $XV0_{IN}$ & $XV0_S$ should be connected together in FPC.</td></tr>
<tr><td>Vg_{OUT}
Vg_{IN}
Vg_S
Vm</td><td>I/O</td><td>Bias LCD driver supply voltages.
Vg_{OUT} is the output voltage of Vg generated by ST7689.
Vg_{IN} is the input pin of power supply to generate Vg voltage for LCD.
Vg_S is the input pin of power supply to sense the Vg voltage.
Vg_{OUT}, Vg_{IN} & Vg_S should be connected together in FPC.
Vm is the I/O pin of LCD bias supply voltage.
Voltages should have the following relationship;
V0≧ Vg ≧ Vm ≧ VSS ≧ XV0
VDDA-0.7V>Vm>0.7V
VDDA≧2.5V: (2xVDDA)-0.6V≧Vg ≧1.8V
VDDA< 2.5V: (2xVDDA)-0.6V≧Vg ≧2.5V
When the internal power circuit is active, these voltages are generated as following table according to the state of LCD bias.
<table><tr><th>LCD bias</th><th>Vg</th><th>Vm</th></tr><tr><td>1/N bias</td><td>(2/N) x V0</td><td>(1/N) x V0</td></tr></table>
NOTE: N = 9,10,11,12,13 and 14</td></tr>
<tr><td>$VD1_{out}$
$VD1_{in}$</td><td>I/O</td><td>Voltage regulator for digital circuit.
$VD1_{out}$ is voltage output from regulator circuit.
$VD1_{in}$ is voltage input to digital circuit.
$VD1_{in}$ and $VD1_{out}$ should be connected together by FPC.</td></tr>
</table>

6.3. System Control

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>CLS</td><td>I</td><td>Reserved for testing only.
Please fix this pin to VDDI.</td></tr>
<tr><td>CL</td><td>O</td><td>Reserved for testing only. Leave this pin open.</td></tr>
<tr><td>TCAP</td><td>O</td><td>Reserved for testing only. Leave this pin open.</td></tr>
<tr><td>VREF</td><td>O</td><td>Reserved for testing only. Leave this pin open.</td></tr>
<tr><td>VPP</td><td>I</td><td>When writing PROM, it needs outer power supply voltage 6.5~6.75V (>8mA) input to write successfully.</td></tr>
<tr><td>INTVD1</td><td>I</td><td>
<table>
<tr><th>Typical VDDI</th><th>Tolerance</th><th>Capacitor of VD1 to VSS</th><th>Level of INTVD1</th></tr>
<tr><td>1.8V</td><td rowspan="2">1.65V~2.9V</td><td>Unnecessary</td><td>VSS</td></tr>
<tr><td>2.8V</td><td>Unnecessary</td><td>VSS</td></tr>
<tr><td>3.0V</td><td rowspan="2">2.9V~3.3V</td><td>necessary</td><td>VDD</td></tr>
<tr><td>3.3V</td><td>necessary</td><td>VDD</td></tr>
</table>
</td></tr>
</table>

6.4. Microprocessor Interface

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>/RST</td><td>I</td><td>Reset input pin. When RST is “L”, and initialization is executed.</td></tr>
<tr><td>IF[3:1]</td><td>I</td><td>Parallel / Serial data input select input
<table>
<tr><th>IF3</th><th>IF2</th><th>IF1</th><th>MPU interface type</th></tr>
<tr><td>H</td><td>H</td><td>H</td><td>80 series 16-bit parallel</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>80 series 8-bit parallel</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>68 series 16-bit parallel</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>68 series 8-bit parallel</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>8-bit serial (4 line)</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>9-bit serial (3 line)</td></tr>
</table>
Note:
1. When fixing IF2=H & IF1=L, IF3 can be defined as parallel/Serial selection pin.
IF3=H: Parallel interface (80 8-bit); IF3=L: Serial interface (3-line)
2. Refer to Table 1.for detail interface connection.</td></tr>
<tr><td>/CS</td><td>I</td><td>Chip select input pin.
Data / Instruction I/O is enabled only when /CS is "L". When chip select is non-active, D0 to D15 become high impedance.</td></tr>
<tr><td>A0</td><td>I</td><td>Register select input pin
A0 = "H": D0 to D15 or SI are display data
A0 = "L": D0 to D15 or SI are control data
** In 3-line/4-line interface this pad will be used for SCL function</td></tr>
<tr><td>RW_WR</td><td>I</td><td>Read / Write execution control pin. (This pin is only used in parallel interface)
<table>
<tr><th>MPU type</th><th>RW_WR</th><th>Description</th></tr>
<tr><td>6800-series</td><td>RW</td><td>Read / Write control input pin
RW = “H” : read
RW = “L” : write</td></tr>
<tr><td>8080-series</td><td>/WR</td><td>Write enable clock input pin.
The data on D0 to D15 are latched at the rising edge of the /WR signal.</td></tr>
</table>
When in the serial interface, connect it to VDDI.</td></tr>
<tr><td>E_RD</td><td>I</td><td>Read / Write execution control pin. (This pin is only used in parallel interface)
<table>
<tr><th>MPU Type</th><th>E_RD</th><th>Description</th></tr>
<tr><td>6800-series</td><td>E</td><td>Read / Write control input pin
RW= “H”: If E is “H”, D0 to D15 are in an output status.
RW = “L”: The data on D0 to D15 are latched at the falling edge of the E signal.</td></tr>
</table></td></tr>
</table>

<table>
<tr><td></td><td></td><td><table><tr><td>8080-series</td><td>/RD</td><td>Read enable clock input pin
When /RD is “L”, D0 to D15 are in an output status.</td></tr></table>When in the serial interface, connect it to VDDI.</td></tr>
<tr><td>D15 to D0</td><td>I/O</td><td>They connect to the standard 8-bit or 16 bit MPU bus via the 8/16 –bit bi-directional bus.
When the following interface is selected and the /CS pin is high, the following pins become high impedance.
1. In 8-bit parallel: D15-D8 pins are in the state of high impedance should connect to VDDI.
2. In 3-line/4-line interface D0 pad will be used for SI function
3. In 4-line interface D1 pad will be used for A0 function
4. In Serial interface: no-used pins are in the state of high impedance should connect to VDDI.</td></tr>
<tr><td>SI</td><td>I</td><td>SI is used to input serial data when the serial interface is selected.(3 line and 4 line)
In ST7689, D0 is the SI when select serial interface. See Table 1.</td></tr>
<tr><td>SCL</td><td>I</td><td>SCL is used to input serial clock when the serial interface is selected.
The data is converted in the rising edge. (3 line and 4 line)
In ST7689, A0 is the SCL when select serial interface. See Table 1.</td></tr>
<tr><td>TE</td><td>O</td><td>Tearing effect output.</td></tr>
<tr><td>/EXT</td><td>I</td><td>PROM burn-in control pin.
When burning PROM, please add an external VSS on /EXT.
When ST7689 is normal operation, please let it open.
There is a pull-high resistor between /EXT & VDDI in ST7689.</td></tr>
</table>

NOTE：1. In any status the control bus and data bus can’t be floating.

2. The no-used pins should connect to VDDI (Supply Digital Voltage)

6.5. LCD DRIVER OUTPUTS

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>SEG0
to
SEG383</td><td>O</td><td>LCD segment driver outputs
The display data and the M signal control the output voltage of segment driver.
<table>
<tr><th rowspan="2">Display data</th><th rowspan="2">M (Internal)</th><th colspan="2">Segment driver output voltage</th></tr>
<tr><th>Normal display</th><th>Reverse display</th></tr>
<tr><td>H</td><td>H</td><td>Vg</td><td>VSS</td></tr>
<tr><td>H</td><td>L</td><td>VSS</td><td>Vg</td></tr>
<tr><td>L</td><td>H</td><td>VSS</td><td>Vg</td></tr>
<tr><td>L</td><td>L</td><td>Vg</td><td>VSS</td></tr>
<tr><td colspan="2">Sleep-In mode</td><td>VSS</td><td>VSS</td></tr>
</table></td></tr>
<tr><td>COM0
to
COM159</td><td>O</td><td>LCD common driver outputs
The internal scanning data and M signal control the output voltage of common driver.
<table>
<tr><th>Scan data</th><th>M (Internal)</th><th>Common driver output voltage</th></tr>
<tr><td>H</td><td>H</td><td>XV0</td></tr>
<tr><td>H</td><td>L</td><td>V0</td></tr>
<tr><td>L</td><td>H</td><td>Vm</td></tr>
<tr><td>L</td><td>L</td><td>Vm</td></tr>
<tr><td colspan="2">Sleep-In mode</td><td>VSS</td></tr>
</table></td></tr>
</table>

Driving Waveform

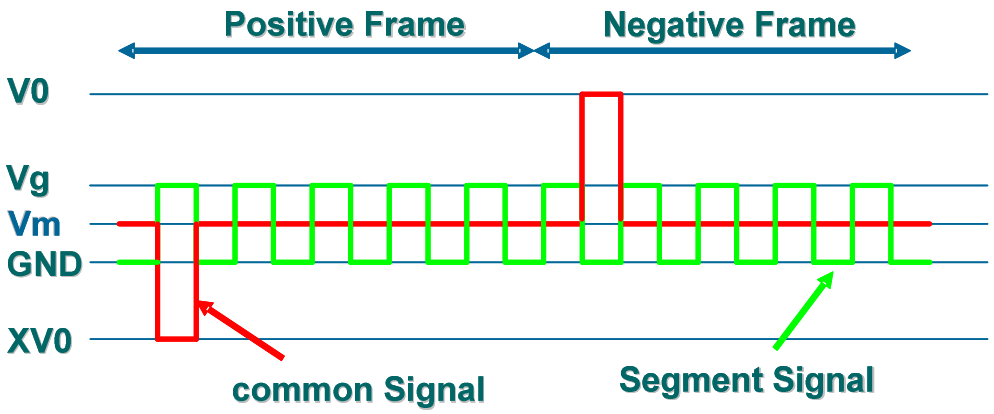


Figure 1 ST7689 COM/SEG Driving Waveform

ST7689 I/O PIN ITO Resister Limitation

Pin Name	ITO Resister
VDD, VDD1, VDD2~VDD5, VSS, VSS1, VSS2, VSS4, $VD1_{IN}$, $VD1_{OUT}$	<100Ω
$V0_{IN}$, $V0_{OUT}$, $V0_S$,$XV0_{IN}$, $XV0_{OUT}$,$XV0_S$, Vg_{IN}, Vg_{OUT} ,Vg_S ,Vm	<300Ω
VPP	<50Ω
A0, E_RD, RW_WR, /CS, D0 …D15, (SI), (SCL), TE	<1KΩ
/RST	<10KΩ
IF[3:1], CLS, /EXT, INTVD1	<1KΩ
TCAP, CL, VREF	Floating

NOTE: 1. Make sure that the ITO resistance of COM0 ~ COM159 is equal, and so is it of SEG0 ~ SEG383. These limitations include the bottleneck of ITO layout.

2. The ITO layout suggestion is shown as below:

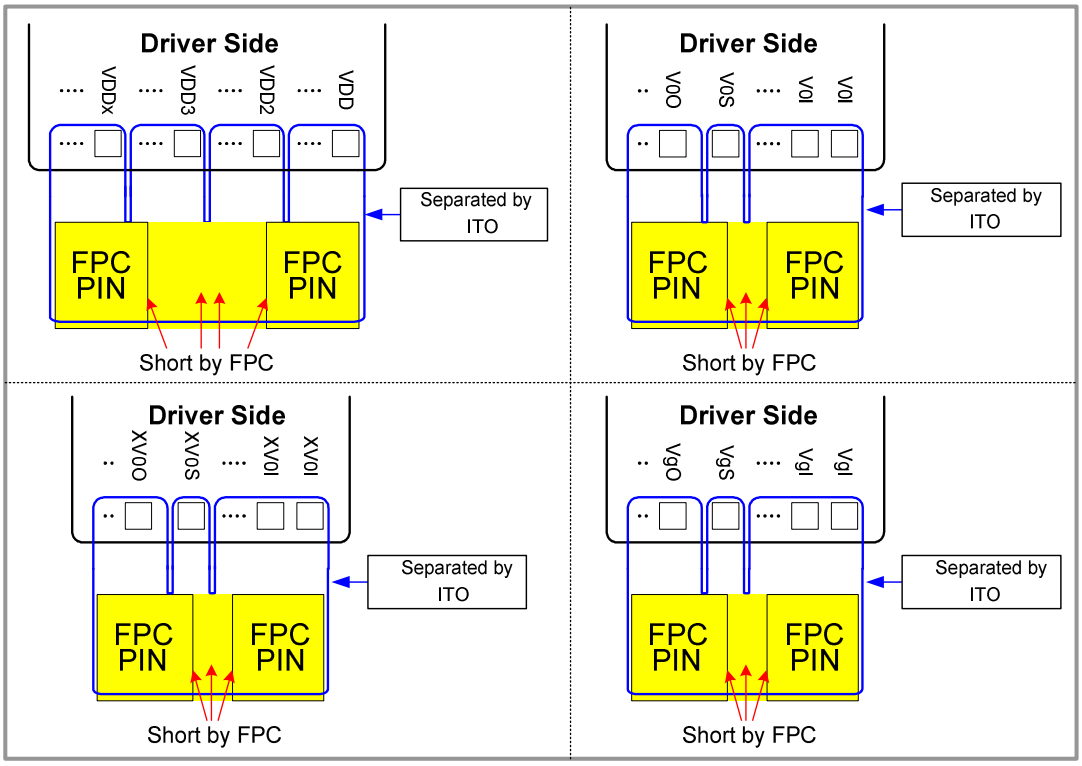


Figure 2 Power ITO layout suggestion

7. FUNCTIONAL DESCRIPTION

7.1. Microprocessor Interface

Chip Select Input

/CS pin is for chip selection. The ST7689 is active when /CS=L. In serial interface mode, the internal shift register and the counter are reset when /CS=H.

7.1.1. Selecting Parallel / Serial Interface

ST7689 has six types of interface with an MPU, which are two serial and four parallel interfaces. This parallel or serial interface is determined by IF pin as shown in Table 1.

Table 1 Parallel / Serial Interface Mode

I/F Mode			I/F Description	Pin Assignment						
IF3	IF2	IF1		/CS	A0	E_RD	RW_WR	Used Data Bus	D1	D0
H	H	L	80 serial 8-bit parallel	/CS	A0	/RD	/WR	D7~D2	D1	D0
H	H	H	80 serial 16-bit parallel	/CS	A0	/RD	/WR	D15~D2	D1	D0
H	L	L	68 serial 8-bit parallel	/CS	A0	E	R/W	D7~D2	D1	D0
H	L	H	68 serial 16-bit parallel	/CS	A0	E	R/W	D15~D2	D1	D0
L	H	H	8-bit SPI mode (4 line)	/CS	SCL	--	--	--	A0	SI
L	H	L	9-bit SPI mode (3 line)	/CS	SCL	--	--	--	---	SI

NOTE: When these pins are set to any other combination, A0, E_RD and RW_WR inputs are disabled and D0 to D15 are to be high impedance.

7.1.2. 8-bit or 16-bit Parallel Interface

The ST7689 identifies the type of the data bus signals according to the combination of A0, /RD (E) and /WR (W/R) signals, as shown in Table 2.

Table 2 Parallel Data Transfer

Common	6800-series		8080-series		Description
A0	R/W	E	/RD	/WR	
H	H	↑	↓	H	Display data read out
H	H	↑	↓	H	Register status read
L	L	↓	H	↑	Instruction write
H	L	↓	H	↑	Display data write

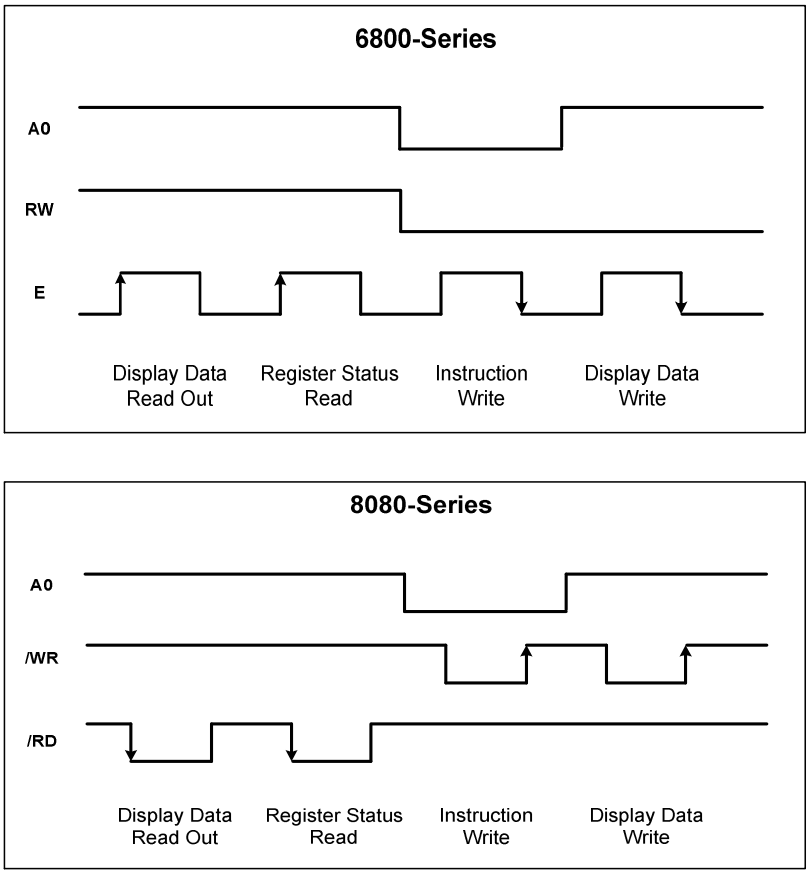


Figure 3 Parallel Data Transfer Example Chart

Relation between Data Bus and Gradation Data

ST7689 offers 256 color display, 4096 color display, 65K color display, and 262K color display. When using 256 colors, 4096, 65K, and 262K display; you can specify color for each of R, G, and B using the palette function. Use the command for switching between these modes.

(1) 256 color input mode

8-bit interface

D7, D6, D5, D4, D3, D2, D1, D0: RRRGGGBB 1st -write

There is only 1 write operation for 1 pixel data.

1 pixel data is written in the display data RAM when 1st -write operation finishes.

(2) 4096-color display

1. 8-bit mode

D7, D6, D5, D4, D3, D2, D1, D0: RRRRGGGG 1st-write

D7, D6, D5, D4, D3, D2, D1, D0: BBBBRRRR 2nd-write

D7, D6, D5, D4, D3, D2, D1, D0: GGGGBBBB 3rd-write

There are 3 write operations for 2 pixel data.

1st pixel data is written in the display data RAM when 2nd –write operation finishes, and 2nd pixel data is written in the display data RAM when 3rd–write operation finishes.

2. 16-bit mode

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: RRRRGGGGBBBBXXXX 1st-write

There is only 1 write operation for 1 pixel data.

1 pixel data is written in the display data RAM when 1st –write operation finishes. "X" are ignored dummy bits.

(3) 65K color input mode

1. 8-bit mode

D7, D6, D5, D4, D3, D2, D1, D0: RRRRRGGG 1st-write

D7, D6, D5, D4, D3, D2, D1, D0: GGGBBBBB 2nd-write

There are 2 write operations for 1 pixel data.

1st pixel data is written in the display data RAM when 2nd –write operation finishes.

2. 16-bit mode

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: RRRRRGGGGGGBBBBB

There is only 1 write operation for 1 pixel data.

1 pixel data is written in the display data RAM when 1st –write operation finishes.

(4) Truncated 262K color input mode

1. 8-bit mode

D7, D6, D5, D4, D3, D2, D1, D0: RRRRRRXX 1st-write

D7, D6, D5, D4, D3, D2, D1, D0: GGGGGGXX 2nd-write

D7, D6, D5, D4, D3, D2, D1, D0: BBBBBBXX 3rd-write

There are 3 write operations for 1 pixel data.

1st pixel data is written in the display data RAM when 3rd–write operation finishes. "X" are ignored dummy bits.

2. 16 bit mode

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: RRRRRRXXGGGGGGXX 1st-write

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: BBBBBBXXXXXXXXXXXX 2nd-write

There are 2 write operations for 1 pixel data.

1st pixel data is written in the display data RAM when 2nd –write operation finishes. "X" are ignored dummy bits.

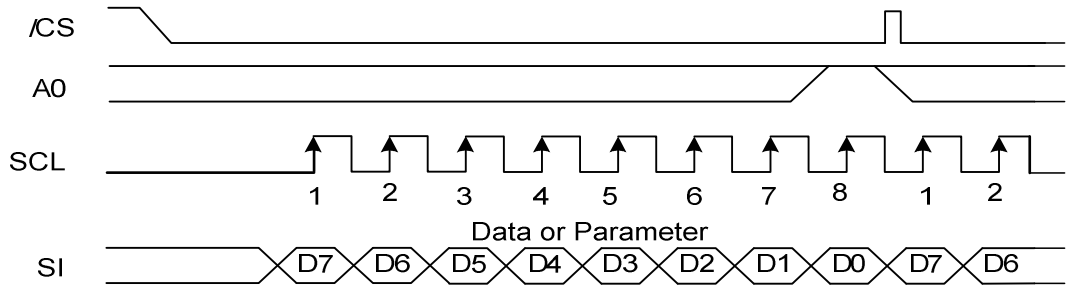
7.1.3. 8- and 9-bit Serial Interface

The 8-bit serial interface uses four pins /CS, SI, SCL, and A0 to enter commands and data. Meanwhile, the 9-bit serial interface uses three pins /CS, SI and SCL for the same purpose.

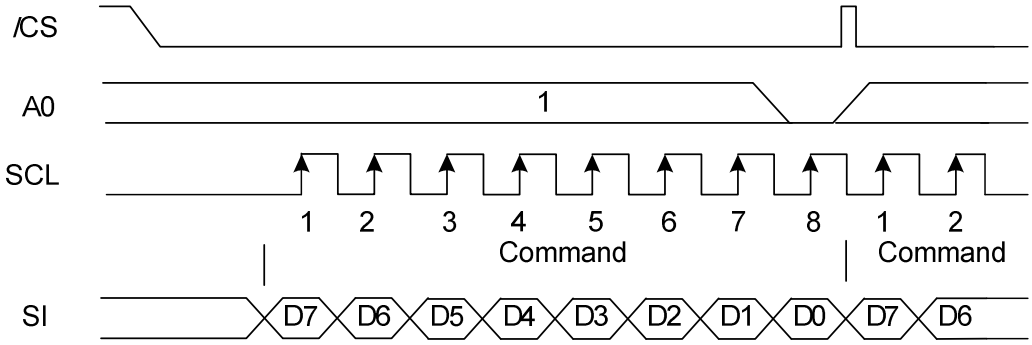
Data read is not available in the serial interface. Data entered must be 8 bits. The relation between gray-scale data and data bus in the serial input is the same as that in the 8-bit parallel interface mode at every gradation.

(1) 8-bit serial interface (4-line)

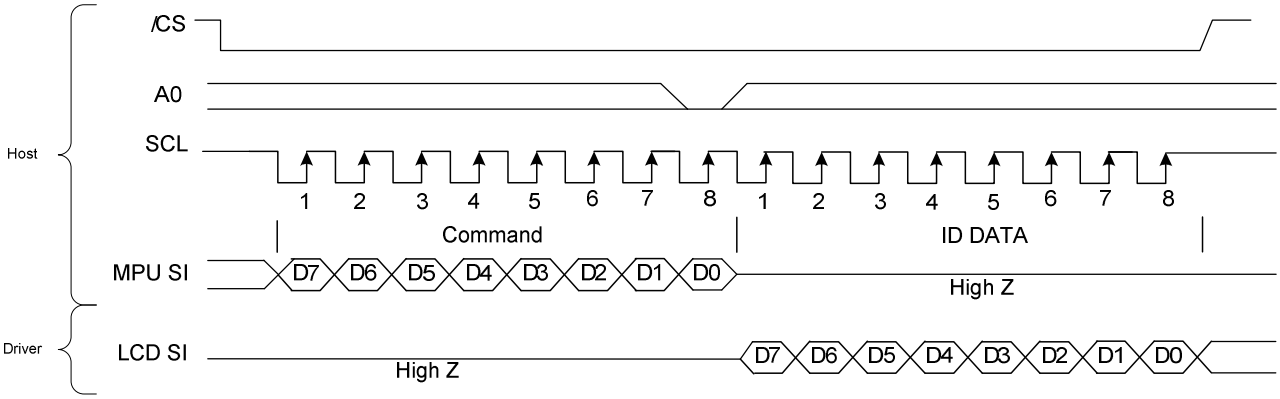
When entering data (parameters): A0= HIGH at the rising edge of the 8th SCL.



When entering command: A0= LOW at the rising edge of the 8th SCL

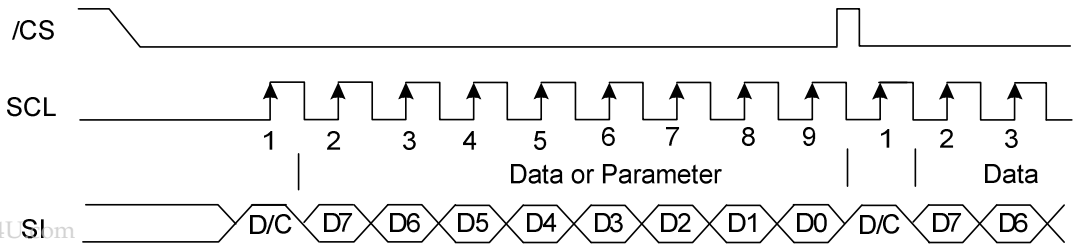


When entering reading command:

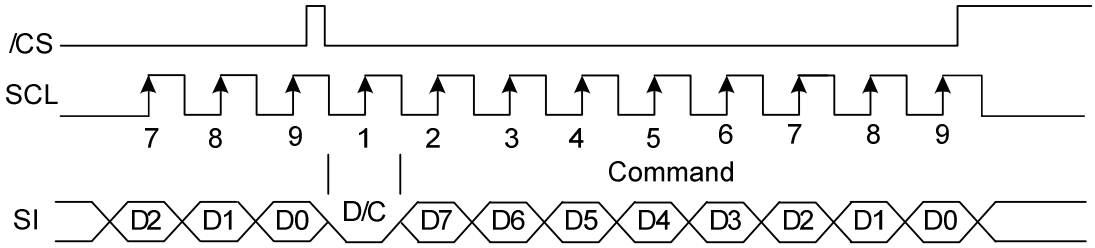


(2) 9-bit serial interface (3-line)

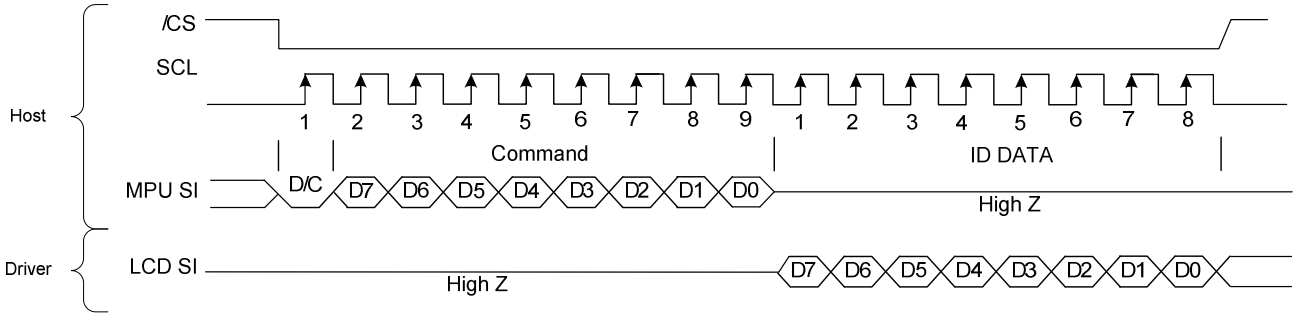
When entering data (parameters): SI= HIGH at the rising edge of the 1st SCL.



When entering command: SI= LOW at the rising edge of the 1st SCL.



When entering reading command :



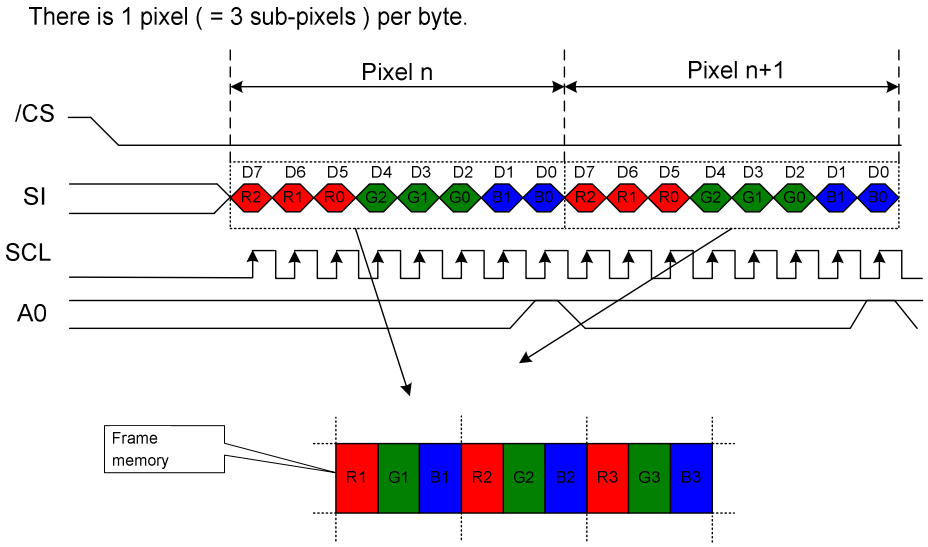
- If /CS is set to HIGH while the 8 bits from D7 to D0 are entered, the data concerned is invalidated. Before entering succeeding sets of data, you must correctly input the data concerned again.
- In order to avoid data transfer error due to incoming noise, it is recommended to set /CS at HIGH on byte basis to initialize the serial-to-parallel conversion counter and the register.

7.1.4. 8-bit and 9-bit Serial Interface Data Color Coding

8-bit serial interface (4-line)

(1) R 3-bit, G 3-bit, B 2-bit, 256 colors

There is 1 pixel (= 3 sub-pixels) per byte.

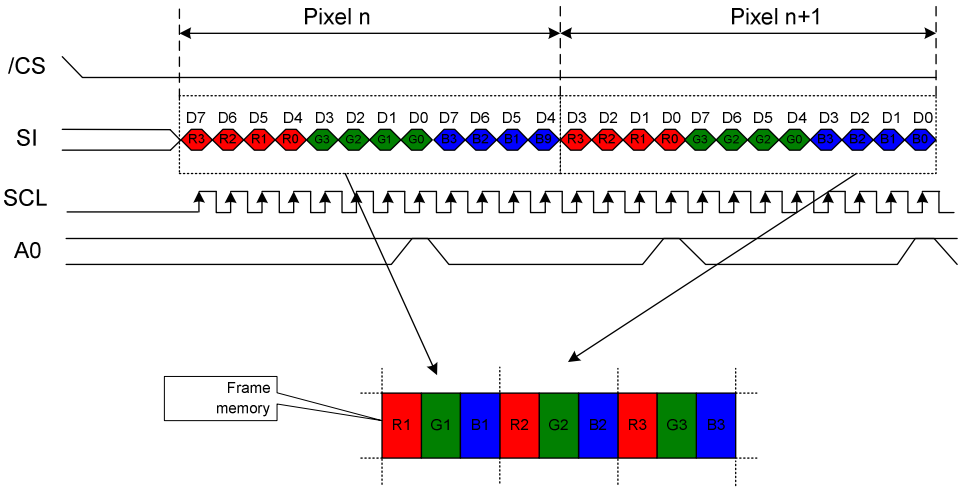


Note: R2, G2, B1 are the most significant bits and R0, G0, B0 are the least significant bits.

(2) R 4-bit, G 4-bit, B 4-bit, 4,096 colors

There are 2 pixel (= 3 sub-pixels) per 3 byte.

There are 2 pixel (= 3 sub-pixels) per 3 byte.

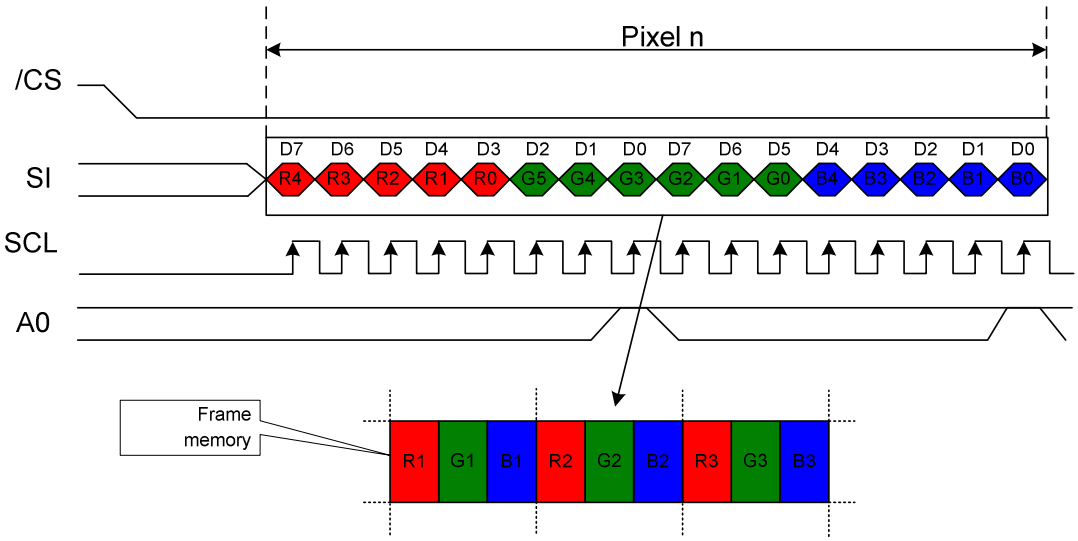


Note: R3, G3, B3 are the most significant bits and R0, G0, B0 are the least significant bits.

(3) R 5-bit, G 6-bit, B 5-bit, 65,536 colors

There is 1 pixel (= 3 sub-pixels) per 2 byte.

There is 1 pixel (= 3 sub-pixels) per 2 byte.



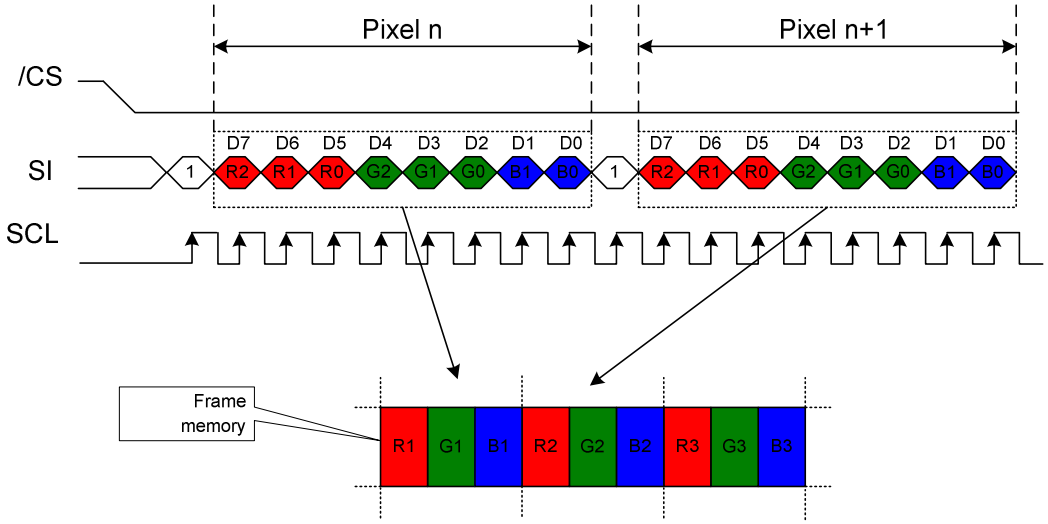
Note: R4, G5, B4 are the most significant bits and R0, G0, B0 are the least significant bits.

9-bit serial interface (3-line)

(1) R 3-bit, G 3-bit, B 2-bit, 256 colors

There is 1 pixel (= 3 sub-pixels) per byte.

There is 1 pixel (= 3 sub-pixels) per byte.

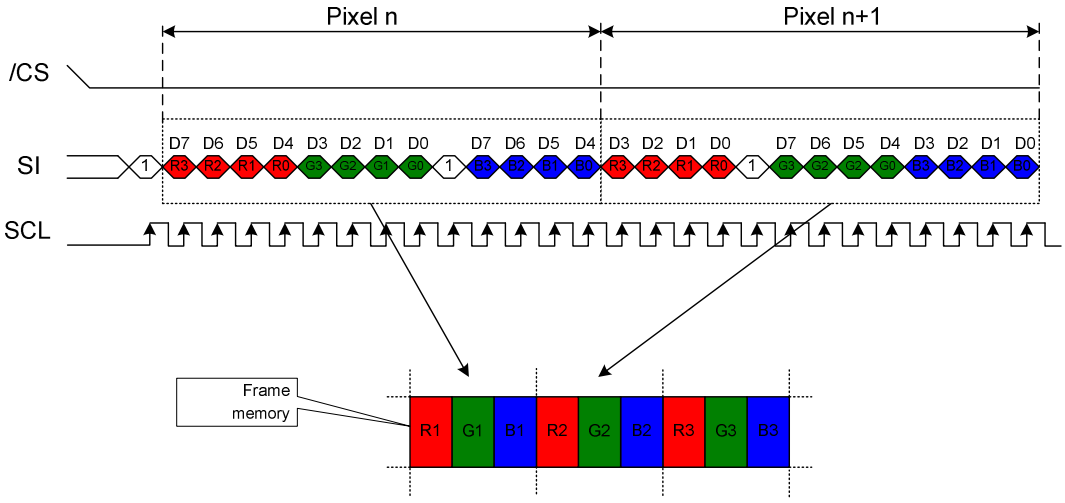


Note: R2, G2, B1 are the most significant bits and R0, G0, B0 are the least significant bits.

(2) R 4-bit, G 4-bit, B 4-bit, 4,096 colors

There are 2 pixel (= 3 sub-pixels) per 3 byte.

There are 2 pixel (= 3 sub-pixels) per 3 byte.

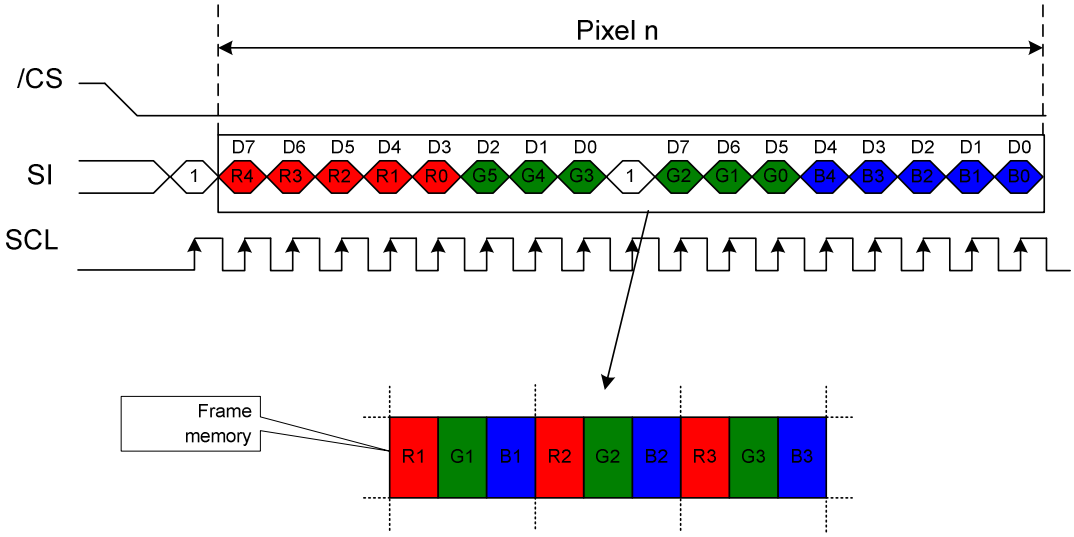


Note: R3, G3, B3 are the most significant bits and R0, G0, B0 are the least significant bits.

(3) R 5-bit, G 6-bit, B 5-bit, 65,536 colors

There is 1 pixel (= 3 sub-pixels) per 2 byte.

There is 1 pixel (= 3 sub-pixels) per 2 byte.



Note: R4, G5, B4 are the most significant bits and R0, G0, B0 are the least significant bits.

7.2. Access to DDRAM and Internal Registers

ST7689 realizes high-speed data transfer because the access from MPU is a sort of pipeline processing done via the bus holder attached to the internal, requiring the cycle time alone without needing the wait time.

For example, when MPU writes data to the DDRAM, the data is once held by the bus holder and then written to the DDRAM before the succeeding write cycle is started. When MPU reads data from the DDRAM, the first read cycle is dummy and the bus holder holds the data read in the dummy cycle, and then it read from the bus holder to the system bus in the succeeding read cycle. Figure 4 illustrates these relations.

In 80-series interface mode:

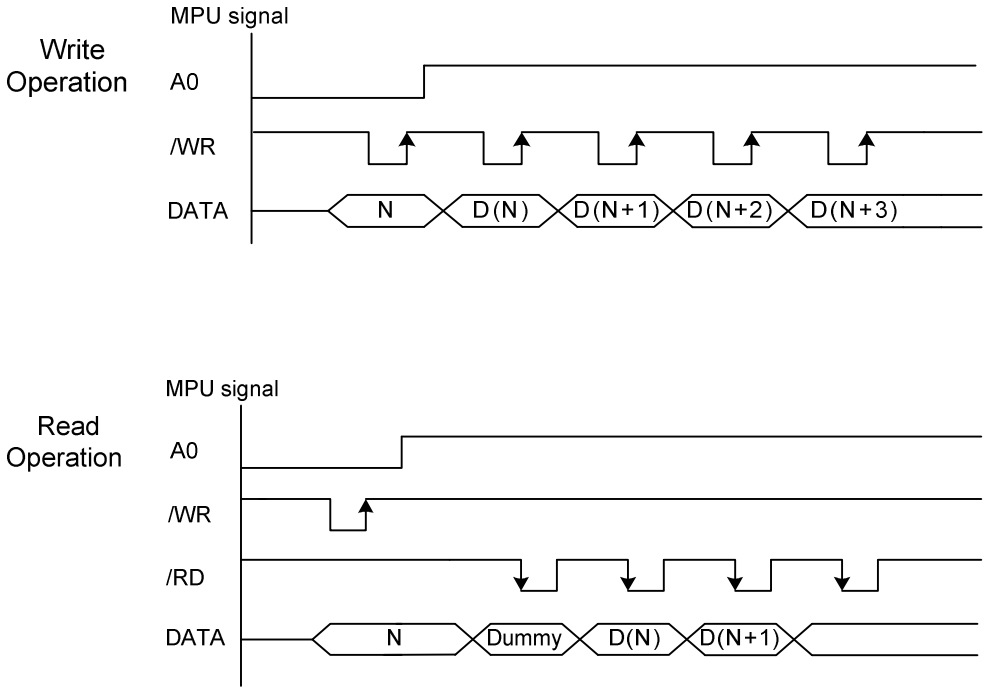


Figure 4 Write / Read Operation between MPU and ST7689

7.3. Display Data RAM (DDRAM)

7.3.1. DDRAM

It is 128 X 160 X 16 bits capacity RAM prepared for storing dot data. Refer to the following memory map for the RAM configuration.

Memory Map

RGB alignment												
Data control command			Column									
	(MADCTL) MX=0		0		1		…		127			
	(MADCTL) MX=1		127		126		…		0			
	Color		R	G	B	R	G	B		R	G	B
	Data / Page											
	(MADCTL) MY=0	(MADCTL) MY=1										
	0	159										
	1	158										
	2	157										
	3	156										
	4	155										
	5	154										
	6	:										
	7	:										
	:	:										
	:	7										
	:	6										
	154	5										
	155	4										
	156	3										
	157	2										
	158	1										
	159	0										
SEGout			0	1	2	3	4	5	…	381	382	383

Note:You can change position of R and B with MADCTL command.

7.3.2. Address Control

The address counter sets the addresses of the display data RAM for writing.

Data is written pixel into the RAM matrix of ST7689. The data for one pixel or two pixels is collected (RGB 5-6-5 bit), according to the data formats. As soon as this pixel-data information is complete, the “Write access” is activated on the RAM. The locations of RAM are addressed by the address pointers. The address ranges are X=0 to X=127 (7Fh) and Y=0 to Y=159 (9Fh). Addresses outside these ranges are not allowed.

Before writing to the RAM, a window must be defined into which will be written. The window is programmable via the command registers XS, YS designating the start address and XE, YE designating the end address.

For example the whole display contents will be written, the window is defined by the following values: XS=0 (0h) YS=0 (0h) and XE=127 (7Fh), YE=159 (9Fh).

In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (MV=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to SC and Y increments to address the next row. After the every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS). For flexibility in handling a wide variety of display architectures, the commands “CASET, RASET” and “MADCTL”, define flags MX, MY and MV, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Figure 5 show the available combinations of writing to the display RAM. When MX, MY and MV will be changed the data must be rewritten to the display RAM.

For each image condition, the controls for the column and row counters apply as below:

Condition	Column Counter	Row Counter
When RAMWR command is accepted	Return to “Start Column (XS)”	Return to “Start Row (YS)”
Complete Pixel Read / Write action	Increment by 1	No change
The Column counter value is larger than “End Column (XE)”	Return to “Start Column (XS)”	Increment by 1
The Row counter value is larger than “End Row (YE)”	Return to “Start Column (XS)”	Return to “Start Row (YS)”

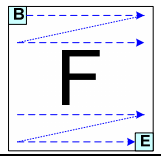
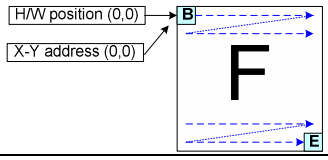
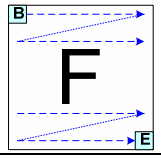
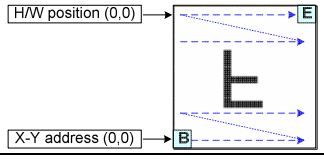
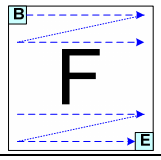
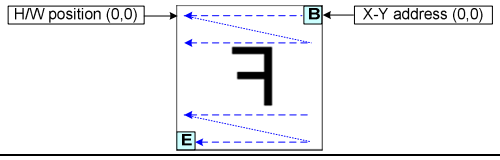
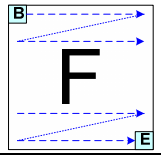
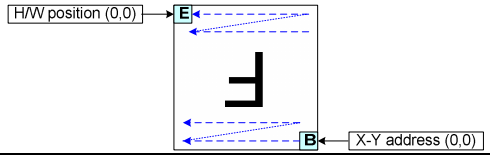
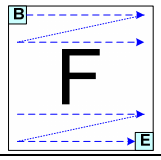
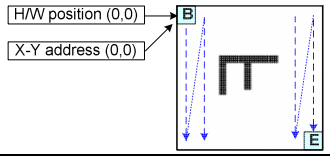
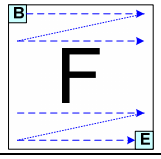
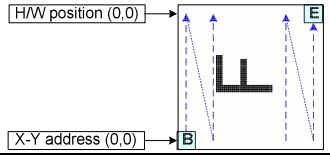
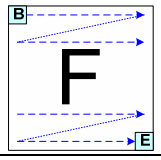
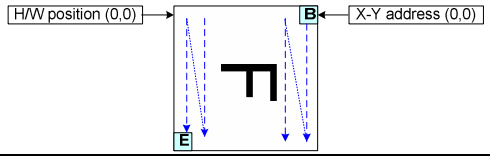
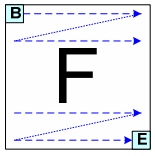
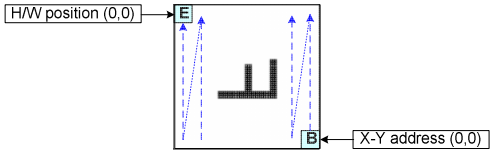
Display Data Direction	MADCTL Parameter			Image in the Host (MPU)	Image in the Driver (DDRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

Figure 5 Frame Data Write Direction According to the MADCTL parameters (MV, MX and MY)

7.3.3. I/O Buffer Circuit

It is the bi-directional buffer used when MPU reads or writes the DDRAM. Since MPU's read or write of DDRAM is performed independently from data output to the display data latch circuit, asynchronous access to the DDRAM when the LCD is turned on does not cause troubles such as flicking of the display images.

7.3.4. Scroll Address Circuit

The circuit associates pages on DDRAM with COM output. ST7689 processes signals for the liquid crystal display on 1-page basis. Thus, when specifying a specific area in the area scroll display or partial display, you must designate it in block.

7.3.5. Display data Latch Circuit

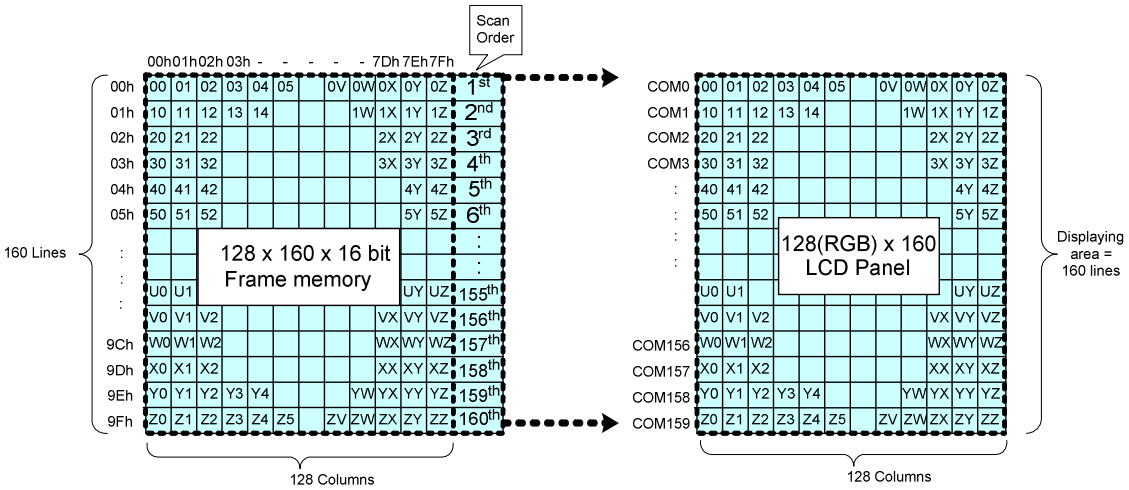
This circuit is used to temporarily hold display data to be output from the DDRAM to the SEG decoder circuit. Since display normal/inverse and display on/off commands are used to control data in the latch circuit alone, they do not modify data in the DDRAM.

7.3.6. Normal Display On or Partial Mode On Vertical Scroll Off

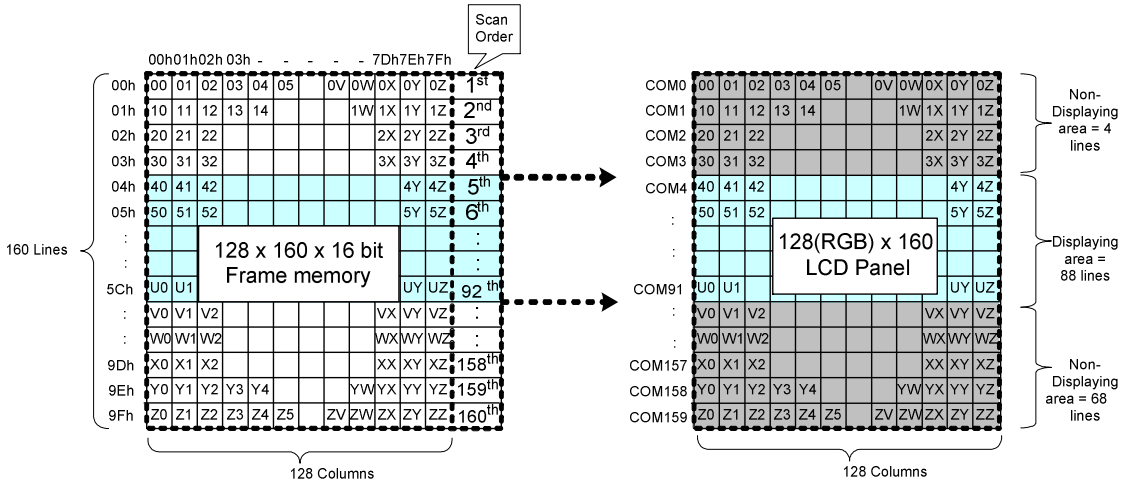
In this mode, contents of the frame memory within an area where column address is 00h to 7Fh and row address is 00h to 9Fh is displayed.

To display a dot on leftmost top corner, store the dot data at (column address, row address) = (0,0).

Example1) Normal Display On



Example2) Partial Display On: SR[15:0] = 0004h, ER[15:0] = 005Ch, MADCTL (ML)=0



7.3.7. Vertical Scroll/Rolling Scroll

Rolling Scroll

There is just one types of vertical scrolling, which are determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

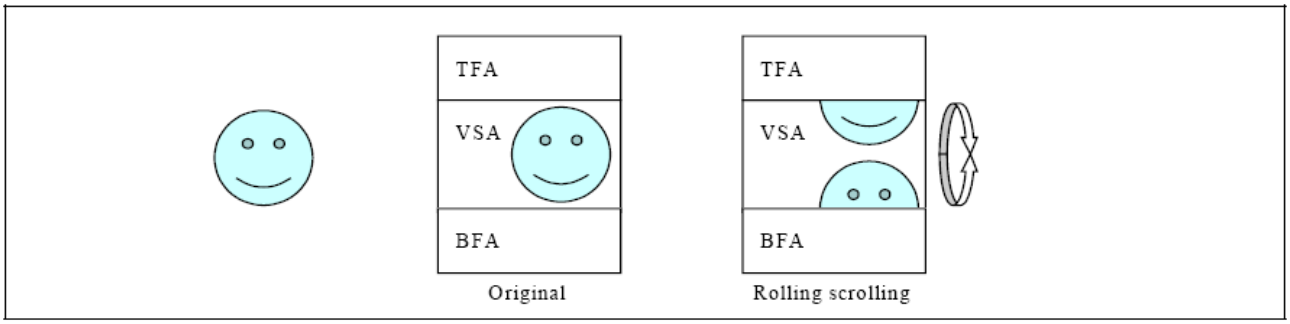
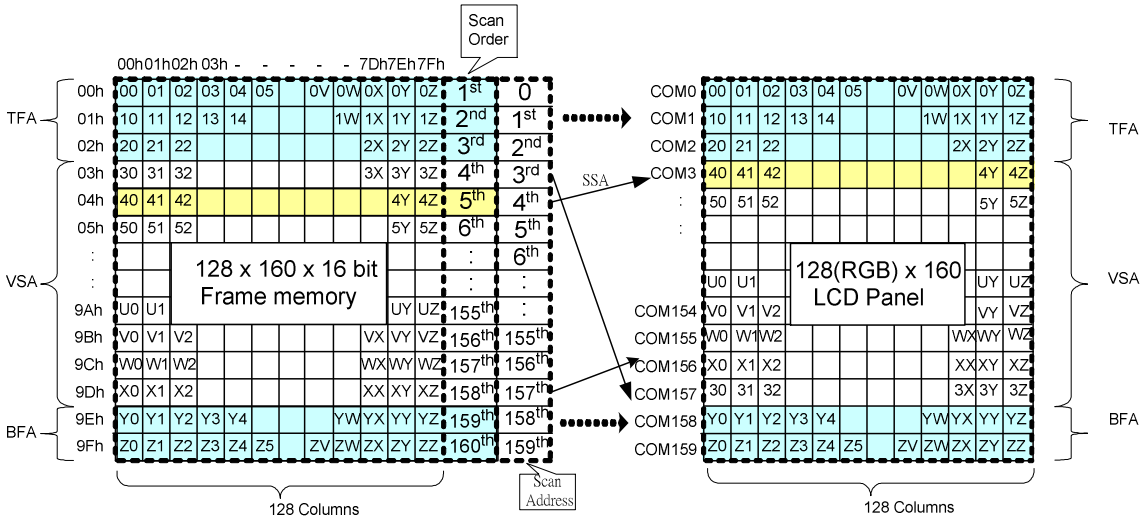


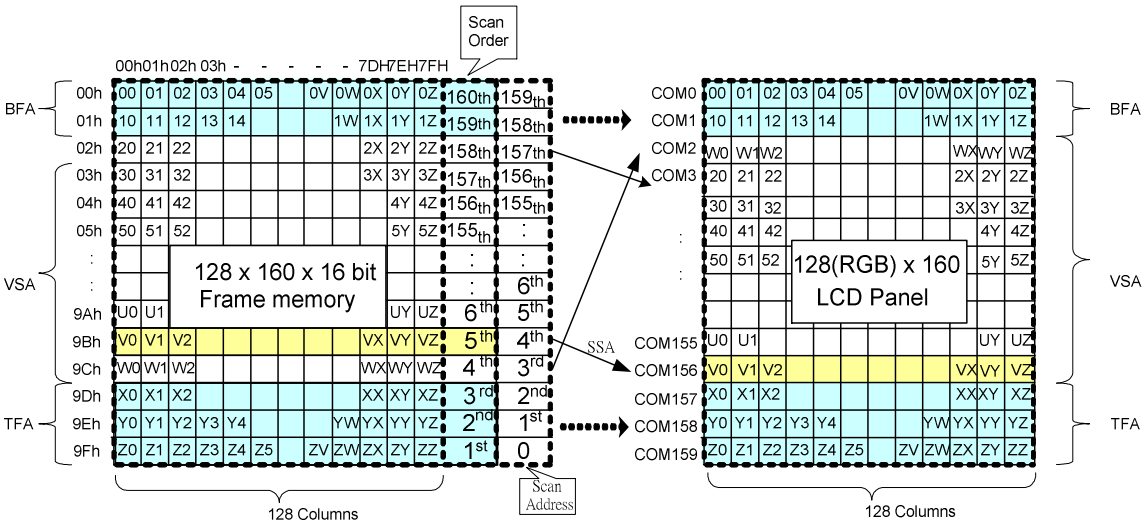
Figure 6 Rolling Scroll Definition

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) =160. In this case, ‘rolling’ scrolling is applied as shown below. All the memory contents will be used.

Example1) Panel size=128 x 160, TFA =3, VSA=155, BFA=2, SSA=4, MADCTL (ML)=0: Rolling Scroll



Example2) Panel size=128 x 160, TFA =2, VSA=155, BFA=3, SSA=4, MADCTL (ML)=1: Rolling Scroll (TFA and BFA are exchanged)



Vertical Scroll Example

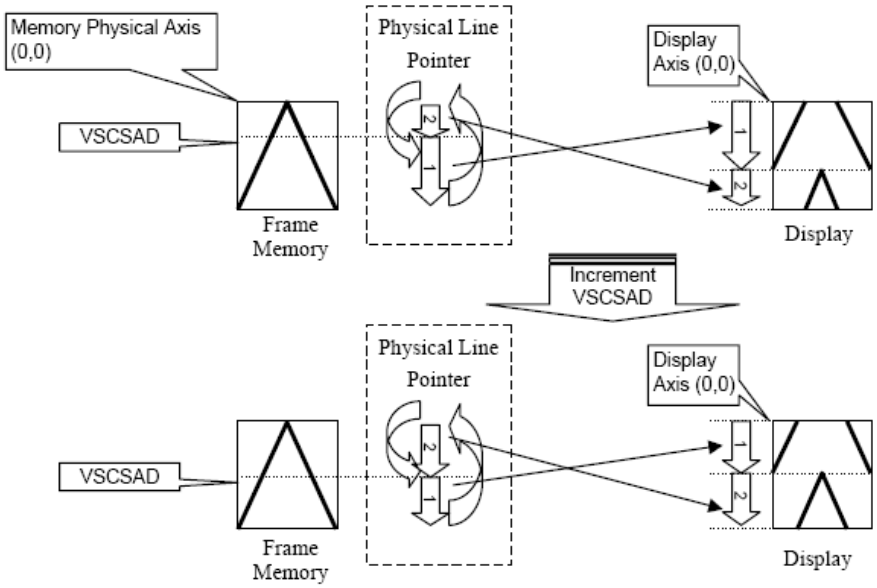
There are 2 types of vertical scrolling, which are determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

Case 1: TFA + VSA + BFA<160

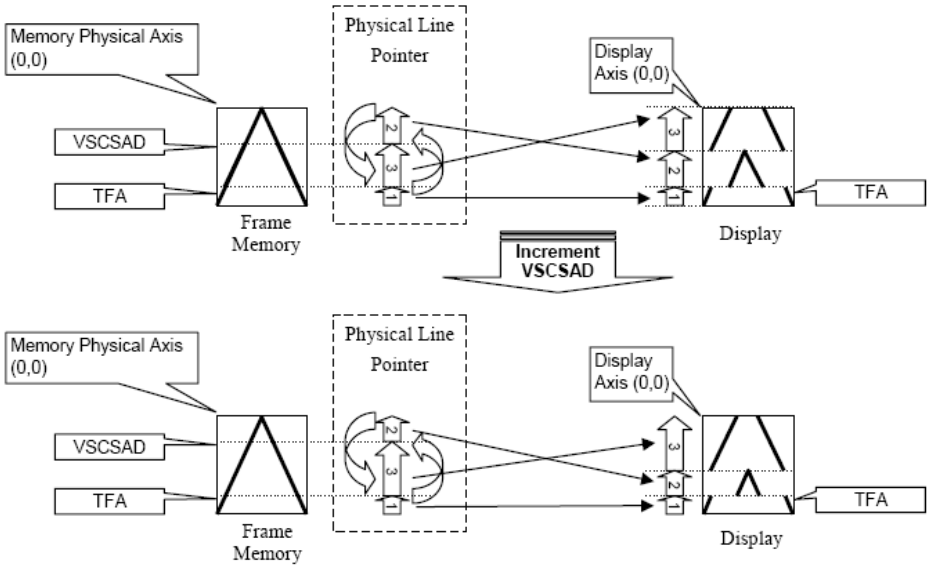
N/A. Do not set TFA + VSA + BFA<160. In that case, unexpected picture will be shown.

Case 2: TFA + VSA + BFA=160 (Rolling Scrolling)

Example1) When MADCTL parameter ML="0", TFA=0, VSA=160, BFA=0 and VSCSAD=40.



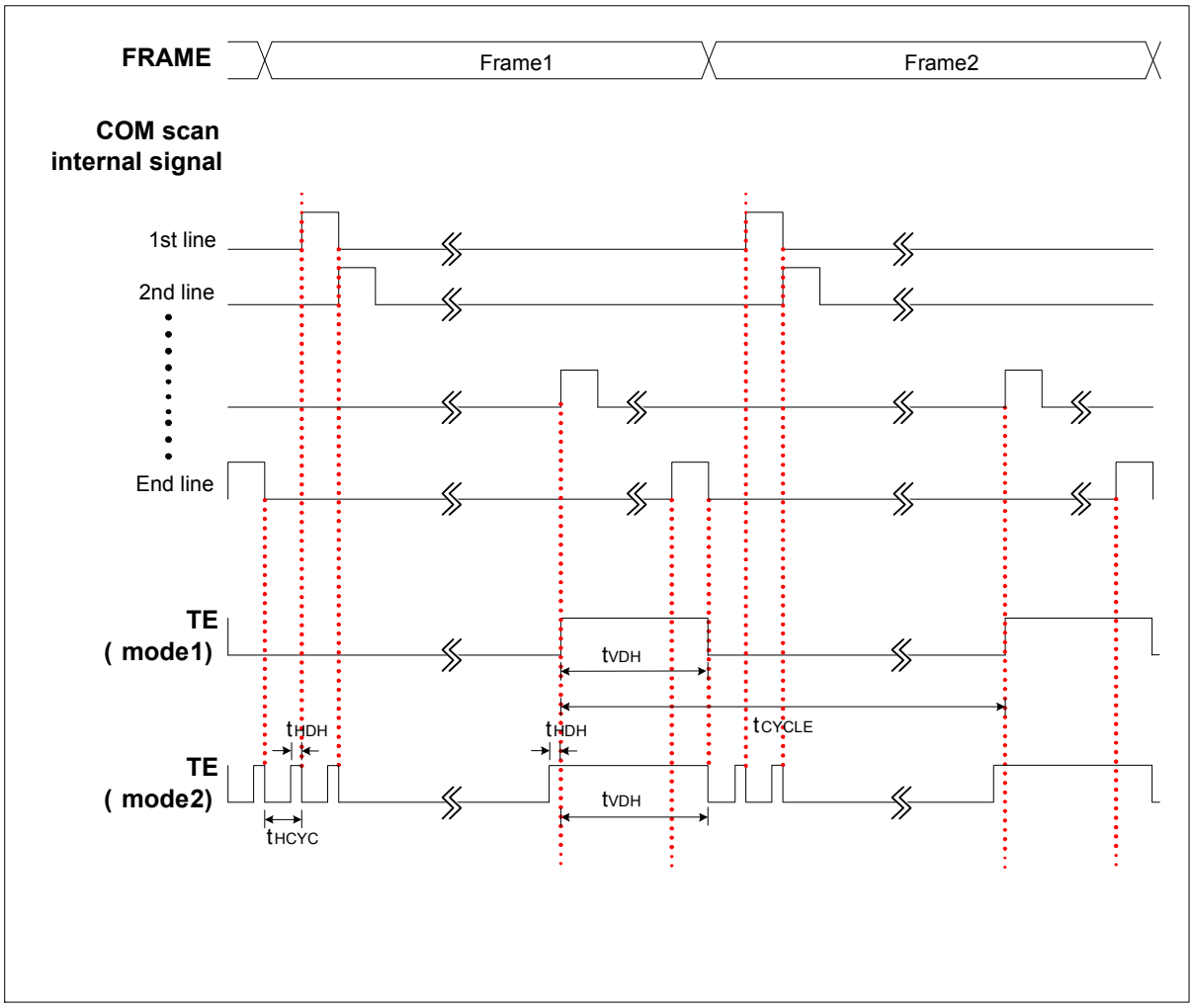
Example2) When MADCTL parameter ML="1", TFA=10, VSA=150, BFA=0 and VSCSAD=30.



7.3.8. Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

Tearing Effect Line Modes



Mode 1, the Tearing Effect Output signal consists of V-Sync(tVDH) information. There is one high pulse during each frame.

Mode 2, the Tearing Effect Output signal consists of both H-Sync(tHDH) and V-Sync(tVDH) information. TE pin output tHDH pulse on each COM scan signal.

Note: During Sleep In Mode, the Tearing Effect Output Pin is active Low.

Tearing Effect Line Timing

The Tearing Effect signal is described below:

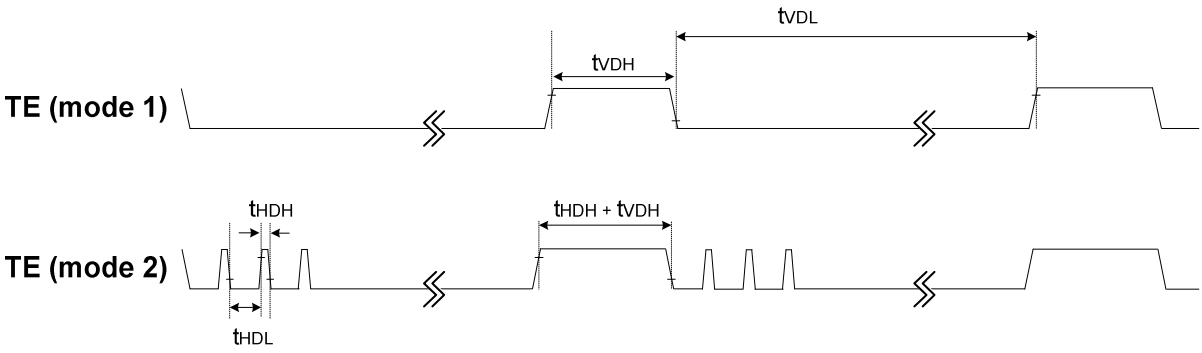
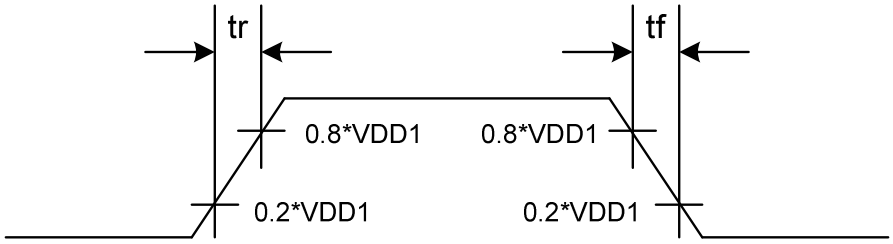


Figure 7 AC characteristics of Tearing Effect Signal

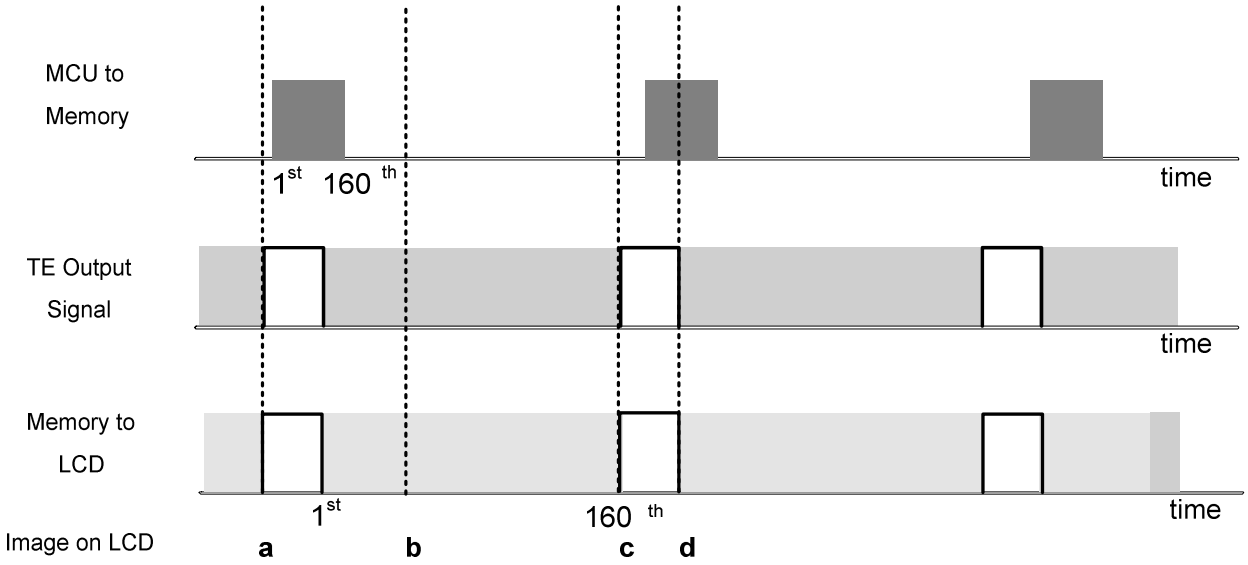
Idle Mode Off (Frame Rate = 77Hz, N-line = 0x8C, Vop=16.48V, VDDI/VDDA=1.8V/2.8V)

Symbol	Parameter	Typ	Unit	description
t_{VDL}	Vertical Timing Low Duration	11.13	ms	Mode1
t_{VDH}	Vertical Timing High Duration	1.84	ms	
t_{HDL}	Horizontal Timing Low Duration	72.61	us	Mode2
t_{HDH}	Horizontal Timing High Duration	4.87	us	

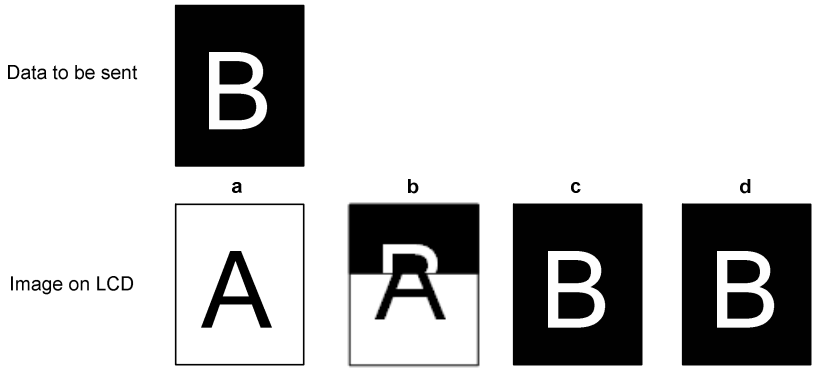
NOTE: The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.



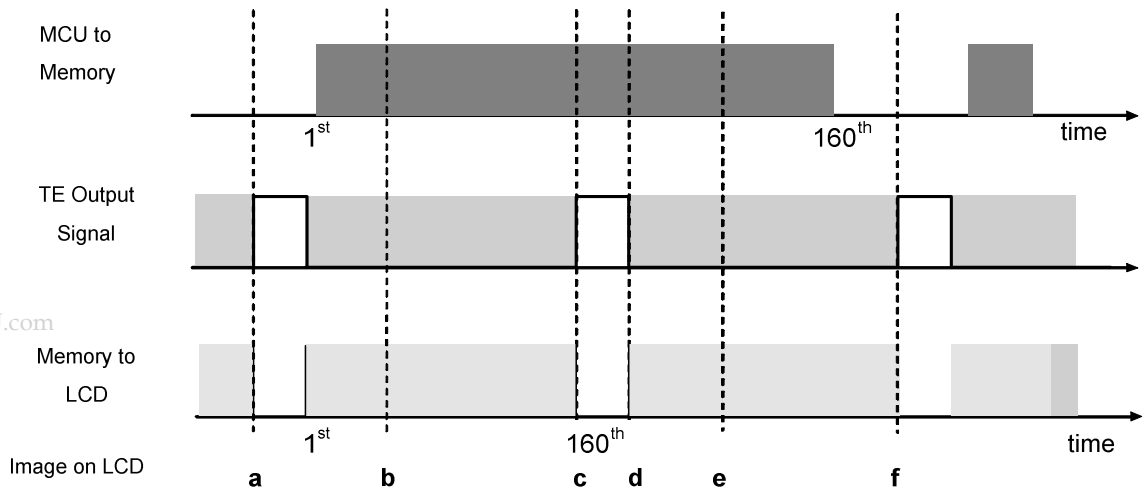
Example 1: MPU Write is faster than Panel Read.



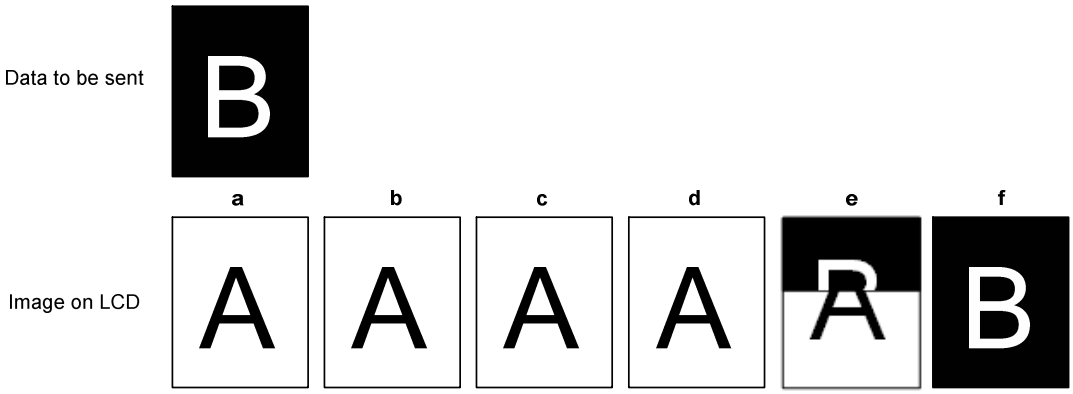
Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:



Example 2: MPU Write is slower than Panel Read.



The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MPU to Frame memory write position.



7.4. Gray-Scale Display

ST7689 incorporates a 4FRC & 31 PWM function circuit to display a 64 gray-scale display.

7.5. Oscillation Circuit

ST7689 is built-in an oscillator circuit. It provides internal clock without external resistor. This oscillator signal is used in the voltage converter and display timing generation circuit.

7.6. Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock, which is generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock and the display data latch circuit latches the display data in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal (M), which enables the LCD driver to make an AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. The frame signal or the line signal changes the M by setting internal instruction. Driving waveform and internal timing signal are shown in Figure 8.

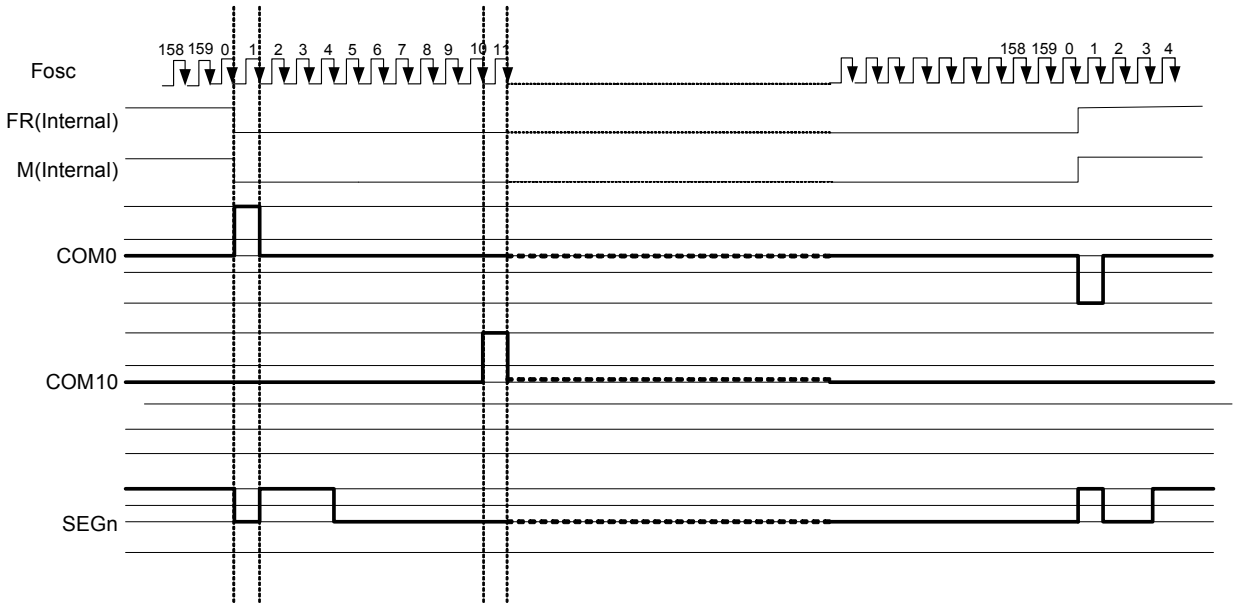


Figure 8 2 frame AC Driving Waveform (Duty Ratio: 1/160)

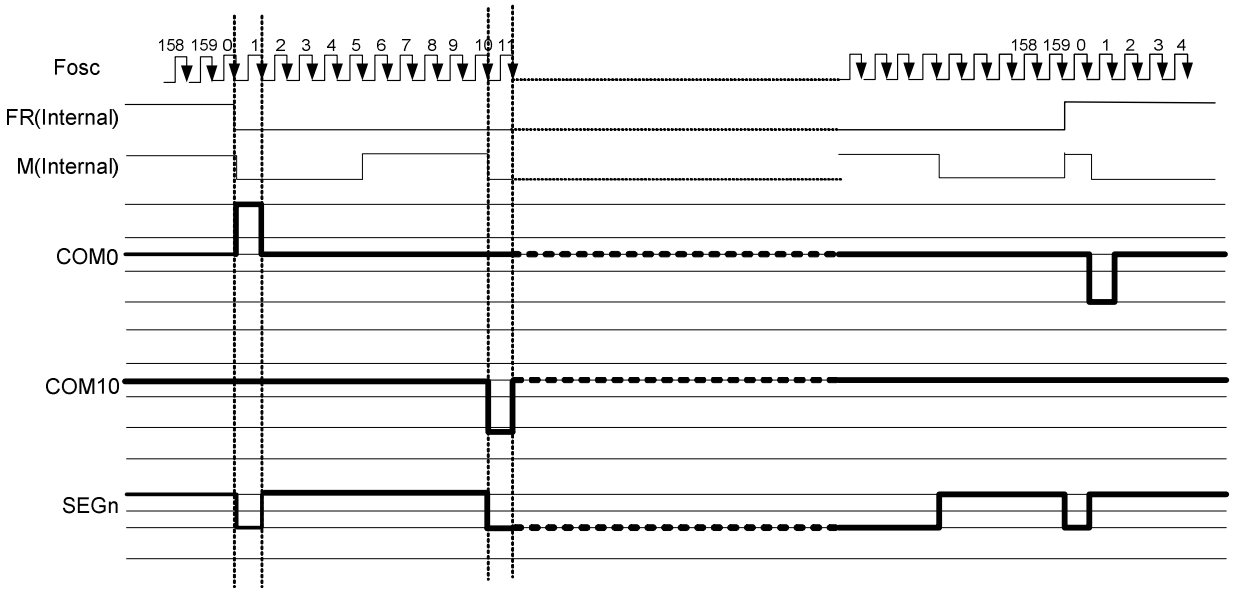


Figure 9 N-Line Inversion Driving Waveform (N=10, Duty Ratio=1/160)

7.7. Power Level Definition

7.7.1. Power ON/OFF Sequence

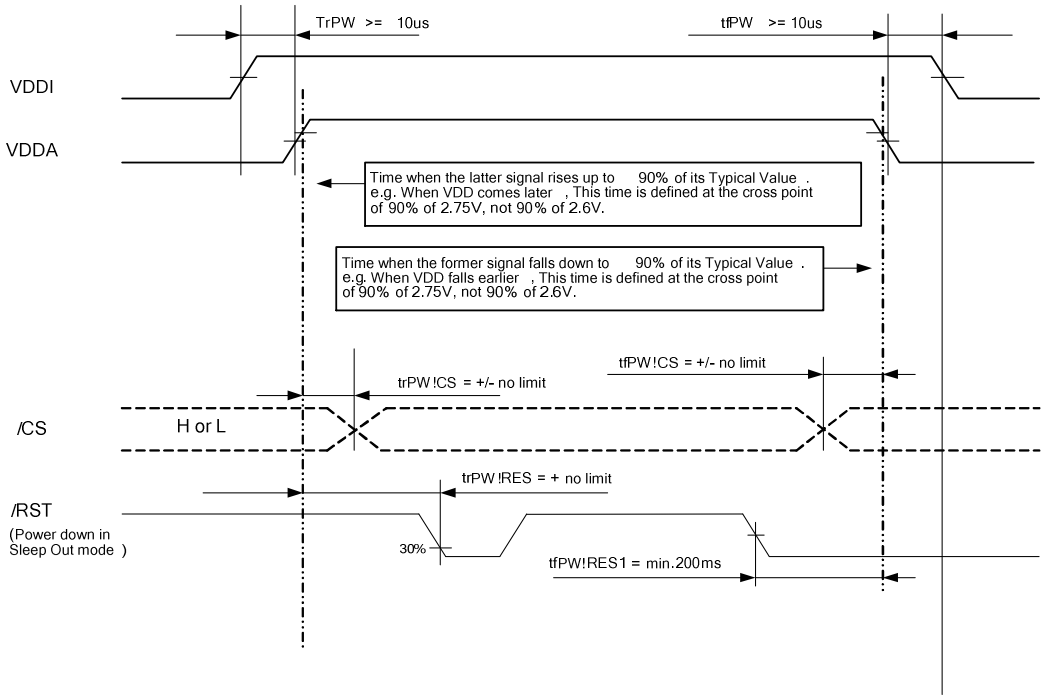
During power off, if LCD is in the Sleep Out mode, VDDA and VDDI must be powered down minimum 200msec after /RST has been released. During power off, if LCD is in the Sleep In mode, VDDI or VDDA can be powered down minimum 0msec after /RST has been released.

/CS can be applied at any timing or can be permanently grounded. /RST has priority over /CS.

The power on/off sequence is illustrated below:

/RST line is held High or Unstable by Host at Power On

If /RST line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VDDA and VDDI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

7.7.2. Power Levels

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out:

In this mode, the display is able to show maximum 65K colors.

2. Partial Mode On, Idle Mode Off, Sleep Out:

In this mode part of the display is used with maximum 65K colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out:

In this mode, the full display area is used but with 8 colors.

4. Partial Mode On, Idle Mode On, Sleep Out:

In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode:

In this mode, the DC:DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with Digital VDDI power supply. Contents of the memory are safe.

6. Power Off Mode:

In this mode, both Analog VDDA and Digital VDDI are removed.

Note: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

7.8. Liquid Crystal Driver Power Circuit

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are controlled by power control instruction.

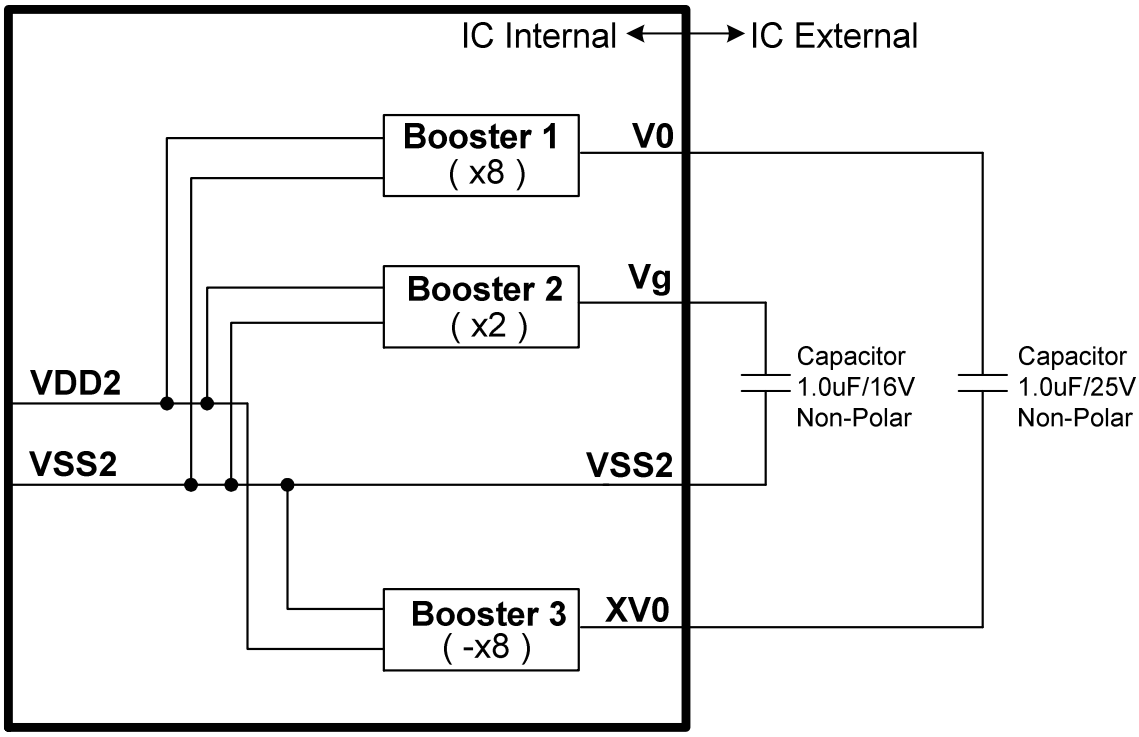


Figure 10 DC/DC Booster Block Diagram

7.8.1. Voltage Regulator Circuits

There is a built-in voltage regulator circuits in ST7689 for generating V0. After internal voltage is regulated by voltage regulator circuit, V0 is generated. Detail explanation of V0 set is listed below:

◆ **SET V0 (Temperature = 24℃)**

V0=3.6+{Vop[8:0] + VopOffset[6:0]+ (EV[6:0]-3Fh)}x0.04 (V)

Example1 (V0 setting>16.48V):

Vop[8:0]=1 01000010 (142h)

VopOffset[6:0]=0000010 (02h)

EV[6:0]=0111111 (3Fh)

V0=3.6 + {322 + 2 + (63-63) } x 0.04 =16.56 (V)

Example2 (V0 setting<16.48V):

Vop[8:0]= 1 01000010 (142h)

VopOffset [6:0]=1000010 (42h)

EV[6:0]=0111111 (3Fh)

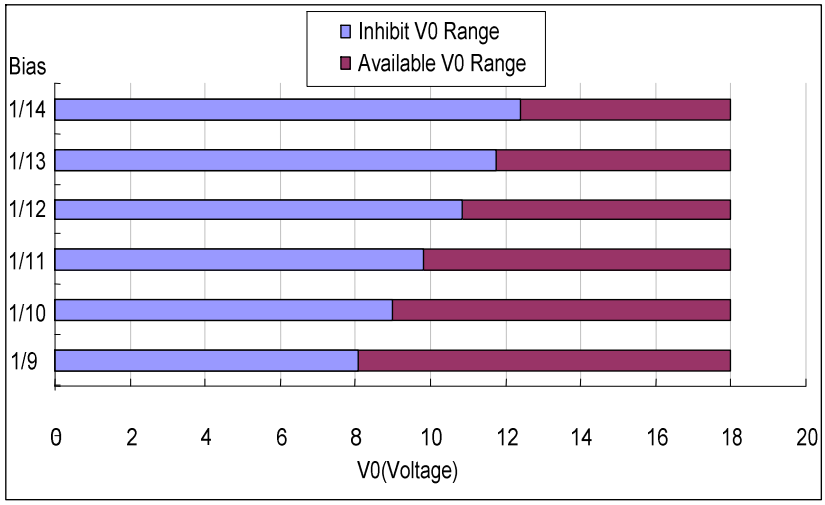
V0=3.6 + {322 -62 + (63-63)} x 0.04 =14 (V)

◆ **V0 restriction:**

Because Vg should larger than 1.8V, ST7689 V0 value should be higher than 1.8 x Bias / 2 (V) and lower than 18V. V0 value outside the available range is undefined. Users has to ensure while selecting the temperature compensation that under all conditions and including all tolerances that the V0 voltage remains in the range.

Bias	V0 setting	
	Min	Max
1/9	8.1	18.0
1/10	9.0	18.0
1/11	9.9	18.0
1/12	10.8	18.0
1/13	11.7	18.0
1/14	12.6	18.0

(VDDA≧2.5V)



◆ **SET V0 with temperature compensation (Temperature ≠ 24℃)**

There are 16-line slope in each temperature steps and customer can select one line slope of temperature compensation coefficient for each temperature step. Each temperature step is 8°C. Please see Figure 11 as below.

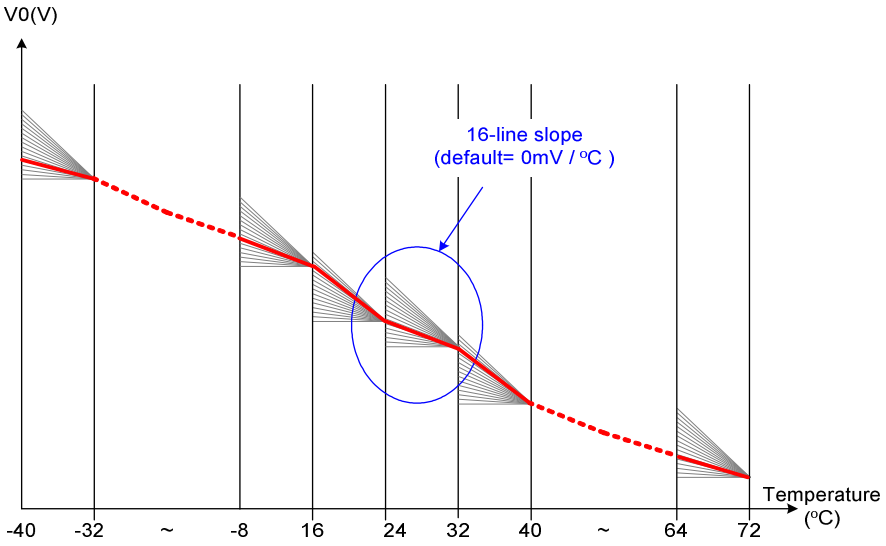
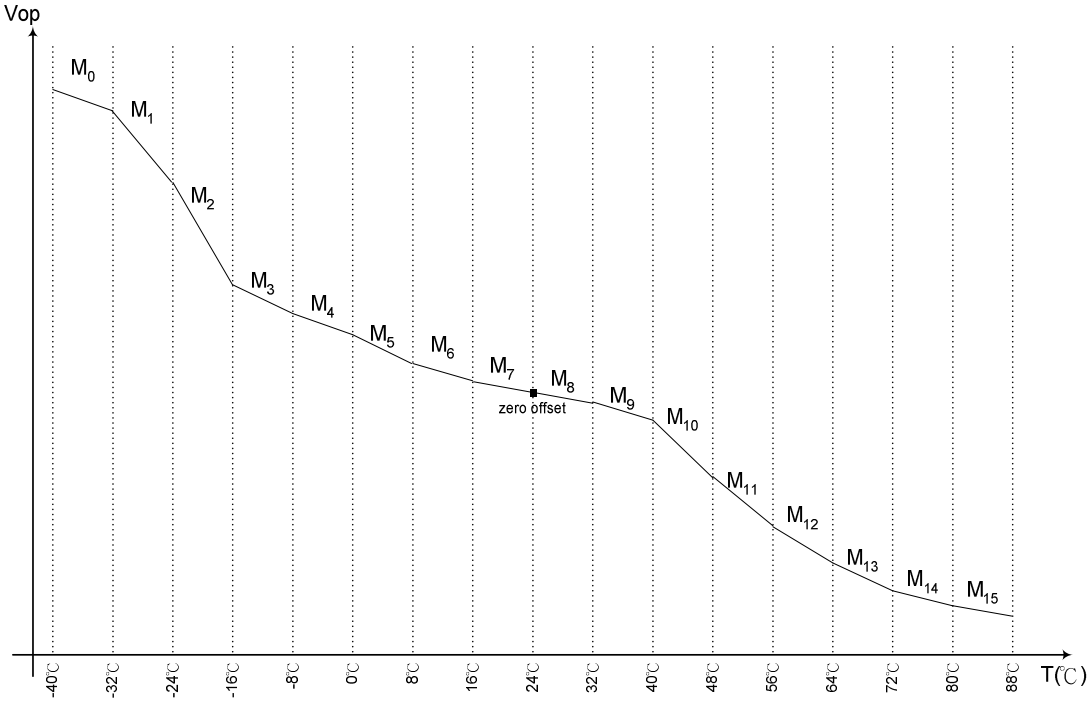


Figure 11 Relationship of V0 and Temperature Compensation

In command TEMPSET each MTx, where x=0, 1, 2,…, E, F, has a value between 0 and 15. MTx = 0 results in 0V increment on V0, MTx = 1 results in Mx=5mV increment, …, MTx = 15 results in Mx=15x5mV=75mV increment. Note that each MTx individually corresponds to a temperature interval; The relations between Mx and V0 quantity due to temperature V0(T) are described in the equations shown as follows:

Temperature range	Equation V0(V) at temperature=T℃
-40℃ ≦ T < -32℃	V0(T) = V0(T24)+ (-32-T) · M0 +(M1 + M2 + M3 + M4 + M5 + M6 + M7) · 8
-32℃ ≦ T < -24℃	V0(T) = V0(T24)+ (-24-T) · M1 +(M2 + M3 + M4 + M5 + M6 + M7) · 8
-24℃ ≦ T < -16℃	V0(T) = V0(T24)+ (-16-T) · M2 +(M3 + M4 + M5 + M6 + M7) · 8
-16℃ ≦ T < -8℃	V0(T) = V0(T24)+ (-8-T) · M3 +(M4 + M5 + M6 + M7) · 8
-8℃ ≦ T < 0℃	V0(T) = V0(T24)+ (0-T) · M4 +(M5 + M6 + M7) · 8
0℃ ≦ T < 8℃	V0(T) = V0(T24)+ (8-T) · M5 +(M6 + M7) · 8
8℃ ≦ T < 16℃	V0(T) = V0(T24)+ (16-T) · M6 + M7 · 8
16℃ ≦ T < 24℃	V0(T) = V0(T24)+ (24-T) · M7
24℃ ≦ T < 32℃	V0(T) = V0(T24)－(T-24) · M8
32℃ ≦ T < 40℃	V0(T) = V0(T24)－(T-32) · M9－M8 · 8
40℃ ≦ T < 48℃	V0(T) = V0(T24)－(T-40) · M10－(M9 + M8) · 8
48℃ ≦ T < 56℃	V0(T) = V0(T24)－(T-48) · M11－(M10 + M9 + M8) · 8
56℃ ≦ T < 64℃	V0(T) = V0(T24)－(T-56) · M12－(M11 + M10 + M9 + M8) · 8
64℃ ≦ T < 72℃	V0(T) = V0(T24)－(T-64) · M13－(M12 + M11 + M10 + M9 + M8) · 8
72℃ ≦ T < 80℃	V0(T) = V0(T24)－(T-72) · M14－(M13 + M12 + M11 + M10 + M9 + M8) · 8
80℃ ≦ T < 88℃	V0(T) = V0(T24)－(T-80) · M15－(M14 + M13 + M12 + M11 + M10 + M9 + M8) · 8



Note:

Please make sure to avoid any kind of heating source closing to Driver IC such as back light, to prevent Vop is not anticipative because of temperature compensate circuit worked.

◆ V0 fine tuning

ST7689 has 2 commands for fine tuning V0. These commands are VopOfsetInc (see section 8.1.41) and VopOfsetDec (see section 8.1.42). When writing VopOfsetInc into IC for each time, V0 would increase 40mV; when writing VopOfsetDec into IC for each time, V0 would decrease 40mV.

Example:

Vop[8:0]=1 01000010 (142h)

VopOffset[6:0]=0000010 (02h)

EV[6:0]=0111111 (3Fh)

VopOfsetInc x5

V0=3.6 + { 322 + 2 + (63-63) } x 0.04 + **0.04x5** = 16.76 (V)

7.8.2. Voltage Follower Circuits

There is a build-in voltage follower circuits in ST7689 for generating Vg and Vm. These voltages are decided by bias ratio selection circuitry which is set by users with software to control 1/9 to 1/14 bias ratios to match the optimum display performance of LCD panel. Bias driving rule is listed below:

LCD bias	Vg	Vm
1/N bias	(2/N) x V0	(1/N) x V0

N=9 to 14

7.8.3. PROM Setting Flow

ST7689 provides the Write and Read function to write the electronic control value and built-in resistance ratio into built-in PROM (Programmable Read Only Memory), and then read them from it. Using the Write and Read functions, you can store these values appropriate to each LCD panel. This function is very convenient for user in setting from some different panel's voltage. But using this function must attention the setting procedure. Please see the following diagram.

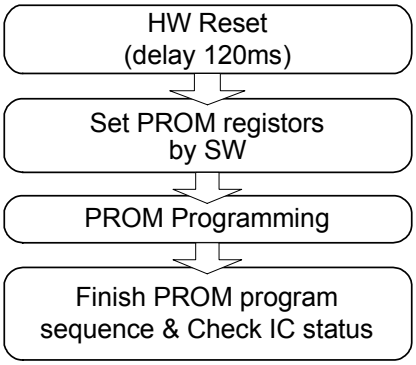


Figure 12 PROM programming flow

Note1: This setting flow is used for LCM assembler.

Note2: PROM shouldn't be written without preceding loading correctly from PROM in order to avoid some errors during IC operation.

Note3: When writing value to PROM, the voltage of VPP must be 6.5V~6.75V; the current of Ivpp must be more than 8mA.

Note4: If the PROM is exposed to a high temperature for hours, data in the memory cell may probably be lost before the data retention guarantee period. To retain data in the memory cell, keep the memory cell below 90℃. The data retention guarantee period is specified including the retention period.

Note5: The PROM function can not guaranteed after burned-in over 4 times.

7.9. Frequency Temperature Gradient Compensation Coefficient

7.9.1. Register loading Detection

ST7689 will auto-switch frame rate on different temperature such as Figure 13. TA, TB and TC are frame rate switching temperatures which can be defined by customer with command TMPRNG. FA, FB, FC and FD are switched frame rate which also can be defined by customer with command FRMSEL. The frame rate range is from 38.5Hz to 153Hz.

When the temperature is in increasing state, frame rate changes to the higher step at TA/TB/TC+TH (℃). When the temperature is in decreasing state, frame rate changes to the lower step at TA/TB/TC. For example: TC=10℃ and TH=5℃, FC switches to FD at 15℃ but FD switches to FC at 10℃. Please take Figure 13 for reference.

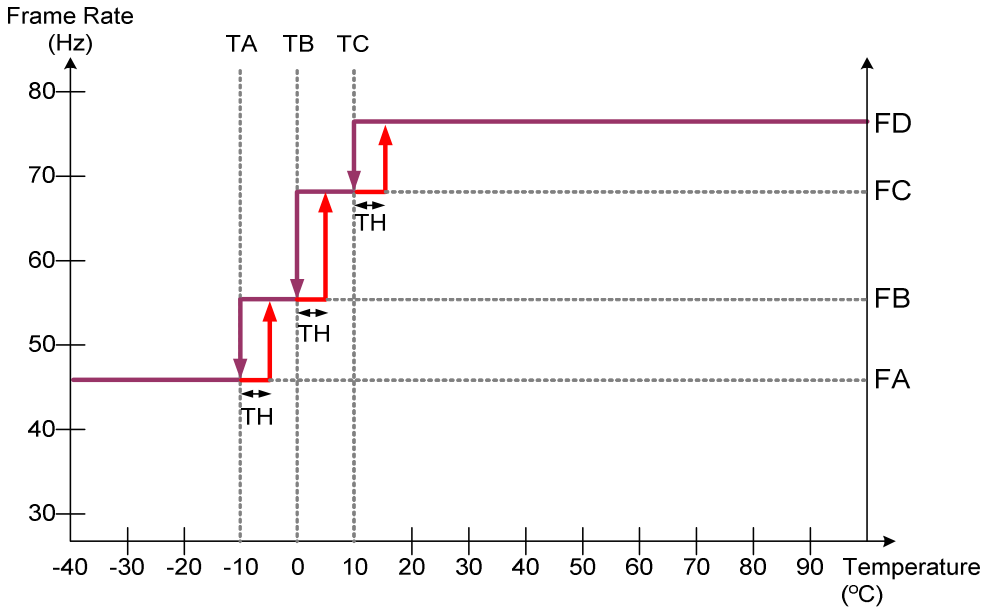


Figure 13 Relationship of Frequency and Temperature Compensation

8. COMMANDS

8.1. Instruction Table

Command Table-1														
Hex	**Command**	**A0**	**/RD**	**/WR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Function**	**Ref**
(00h)	NOP	0	1	0	0	0	0	0	0	0	0	0	No Operation	8.1.1
(01h)	SWRESET	0	1	0	0	0	0	0	0	0	0	1	Software reset	8.1.2
(09h)	RDDST	0	1	0	0	0	0	0	1	0	0	1	Read Display Status	8.1.3
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	ST31	ST30	ST29	ST28	ST27	ST26	ST25	ST24	(D31-D24)	
-		1	0	1	ST23	ST22	ST21	ST20	ST19	ST18	ST17	ST16	(D23-D16)	
-		1	0	1	ST15	ST14	ST13	ST12	ST11	ST10	ST9	ST8	(D15-D8)	
-		1	0	1	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0	(D7-D0)	
(0Bh)	RDDMADCTL	0	1	0	0	0	0	0	1	0	1	1	Read Display MADCTL	8.1.4
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	D7	D6	D5	D4	D3	0	0	0	-	
(0Ch)	RDDCOLMOD	0	1	0	0	0	0	0	1	1	0	0	Read Display Pixel Format	8.1.5
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	0	0	0	0	0	D2	D1	D0	-	
(0Dh)	RDDIM	0	1	0	0	0	0	0	1	1	0	1	Read Display Image Mode	8.1.6
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	D7	0	D5	D4	D3	0	0	0	-	
(10h)	SLPIN	0	1	0	0	0	0	1	0	0	0	0	Sleep in & booster off	8.1.7
(11h)	SLPOUT	0	1	0	0	0	0	1	0	0	0	1	Sleep out & booster on	8.1.8
(12h)	PTLON	0	1	0	0	0	0	1	0	0	1	0	Partial mode on	8.1.9
(13h)	NORON	0	1	0	0	0	0	1	0	0	1	1	Partial off (Normal)	8.1.10
(20h)	INVOFF	0	1	0	0	0	1	0	0	0	0	0	Display inversion off (normal)	8.1.11
(21h)	INVON	0	1	0	0	0	1	0	0	0	0	1	Display inversion on	8.1.12
(22h)	APOFF	0	1	0	0	0	1	0	0	0	1	0	All pixel off (Only for test purpose)	8.1.13
(23h)	APON	0	1	0	0	0	1	0	0	0	1	1	All pixel on (Only for test purpose)	8.1.14
(25h)	WRCNTR	0	1	0	0	0	1	0	0	1	0	1	Write contrast	8.1.15
-		1	1	0	0	EV6	EV5	EV4	EV3	EV2	EV1	EV0	EV = 0 to 127	
(28h)	DISPOFF	0	1	0	0	0	1	0	1	0	0	0	Display off	8.1.16
(29h)	DISPON	0	1	0	0	0	1	0	1	0	0	1	Display on	8.1.17

Hex	Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Function	Ref
(2Ah)	CASET	0	1	0	0	0	1	0	1	0	1	0	Column address set	8.1.18
		1	1	0	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8	X_ADR start: 0≦XS≦7Fh	
		1	1	0	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0		
		1	1	0	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8	X_ADR end: XS≦XE ≦7Fh	
		1	1	0	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0		
(2Bh)	RASET	0	1	0	0	0	1	0	1	0	1	1	Row address set	8.1.19
		1	1	0	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8	Y_ADR start: 0≦YS≦9Fh	
		1	1	0	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0		
		1	1	0	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8	Y_ADR end: YS≦YE≦9Fh	
		1	1	0	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0		
(2Ch)	RAMWR	0	1	0	0	0	1	0	1	1	0	0	Memory write	8.1.20
		1	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data	
(2Eh)	RAMRD	0	1	0	0	0	1	0	1	1	1	0	Memory Read	8.1.21
		1	0	1	-	-	-	-	-	-	-	-		
		1	0	1	D7	D6	D5	D4	D3	D2	D1	D0		
(30h)	PTLAR	0	1	0	0	0	1	1	0	0	0	0	Partial start/end address set	8.1.22
-		1	1	0	PS15	PS14	PS13	PS12	PS11	PS10	PS9	PS8	Start address (0~159)	
		1	1	0	PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0		
		1	1	0	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	End address (0~159)	
-		1	1	0	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0		
(33h)	RLAR	0	1	0	0	0	1	1	0	0	1	1	Scroll Area	8.1.23
-		1	1	0	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	TFA=0~160	
-		1	1	0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	VSA=0~160	
-		1	1	0	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	BFA=0~160	
(34h)	TEOFF	0	1	0	0	0	1	1	0	1	0	0	Tearing effect line off	8.1.24
(35h)	TEON	0	1	0	0	0	1	1	0	1	0	1	Tearing effect mode set & on	8.1.25
-		1	1	0	-	-	-	-	-	-	-	M	“0”: mode1, “1”: mode2	
(36h)	MADCTL	0	1	0	0	0	1	1	0	1	1	0	Memory data access control	8.1.26
-		1	1	0	MY	MX	MV	ML	RGB	-	-	-	-	
(37h)	VSCSAD	0	1	0	0	0	1	1	0	1	1	1	Scroll start address of RAM	8.1.27
		1	1	0	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	SSA = 0~159	

Hex	Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Function	Ref
(38h)	IDMOFF	0	1	0	0	0	1	1	1	0	0	0	Idle mode off	8.1.28
(39h)	IDMON	0	1	0	0	0	1	1	1	0	0	1	Idle mode on	8.1.29
(3Ah)	COLMOD	0	1	0	0	0	1	1	1	0	1	0	Interface pixel format	8.1.30
-		1	1	0	-	-	-	-	-	P2	P1	P0	Interface format	
(DBh)	RDID	0	1	0	1	1	0	1	1	0	1	1	Read ID	8.1.31
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	1	-	-	-	ID3	ID2	ID1	ID0	(D3-D0)	

Note 1: When /EXT connects to H or floating, commands which are not defined in "Command Table-1" are treated as NOP (00H) command.

Note 2: Commands 10H, 12H, 13H, 20H, 21H, 25H, 28H, 29H, 30H, 36H (Bit ML only), 38H and 39H are updated during V-sync when Module is in Sleep Out Mode to avoid abnormal visual effects.

During Sleep In mode, these commands are updated immediately.

Read status (09H), Read Display Power Mode (0AH), Read Display MADCTL (0BH), Read Display Pixel Format (0CH), Read Display Image Mode (0DH), Read Display Signal Mode (0EH) and Read Display Self Diagnostic Result (0FH) of these commands is updated immediately both in Sleep In mode and Sleep Out mode.

Command Table-2														
Hex	**Command**	**A0**	**/RD**	**/WR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Function**	**Ref**
(B0h)	DutySet	0	1	0	1	0	1	1	0	0	0	0	Display Duty setting	8.1.32
		1	1	0	Du7	Du6	Du5	Du4	Du3	Du2	Du1	Du0		
(B1h)	FirstCom	0	1	0	1	0	1	1	0	0	0	1	First Com. Page address	8.1.33
		1	1	0	F7	F6	F5	F4	F3	F2	F1	F0		
(B3h)	OscDiv	0	1	0	1	0	1	1	0	0	1	1	FOSC divider	8.1.34
		1	1	0	-	-	-	-	-	-	CLD1	CLD0		
(B5h)	NLInvSet	0	1	0	1	0	1	1	0	1	0	1	N-line control	8.1.35
		1	1	0	M	N6	N5	N4	N3	N2	N1	N0		
(B7h)	ComScanDir	0	1	0	1	0	1	1	0	1	1	1	Com/Seg Scan Direction for Glass layout	8.1.36
		1	1	0	0	SMX	0	0	SBGR	0	0	-		
(B8h)	RmwIn	0	1	0	1	0	1	1	1	0	0	0	read modify write control IN	8.1.37
(B9h)	RmwOut	0	1	0	1	0	1	1	1	0	0	1	read modify write control Out	8.1.38
(BDh)	DispCompStep1	0	1	0	1	0	1	1	1	1	0	1	Display Compensation Step	8.1.39
		1	1	0	0	0	0	0	0	Step2	Step1	Step0		
(C0h)	VopSet	0	1	0	1	1	0	0	0	0	0	0	Vop setting	8.1.40
		1	1	0	Vop7	Vop6	Vop5	Vop4	Vop3	Vop2	Vop1	Vop0		
		1	1	0	-	-	-	-	-	-	-	Vop8		
(C1h)	VopOfsetInc	0	1	0	1	1	0	0	0	0	0	1	+40mv/setp	8.1.41
(C2h)	VopOfsetDec	0	1	0	1	1	0	0	0	0	1	0	-40mv/setp	8.1.42
(C3h)	BiasSel	0	1	0	1	1	0	0	0	0	1	1	Bias selection	8.1.43
		1	1	0	-	-	-	-	-	Bias2	Bias1	Bias0		
(C4h)	BstBmpXSel	0	1	0	1	1	0	0	0	1	0	0	Booster setting	8.1.44
		1	1	0	-	-	-	-	-	BST2	BST 1	BST0		
(C7h)	VopOffset	0	1	0	1	1	0	0	0	1	1	1	Vop offset fuse bit adjust	8.1.45
		1	1	0	0	VOS6	VOS5	VOS4	VOS3	VOS2	VOS1	VOS0		
(CBh)	VgSorcSel	0	1	0	1	1	0	0	1	0	1	1	Vg with Booster x2 control	8.1.46
		1	1	0	-	-	-	-	-	-	-	2BT0		
(CDh)	IDSet	0	1	0	1	1	0	0	1	1	0	1	ID setting	8.1.47
		1	1	0	-	-	-	-	ID3	ID2	ID1	ID0		

Hex	Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Function	Ref
(D0h)	ANASET	0	1	0	1	1	0	1	0	0	0	0	Analog circuit setting	8.1.48
		1	1	0	0	0	0	1	1	1	0	1		
(D7h)	AutoLoadSet	0	1	0	1	1	0	1	0	1	1	1	mask rom data auto re-load control	8.1.49
		1	1	0	1	0	-	ARD	1	1	1	1		
(E0h)	EPCTIN	0	1	0	1	1	1	0	0	0	0	0	Control PROM WR/RD	8.1.50
		1	1	0	0	0	WR /XRD	0	0	0	0	0		
(E1h)	EPCTOUT	0	1	0	1	1	1	0	0	0	0	1	PROM control cancel	8.1.51
(E2h)	EPMWR	0	1	0	1	1	1	0	0	0	1	0	Write to PROM	8.1.52
(E3h)	EPMRD	0	1	0	1	1	1	0	0	0	1	1	Read from PROM	8.1.53
(E4h)	PROMSEL	0	1	0	1	1	1	0	0	1	0	0	Select PROM	8.1.54
		1	1	0	MS1	MS0	0	1	1	0	0	1		
(E5h)	ROMSET	0	1	0	1	1	1	0	0	1	0	1	Programmable ROM setting	8.1.55
		1	1	0	0	0	0	D4	D3	D2	D1	D0		
(EC)	DispCompStep2	0	1	0	1	1	1	0	1	1	0	0	Display Compensation Step	8.1.56
		1	1	0	0	0	0	0	0	Step2	Step1	Step0		
(F0h)	FRMSEL	0	1	0	1	1	1	1	0	0	0	0	Frame Freq. in Temp range A,B,C and D	8.1.57
		1	1	0	-	-	-	FA4	FA3	FA2	FA1	FA0		
		1	1	0	-	-	-	FB4	FB3	FB2	FB1	FB0		
		1	1	0	-	-	-	FC4	FC3	FC2	FC1	FC0		
		1	1	0	-	-	-	FD4	FD3	FD2	FD1	FD0		
(F1h)	FRM8SEL	0	1	0	1	1	1	1	0	0	0	1	Frame Freq. in Temp range A,B,C and D (idle)	8.1.58
		1	1	0	-	-	-	F8A4	F8A3	F8A2	F8A1	F8A0		
		1	1	0	-	-	-	F8B4	F8B3	F8B2	F8B1	F8B0		
		1	1	0	-	-	-	F8C4	F8C3	F8C2	F8C1	F8C0		
		1	1	0	-	-	-	F8D4	F8D3	F8D2	F8D1	F8D0		

Hex	Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Function	Ref
(F2h)	TMPRNG	0	1	0	1	1	1	1	0	0	1	0	Temp range A,B and C	8.1.59
		1	1	0	-	TA6	TA5	TA4	TA3	TA2	TA1	TA0		
		1	1	0	-	TB6	TB5	TB4	TB3	TB2	TB1	TB0		
		1	1	0	-	TC6	TC5	TC4	TC3	TC2	TC1	TC0		
(F3h)	TMPHYS	0	1	0	1	1	1	1	0	0	1	1	Hysteresis value set	8.1.60
		1	1	0	-	-	-	-	TH3	TH2	TH1	TH0		
(F4h)	TEMPSEL	0	1	0	1	1	1	1	0	1	0	0	TEMPSEL	8.1.61
		1	1	0	MT13	MT12	MT11	MT10	MT03	MT02	MT01	MT00		
		1	1	0	MT33	MT32	MT31	MT30	MT23	MT22	MT21	MT20		
		1	1	0	MT53	MT52	MT51	MT50	MT43	MT42	MT41	MT40		
		1	1	0	MT73	MT72	MT71	MT70	MT63	MT62	MT61	MT60		
		1	1	0	MT93	MT92	MT91	MT90	MT83	MT82	MT81	MT80		
		1	1	0	MTB3	MTB2	MTB1	MTB0	MTA3	MTA2	MTA1	MTA0		
		1	1	0	MTD3	MTD2	MTD1	MTD0	MTC3	MTC2	MTC1	MTC0		
		1	1	0	MTF3	MTF2	MTF1	MTF0	MTE3	MTE2	MTE1	MTE0		
(F7h)	THYS	0	1	0	1	1	1	1	0	1	1	1	Temperature detection threshold	8.1.62
		1	1	0	-	-	THYS5	THYS4	THYS3	THYS2	THYS1	THYS0		
(F9h)	Frame Set	0	1	0	1	1	1	1	1	0	0	1	Set Frame RGB PWM	8.1.63
		1	1	0	-	-	-	P14	P13	P12	P11	P10		
		1	1	0	-	-	-	P24	P23	P22	P21	P20		
		:	:	:	:	:	:	:	:	:	:	:		
		1	1	0	-	-	-	P154	P153	P152	P151	P150		
		1	1	0	-	-	-	P164	P163	P162	P161	P160		

8.1.1. NOP: No Operation (00H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	0	0	0	0	0	0	00H
Parameter	No parameter											

Description	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands.
Restriction	
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart

8.1.2. SWRESET: Software Reset (01H)

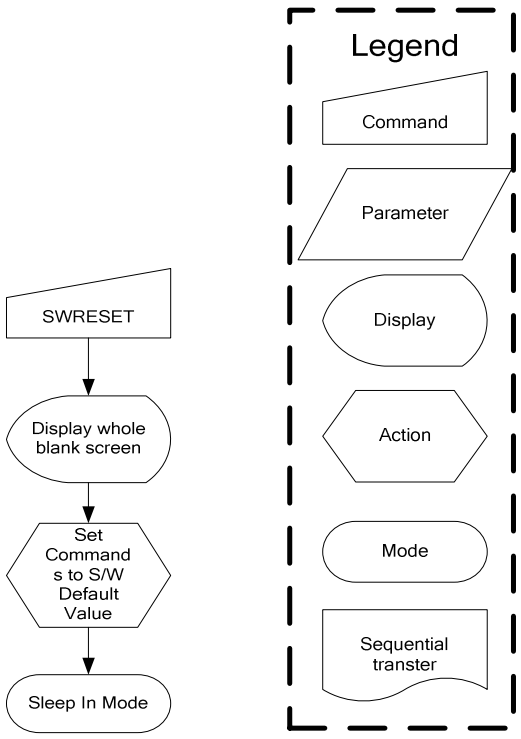
	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	0	0	0	0	0	1	01H
Parameter	No parameter											

Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values and all segment & common outputs are set to Vm (display off: blank display). (See default tables in each command description) Note: The Frame Memory contents are unaffected by this command
Restriction	It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display suppliers' factory default values to the registers during 5msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep Out command. Software Reset command cannot be sent during Sleep Out sequence.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart	

8.1.3. RDDST: Read Display Status (09H)

NOTE: "-" Don't care

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	0	0	1	0	0	1	09H
Dummy Read	1	0	1	-	-	-	-	-	-	-	-	-
2nd parameter	1	0	1	ST31	ST30	ST29	ST28	ST27	ST26	ST25	ST24	-
3rd parameter	1	0	1	ST23	ST22	ST21	ST20	ST19	ST18	ST17	ST16	-
4th parameter	1	0	1	ST15	ST14	ST13	ST12	ST11	ST10	ST9	ST8	-
5th parameter	1	0	1	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0	-

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
ST31	Booster Voltage Status	"1"=Booster on (Booster is OK), "0"=off
ST30	Row Address Order (MY)	"1"=Decrement, "0"=Increment
ST29	Column Address Order (MX)	"1"=Decrement, "0"=Increment
ST28	Row/Column Order (MV)	"1"= Row/column exchange (MV=1) "0"= Normal (MV=0)
ST27	Scan Address Order (ML)	"1"=Decrement, "0"=Increment
ST26	RGB/BGR Order (RGB)	"1"=BGR, "0"=RGB
ST25	Not Used	"0"
ST24	Not Used	"0"
ST23	Not Used	"0"
ST22	Interface Color Pixel Format Definition	"010" = 8-bit / pixel "011" = 12-bit / pixel "100" = Not defined "101" = 16-bit / pixel, "110" = 18-bit / pixel, "111" = Not defined
ST21		
ST20		
ST19	Idle Mode On/Off	"1" = On, "0" = Off
ST18	Partial Mode On/Off	"1" = On, "0" = Off
ST17	Sleep In/Out	"1" = Out, "0" = In
ST16	Display Normal Mode On/Off	"1" = Normal Display On, "0" = Normal Display Off
ST15	Vertical Scrolling Status	"1" = Scroll on, "0" = Scroll off
ST14	Not Used	"0"
ST13	Inversion Status	"1" = On, "0" = Off
ST12	All Pixels On	"1" = mode On, "0" = mode Off
ST11	All Pixels Off	"1" = mode On, "0" = mode Off
ST10	Display On/Off	"1" = On, "0" = Off
ST9	Tearing effect line on/off	"1" = On, "0" = Off
ST8	Not Used	"0"
ST7	Not Used	"0"
ST6	Not Used	"0"
ST5	Tearing effect line mode	"0" = mode1, "1" = mode2
ST4	Not Used	"0"
ST3	Not Used	"0"
ST2	Not Used	"0"

	ST1	Not Used	“0”
	ST0	Not Used	“0”
Restriction			

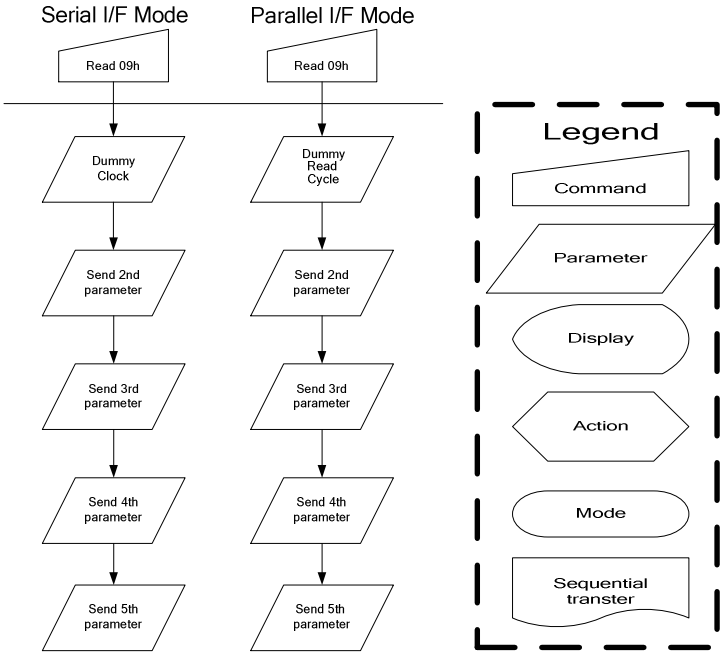
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000 0000_0101 0001_0000 0000_0000 0000
S/W Reset	0xxx xx00_0xxx 0001_0000 0000_0000 0000
H/W Reset	0000 0000_0101 0001_0000 0000_0000 0000

Flow Chart



8.1.4. RDDMADCTL: Read Display MADCTL (0BH)

NOTE: "-" Don't care

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	0	0	1	0	1	1	0BH
1st parameter	1	0	1	-	-	-	-	-	-	-	-	-
2nd parameter	1	0	1	D7	D6	D5	D4	D3	0	0	0	-

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Row Address Order (MY)	"1"=Decrement, "0"=Increment
D6	Column Address Order (MX)	"1"=Decrement, "0"=Increment
D5	Row/Column Order (MV)	"1"= Row/column exchange (MV=1) "0"= Normal (MV=0)
D4	Scan Address Order (ML)	"1"=Decrement, "0"=Increment
D3	RGB/BGR Order (RGB)	"1"=BGR, "0"=RGB

Restriction

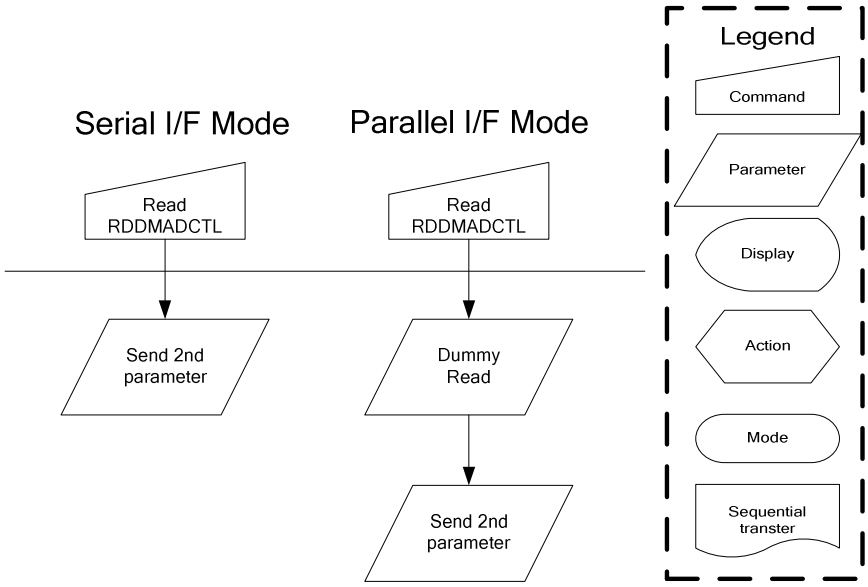
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000_0000 (00h)
S/W Reset	No change
H/W Reset	0000_0000 (00h)

Flow Chart



8.1.5. RDDCOLMOD: Read Display Pixel Format (0CH)

NOTE: "-" Don't care

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	0	0	1	1	0	0	0CH
1st parameter	1	0	1	-	-	-	-	-	-	-	-	-
2nd parameter	1	0	1	0	0	0	0	0	D2	D1	D0	-

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D2	Control Interface Color Format	"010"=8 bit/pixel "011"=12 bit/pixel "101"=16 bit/pixel "110"=18 bit/pixel The others = not defined
D1		
D0		

Restriction

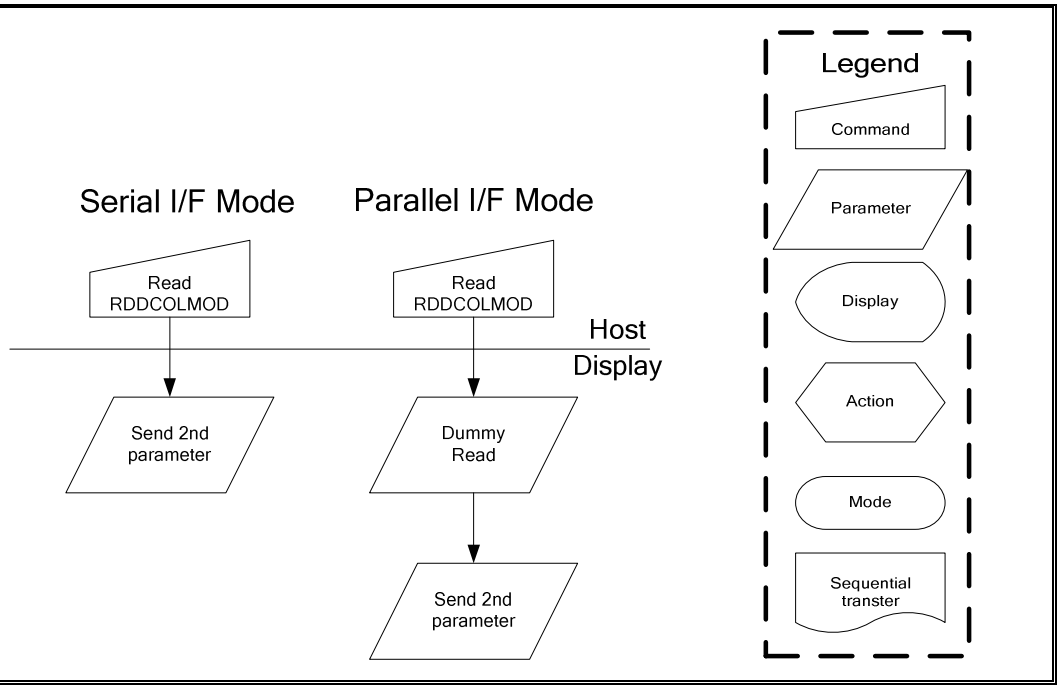
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	16 bit/pixel
S/W Reset	No change
H/W Reset	16 bit/pixel

Flow Chart



8.1.6. RDDIM: Read Display Image Mode (0DH)

NOTE: "-" Don't care

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	0	0	1	1	0	1	0DH
1st parameter	1	0	1	-	-	-	-	-	-	-	-	-
2nd parameter	1	0	1	D7	0	D5	D4	D3	0	0	0	-

Description

This command indicates the current status of the display as described in the table below:

Bit	Description		Command
D7	Vertical Scrolling On/Off	0	Vertical scrolling off
		1	Vertical scrolling is On,
D5	Inversion On/Off	0	Inversion is Off
		1	Inversion is On
D4	All Pixels On	0	Normal Mode
		1	All Pixels are on
D3	All Pixels Off	0	Normal Mode
		1	All Pixels are off

Restriction

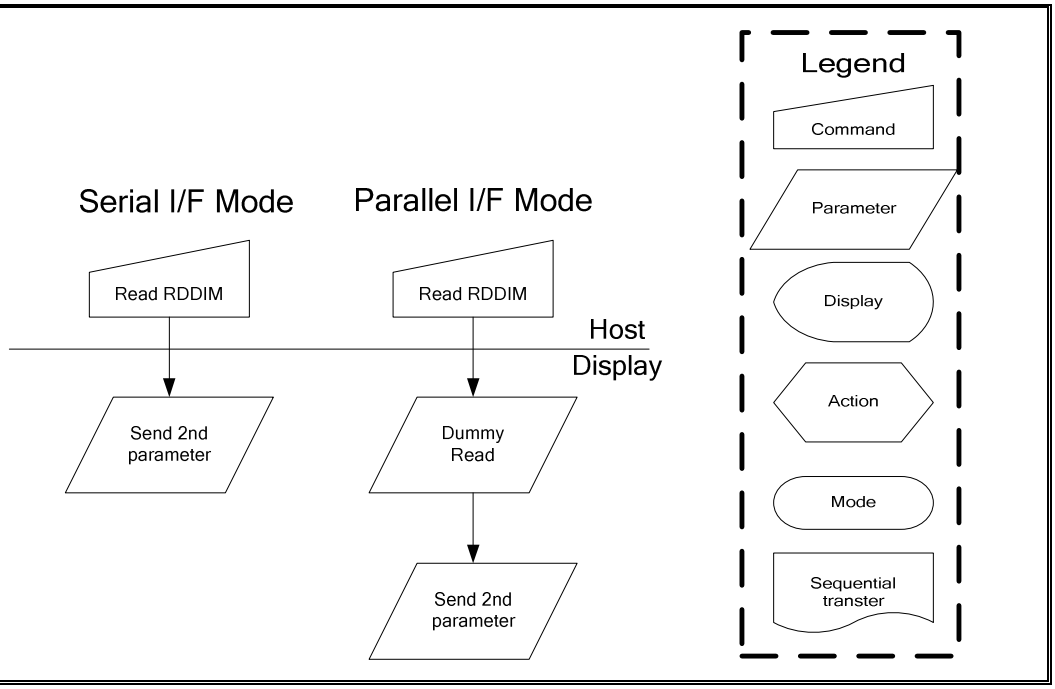
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

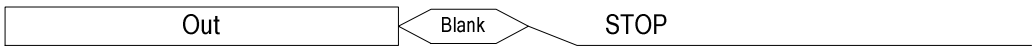
Status	Default Value (D7 to D0)
Power On Sequence	0000_0000 (00h)
S/W Reset	0000_0000 (00h)
H/W Reset	0000_0000 (00h)

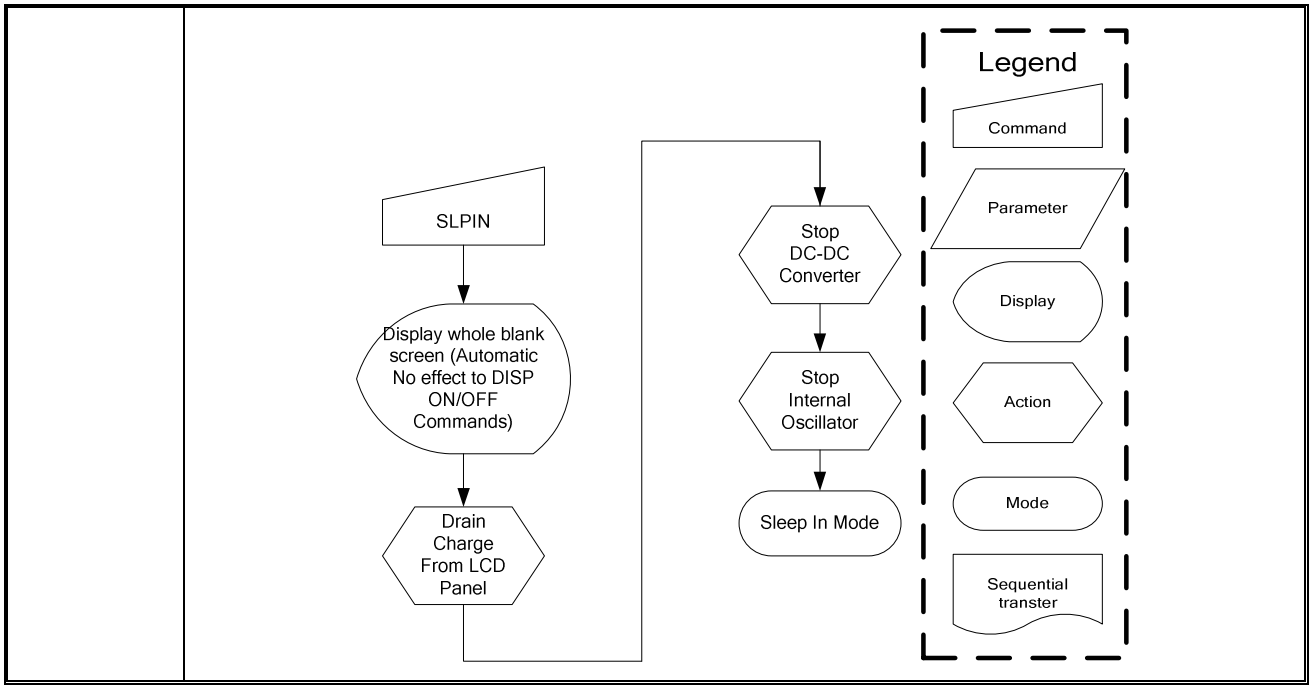
Flow Chart



8.1.7. SLPIN : Sleep In(10H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	0	1	0	0	0	0	10H
Parameter	No parameter											

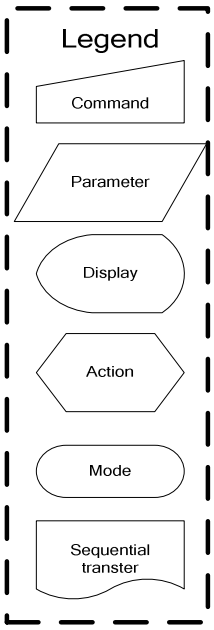
Description	This command causes the LCD module to enter the minimum power consumption mode. In this mode e.g. the DC/DC converter, Internal oscillator, and panel scanning are all stopped.  MCU interface and memory are still working and the memory keeps its contents.
Restriction	This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.
Register Availability	**Status** / **Availability** Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes
Default	**Status** / **Default Value** Power On Sequence: Sleep In Mode S/W Reset: Sleep In Mode H/W Reset: Sleep In Mode
Flow Chart	It takes about 120 msec to get into Sleep In mode (booster off state) after SLPIN command issued. The results of booster off can be check by RDDST (09h) command Bit31.



8.1.8. SLPOUT: Sleep Out (11H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	0	1	0	0	0	1	11H
Parameter	No parameter											

Description	This command turns off sleep mode. In this mode e.g. the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started. 
Restriction	This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode. The display module is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep In Mode</td></tr><tr><td>S/W Reset</td><td>Sleep In Mode</td></tr><tr><td>H/W Reset</td><td>Sleep In Mode</td></tr></table>
Flow Chart	It takes 120msec to become Sleep Out mode (booster on mode) after SLPOUT command issued. The results of booster on can be check by RDDST (09h) command Bit31.



8.1.9. PTLON : Partial Mode On (12H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	0	1	0	0	1	0	12H
Parameter	No parameter											

Description	This command turns on partial mode The partial mode window is described by the Partial Area command (30H). Exit from PTLON by Normal Display Mode On command (13H) There is no abnormal visual effect during mode change between Normal mode On <-> Partial mode On.
Restriction	This command has no effect when Partial mode is active.
Register Availability	
Default	
Flow Chart	See Partial Area (30h)

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	Partial mode off
S/W Reset	Partial mode off
H/W Reset	Partial mode off

8.1.10. NORON: Normal Display Mode On (13H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	0	1	0	0	1	1	13H
Parameter	No parameter											

Description	This command returns the display to normal mode. Normal display mode on means Partial mode off. Exit from NORON by the Partial mode On command (12h) There is no abnormal visual effect during mode change between Normal mode On <-> Partial mode On.
Restriction	This command has no effect when Normal Display mode is active.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

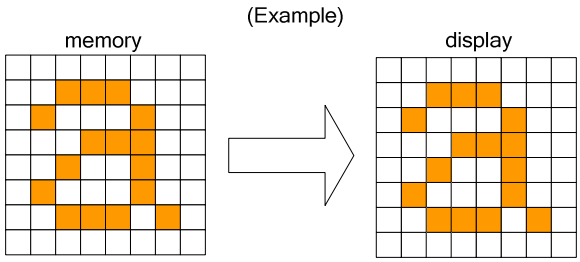
Default

Status	Default Value
Power On Sequence	Normal Mode On
S/W Reset	Normal Mode On
H/W Reset	Normal Mode On

Flow Chart	See Partial Area and Vertical Scrolling Definition Descriptions for details of when to use this command

8.1.11. INVOFF: Display Inversion Off (20H)

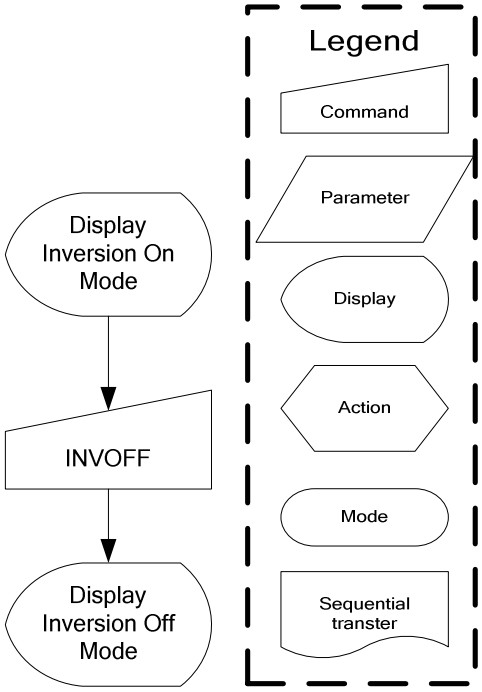
	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	1	0	0	0	0	0	20H
Parameter	No parameter											

Description	This command is used to recover from display inversion mode. This command makes no change of contents of frame memory. This command does not change any other status. 
Restriction	This command has no effect when IC is already in inversion off mode.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

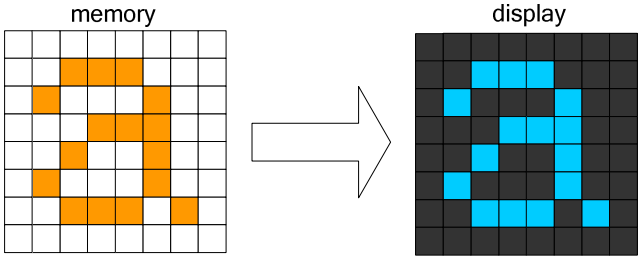
Default

Status	Default Value
Power On Sequence	Display Inversion Off
S/W Reset	Display Inversion Off
H/W Reset	Display Inversion Off

Flow Chart	

8.1.12. INVON: Display Inversion On (21H)

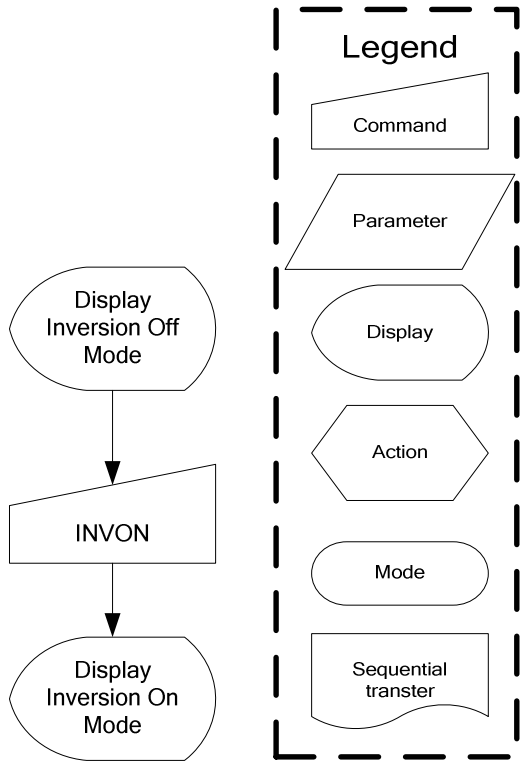
	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	1	0	0	0	0	1	21H
Parameter	No parameter											

Description	This command is used to enter into display inversion mode. This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display. This command does not change any other status. (Example) memory display 
Restriction	This command has no effect when IC is already in inversion on mode.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion Off
S/W Reset	Display Inversion Off
H/W Reset	Display Inversion Off

Flow Chart	

8.1.13. ALLPOFF : ALL Pixels Off (22H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	1	0	0	0	1	0	22H
Parameter	No parameter											

Description

This command is only used for test purposes e.g. pixel response time (on/off) measurements on the passive matrix display. Therefore, it is possible that this command is not used for final product software.

There is not used PWM or Mixed FRC/PWM driving method on the display.

All driver outputs become “Low” data state and display becomes black.

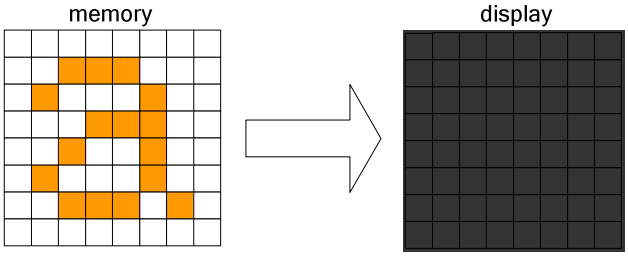
This command makes no change of contents of display memory.

This command does not change any other status.

Exit commands are “All Pixels On”, “Normal Display Mode On” and “Partial Display On”.

The display is showing the contents of the frame memory after “Normal Display Mode On” and “Partial Display On” commands.

(Example)



Restriction

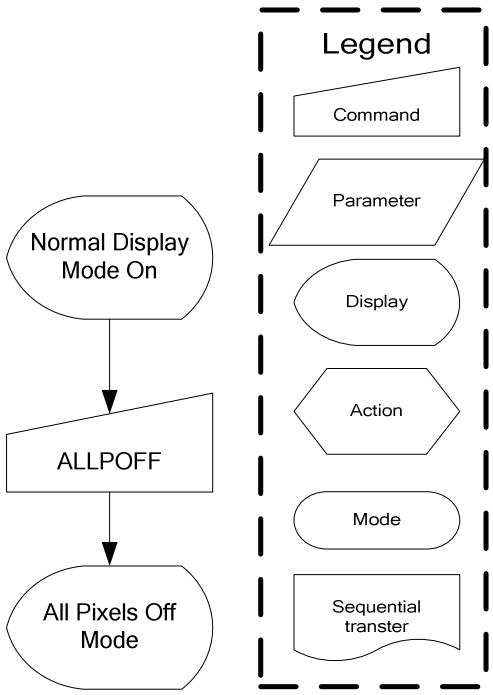
This command has no effect when IC is already in all pixels off mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

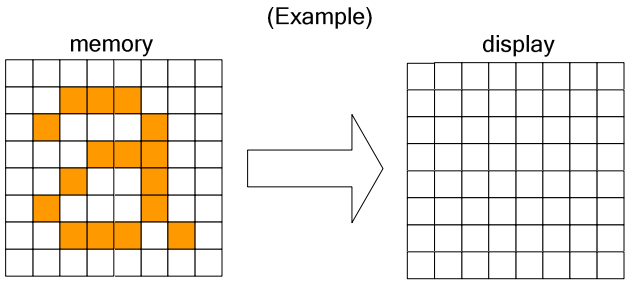
Default

Status	Default Value
Power On Sequence	All pixel off mode disable
S/W Reset	All pixel off mode disable
H/W Reset	All pixel off mode disable

Flow Chart	

8.1.14. ALLPON: All Pixels On (23H) (Only for Test Purposes)

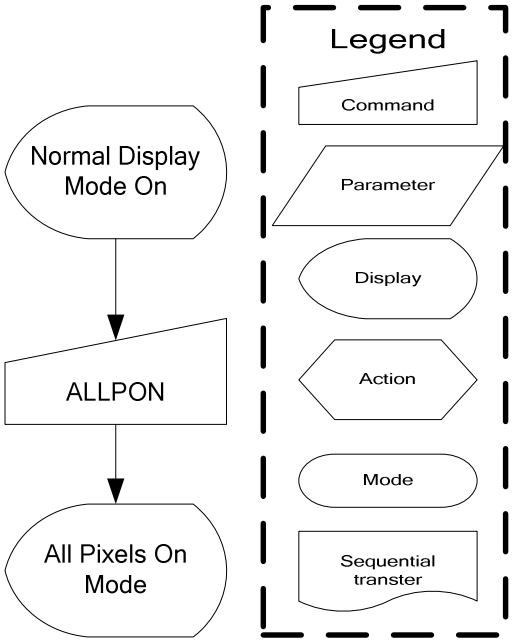
	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	1	0	0	0	1	1	23H
Parameter	No parameter											

Description	This command is only used for test purposes e.g. pixel response time (on/off) measurements on the passive matrix display. Therefore, it is possible that this command is not used for final product software. There is not used PWM or Mixed FRC/PWM driving method on the display. All driver outputs become “High” data state and display becomes white. This command makes no change of contents of display memory. This command does not change any other status. Exit commands are “All Pixels On”, “Normal Display Mode On” and “Partial Display On”. The display is showing the contents of the frame memory after “Normal Display Mode On” and “Partial Display On” commands. 
Restriction	This command has no effect when IC is already in all pixels on mode.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	All pixel on mode disable
S/W Reset	All pixel on mode disable
H/W Reset	All pixel on mode disable

Flow Chart	

8.1.15. WRCNTR: Write Contrast (25H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	1	0	0	1	0	1	25H
Parameter	1	1	0	0	EV6	EV5	EV4	EV3	EV2	EV1	EV0	00H~7FH

Description

This command is used to fine tuning the contrast of the current display.

This contrast values can affect segment and common outputs.

Parameter range: 0-127dec. MSB is EV6 and LSB is EV0.

Default value: 63dec (3Fh)

Restriction

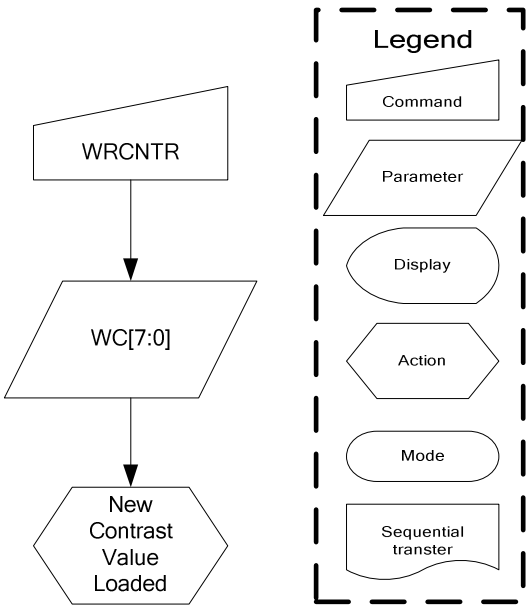
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	3Fh
S/W Reset	3Fh
H/W Reset	3Fh

Flow Chart



8.1.16. DISPOFF: Display Off (28H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	1	0	1	0	0	0	28H
Parameter	No parameter											

Description

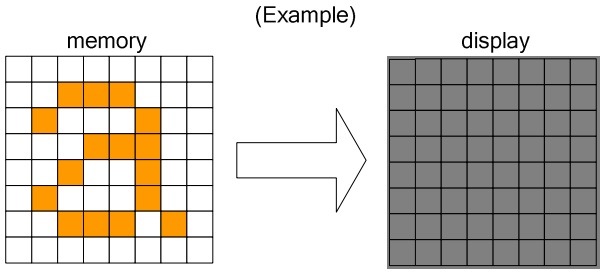
This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted.

This command makes no change of contents of frame memory.

This command does not change any other status.

There will be no abnormal visible effect on the display.

Exit from this command by Display On (29h)



Restriction

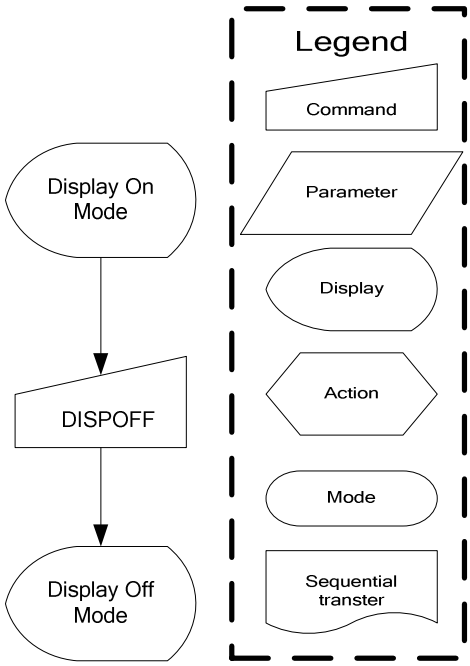
This command has no effect when module is already in display off mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

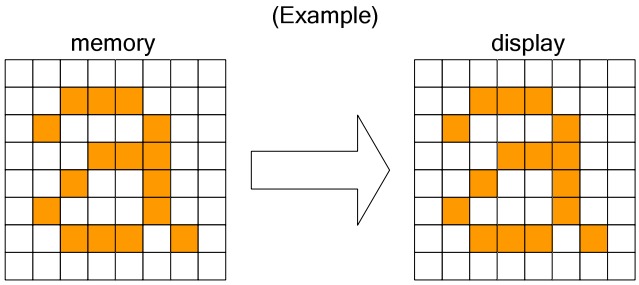
Default

Status	Default Value
Power On Sequence	Display Off
S/W Reset	Display Off
H/W Reset	Display Off

Flow Chart	

8.1.17. DISPON: Display On (29H)

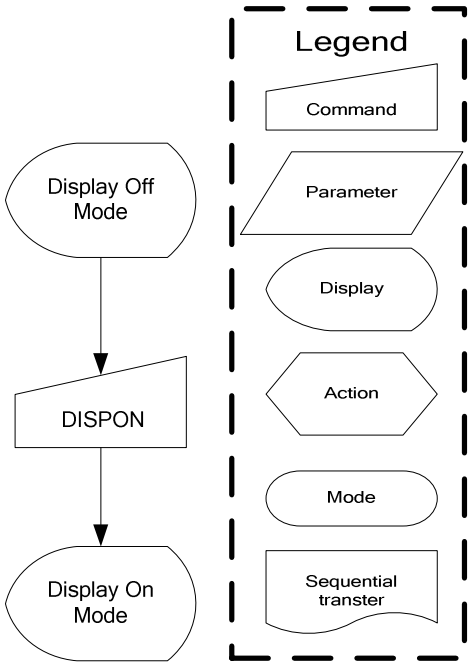
	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	1	0	1	0	0	1	29H
Parameter	No parameter											

Description	Turn on the display screen according to the current display data RAM content and the display timing and setting. This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled. This command makes no change of contents of frame memory. This command does not change any other status. 
Restriction	This command has no effect when module is already in display on mode.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Off
S/W Reset	Display Off
H/W Reset	Display Off

Flow Chart	

8.1.18. CASET: Column Address Set (2AH)

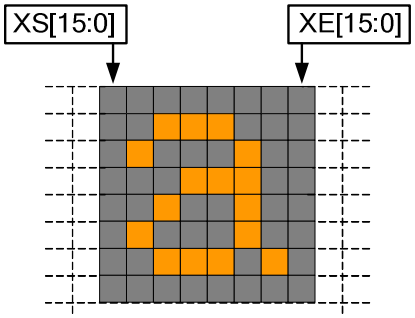
	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	1	0	1	0	1	0	2AH
1st parameter	1	1	0	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8	Note1
2nd parameter	1	1	0	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	Note1
3rd parameter	1	1	0	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8	Note1
4th parameter	1	1	0	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	Note1

Description

This command is used to define area of frame memory where MCU can access.

This command makes no change on the other driver status.

The values of XS[15:0] and XE[15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.



Restriction

XS[15:0] always must be equal to or less than XE[15:0]

Note 1: When XS[15:0] or XE[15:0] is greater than 7Fh (when MADCTL's MV=0) or 9Fh (when MADCTL's MV=1), data of out of range will be ignored

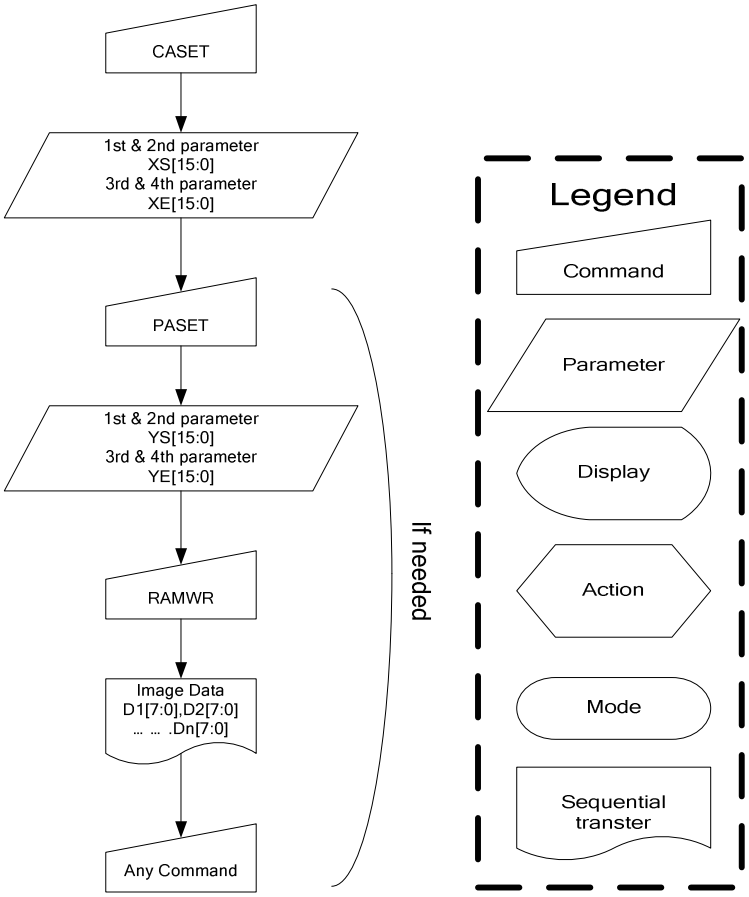
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	XS [15:0]	XE [15:0] (MV=0)	XE [15:0] (MV=1)
Power On Sequence	00h	7Fh	
S/W Reset	00h	7Fh	9Fh
H/W Reset	00h	7Fh	

Flow Chart



8.1.19. RASET: Row Address Set (2BH)

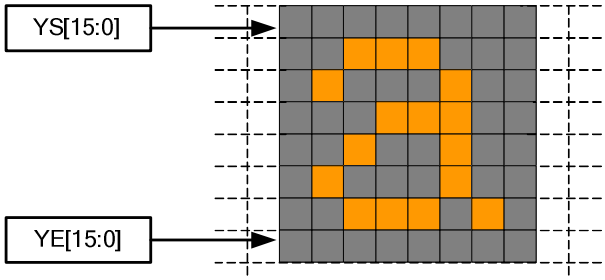
	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	1	0	1	0	1	1	2BH
1st parameter	1	1	0	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8	Note1
2nd parameter	1	1	0	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	Note1
3rd parameter	1	1	0	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8	Note1
4th parameter	1	1	0	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	Note1

Description

This command is used to define area of frame memory where MCU can access.

This command makes no change on the other driver status.

The values of YS[15:0] and YE[15:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory.



Restriction

YS[15:0] always must be equal to or less than YE[15:0]

Note 1: When YS[15:0] or YE[15:0] are greater than 9Fh (When MADCTL's MV=0) or 7Fh (When MADCTL's MV=1), data of out of range will be ignored.

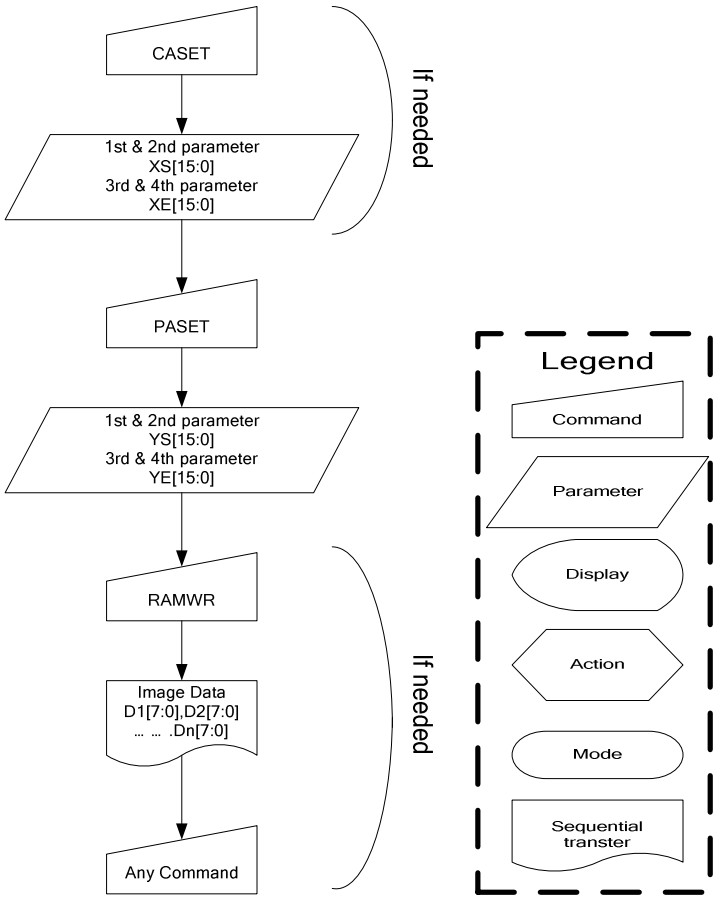
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	YS [15:0]	YE [15:0] (MV=0)	YE [15:0] (MV=1)
Power On Sequence	00h	9Fh	
S/W Reset	00h	9Fh	7Fh
H/W Reset	00h	9Fh	

Flow Chart



8.1.20. RAMWR: Memory Write (2CH)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	1	0	1	1	0	0	2CH
Write D1[7:0]	1	1	0	D17	D16	D15	D14	D13	D12	D11	D10	00H ~ FFH
…	1	1	0	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	00H ~ FFH
Write Dn[7:0]	1	1	0	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	00H ~ FFH

Description

This command is used to transfer data from MCU to frame memory.

This command makes no change to the other driver status.

When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions.

The Start Column/Start Row positions are different in accordance with MADCTL setting.

Then D [7:0] is stored in frame memory and the column register and the row register incremented as in section 7.3.

Frame Write can be canceled by sending any other command.

Restriction

In all color modes, there is no restriction on length of parameters.

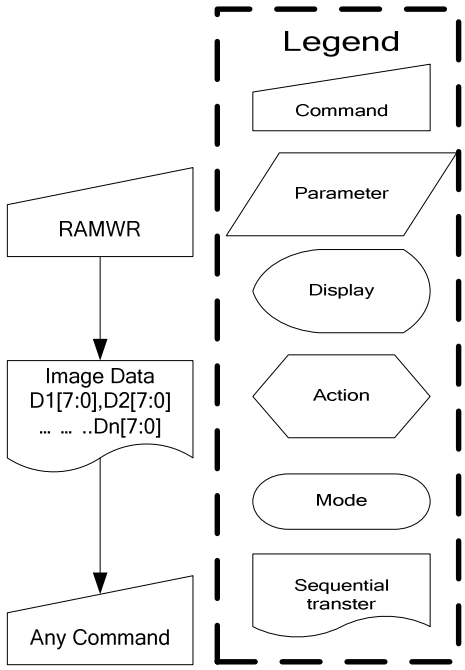
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is remained
H/W Reset	Contents of memory is remained

Flow Chart



8.1.21. RAMRO : Memory Read (2EH)

NOTE: "-" Don't care

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	1	0	1	1	1	0	2EH
1st parameter	1	0	1	-	-	-	-	-	-	-	-	-
2nd parameter	1	0	1	D17	D16	D15	D14	D13	D12	D11	D10	00H ~ FFH
…	1	0	1	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	00H ~ FFH
(N+1)th parameter	1	0	1	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	00H ~ FFH

Description

This command is used to transfer data from frame memory to MCU.

This command makes no change to the other driver status.

When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions.

The Start Column/Start Page positions are different in accordance with MADCTL setting. (See section7.3)

Then D[7:0] is read back from the frame memory and the column register and the page register incremented as in section 7.3

Frame Read can be stopped by sending any other command.

Restriction

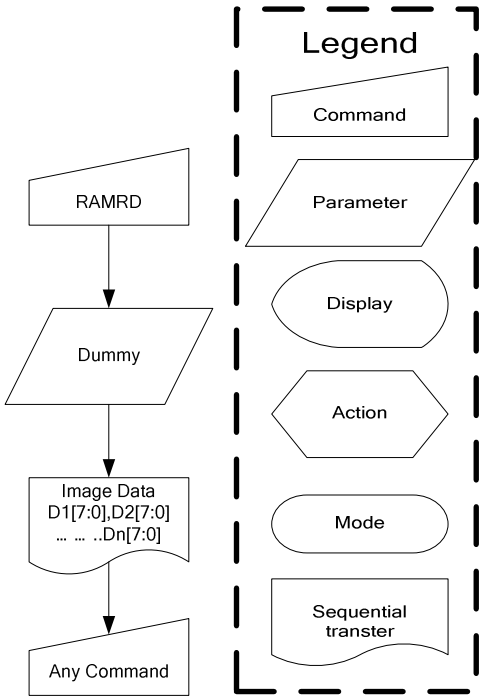
Memory Read is only possible via the Parallel Interface.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart	

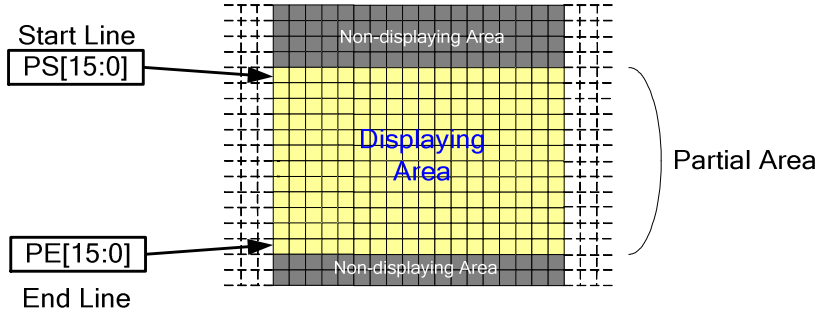
8.1.22. PTLAR: Partial Area (30H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	1	1	0	0	0	0	30H
1st parameter	1	1	0	PS15	PS14	PS13	PS12	PS11	PS10	PS9	PS8	00H ~ 9FH
2nd parameter	1	1	0	PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0	
3rd parameter	1	1	0	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	00H ~ 9FH
4th parameter	1	1	0	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0	

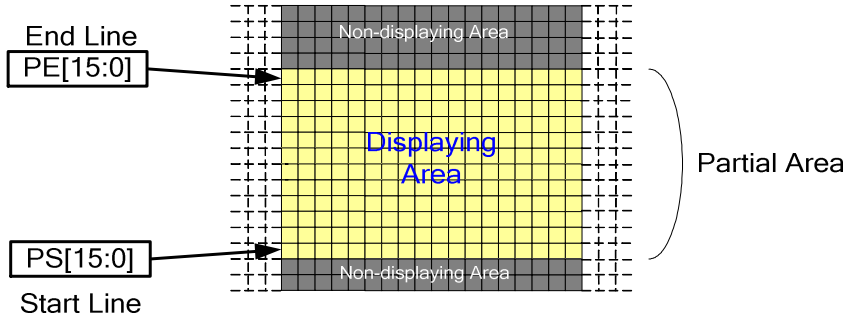
Description

This command defines the partial mode's display area. There are 4 parameters associated with this command, the first part defines the Start Line (PS) and the second defines End Line (PE), as illustrated in the figures below. PS and PE refer to the Frame Memory Line counter.

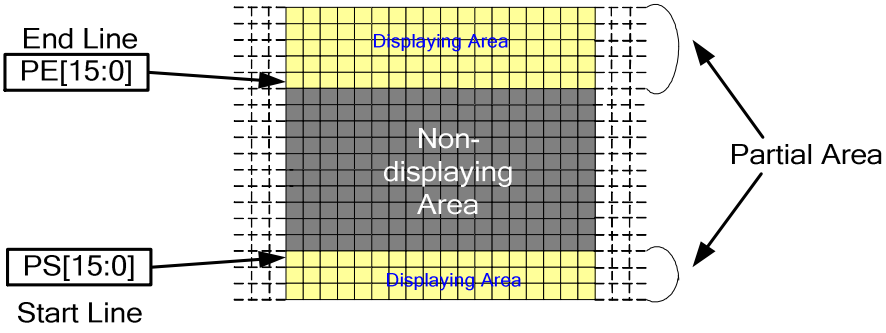
If End Line > Start Line when MADCTL ML=0:



If End Line > Start Line when MADCTL ML=1:



If End Line < Start Line when MADCTL ML=0:



* Row1: Frame memory row address 1.

If End Line = Start Line then the Partial Area will be one line deep.

Restriction

PS[15:0] and PE[15:0] cannot be greater than 9Fh.

Register Availability

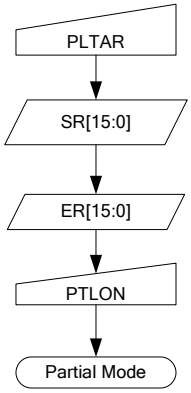
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

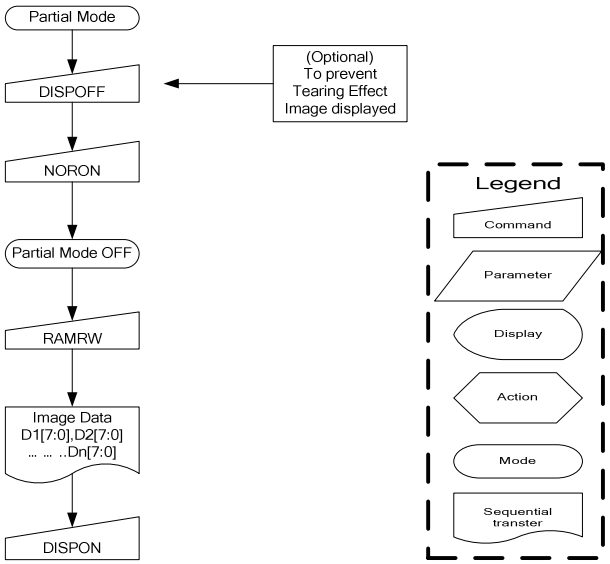
Status	Default Value	
Power On Sequence	PS[15:0]=0000H	PE[15:0]=009FH
S/W Reset	PS[15:0]=0000H	PE[15:0]=009FH
H/W Reset	PS[15:0]=0000H	PE[15:0]=009FH

Flow Chart

1. TO Enter Partial Mode:



2. Leave Partial Mode



8.1.23. RLAR: Scroll Area (33h)

NOTE: "-" Don't care

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RLAR	0	1	0	0	0	1	1	0	0	1	1	(33h)
1st parameter	1	1	0	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	-
2nd parameter	1	1	0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	-
3rd parameter	1	1	0	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	-

Description

This command just defines the Vertical Scrolling Area of the display and not performs vertical scroll.

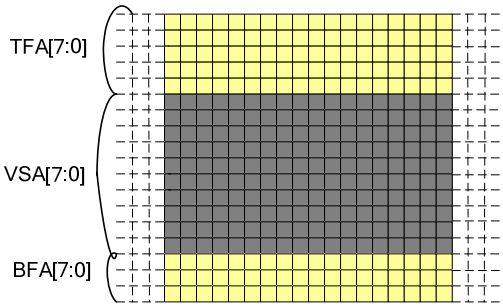
When MADCTL ML=0

The 1st parameter TFA [7:0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).

The 2nd parameter VSA [7:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address) The first line appears immediately after the bottom most line of the Top Fixed Area.

The 3rd parameter BFA [7:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

TFA, VSA and BFA refer to the Frame Memory Line Pointer.



Restriction

The condition is (TFA+VSA+BFA) = 160.

Register Availability

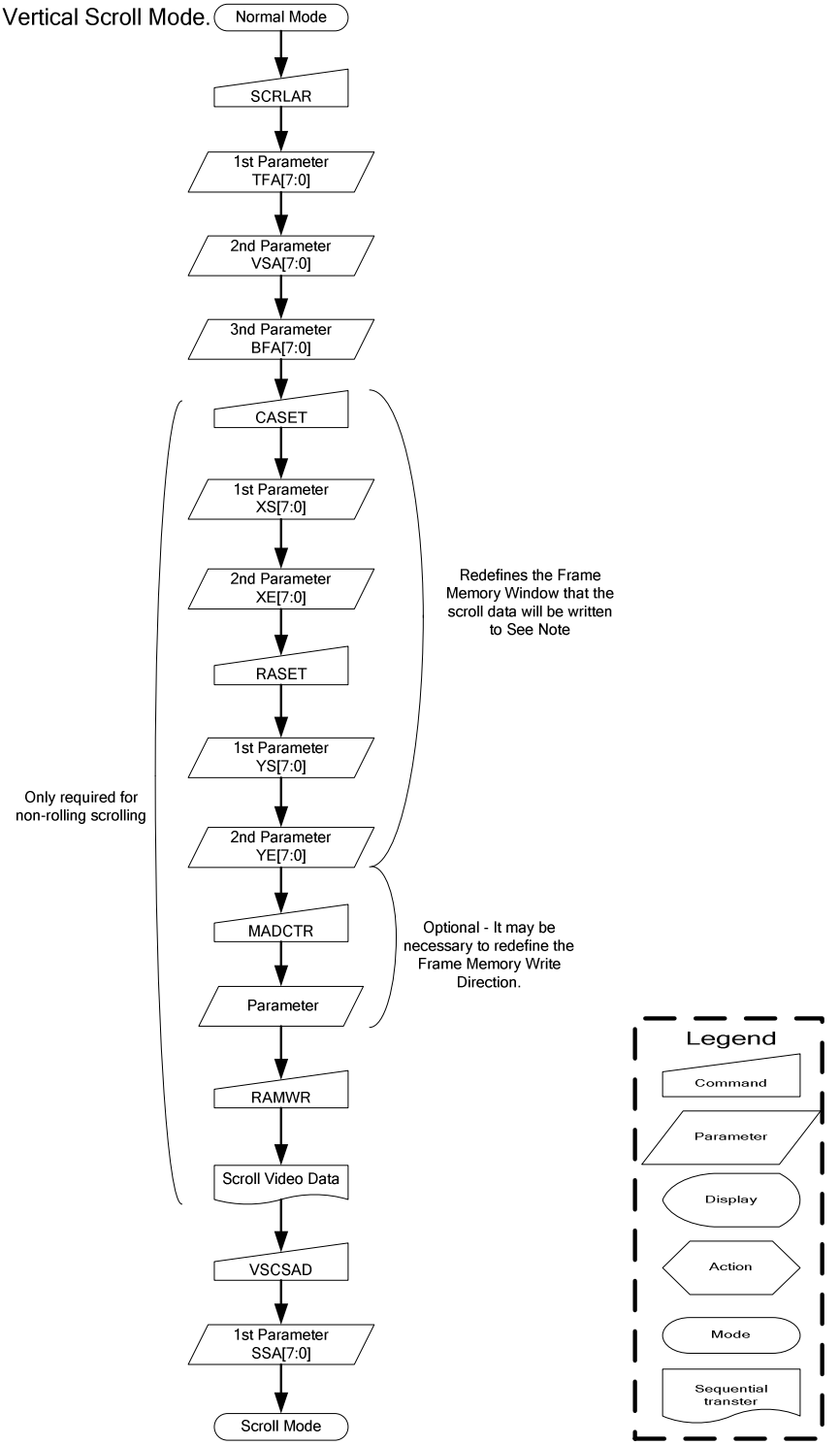
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	TFA [7:0]	VSA [7:0]	BFA [7:0]
Power On Sequence	00h	A0h	00h
S/W Reset	00h	A0h	00h
H/W Reset	00h	A0h	00h

Flow Chart

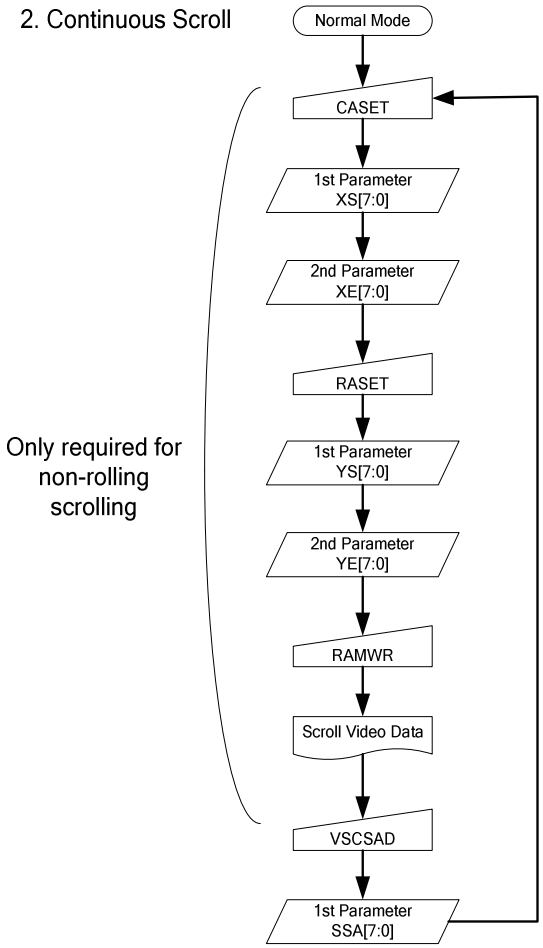
1.To enter Vertical Scroll Mode.



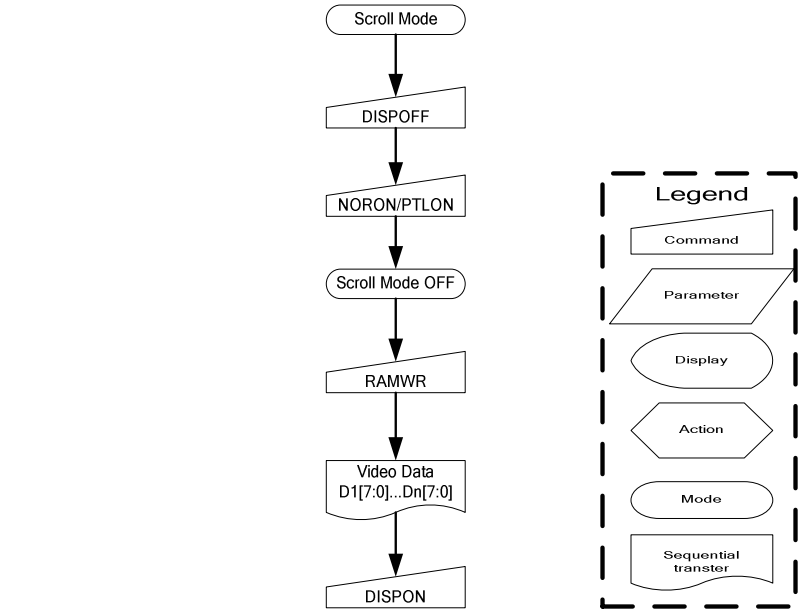
NOTE: The Frame Memory Window size must be defined correctly otherwise undesirable image will be displayed.

Flow Chart

2. Continuous Scroll



3. To Exit Vetical Scroll mode



NOTE: Scroll Mode can be exit by both the Normal Display Mode On(13h) and Partial Mode On (12h) commands.

8.1.24. TEOFF: Tearing Effect Line Off (34H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	1	1	0	1	0	0	34H
Parameter	No Parameter											

Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.
Restriction	This command has no effect when Tearing Effect output is already OFF.

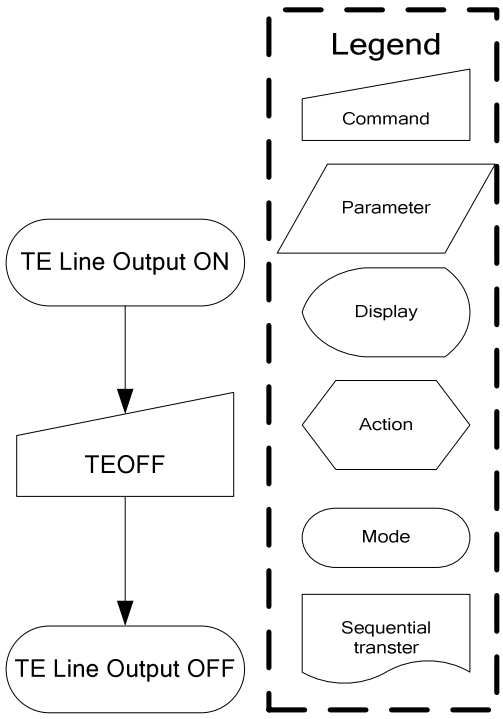
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Tearing effect off
S/W Reset	Tearing effect off
H/W Reset	Tearing effect off

Flow Chart



8.1.25. TEON: Tearing Effect Line On (35H)

NOTE: "-" Don't care

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	1	1	0	1	0	1	35H
Parameter	1	1	0	-	-	-	-	-	-	-	M	-

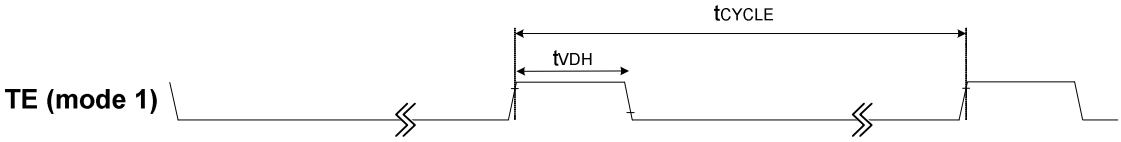
Description

This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit ML.

The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line. ("-"=Don't Care).

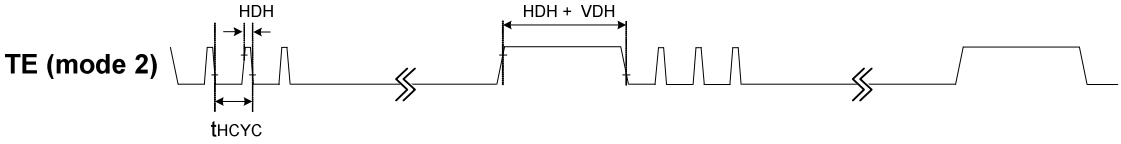
When M=0:

The Tearing Effect Output signal consists of V-Sync(tVDH) information.



When M=1:

The Tearing Effect Output signal consists of both H-Sync(tHDH) and V-Sync(tVDH) information.



Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Restriction

This command has no effect when Tearing Effect output is already ON.

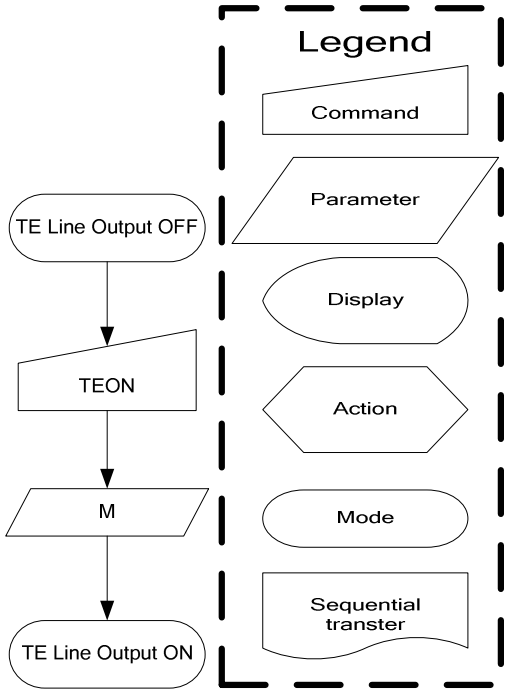
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Tearing effect off & M=0
S/W Reset	Tearing effect off & M=0
H/W Reset	Tearing effect off & M=0

Flow Chart



8.1.26. MADCTL: Memory Access Control (36H)

NOTE: "-" Don't care

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	1	1	0	1	1	0	36H
Parameter	1	1	0	MY	MX	MV	ML	RGB	-	-	-	-

Description

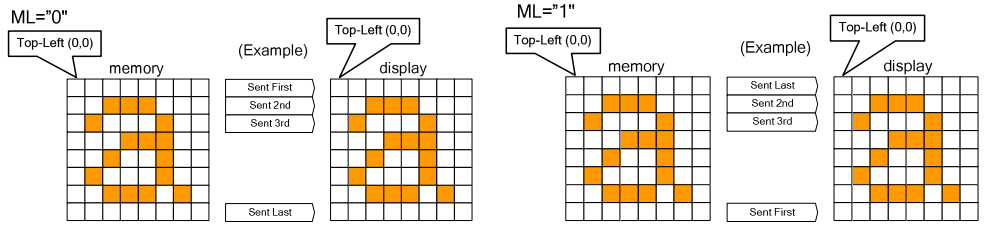
This command defines read/write scanning direction of frame memory.

This command makes no change on the other driver status.

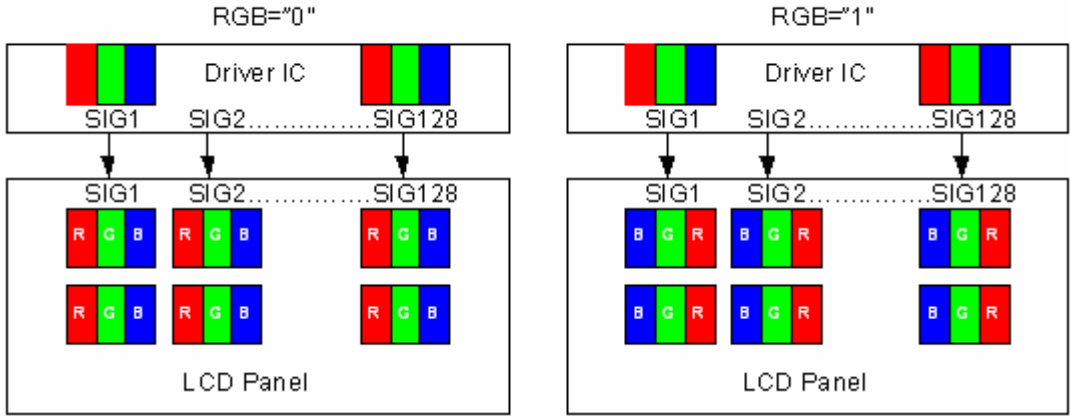
Note: ML affects to Partial Area (30h), Vertical Scrolling Definition (33h), Vertical Scrolling Start address (37h), Partial On (12h) commands

Bit	NAME	DESCRIPTION
MY	Page Address Order	These 3 bits controls MCU to memory write/read direction.
MX	Column Address Order	
MV	Page/Column Selection	
ML	Vertical Order	LCD vertical refresh direction control
RGB	RGB-BGR Order	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel) The contents of the frame memory are not changed.

ML:Line(Scan) Address Order



RGB: RGB-BGR Order



Note: Top-Left (0,0) means a physical memory location.

Restriction

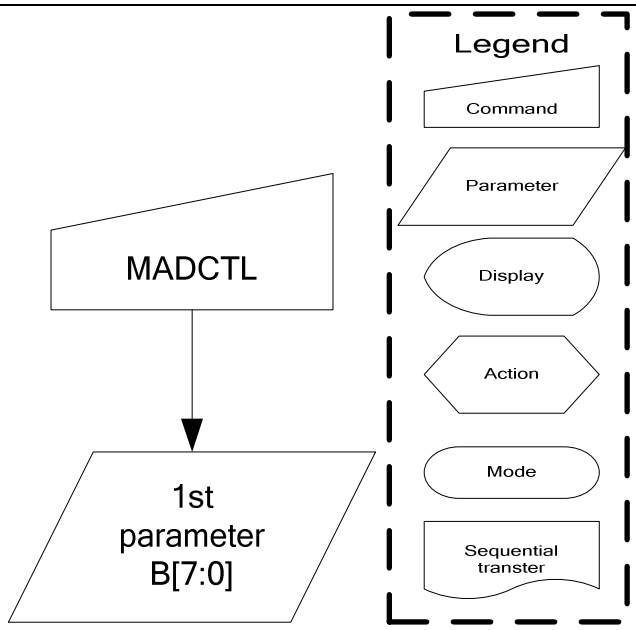
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	MY=0,MX=0, MV=0, ML=0,RGB=0
S/W Reset	No Change
H/W Reset	MY=0,MX=0, MV=0, ML=0,RGB=0

Flow Chart



8.1.27. VSCSAD: Vertical Scroll Start Address of RAM (37h)

NOTE: "-" Don't care

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VSCSAD	0	1	0	0	0	1	1	0	1	1	1	(37h)
Parameter	1	1	0	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	-

Description

This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode.

The Vertical Scrolling Start Address command has one parameter which describes which line in the Frame Memory will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:

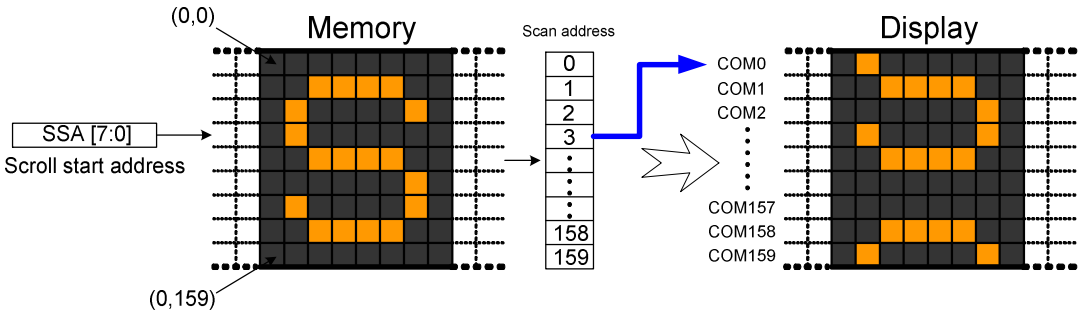
This command starts the scrolling.

Exit from V-scrolling mode by commands Partial mode On (12h) or Normal mode On (13h).

When MADCTL ML=0

Example:

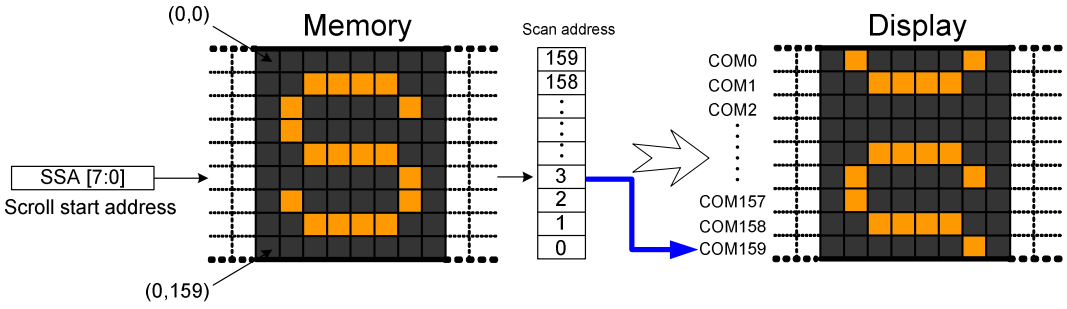
When Top Fixed Area=Bottom Fixed Area=00, Vertical Scrolling Area=160 and Vertical Scrolling Pointer SSA='3'.



When MADCTL ML=1

Example:

When Top Fixed Area=Bottom Fixed Area=00, Vertical Scrolling Area=160 and Vertical Scrolling Pointer SSA='3'.



NOTE: When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect.

<table>
<tr><td></td><td>SSA refers to the Frame Memory line Pointer.</td></tr>
<tr><td>Restriction</td><td>Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h)-otherwise undesirable image will be displayed on the Panel.

SSA [7:0] is based on line unit.
SSA [7:0] = 00h, 01h, 02h, 03h, … , 9Fh</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>See Vertical Scrolling Definition (33h) description.</td></tr>
</table>

8.1.28. IDMOFF: Idle Mode Off (38H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	1	1	1	0	0	0	38H
Parameter	No Parameter											

Description	This command is used to recover from Idle mode on. There will be no abnormal visible effect on the display mode change transition. In the idle off mode, 1. LCD can display maximum 65,536 colors. 2. Normal frame frequency is applied.
Restriction	This command has no effect when module is already in idle off mode.

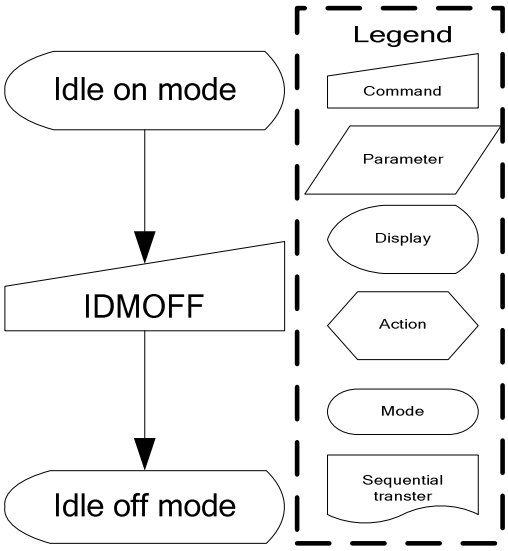
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle Off Mode
S/W Reset	Idle Off Mode
H/W Reset	Idle Off Mode

Flow Chart



8.1.29. IDMON: Idle Mode On (39H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	1	1	1	0	0	1	39H
Parameter	No Parameter											

Description

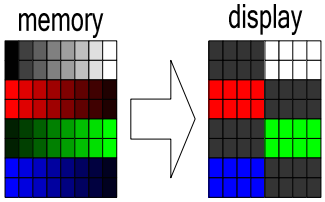
This command is used to enter into Idle mode on.

There will be no abnormal visible effect on the display mode change transition.

In the idle on mode,

1. Color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.
2. 8-Color mode frame frequency is applied.
3. Exit from IDMON by Idle Mode Off (38h) command

(Example)



Memory contents V.S Display Color			
	R5 R4 R3 R2 R1 R0	G5 G4 G3 G2 G1 G0	B5 B4 B3 B2 B1 B0
Black	**0XXXXX**	**0XXXXX**	**0XXXXX**
Blue	**0XXXXX**	**0XXXXX**	**1XXXXX**
Red	**1XXXXX**	**0XXXXX**	**0XXXXX**
Magenta	**1XXXXX**	**0XXXXX**	**1XXXXX**
Green	**0XXXXX**	**1XXXXX**	**0XXXXX**
Cyan	**0XXXXX**	**1XXXXX**	**1XXXXX**
Yellow	**1XXXXX**	**1XXXXX**	**0XXXXX**
White	**1XXXXX**	**1XXXXX**	**1XXXXX**
X=don't care			

Restriction

This command has no effect when module is already in idle on mode.

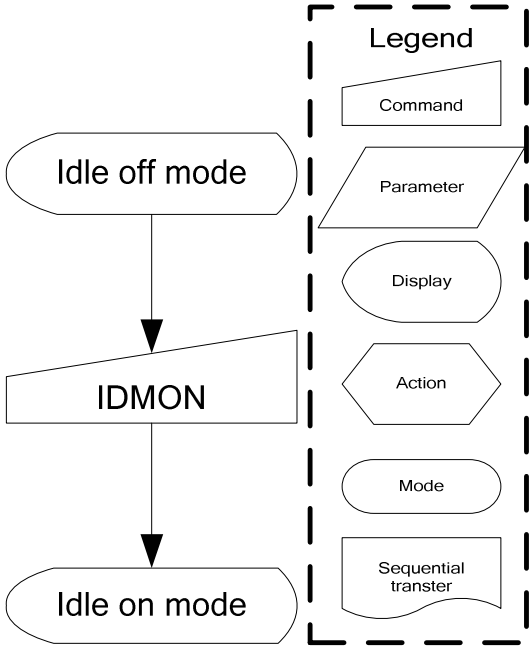
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle Off Mode
S/W Reset	Idle Off Mode
H/W Reset	Idle Off Mode

Flow Chart



8.1.30. COLMOD: Interface Pixel Format (3AH)

NOTE: "-" Don't care

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	0	0	1	1	1	0	1	0	3AH
Parameter	1	1	0	-	-	-	-	-	D2	D1	D0	-

Description

This command is used to define the format of RGB picture data, which is transferred via the MCU Interface. The formats are shown in the table:

Interface Format	D2	D1	D0
Not Defined	0	0	0
Not Defined	0	0	1
8 Bit/Pixel	0	1	0
12 Bit/Pixel	0	1	1
Not Defined	1	0	0
16 Bit/Pixel	1	0	1
18 Bit/Pixel	1	1	0
Not Defined	1	1	1

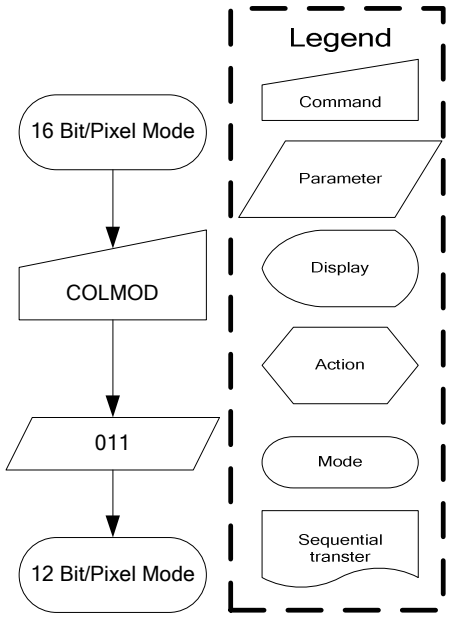
Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	05h (16Bit/Pixel)
S/W Reset	No Change
H/W Reset	05h (16Bit/Pixel)

Flow Chart	

8.1.31. RDID2: Read ID (DBH)

NOTE: "-" Don't care

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	0	1	1	0	1	1	DBH
1st parameter	1	0	1	-	-	-	-	-	-	-	-	-
2nd parameter	1	0	1	1	-	-	-	ID3	ID2	ID1	ID0	-

Description

This read byte returns 8-bit LCD module/driver version ID

D3-D0 (ID3 to ID0): LCD module/driver version ID

Parameter Range: ID=80h to 8Fh

Restriction

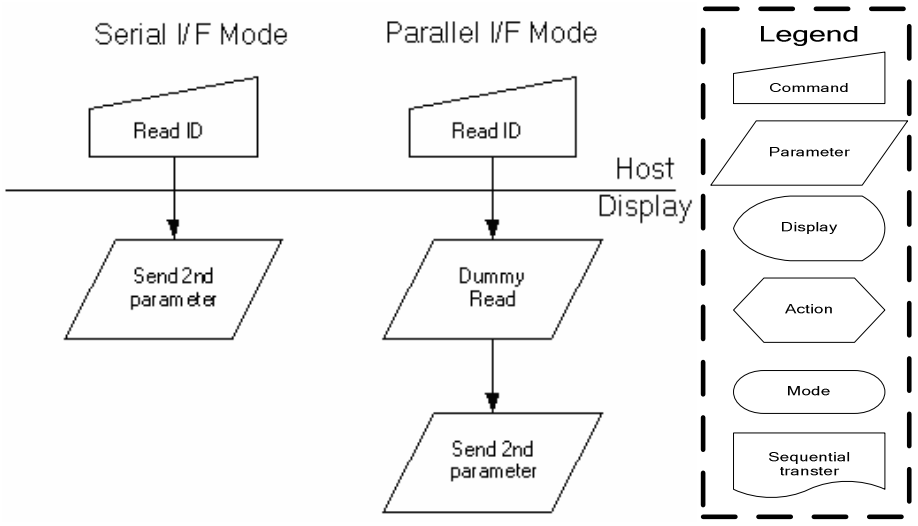
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	80H
S/W Reset	80H
H/W Reset	80H

Flow Chart



8.1.32. DutySet: Display Duty setting (B0H)

NOTE: "-" Don't care

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
DutySet	0	1	0	1	0	1	1	0	0	0	0	(B0h)
Parameter	1	1	0	Du7	Du6	Du5	Du4	Du3	Du2	Du1	Du0	-

Description

This command is used to set display duty. Command set = display duty numbers - 1.

Example:

Duty	Du7	Du6	Du5	Du4	Du3	Du2	Du1	Du0	Command set= Display duty numbers-1
Example: 1/160 duty	1	0	0	1	1	1	1	1	160-1=159

Restriction

Display duty must 3 (1/4 duty)< Duty < 159 (1/160 duty)

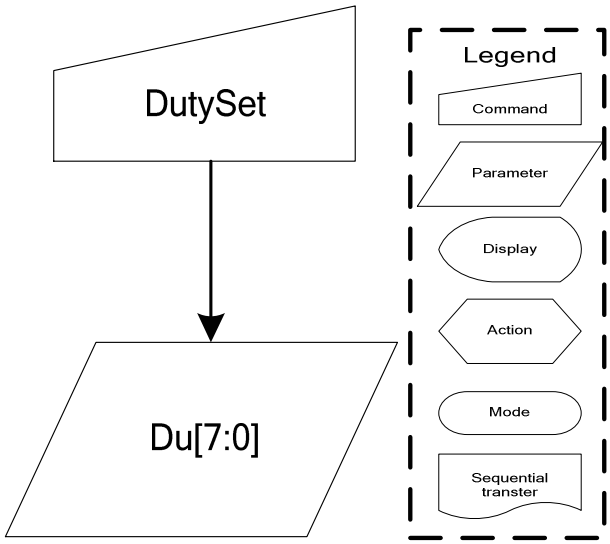
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Du[7:0])
Power On Sequence	10011111b (9Fh)
S/W Reset	10011111b (9Fh)
H/W Reset	10011111b (9Fh)

Flow Chart



8.1.33. FirstCom: First Com. Page address (B1H)

NOTE: "-" Don't care

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
FirstCom	0	1	0	1	0	1	1	0	0	0	1	(B1H)
Parameter	1	1	0	F7	F6	F5	F4	F3	F2	F1	F0	-

Description

This command defines the first output COM number that mapping to the RAM page address 0. For detail setting value, please see the table as below.

F7	F6	F5	F4	F3	F2	F1	F0	Line address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
:	:	:	:	:	:	:	:	:
1	0	0	1	1	1	1	0	158
1	0	0	1	1	1	1	1	159

Example:

If FirstCom=8, common 8 would output the data of RAM page address 0.

Restriction

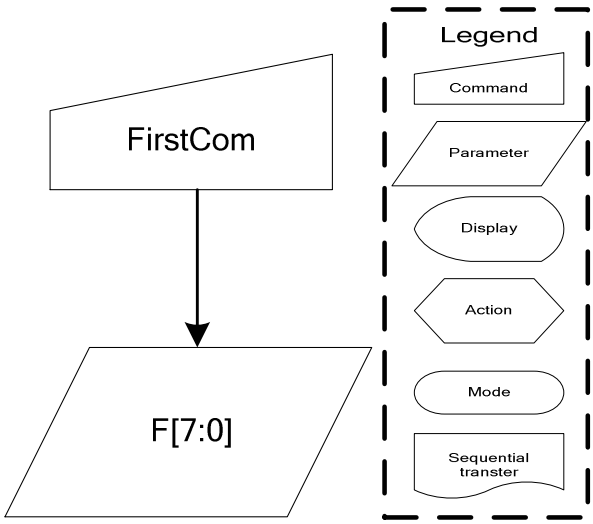
The First COM range is 0~159.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (F[7:0])
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart	

8.1.34. OscDiv: FOSC Divider (B3H)

NOTE: "-" Don't care

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
OscDiv	0	1	0	1	0	1	1	0	0	1	1	(B3H)
Parameter	1	1	0	-	-	-	-	-	-	CLD1	CLD0	-

Description

This command is used to specify the Fosc dividing ratio.

CLD1, CLD0: Fosc dividing ratio. They are used to change number of dividing stages of internal clock.

CLD1	CLD0	Fosc dividing ratio
0	0	Not divide
0	1	2 divisions
1	0	4 divisions
1	1	8 divisions

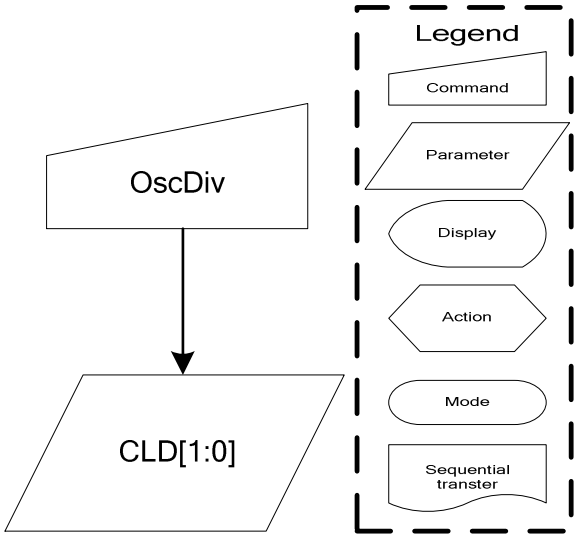
Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (CLD[0:1])
Power On Sequence	00b
S/W Reset	00b
H/W Reset	00b

Flow Chart	

8.1.35. NLInvSet: N-Line control (B5H)

NOTE: "-" Don't care

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NLInvSet	0	1	0	1	0	1	1	0	1	0	1	(B5H)
Parameter	1	1	0	M	-	-	N4	N3	N2	N1	N0	-

Description

This command is used to set the inverted line number with range of 2 to (duty-1) to improve display quality. When M=0, inversion occurs in every frame; when M=1, inversion is independent from frames. If N[4:0]=0, N-line inversion function is disable.

Line inversion numbers=N[4:0] +1.

Example:

If N[4:0]=7, inversion occurs per 8 line.

Restriction

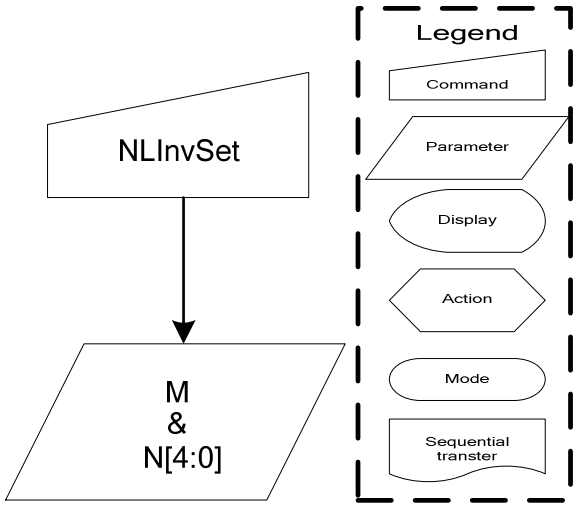
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	M	N[4:0]
Power On Sequence	0b	0000000b
S/W Reset	0b	0000000b
H/W Reset	0b	0000000b

Flow Chart



8.1.36. ComScanDir: Com/Seg Scan Direction for glass layout(B7H)

NOTE: "-" Don't care

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
ComScanDir	0	1	0	1	0	1	1	0	1	1	1	(B7H)
Parameter	1	1	0	0	SMX	0	0	SBGR	0	0	-	-

Description

	Function	0	1
SMX	Inverse the MX setting	Inverse MX	Keep MX
SBGR	Inverse the BGR setting	Keep BGR	Inverse BGR

Restriction

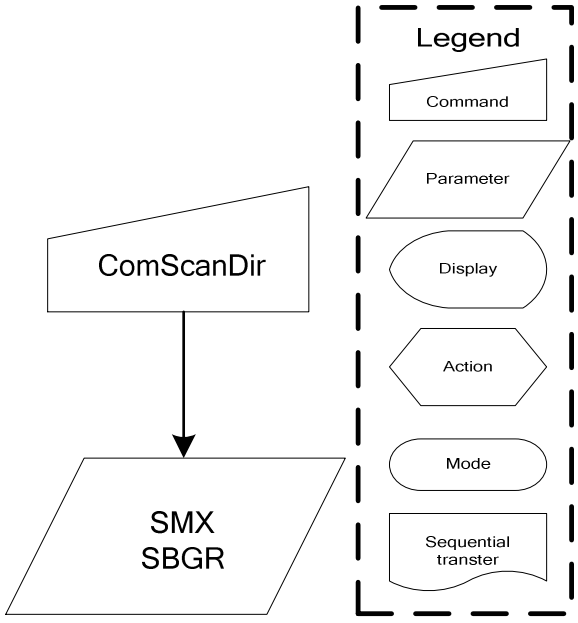
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	48h
S/W Reset	48h
H/W Reset	48h

Flow Chart



8.1.37. RMWIN: Read Modify Write control in (B8H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RMWIN	0	1	0	1	0	1	1	1	0	0	0	(B8H)
Parameter	No Parameter											

Description	Read modify write control IN.
Restriction	
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	--
S/W Reset	--
H/W Reset	--

8.1.38. RMWOUT: Read Modify Write control out(B9H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RMWOUT	0	1	0	1	0	1	1	1	0	0	1	(B9H)
Parameter	No Parameter											

Description	Read modify write control OUT
Restriction	
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	--
S/W Reset	--
H/W Reset	--

8.1.39. DispCompStep1: Display Compensation Step1(BDH)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DispCompStep1	0	1	0	1	0	1	1	1	1	0	1	(BDH)
Parameter	1	1	0	0	0	0	0	0	Step2	Step1	Step0	-

Description

The command is used to program the optimum LCD display quality.

Restriction

Step2	Step1	Step0	STEP
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	100b
S/W Reset	100b
H/W Reset	100b

8.1.40. VopSet: Vop set (C0H)

NOTE: "-" Don't care

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VopSet	0	1	0	1	1	0	0	0	0	0	0	(C0H)
1st parameter	1	1	0	Vop7	Vop6	Vop5	Vop4	Vop3	Vop2	Vop1	Vop0	-
2nd parameter	1	1	0	-	-	-	-	-	-	-	Vop8	

Description

The command is used to program the optimum LCD supply voltage V0.

Restriction

The range of Vop[8:0] is from 96 to 511.

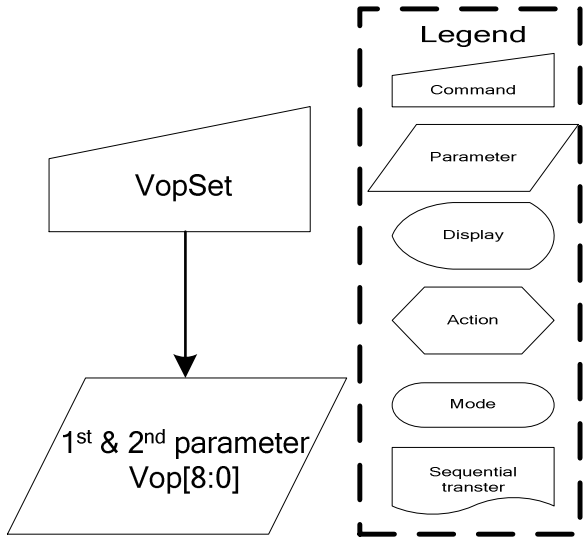
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Vop=16.48V)	
	Vop8	Vop[7:0]
Power On Sequence	1	01000010b (42h)
S/W Reset	1	01000010b (42h)
H/W Reset	1	01000010b (42h)

Flow Chart



8.1.41. VopOfsetInc: Vop Increase 1 (C1H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VopOfsetInc	0	1	0	1	1	0	0	0	0	0	1	(C1H)

Description

With the VopOfsetInc and VopOfsetDec command the V_{LCD} voltage and therewith the contrast of the LCD can be adjusted. This command increases the value of Vop offset register by 1.
If you set the electronic control value to 1111111, the control value is set to 0000000 after this command has been executed.

Restriction

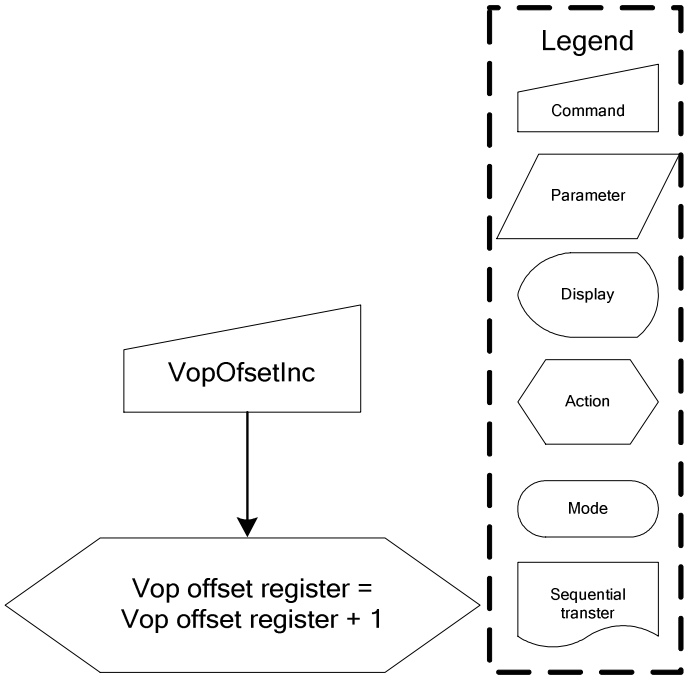
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	--
S/W Reset	--
H/W Reset	--

Flow Chart



8.1.42. VopOfsetDec: Vop Decrease 1 (C2H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VopOfsetDec	0	1	0	1	1	0	0	0	0	1	0	(C2h)

Description

With the VopOfsetInc and VopOfsetDec command the V_{LCD} voltage and therewith the contrast of the LCD can be adjusted. This command decreases the value of Vop offset register by 1.
If you set the electronic control value to 0000000, the control value is set to 1111111 after this command has been executed.

Restriction

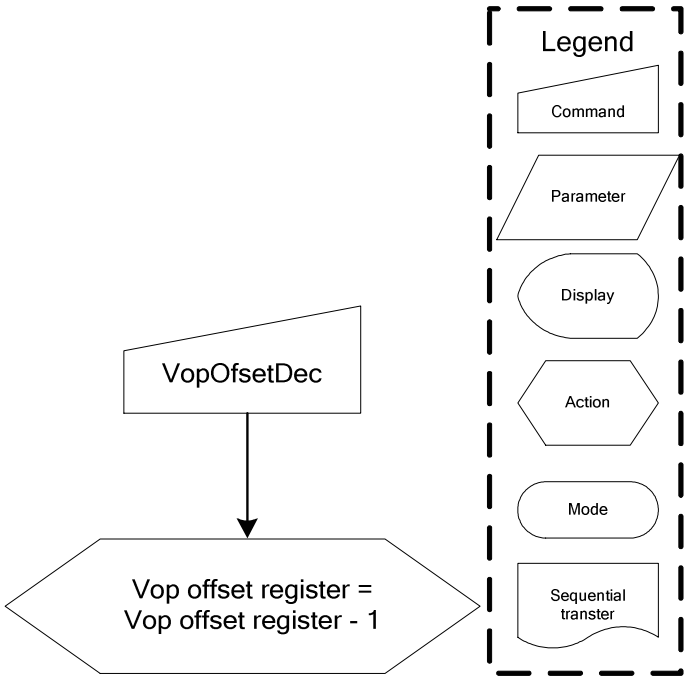
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	--
S/W Reset	--
H/W Reset	--

Flow Chart



8.1.43. BiasSel: Bias Selection(C3H)

NOTE: "-" Don't care

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
BiasSel	0	1	0	1	1	0	0	0	0	1	1	(C3H)
Parameter	1	1	0	-	-	-	-	-	Bias2	Bias1	Bias0	-

Description

Select LCD bias ratio of the voltage required for driving the LCD.

Bias2	Bias1	Bias0	LCD Bias
0	0	0	1/14
0	0	1	1/13
0	1	0	1/12
0	1	1	1/11
1	0	0	1/10
1	0	1	1/9
1	1	0	-
1	1	1	-

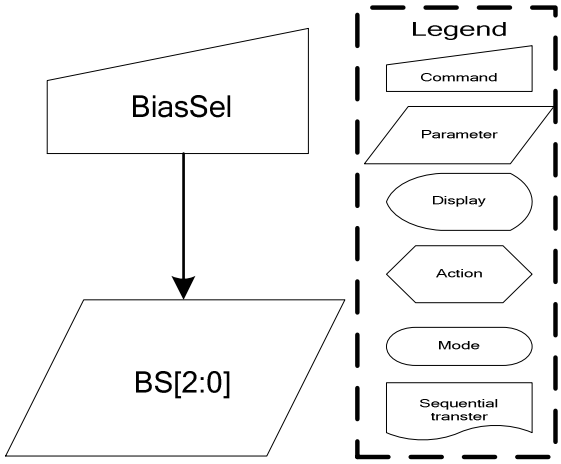
Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Bias[2:0])
Power On Sequence	100b
S/W Reset	100b
H/W Reset	100b

Flow Chart	

8.1.44. BstPmpXSel: Booster Set(C4H)

NOTE: "-" Don't care

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
BstPmpXSel	0	1	0	1	1	0	0	0	1	0	0	(C4H)
Parameter	1	1	0	-	-	-	-	-	BST2	BST1	BST0	-

Description

Booster Setting

BST2	BST1	BST0	
1	0	0	X5 boosting circuit
1	0	1	X6 boosting circuit
1	1	0	X7 boosting circuit
1	1	1	X8 boosting circuit

Restriction

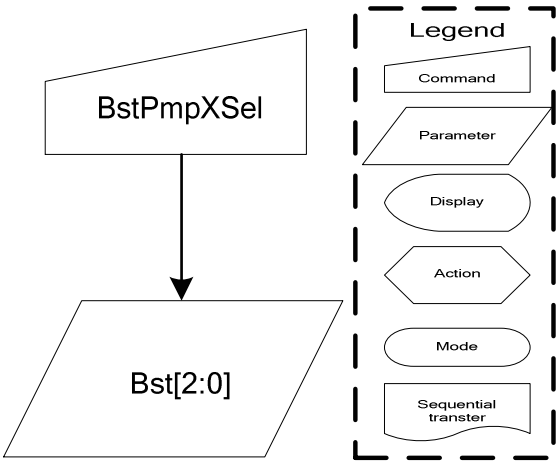
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (BST[2:0])
Power On Sequence	111b
S/W Reset	111b
H/W Reset	111b

Flow Chart



8.1.45. VopOffset: Vop offset fuse bit adjust(C7H)

NOTE: "-" Don't care

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
VopOffset	0	1	0	1	1	0	0	0	1	1	1	(C7h)
Parameter	1	1	0	-	VOS6	VOS5	VOS4	VOS3	VOS2	VOS1	VOS0	-

Description

The command is used to the Vop offset for V0. For VOS[6:0] setting, please see the following table:

VOS6	VOS[5:0]	(Dec)	V0 Offset
0	111111	63	+2520 mV
	111110	62	+2480 mV
	111101	61	+2440 mV
	…	…	…
	000010	2	+80 mV
	000001	1	+40 mV
	000000	0	0 mV
1	111111	-1	-40 mV
	111110	-2	-80 mV
	…	…	…
	000010	-62	-2440 mV
	000001	-63	-2480 mV
	000000	-64	-2520 mV

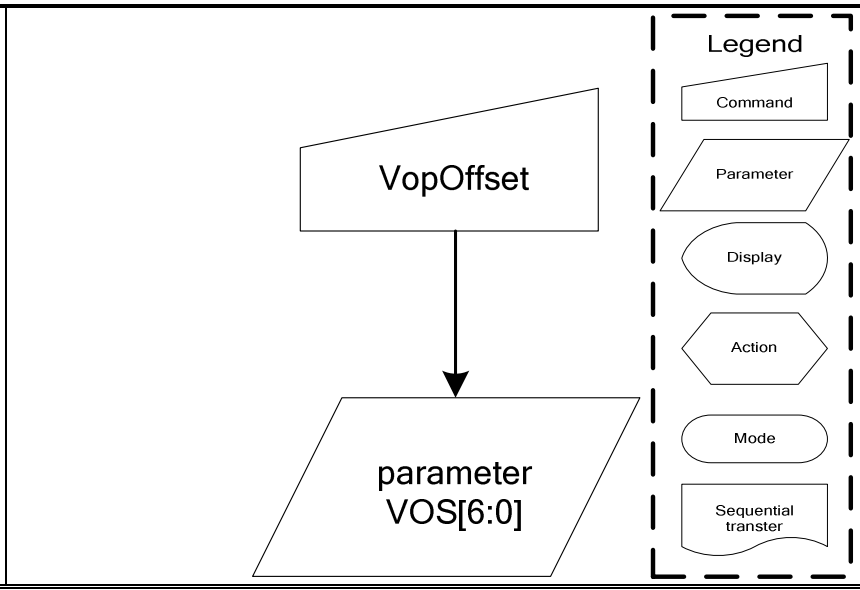
Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	VOS6	VOS[5:0]
Power On Sequence	0	00h
S/W Reset	0	00h
H/W Reset	0	00h

Flow Chart	

8.1.46. V3SorcSel: FV3 with Bst2x control(CBH)

NOTE: "-" Don't care

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
V3SorcSel	0	1	0	1	1	0	0	1	0	1	1	(CBh)
Parameter	1	1	0	-	-	-	-	-	-	-	1	-

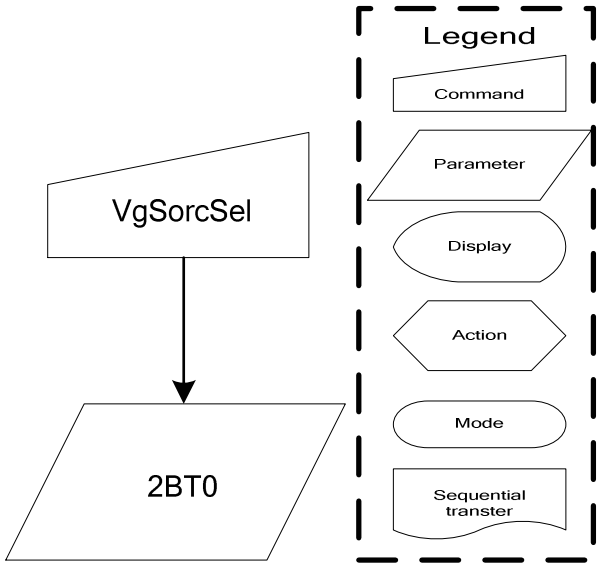
Description	The command is used to set Vg source comes from 2-times charge pump.
Restriction	
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	01h
S/W Reset	01h
H/W Reset	01h

Flow Chart



8.1.47. IDSet : ID setting(CDH)

NOTE: "-" Don't care

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
IDSet	0	1	0	1	1	0	0	1	1	0	1	(CDh)
Parameter	1	1	0	1	-	-	-	ID3	ID2	ID1	ID0	-

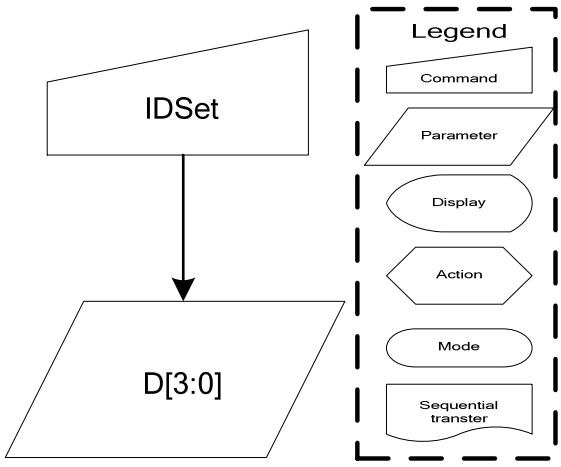
Description	ID setting for PROM program data input
Restriction	
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	-
S/W Reset	-
H/W Reset	-

Flow Chart



8.1.48. ANASET: Analog circuit setting(D0H)

NOTE: "-" Don't care

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
ANASET	0	1	0	1	1	0	1	0	0	0	0	(D0h)
Parameter	1	1	0	0	0	0	1	1	1	0	1	1Dh

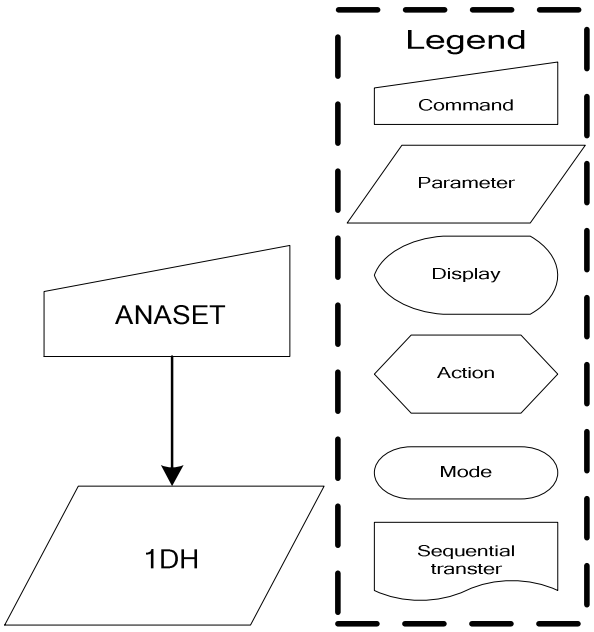
Description	Analog circuit setting.
Restriction	
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	1Dh
S/W Reset	1Dh
H/W Reset	1Dh

Flow Chart



8.1.49. AutoLoadSet : mask rom data auto re-load control(D7H)

NOTE: "-" Don't care

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
AutoLoadSet	0	1	0	1	1	0	1	0	1	1	1	(D7h)
Parameter	1	1	0	1	0	-	ARD	-	-	-	-	-

Description

Mask rom data auto re-load control

ARD: PROM auto read enable control, 1: Disable PROM auto read.

0: Enable PROM auto read.

Restriction

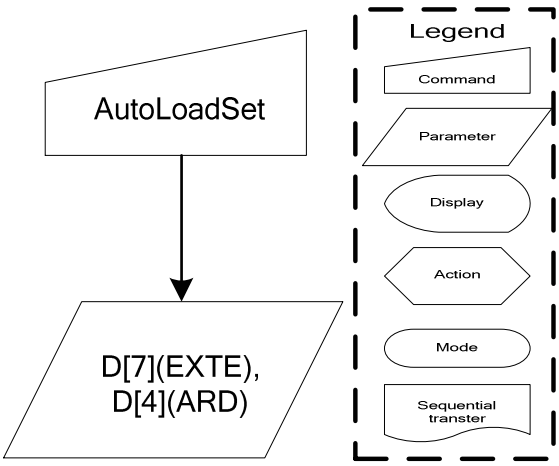
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (ARD)
Power On Sequence	0
S/W Reset	0
H/W Reset	0

Flow Chart



8.1.50. EPCTIN: Control PROM WR/RD(E0H)

NOTE: "-" Don't care

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
EPCTIN	0	1	0	1	1	1	0	0	0	0	0	(E0h)
Parameter	1	1	0	0	0	WR/XRD	0	0	0	0	0	-

Description

WR/XRD: when setting "1" ➔ The Write Enable of PROM will be opened.

WR/XRD: when setting "0" ➔ The Read Enable of PROM will be opened.

Restriction

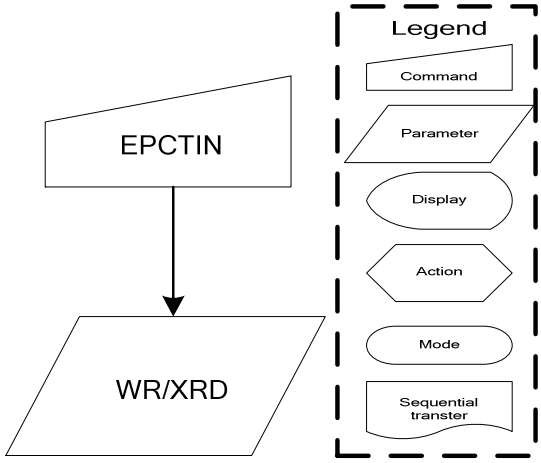
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (WR/XRD)
Power On Sequence	0
S/W Reset	0
H/W Reset	0

Flow Chart



8.1.51. EPCOUT: PROM control cancel(E1H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
EPCOUT	0	1	0	1	1	1	0	0	0	0	1	(E1h)

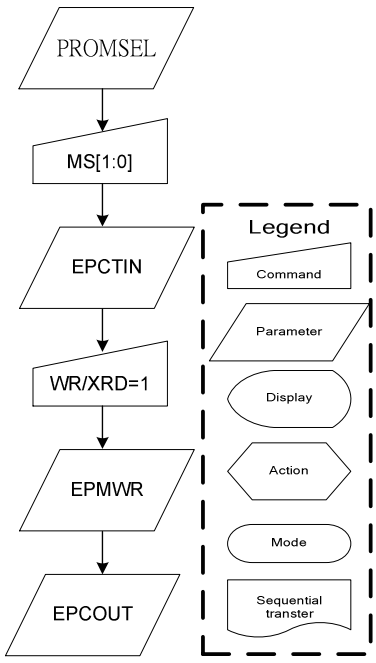
Description	IC exits the PROM control circuit when executing this command.
Restriction	
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	--
S/W Reset	--
H/W Reset	--

Flow Chart



8.1.52. EPMWR: Write to PROM(E2H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
EPMWR	0	1	0	1	1	1	0	0	0	1	0	(E2h)

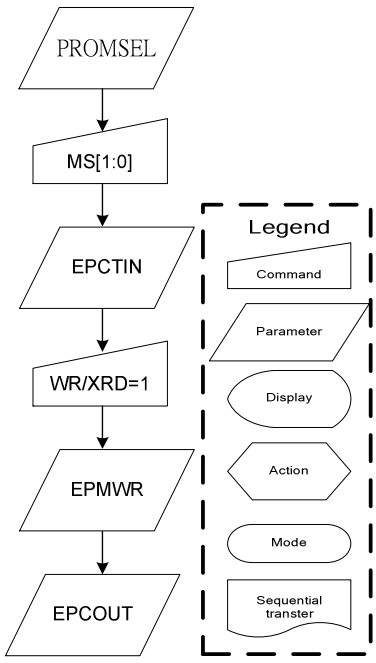
Description	IC actives trigger to start PROM programming when executing this command.
Restriction	
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	--
S/W Reset	--
H/W Reset	--

Flow Chart



8.1.53. EPMRD: Read from PROM(E3H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
EPMRD	0	1	0	1	1	1	0	0	0	1	1	(E3h)

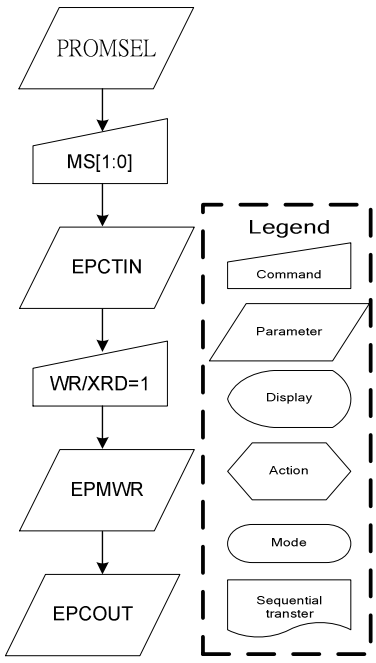
Description	IC actives trigger to start PROM data download to circuit when executing this command.
Restriction	
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	-
S/W Reset	-
H/W Reset	-

Flow Chart



8.1.54. PROMSEL: Select PROM(E4H)

NOTE: "-" Don't care

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PROMSEL	0	1	0	1	1	1	0	0	1	0	0	(E4h)
Parameter	1	1	0	MS1	MS0	0	1	1	0	0	1	-

Description

This command defines PROM selection control. Please see the table as below:

MS1	MS0	Mode
0	0	Disable
0	1	PROM

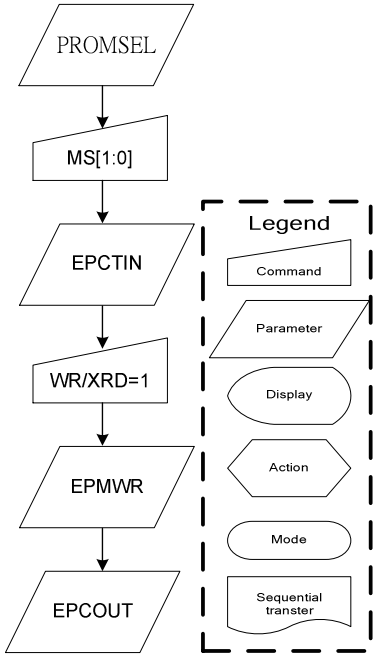
Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (MS[1:0])
Power On Sequence	00b
S/W Reset	00b
H/W Reset	00b

Flow Chart	

8.1.55. ROMSET: Programmable ROM setting(E5H)

NOTE: "-" Don't care

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
ROMSET	0	1	0	1	1	1	0	0	1	0	1	(E5h)
Parameter	1	1	0	0	0	0	D4	D3	D2	D1	D0	-

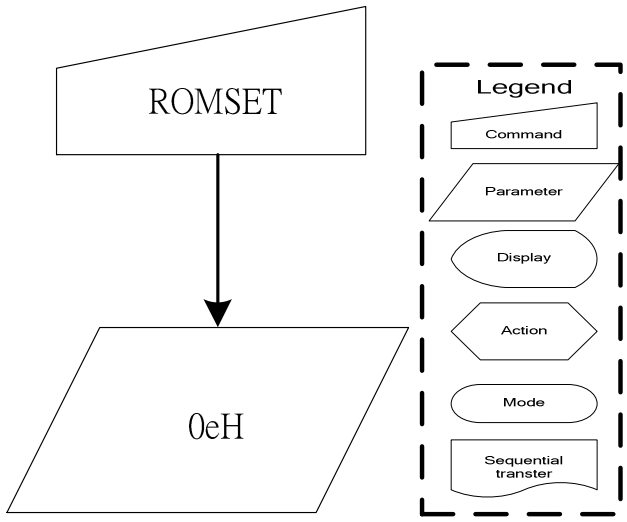
Description	Programmable ROM setting.
Restriction	
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value D[4:0]
Power On Sequence	01111b
S/W Reset	01111b
H/W Reset	01111b

Flow Chart



8.1.56. DispCompStep2: Display Compensation Step2(ECH)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DispCompStep2	0	1	0	1	1	1	0	1	1	0	0	(ECh)
Parameter	1	1	0	0	0	0	0	Step3	Step2	Step1	Step0	-

Description

The command is used to program the optimum LCD display quality.

Restriction

Step3	Step2	Step1	Step0	STEP
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8
1	0	0	0	9
1	0	0	1	10
1	0	1	0	11
1	0	1	1	12
1	1	0	0	13
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	08h
S/W Reset	08h
H/W Reset	08h

8.1.57. FRMSEL: Frame Freq. in Temp. range (F0H)

NOTE: "-" Don't care

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
FRMSEL	0	1	0	1	1	1	1	0	0	0	0	(F0H)
1st parameter	1	1	0	-	-	-	DIVA	FA3	FA2	FA1	FA0	Range A
2nd parameter	1	1	0	-	-	-	DIVB	FB3	FB2	FB1	FB0	Range B
3rd parameter	1	1	0	-	-	-	DIVC	FC3	FC2	FC1	FC0	Range C
4th parameter	1	1	0	-	-	-	DIVD	FD3	FD2	FD1	FD0	Range D

Description

Select Frame Freq. in normal display mode.

1st parameter : Frame freq. value set in temperature range 30(-40℃) to TA

2nd parameter : Frame freq. value set in temperature range TA to TB

3rd parameter : Frame freq. value set in temperature range TB to TC

4th parameter : Frame freq. value set in temperature range TC to 145(87℃)

For command setting to frame rate value look-up-table, please see the following table:

DIVx	Fx[3:0]	Frame Rate(Hz)	DIVx	Fx[3:0]	Frame Rate(Hz)
1	0	77	0	0	38.5
	1	77		1	38.5
	2	77		2	38.5
	3	80		3	40.0
	4	83		4	41.5
	5	92		5	46.0
	6	92		6	46.0
	7	98		7	49.0
	8	102		8	51.0
	9	106		9	53.0
	A	110		A	55.0
	B	110		B	55.0
	C	138		C	69.0
	D	146		D	73.0
	E	153		E	76.5
	F	153		F	76.5

Restriction

If LED is driven by PWM method and PWM frequency is slow, the unexpected phenomenon may occur.

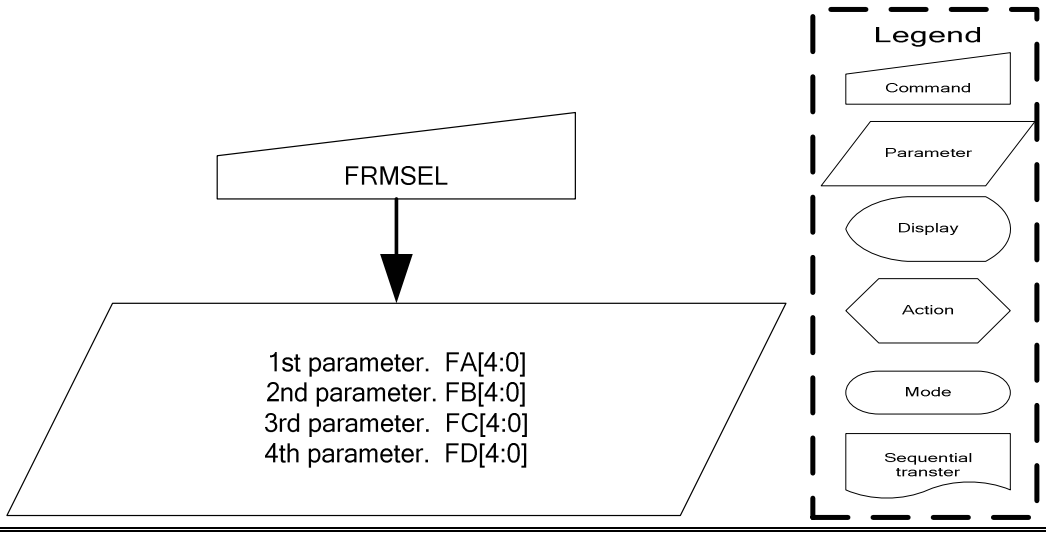
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value			
	FA[4:0]	FB[4:0]	FC[4:0]	FD[4:0]
Power On Sequence	06H	0BH	0DH	12H
S/W Reset	06H	0BH	0DH	12H
H/W Reset	06H	0BH	0DH	12H

Flow Chart



8.1.58. FRM8SEL: Frame Freq. in Temp. range (idel-8 color) (F1H)

NOTE: "-" Don't care

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
FRM8SEL	0	1	0	1	1	1	1	0	0	0	1	(F1H)
1st parameter	1	1	0	-	-	-	F8A4	F8A3	F8A2	F8A1	F8A0	Range A
2nd parameter	1	1	0	-	-	-	F8B4	F8B3	F8B2	F8B1	F8B0	Range B
3rd parameter	1	1	0	-	-	-	F8C4	F8C3	F8C2	F8C1	F8C0	Range C
4th parameter	1	1	0	-	-	-	F8D4	F8D3	F8D2	F8D1	F8D0	Range D

Description

Select Frame Freq. in normal display mode.(idle;8 color mode)

1st parameter : Frame freq. value set in TEMP range 30(-40℃) to TA

2nd parameter : Frame freq. value set in TEMP range TA to TB

3rd parameter : Frame freq. value set in TEMP range TB to TC

4th parameter : Frame freq. value set in TEMP range TC to 145(87℃)

Restriction

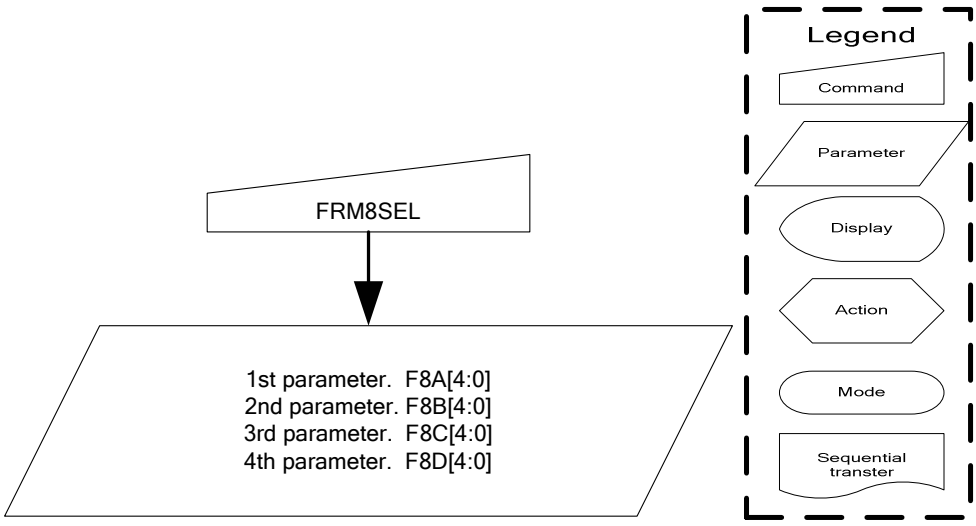
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value			
	FA[4:0]	FB[4:0]	FC[4:0]	FD[4:0]
Power On Sequence	06H	0BH	0DH	12H
S/W Reset	06H	0BH	0DH	12H
H/W Reset	06H	0BH	0DH	12H

Flow Chart



8.1.59. TMPRNG: Temp. range set for Frame Freq. Adj. (F2H)

NOTE: "-" Don't care

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TMPRNG	0	1	0	1	1	1	1	0	0	1	0	(F2H)
1st parameter	1	1	0	-	TA6	TA5	TA4	TA3	TA2	TA1	TA0	Range A
2nd parameter	1	1	0	-	TB6	TB5	TB4	TB3	TB2	TB1	TB0	Range B
3rd parameter	1	1	0	-	TC6	TC5	TC4	TC3	TC2	TC1	TC0	Range C

Description

Temperature range set for automatic frame freq. adj. operation according the current temperature value.

1st parameter: Temperature range A value set

2nd parameter: Temperature range B value set

3rd parameter: Temperature range C value set

TA/TB/TC Temperature(℃) + 40 = TA/TB/TC[6:0]

Example:

If TA wants to be set at 24℃, TA[6:0]=24+40=64(40h),

Restriction

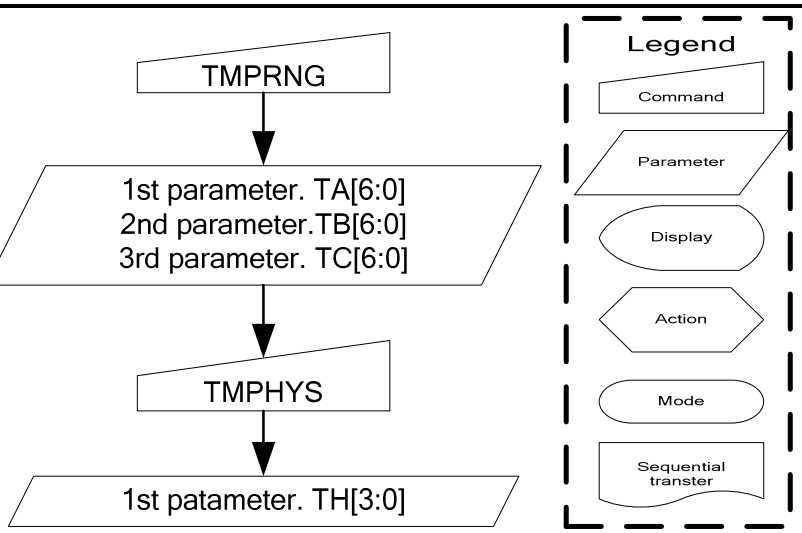
-40℃≦TA≦TA+TH≦TB≦TB+TH≦TC≦87℃

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	TA[6:0]	TB[6:0]	TC[6:0]
Power On Sequence	1Eh	28h	32h
S/W Reset	1Eh	28h	32h
H/W Reset	1Eh	28h	32h

Flow Chart	

8.1.60. TMPHYS: Temperature Hysteresis Set for Frame Freq. Adj.(F3H)

NOTE: "-" Don't care

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TMPHYS	0	1	0	1	1	1	1	0	0	1	1	(F3H)
Parameter	1	1	0	-	-	-	-	TH3	TH2	TH1	TH0	-

Description

Temperature hysteresis range set for frame freq. adj.

Parameter TH[3:0] is used to set Temperature hysteresis range.

The relationship between temperature state and temperature range value is shown below.

TEMP Range Value	TEMP Rising State	TEMP Falling State
Freq. changing point A	TA[6:0]+TH[3:0]	TA[6:0]
Freq. changing point B	TB[6:0]+TH[3:0]	TB[6:0]
Freq. changing point C	TC[6:0]+TH[3:0]	TC[6:0]

TH Temperature(℃) - 1 = TH[3:0]

Example:

If TH wants to set 5℃, TH[3:0]=5-1=4.

Restriction

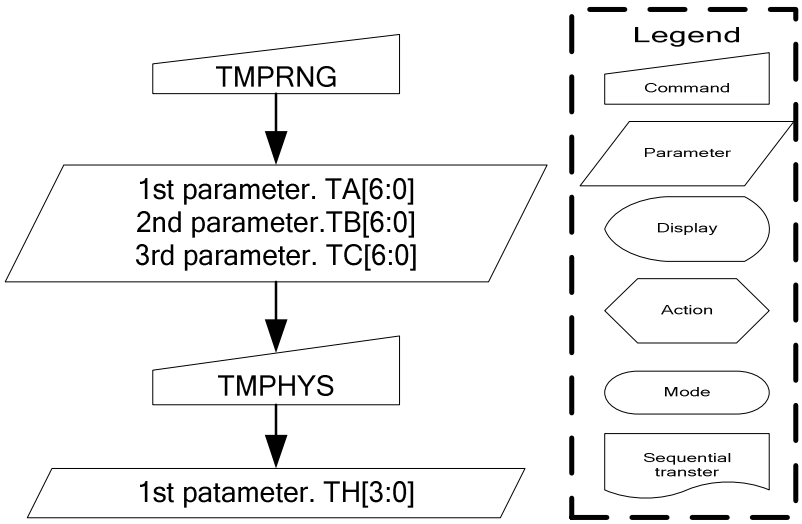
Temperature hysteresis value should be smaller than the gap of temperature range.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value(TH[3:0])
Power On Sequence	0100b
S/W Reset	0100b
H/W Reset	0100b

Flow Chart	

8.1.61. TEMPSEL: Temp. Set(F4H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TEMPSEL	0	1	0	1	1	1	1	0	1	0	0	(F4h)
1st parameter	1	1	0	MT13	MT12	MT11	MT10	MT03	MT02	MT01	MT00	MT1x : (-24 °C to -32 °C) MT0x : (-32 °C to -40 °C)
2nd parameter	1	1	0	MT33	MT32	MT31	MT30	MT23	MT22	MT21	MT20	MT3x : (-8 °C to -16 °C) MT2x : (-16 °C to -24 °C)
3rd parameter	1	1	0	MT53	MT52	MT51	MT50	MT43	MT42	MT41	MT40	MT5x : (8 °C to 0 °C) MT4x : (0 °C to -8 °C)
4th parameter	1	1	0	MT73	MT72	MT71	MT70	MT63	MT62	MT61	MT60	MT7x : (24 °C to16 °C) MT6x : (16 °C to 8 °C)
5th parameter	1	1	0	MT93	MT92	MT91	MT90	MT83	MT82	MT81	MT80	MT9x : (40 °C to 32 °C) MT8x : (32 °C to 24 °C)
6th parameter	1	1	0	MTB3	MTB2	MTB1	MTB0	MTA3	MTA2	MTA1	MTA0	MTBx : (56 °C to 48 °C) MTAx : (48 °C to 40 °C)
7th parameter	1	1	0	MTD3	MTD2	MTD1	MTD0	MTC3	MTC2	MTC1	MTC0	MTDx : (72 °C to 64 °C) MTCx : (64 °C to 56 °C)
8th parameter	1	1	0	MTF3	MTF2	MTF1	MTF0	MTE3	MTE2	MTE1	MTE0	MTFx : (87 °C to 80 °C) MTEx : (80 °C to 72 °C)

Description

This command defines temperature gradient compensation coefficient. For this command detail description and operation, please see Section 7.9.

Parameter n	MT n 3	MT n 2	MT n 1	MT n 0	Voltage / °C (Tolerance: ±3mV/ °C)
0	0	0	0	0	5 mv / °C
1	0	0	0	1	0 mv / °C
2	0	0	1	0	-5 mv / °C
3	0	0	1	1	-10 mv / °C
:	:	:	:	:	:
:	:	:	:	:	:
:	:	:	:	:	:
12	1	1	0	0	-55 mv / °C
13	1	1	0	1	-60 mv / °C
14	1	1	1	0	-65 mv / °C
15	1	1	1	1	-70 mv / °C

Restriction

Please refer to the specification in absolute maximum ratings for operating voltage range.

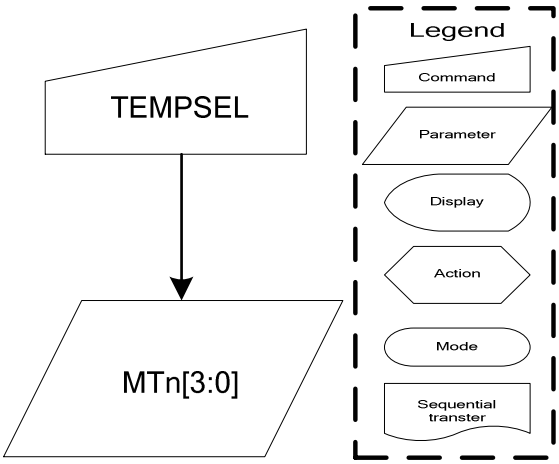
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (MTn[3:0])
Power On Sequence	--
S/W Reset	--
H/W Reset	--

Flow Chart



NOTE:

The default value of temperature gradient compensation coefficient Set

1st parameter	7FH
2nd parameter	22H
3rd parameter	11H
4th parameter	02H
5th parameter	00H
6th parameter	32H
7th parameter	82H
8th parameter	B6H

8.1.62. THYS : Temperature detection threshold(F7H)

NOTE: "-" Don't care

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
THYS	0	1	0	1	1	1	1	0	1	1	1	(F7h)
Parameter	1	1	0	-	-	THYS5	THYS4	THYS3	THYS2	THYS1	THYS0	-

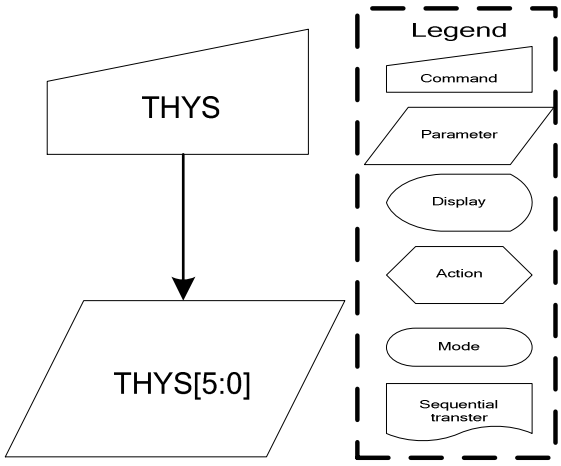
Description	Temperature detection threshold setting.
Restriction	
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (THYS[5:0])
Power On Sequence	00100b
S/W Reset	00100b
H/W Reset	00100b

Flow Chart



8.1.63. Frame Set: Frame PWM Set (F9H)

NOTE: "-" Don't care

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Frame1 Set	0	1	0	1	1	1	1	1	0	0	1	(F9h)
1st parameter	1	1	0	-	-	-	P14	P13	P12	P11	P10	-
2nd parameter	1	1	0	-	-	-	P24	P23	P22	P21	P20	-
:	:	:	:	:	:	:	:	:	:	:	:	-
15th parameter	1	1	0	-	-	-	P154	P153	P152	P151	P150	-
16th parameter	1	1	0	-	-	-	P164	P163	P162	P161	P160	-

Description

This command is used to set frame PWM.

Restriction

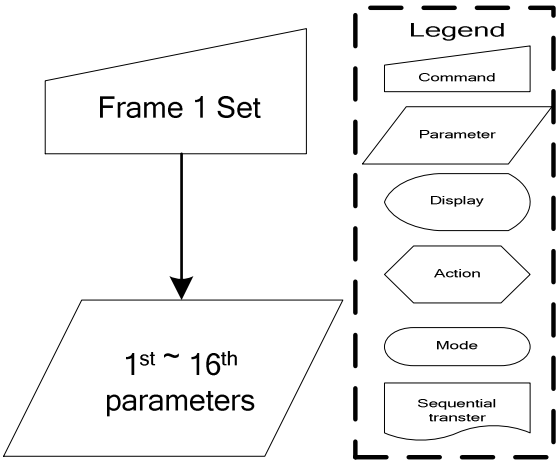
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	--
S/W Reset	--
H/W Reset	--

Flow Chart



NOTE:

The default value of RGB level set

1st parameter	00H
2nd parameter	01H
3rd parameter	02H
4th parameter	04H
5th parameter	06H
6th parameter	07H
7th parameter	09H
8th parameter	0AH
9th parameter	0BH
10th parameter	0CH
11th parameter	0DH
12th parameter	0FH
13th parameter	11H
14th parameter	12H
15th parameter	17H
16th parameter	1AH

All the modulation range of each level for each frame is from 00H to 1FH.

9. SPECIFICATIONS

9.1. Absolute Maximum Ratings

(VSS = 0V)

Item	Symbol	Value	Unit
Supply voltage 1	V_{DD}	- 0.3 ~ + 3.6	V
Supply voltage 2	V_{DD1},V_{DD2},V_{DD3},V_{DD4},V_{DD5}	- 0.3 ~ + 3.6	V
Supply voltage 3	V_{MAX} (V0- XV0)	- 0.3 ~ + 18.0	V
Input voltage range	V_{IN}	- 0.3 ~ V_{DD} + 0.3	V
Operating temperature range	T_{OPR}	- 30 ~ + 85	℃
Storage temperature range	T_{STG}	- 40 ~ + 125	℃

NOTE:

(1). Voltages are all based on VSS = 0V.

(2). Voltage relationship: V0 ≥ Vg ≥ Vm ≥ VSS ≥ XV0 must always be satisfied.

10. DC CHARACTERISTICS

10.1. Basic Characteristics

(VSS=0V, Ta = -30 to 85℃)

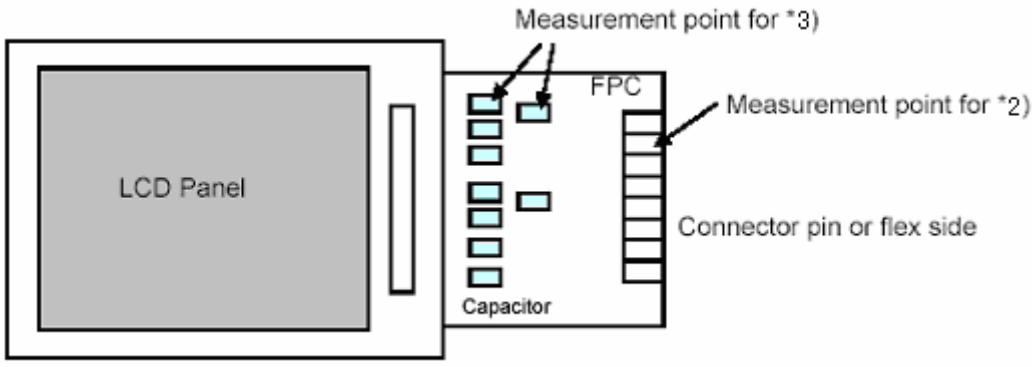
Parameter	Symbol	Conditions	Related Pins	MIN	TYP	MAX	Unit
Logic Operating voltage	VDDI	-	*2) VDD	1.65	1.8	3.3	V
Analog Operating voltage	VDDA	-	*2) VDD1,2,3,4,5	2.4	2.8	3.3	
Driving voltage input	VLCD	V0 – XV0	*3) *4) V0, XV0	-	-	18	
High level input voltage	VIH		*1) *2)	0.7VDD	-	VDD	
Low level input voltage	VIL	-	*1) *2)	VSS	-	0.3VDD	
High level output voltage	VOH	IOH = -1.0mA	*2) SI, TE	0.8VDD	-	VDD	
Low level output voltage	VOL	IOL = +1.0mA		VSS	-	0.2VDD	
Input leakage current	IIL	VIN = VDD or VSS	*1), *2)	-1.0	-	+1.0	μA
Driver on resistance (SEG)	RONSEG	Vg = 3.2V, Ta = 25℃, △V=10%	S0 to S393	-	-	1.0	KΩ
Driver on resistance (COM)	RONCOM	V0 = 16.0V, Ta = 25℃ △V=10%	C0 to C159	-	-	1.0	
Frame rate	FR	Ta = 25℃, N-line=0x8C, Duty=160, FR=0x12	-	-	77	-	Hz

NOTE:

**1) Applies to IF0, IF1, /CS, /RST, /WR, /RD, A0 (SCL) and D15-D2, D1 (A0), D0 (SI) pins*

**2) *3)When the measurements are performed with LCD module, Measurement Points are like below.*

**4) ST7689 does not support external power*



10.2. Current Consumption

Operation mode	Condition	Current consumption	
		Typical	Maximum
		IDD(mA)	IDD(mA)
- Normal Mode	1. 1/2 gray pattern 2. Vddi=1.8V, Vdda=2.8V 3. Vop=16.48V, bias=1/10, N=0x8C, FR=77Hz, x8 booster, Ta=25℃	0.6	0.9
- Sleep In Mode	Vddi=1.8V, Vdda=2.8V, Ta=25℃	0.015	0.025

Note: Bare die

Note:The Current Consumption is DC characteristics.

11. TIMING CHARACTERISTICS

11.1. Parallel Interface Characteristics bus (8080-series MCU)

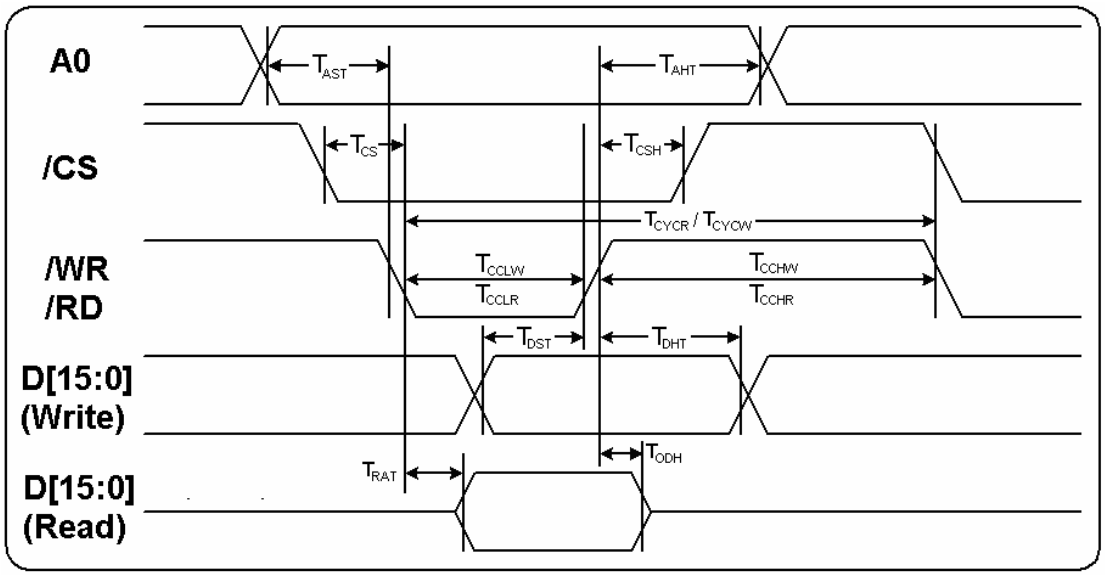


Figure 14 Parallel Interface Characteristics bus (8080-series MCU)

(V_{SS}=0V, V_{DDI}=1.65~3.3V, VDDA=2.4~3.3V, Ta = 25℃)

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Address hold time	A0	T_{AHT}		0	—	ns
Address setup time		T_{AST}		0	—	
Chip select setup time	/CS	T_{CS}		0	—	
Chip select hold time		T_{CSH}		10	—	
System cycle time (WRITE)	WR	T_{CYCW}		160	—	
/WR L pulse width (WRITE)		T_{CCLW}		70	—	
/WR H pulse width (WRITE)		T_{CCHW}		70	—	
System cycle time (READ)	RD (ID)	T_{CYCR}	When read ID data	260	—	
/RD L pulse width (READ)		T_{CCLR}		150	—	
/RD H pulse width (READ)		T_{CCHR}		100	—	
System cycle time (READ)	RD (FM)	T_{CYCR}	When read from frame memory	400	—	
/RD L pulse width (READ)		T_{CCLR}		180	—	
/RD H pulse width (READ)		T_{CCHR}		180	—	
WRITE data setup time	D0 to D15	T_{DS}		15	—	
WRITE data hold time		T_{DH}		15	—	
READ access time		T_{RAT}	CL = 30 pF	—	80	
READ Output disable time		T_{ODH}	CL = 30 pF	10	90	

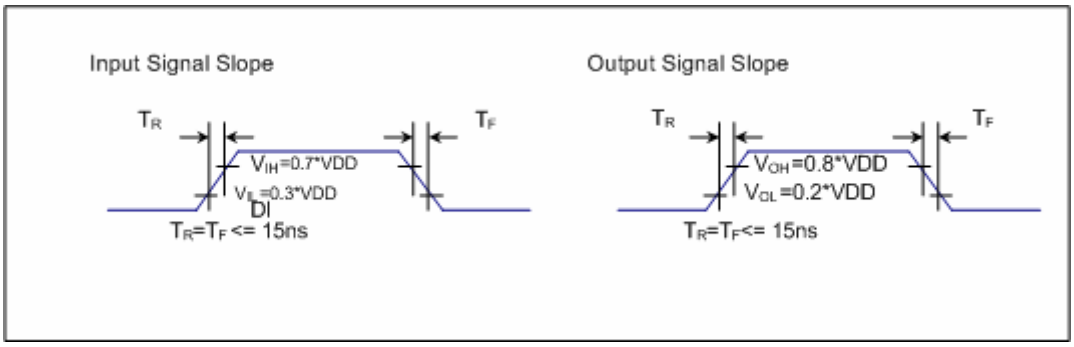


Figure 15 Rising and Falling timing for Input and Output signal

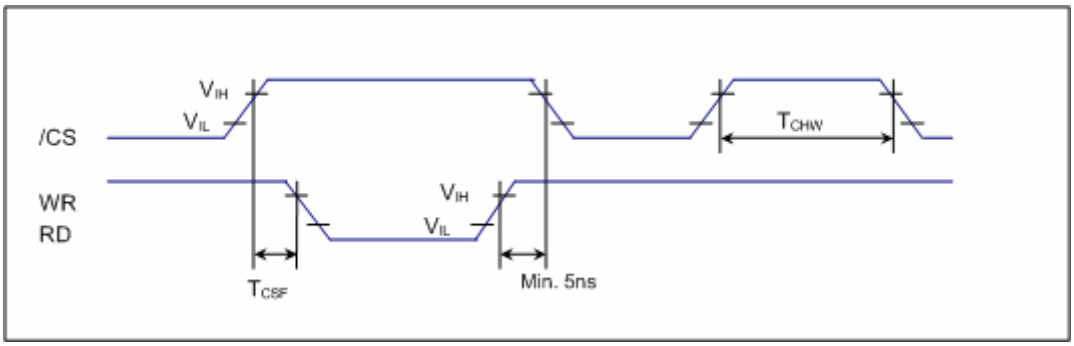


Figure 16 Chip selection (/CS) timing

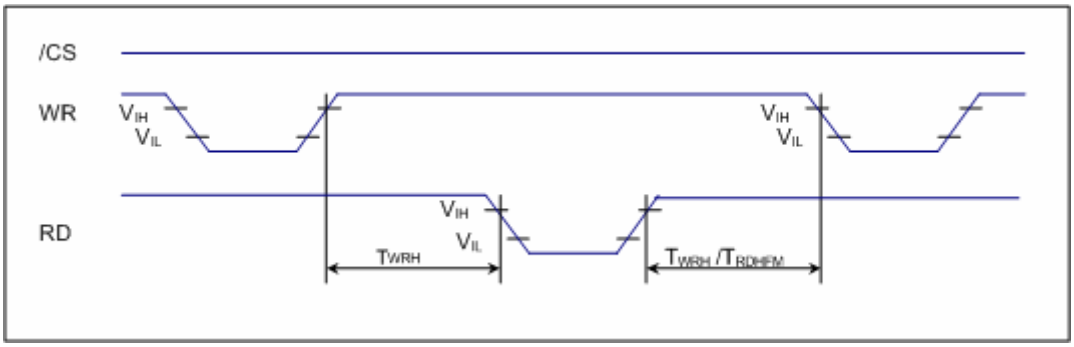


Figure 17 Write to read and Read to write timing

NOTE: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Logic high and low levels are specified as 30% and 70% of VDD for Input signals.

11.2. Parallel Interface Characteristics bus (6800-series MCU)

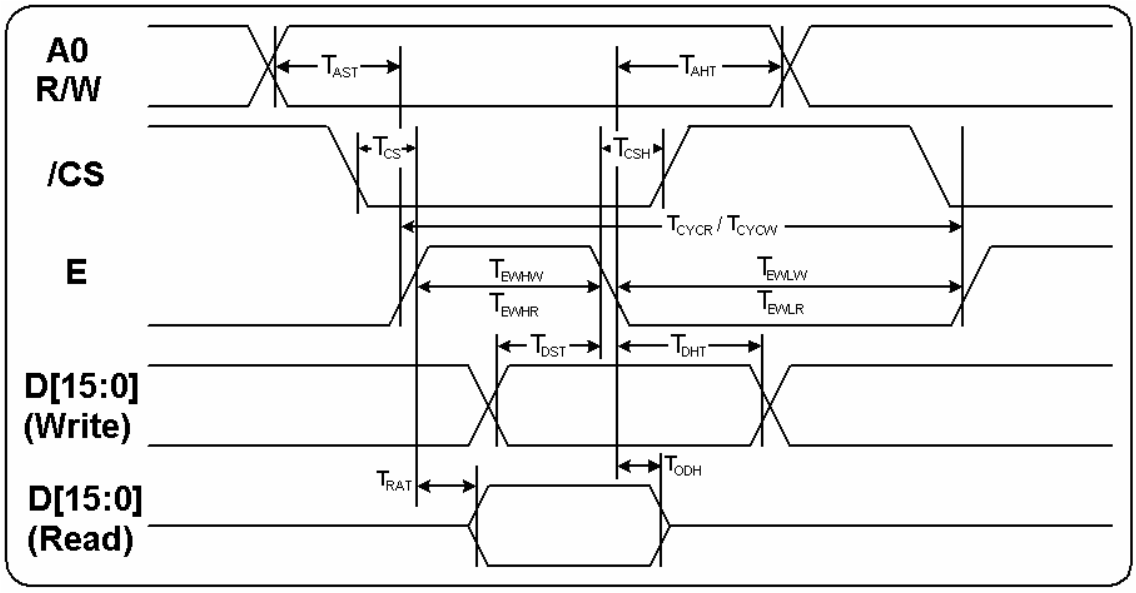


Figure 18 Parallel Interface characteristics (6800-Series MCU)

(V_{SS}=0V, V_{DDI}=1.65~3.3V, VDDA=2.4~3.3V, Ta = 25℃)

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Address hold time	A0	T_{AHT}		0	—	ns
Address setup time		T_{AST}		0	—	
R/W hold time	R/W	T_{AHT}		10	—	
R/W setup time		T_{AST}		10	—	
Chip select setup time	/CS	T_{CS}		0	—	
Chip select hold time		T_{CSH}		10	—	
System cycle time (WRITE)	E	T_{CYCW}		160	—	
Low pulse width (WRITE)		T_{EWLW}		70	—	
High pulse width (WRITE)		T_{EWHW}		70	—	
System cycle time (READ)	E (ID)	T_{CYCR}	When read ID data	260	—	
Low pulse width (READ)		T_{EWLR}		100	—	
High pulse width (READ)		T_{EWHR}		150	—	
System cycle time (READ)	E (FM)	T_{CYCR}	When read from frame memory	400	—	
Low pulse width (READ)		T_{CCLR}		180	—	
High pulse width (READ)		T_{CCHR}		180	—	
WRITE data setup time	D0 to D15	T_{DS}		15	—	
WRITE data hold time		T_{DH}		15	—	
READ access time		T_{RAT}	CL = 30 pF	—	80	
READ Output disable time		T_{ODH}	CL = 30 pF	10	90	

11.3. Serial Interface Characteristics (3-pin Serial)

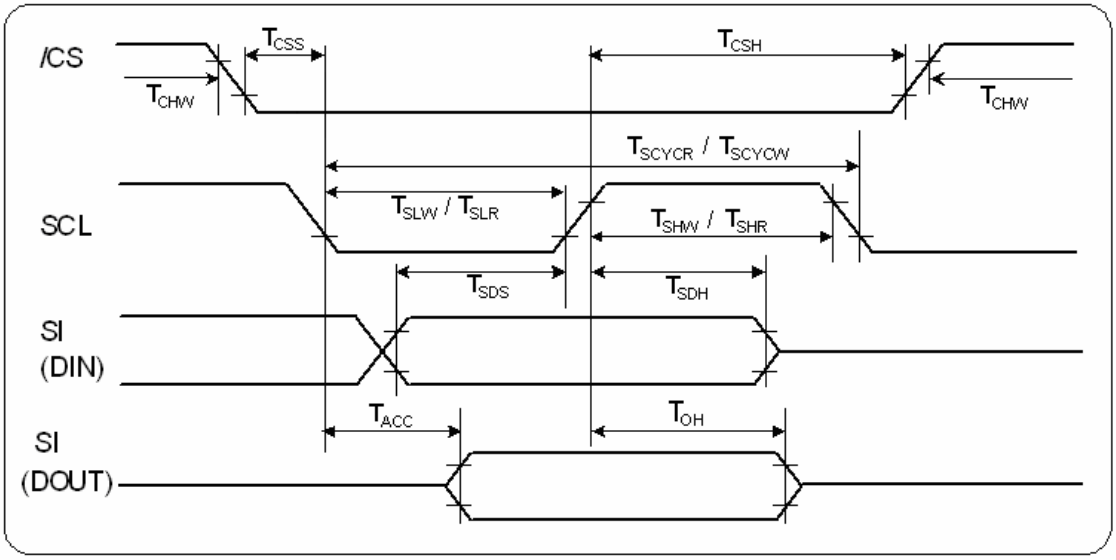


Figure 19 3-pin Serial Interface Characteristics

(V_{SS}=0V, V_{DDI}=1.65~3.3V, VDDA=2.4~3.3V, Ta = 25℃)

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Serial clock period (write)	SCL	T_{SCYCW}		130	—	ns
SCL “H” pulse width (write)		T_{SHW}		90	—	
SCL “L” pulse width (write)		T_{SLW}		40	—	
Serial clock period (read)		T_{SCYCR}		240	—	
SCL “H” pulse width (read)		T_{SHR}		100	—	
SCL “L” pulse width (read)		T_{SLR}		120	—	
Data setup time	SI	T_{SDS}		15	—	
Data hold time		T_{SDH}		15	—	
Access time		T_{ACC}	CL = 30 pF	5	100	
Output disable time		T_{OH}	CL = 30 pF	10	90	
Chip select setup time	/CS	T_{CSS}		20	—	
Chip select hold time		T_{CSH}		20	—	
Chip select “H” pulse width		T_{CHW}		0	—	

11.4. Serial Interface Characteristics (4-pin Serial)

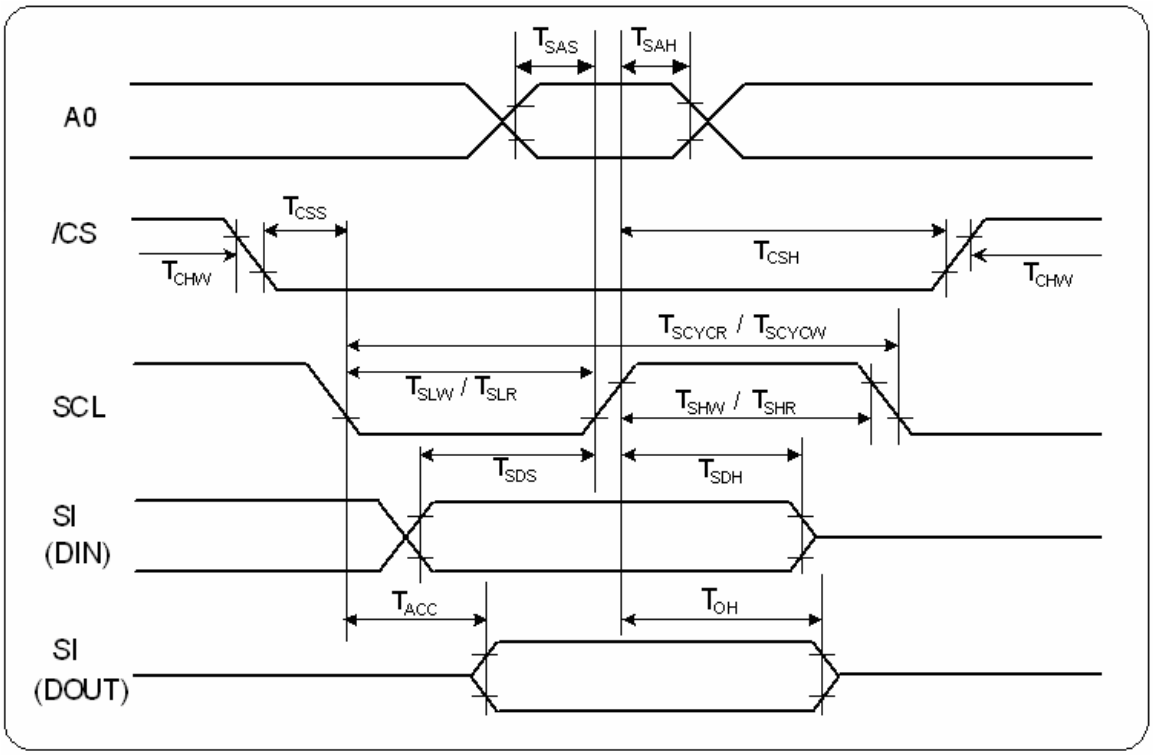


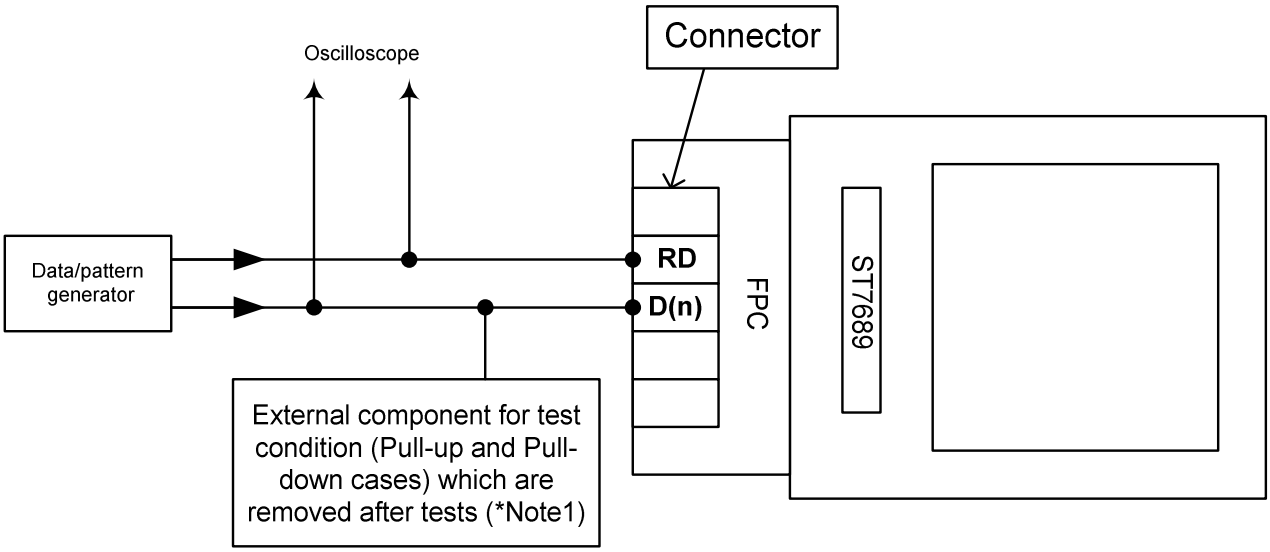
Figure 20 4-pin Serial Interface Characteristics

(V_{SS}=0V, V_{DDI}=1.65~3.3V, VDDA=2.4~3.3V, Ta = 25℃)

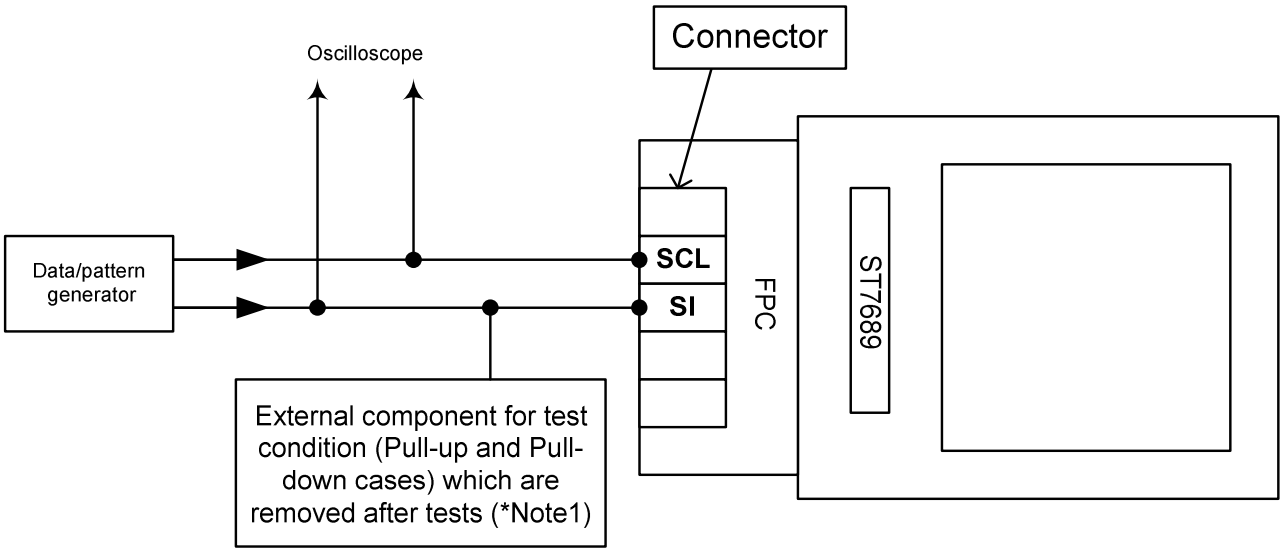
Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Serial clock period (write)	SCL	T_{SCYCW}		130	—	ns
SCL “H” pulse width (write)		T_{SHW}		90	—	
SCL “L” pulse width (write)		T_{SLW}		40	—	
Serial clock period (read)		T_{SCYCR}		240	—	
SCL “H” pulse width (read)		T_{SHR}		100	—	
SCL “L” pulse width (read)		T_{SLR}		120	—	
Address setup time	A0	T_{SAS}		15	—	
Address hold time		T_{SAH}		15	—	
Data setup time	SI	T_{SDS}		15	—	
Data hold time		T_{SDH}		15	—	
Data access time		T_{ACC}	CL = 30 pF	5	100	
Output disable time		T_{OH}	CL = 30 pF	10	90	
Chip select setup time	/CS	T_{CSS}		20	—	
Chip select hold time		T_{CSH}		20	—	
Chip select “H” pulse width		T_{CHW}		0	—	

11.5. Output Access/Disable Timing Measurement Method

◆ Parallel interface (8080-series)



◆ Serial interface (3-line)



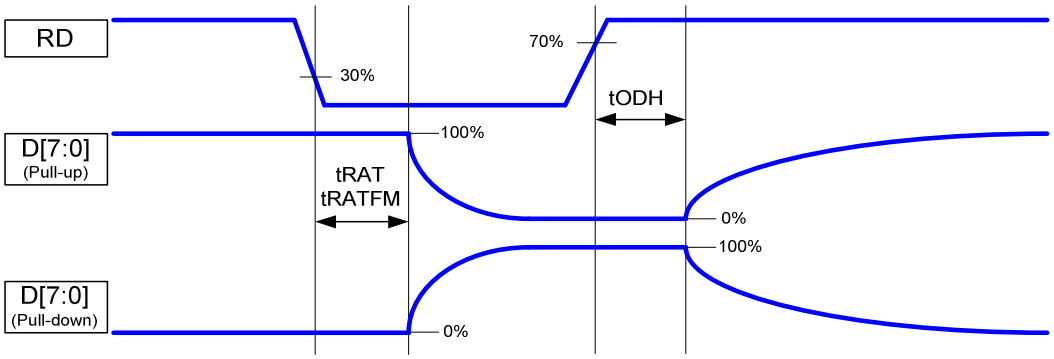
Note:

1. Pull-up/pull-down resistor: ***3KΩ ± 5% ;*** *pull-up/pull-down capacitor:* ***8 or 30 pF ± 10%***

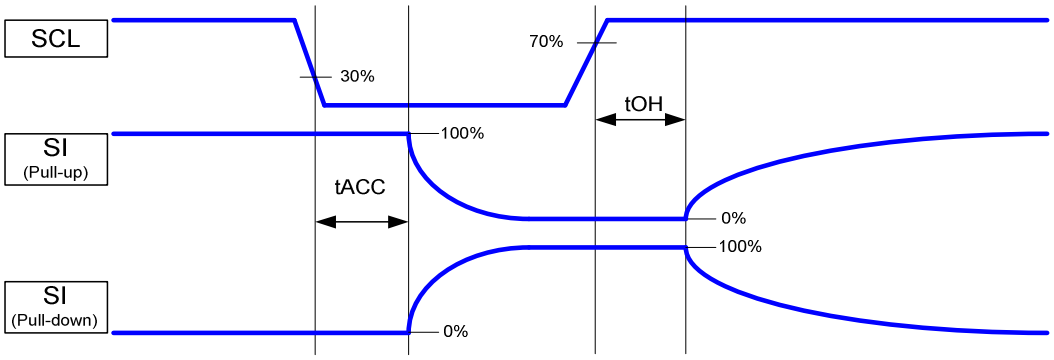
2. Capacitances and resistances of the oscilloscope's probe must be included externals components in these measurements.

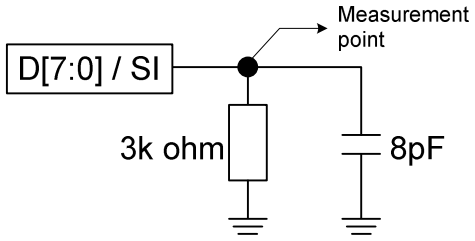
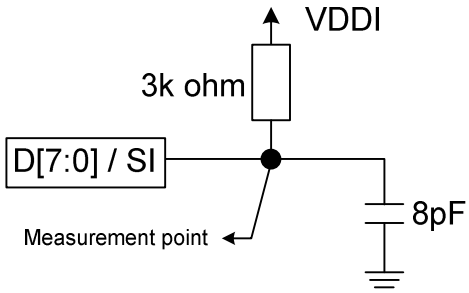
11.6. Minimum Value Measurement

◆ Parallel interface (8080-series)



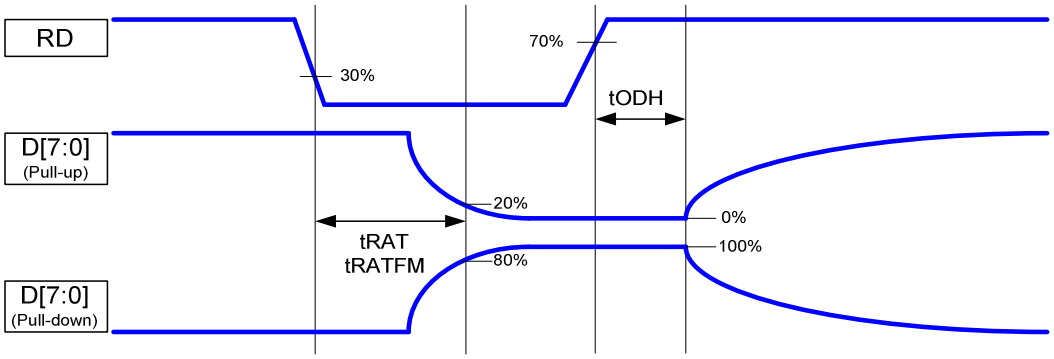
◆ Serial interface (3-line)



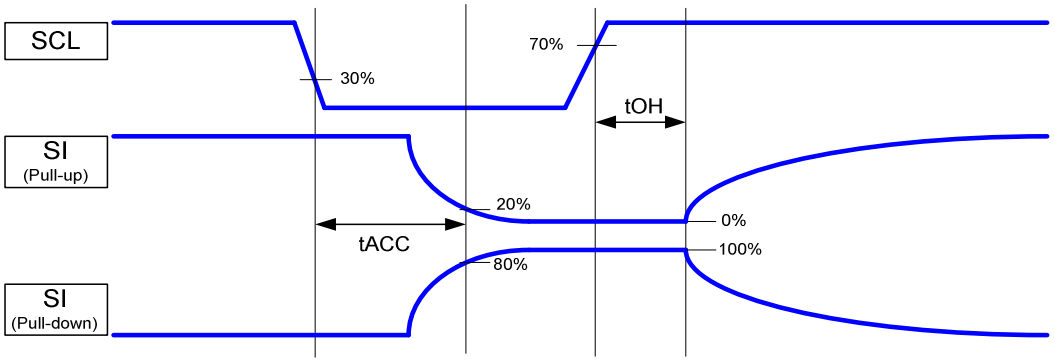
Measurement circuit pull down	Measurement circuit pull up
	

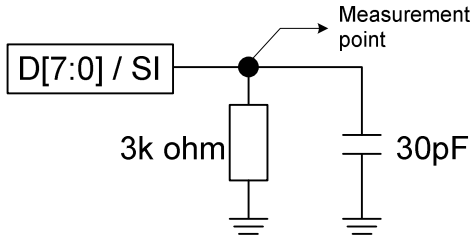
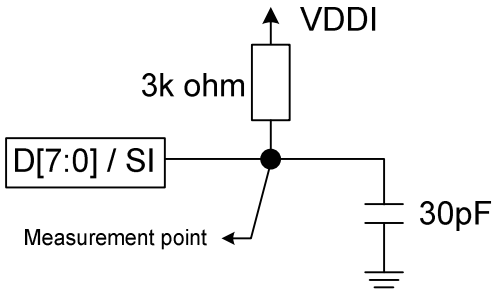
11.7. Maximum Value Measurement

◆ Parallel interface (8080-series)

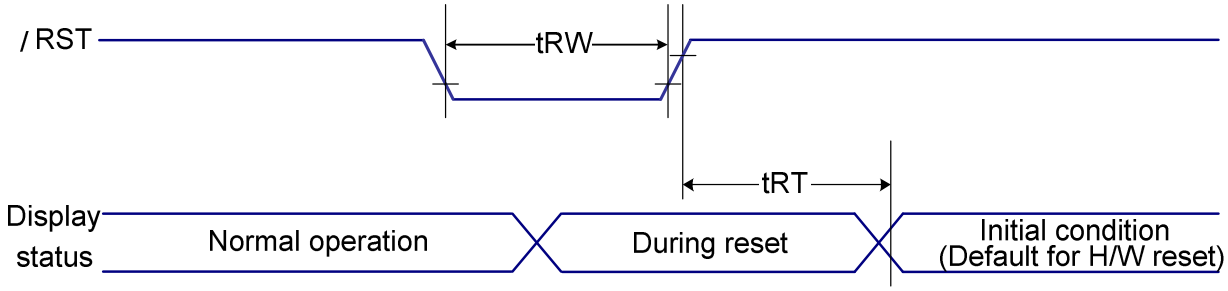


◆ Serial interface (3-line)



Measurement circuit pull down	Measurement circuit pull up
	

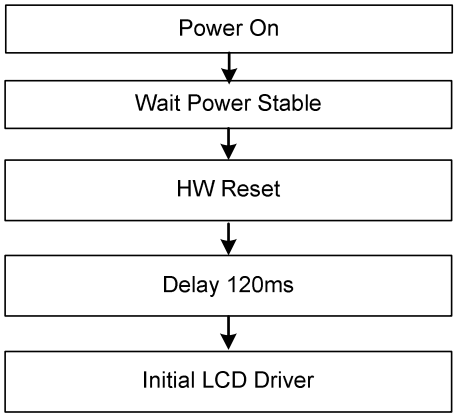
12. RESET TIMING

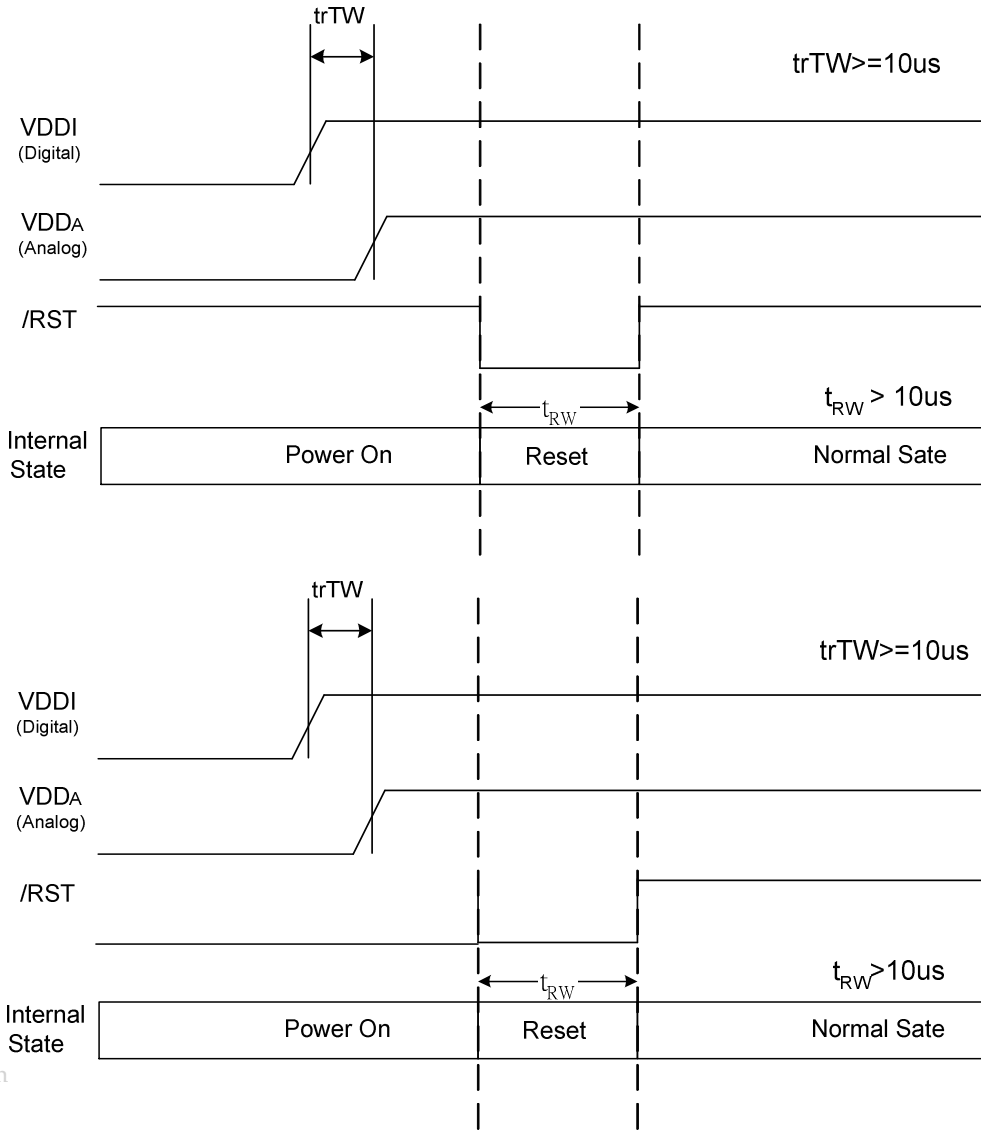


(VSS=0V, Ta = 25℃)

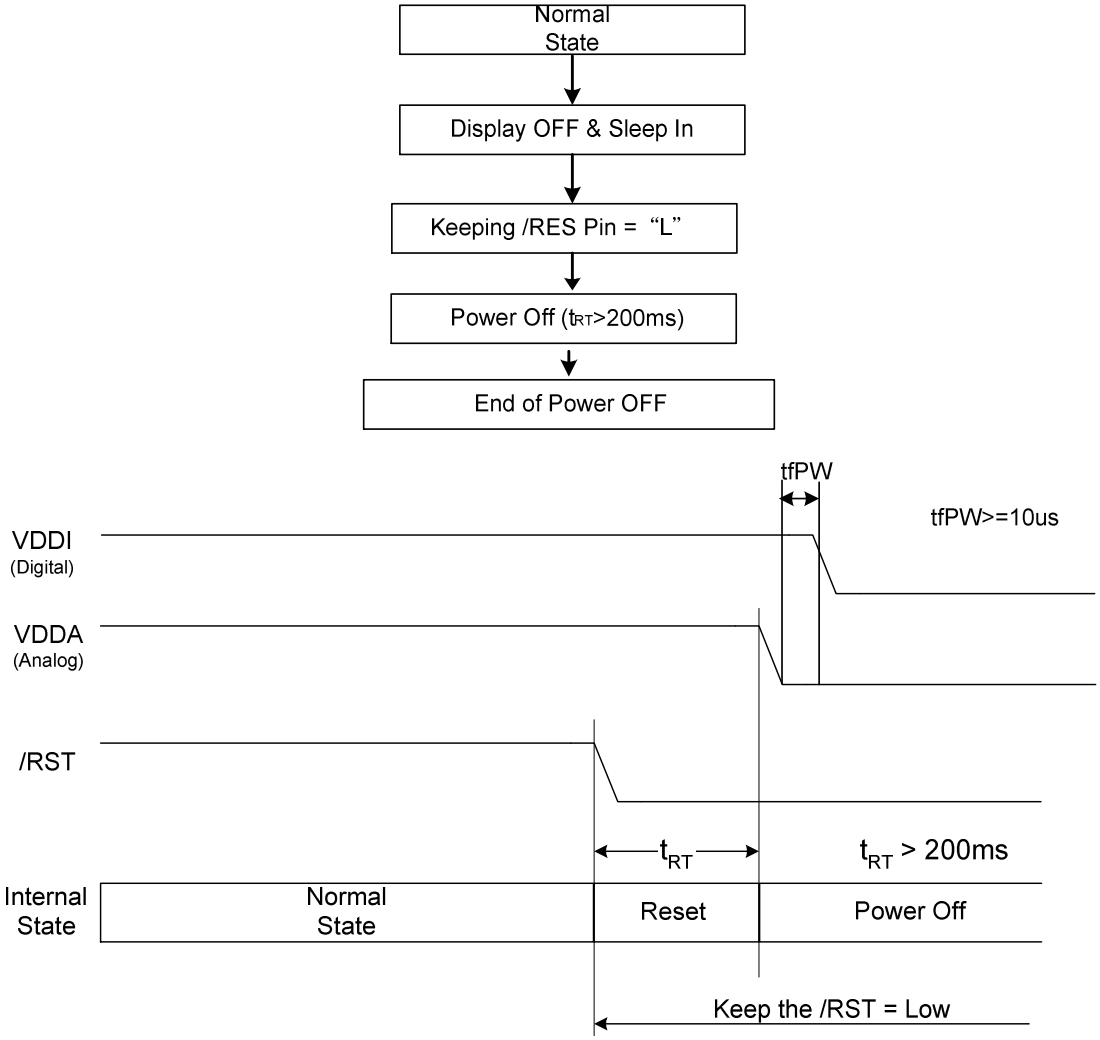
Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Reset “L” pulse width	/RST	tRW	-	10	-	us
Reset time	-	tRT	-	120	-	ms

13. POWER ON FLOW





14. POWER OFF FLOW



15. ITO/FPC LAYOUT GUIDE

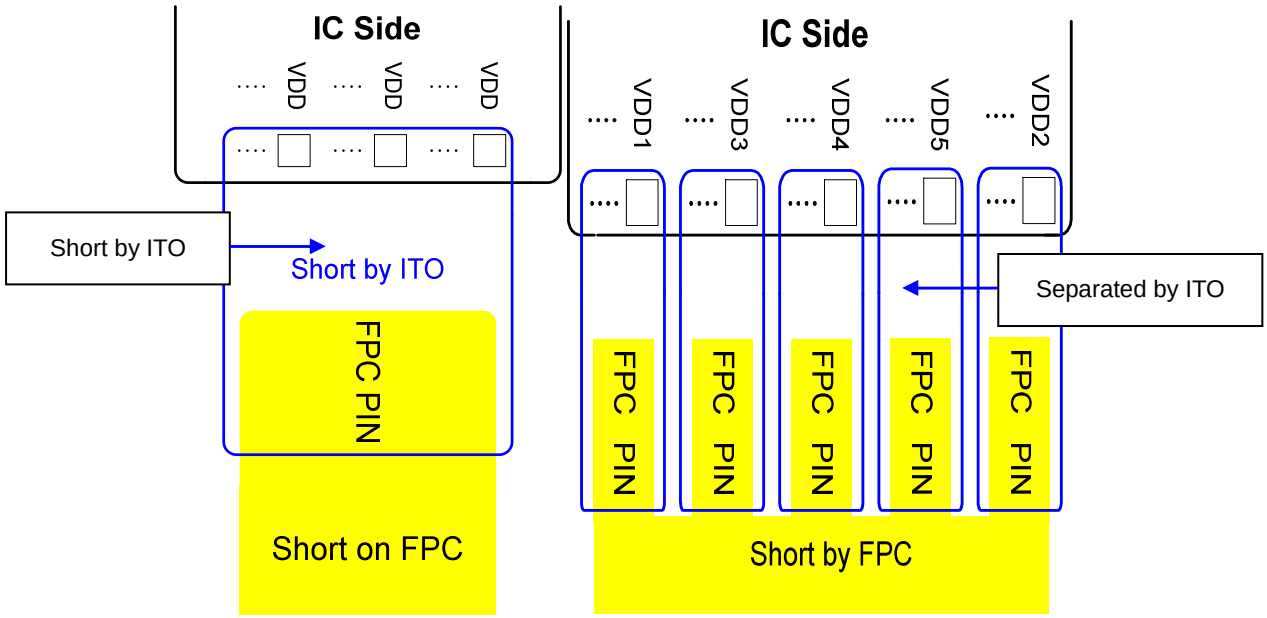
15.1. ITO Layout of Power

◆ **VDD, VDD1~VDD5, VSS, VSS1, VSS2 & VSS4:**

To avoid the noise in different power system affect other power system, please separate different power source on ITO layout (VDD can be short together to get better performance).

To reduce the ITO resistance, the power source should have enough trace width (includes ITO width and FPC trace width). So the separated ITO traces should be connected together by FPC.

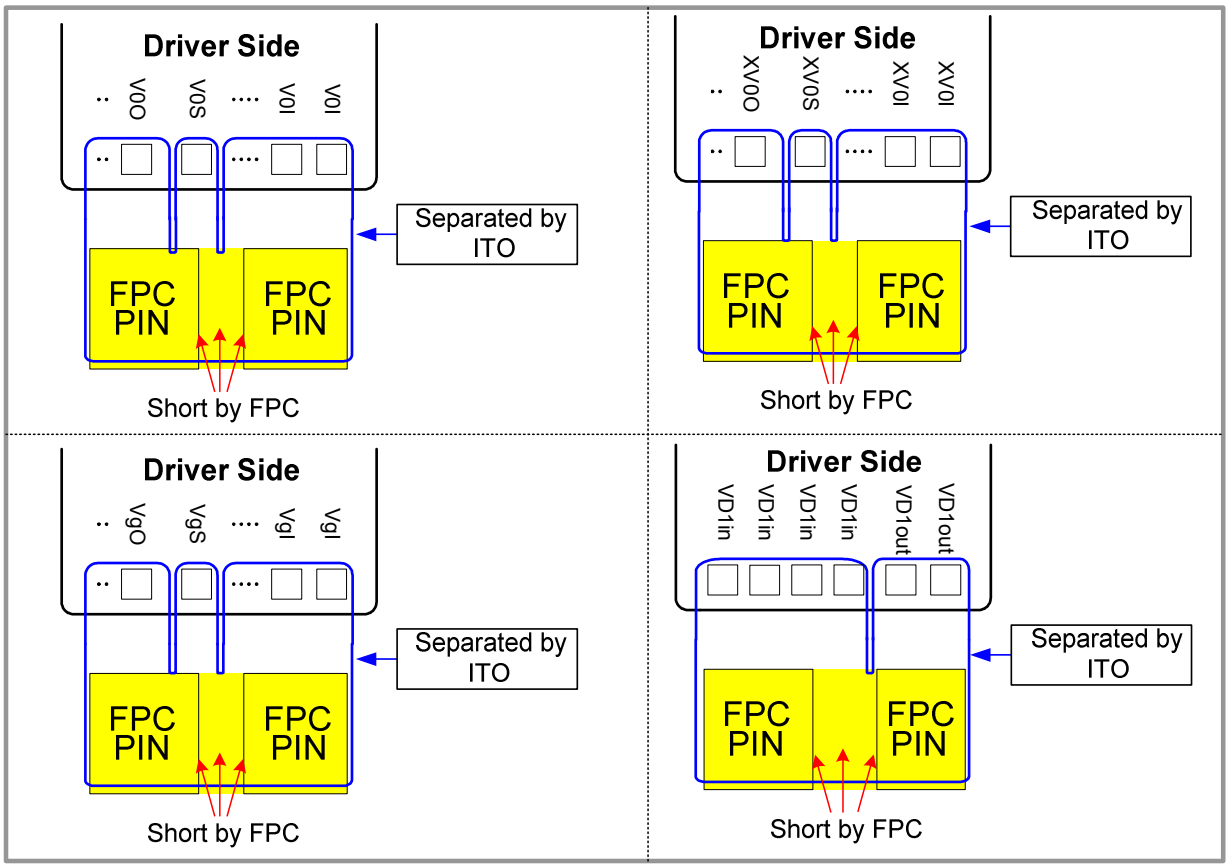
=> The recommended solution is shown below.



◆ **"Output", "Input" and "Sensor" of built-in power circuits:**

The V0, XV0 and Vg power circuits have output pins, input pins and a sensor input. To avoid the power noise affects the sensor input of internal power circuits. The trace should be separated by ITO and should be connected together by FPC. So that the "Sensor" pin has larger ITO resistance (for noise immunity).

The recommended layout topology is shown below:



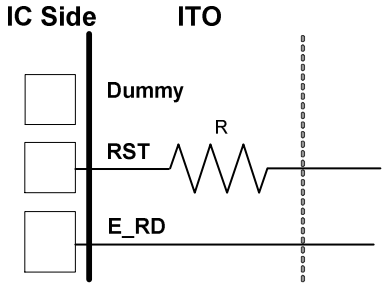
◆ **VPP:**

This is the power source for programming the internal PROM. If the ITO resistance is too high, the operation current will cause the voltage drop while programming PROM. Please try to keep the ITO resistance as low as possible.

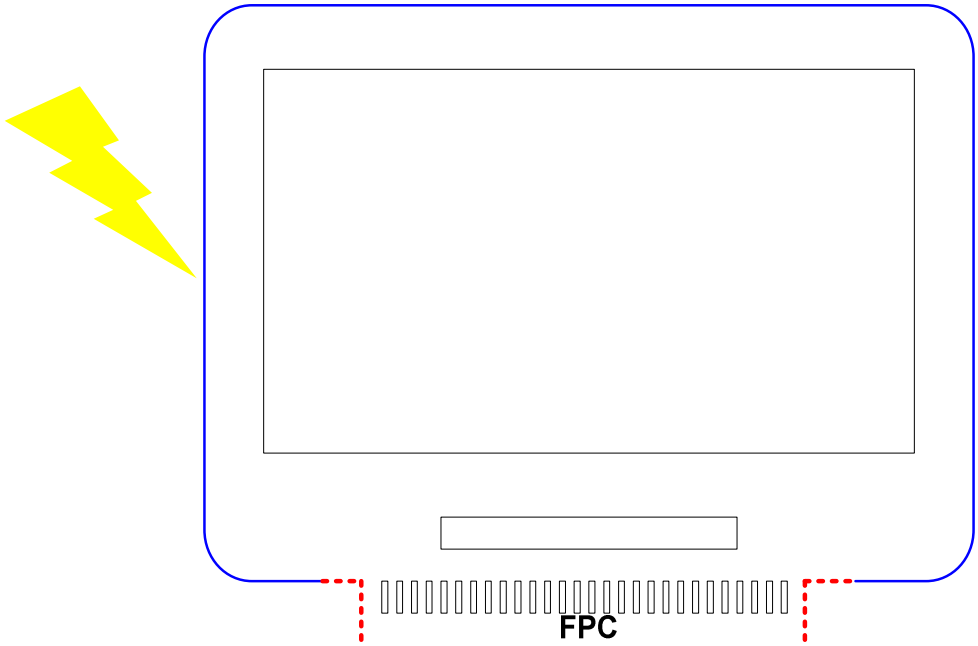
15.2. ESD Protection

◆ **For ESD protection of the LCM, here are some recommendations:**

1. RST (Reset pin): Please increase the resistance of this pin.

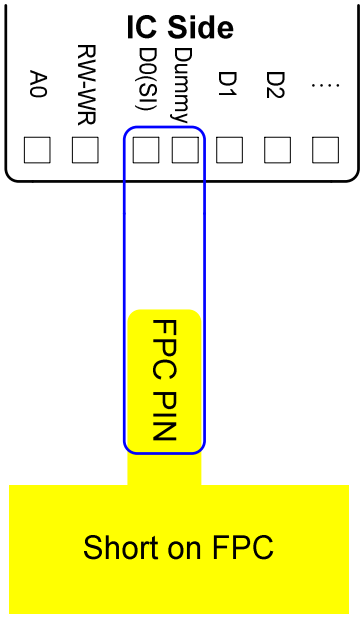


2. ESD Protection Ring: “Shielding Ground” is the first protection of ESD. By connecting the “Blue” (ITO) ring to the FPC, the protection ring is finished.



15.3. SPI (3-Line) ITO Suggestion

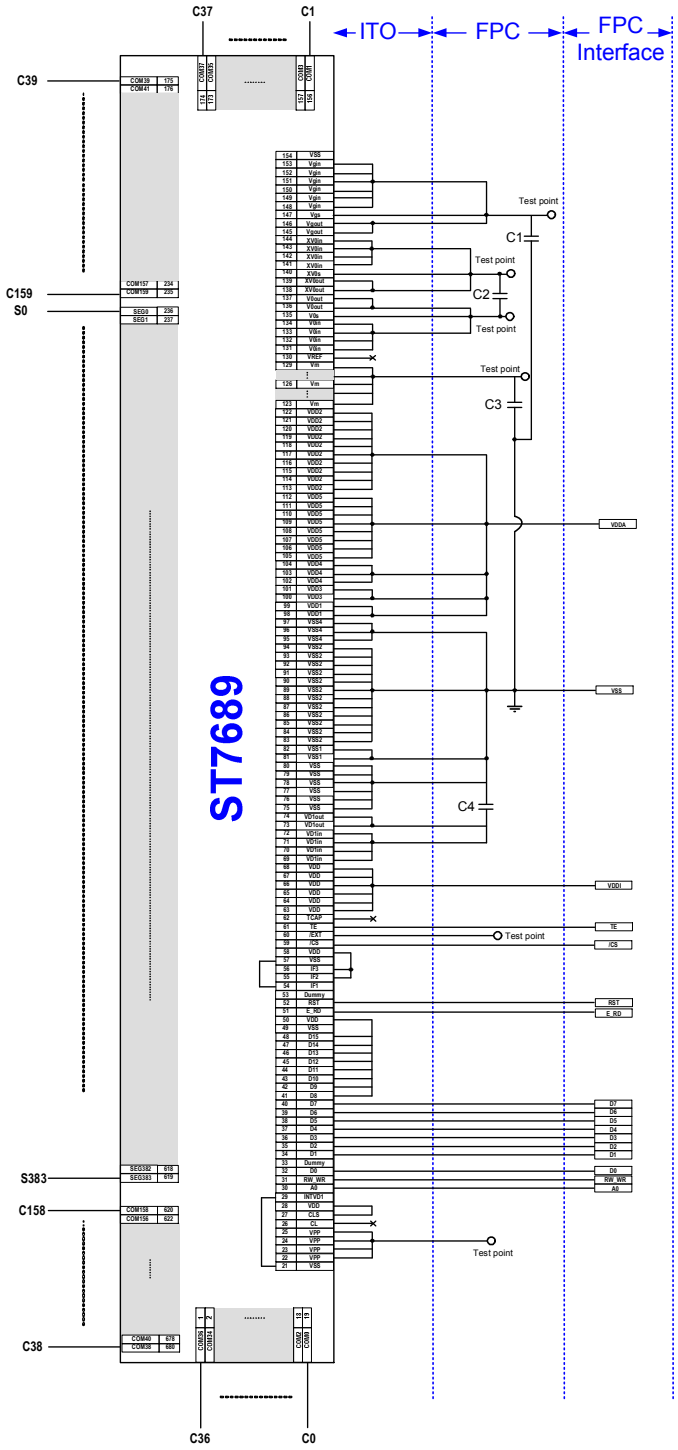
In order to get good transfer quality, the SI should have enough ITO width to reduce the ITO resistance (Interface → SPI 3 Line). The recommended layout topology is shown below:



16. APPLICATION NOTE

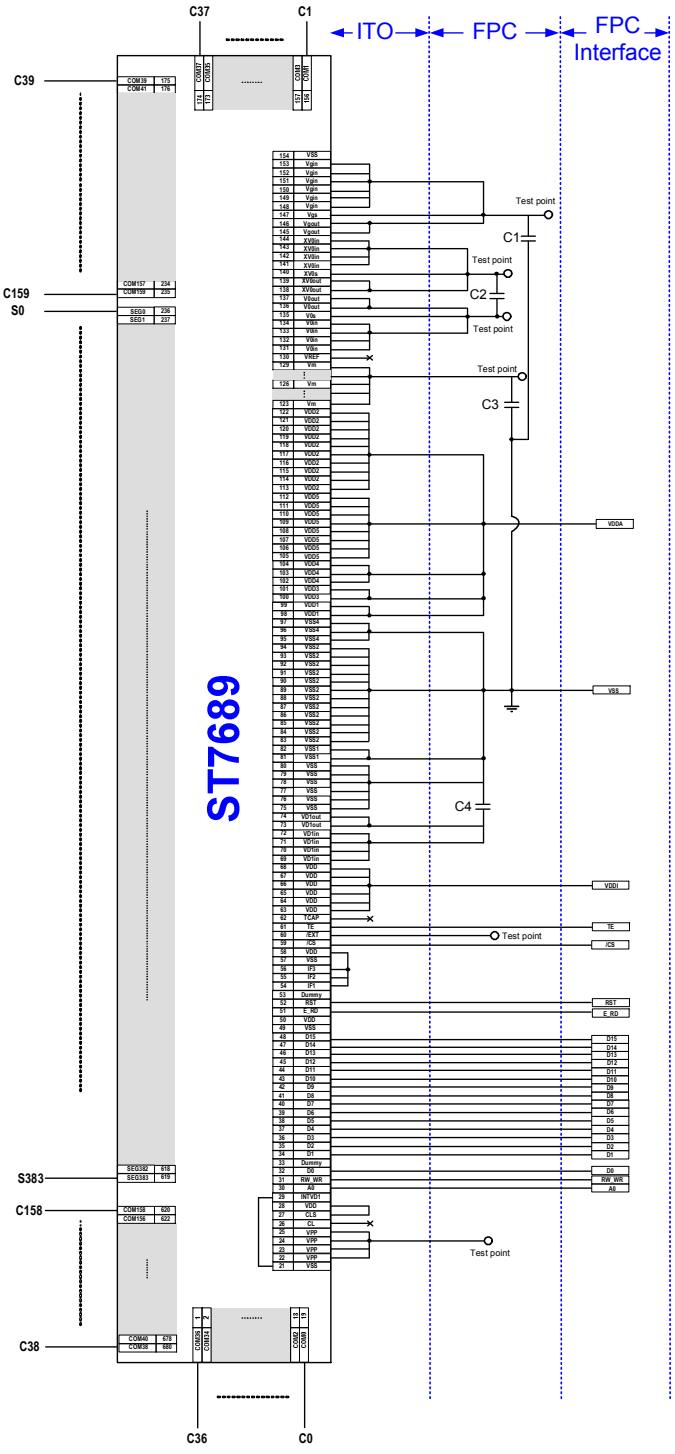
16.1. 8080 series 8-bit parallel mode

Typical VDDI	1.8V/2.8V
VDDA	2.4V≦VDDA≦3.3V
IF[3:1]	H H L
CLS	H (Internal OSC)
INTVD1	L
C1	1uF/16V
C2	1uF/25V
C3	1uF/16V
C4	1uF/16V (optional)



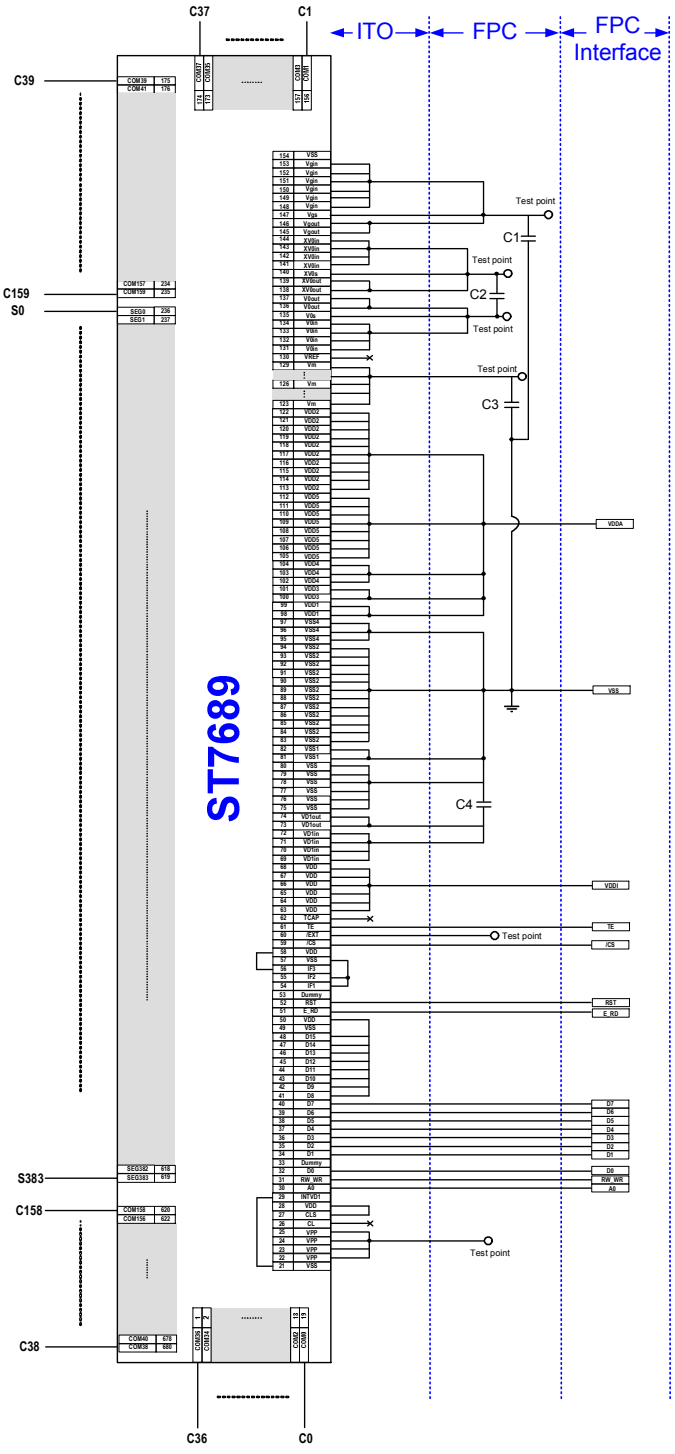
16.2. 8080 series 16-bit parallel mode

Typical VDDI	1.8V/2.8V
VDDA	2.4V≦VDDA≦3.3V
IF[3:1]	H H H
CLS	H (Internal OSC)
INTVD1	L
C1	1uF/16V
C2	1uF/25V
C3	1uF/16V
C4	1uF/16V (optional)



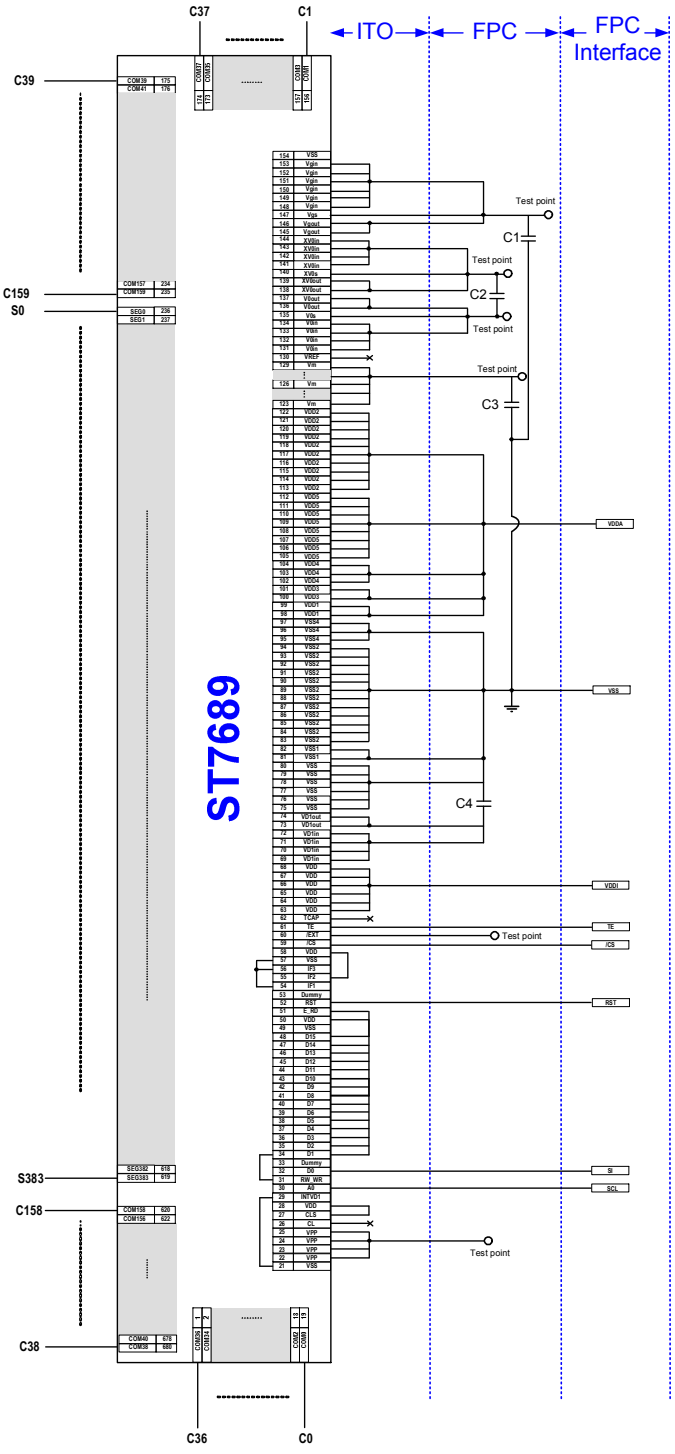
16.3. 6800 series 8-bit parallel mode

Typical VDDI	1.8V/2.8V
VDDA	2.4V≦VDDA≦3.3V
IF[3:1]	H L L
CLS	H (Internal OSC)
INTVD1	L
C1	1uF/16V
C2	1uF/25V
C3	1uF/16V
C4	1uF/16V (optional)



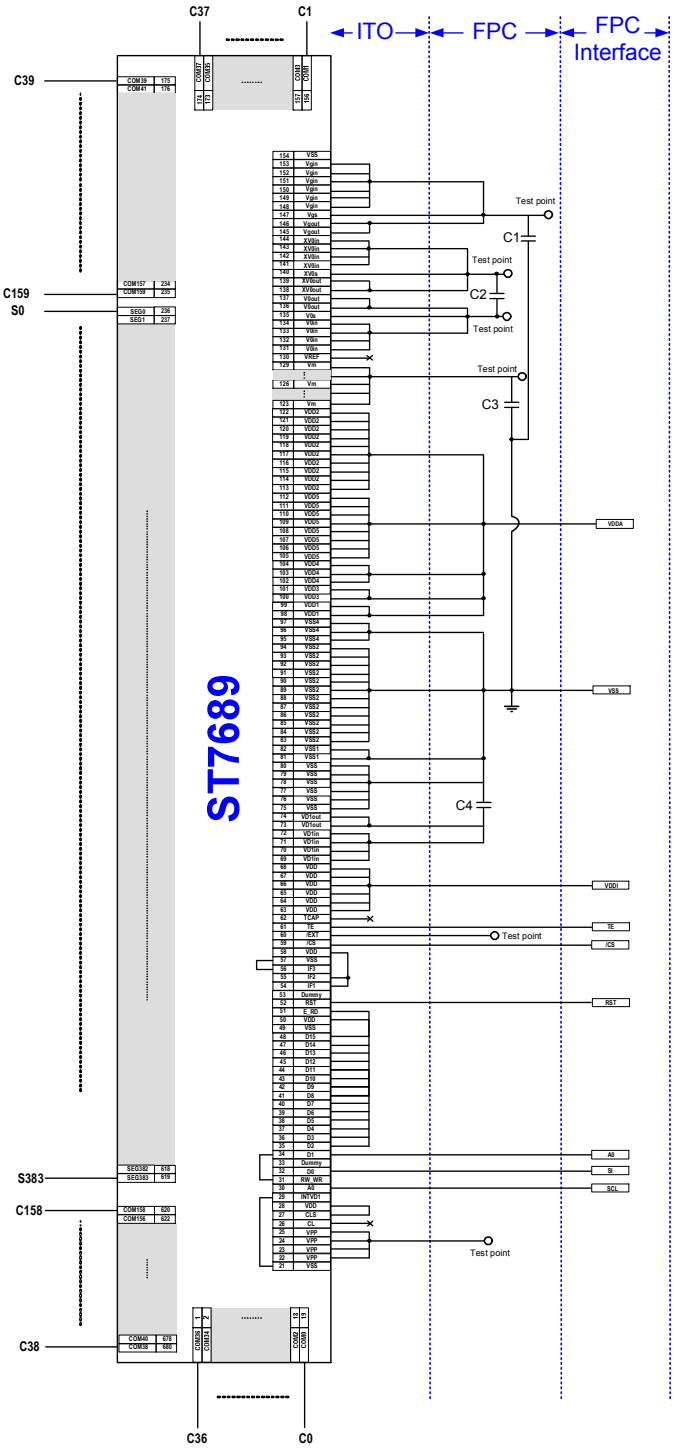
16.4. 9-bit SPI (3 line) mode

Typical VDDI	1.8V/2.8V
VDDA	2.4V≦VDDA≦3.3V
IF[3:1]	L H L
CLS	H (Internal OSC)
INTVD1	L
C1	1uF/16V
C2	1uF/25V
C3	1uF/16V
C4	1uF/16V (optional)



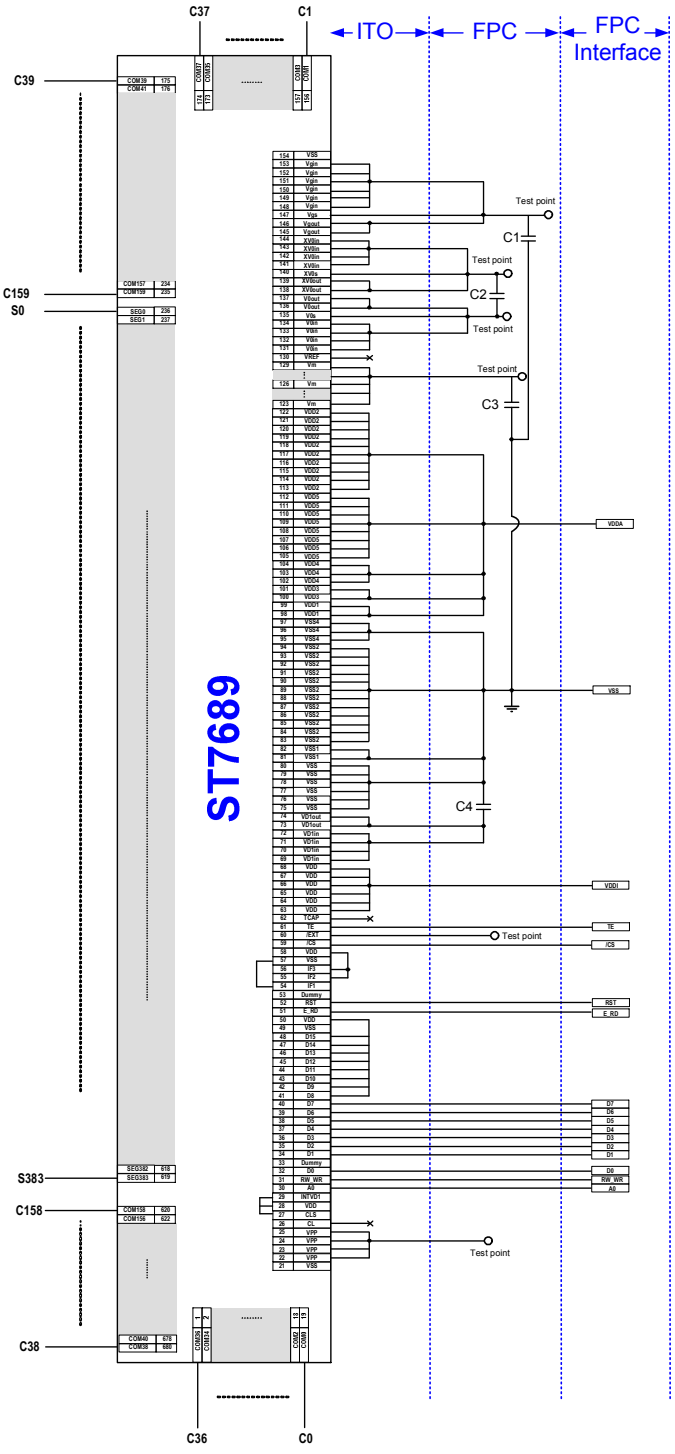
16.5. 8-bit SPI (4 line) mode

Typical VDDI	1.8V/2.8V
VDDA	2.4V≦VDDA≦3.3V
IF[3:1]	L H H
CLS	H (Internal OSC)
INTVD1	L
C1	1uF/16V
C2	1uF/25V
C3	1uF/16V
C4	1uF/16V (optional)



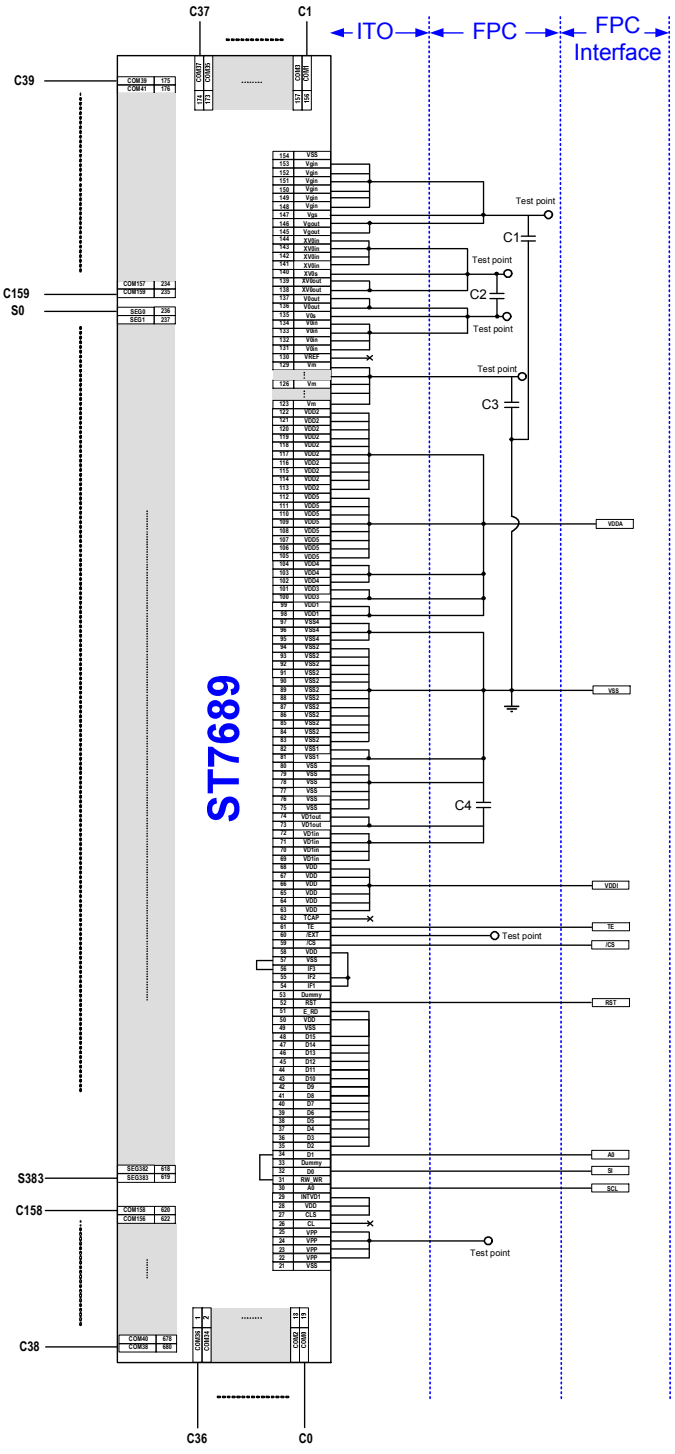
16.6. 8080 series 8-bit parallel mode while typical VDDI=3.0/3.3V

Typical VDDI	3.0V/3.3V
VDDA	2.4V≦VDDA≦3.3V
IF[3:1]	H H L
CLS	H (Internal OSC)
INTVD1	H
C1	1uF/16V
C2	1uF/25V
C3	1uF/16V
C4	1uF/16V

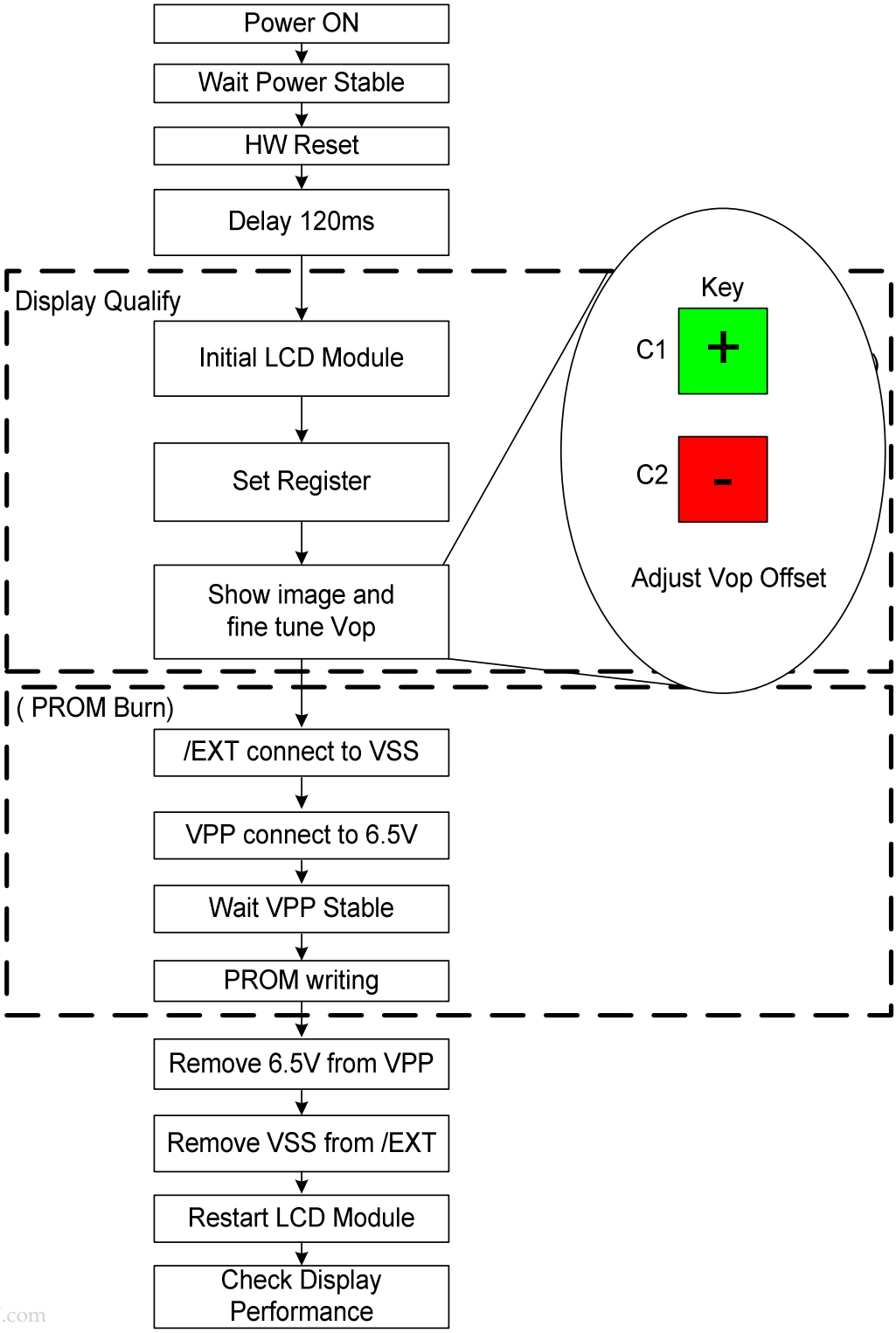


16.7. 8-bit SPI (4 line) mode while typical VDDI=3.0/3.3V

Typical VDDI	3.0V/3.3V
VDDA	2.4V≦VDDA≦3.3V
IF[3:1]	L H H
CLS	H (Internal OSC)
INTVD1	H
C1	1uF/16V
C2	1uF/25V
C3	1uF/16V
C4	1uF/16V



16.8. PROM Programming Flow



16.9. Software Code Flow

```
void Initial_LCM(void)
{
//-----------disable autoread + Manual read once ------------------------------
      Write(COMMAND,0xD7);                  // Auto Load Set
      Write(DATA,0x9F);                     // Auto Load Disable
      Write(COMMAND,0xE0);                  // PROM Read/Write Mode
      Write(DATA,0x00);                     // Set read mode
      delayms(10);                          // Delay 10ms
      Write(COMMAND,0xE3);                  // Read active
      delayms(20);                          // Delay 20ms
      Write(COMMAND,0xE1);                  // Cancel control
//---------------------------------- Sleep OUT ----------------------------------------
      Write(COMMAND, 0x11 );                // Sleep Out
      Write(COMMAND, 0x28 );                // Display OFF
      delayms(50);                          // Delay 50ms
//--------------------------------Vop setting-----------------------------------------
      Write(COMMAND,0xC0);                  // Set Vop by initial Module
      Write(DATA, 0x42);                    // Vop = 16.48V
      Write(DATA, 0x01);                    // based on Module
//--------------------------Set Register-----------------------------------------
      Write(COMMAND,0xC3);                  // Bias select
      Write(DATA,0x04);                     // 1/10 Bias, base on Module
      Write(COMMAND,0xC4);                  // Setting Booster times
      Write(DATA,0x07);                     // Booster X 8
      Write(COMMAND,0xCB);                  // Vg from 2XVDD2 control
      Write(DATA,0x01);                     //
      Write(COMMAND,0xB7);                  // COM / SEG Direction for glass
      Write(DATA,0x48);                     // Setting by LCD module
```

```
    Write(COMMAND,0xD0);                // Analog circuit setting
    Write(DATA,0x1D);                   //
    Write(COMMAND, 0xB5 );              // N-Line Setting
    Write(DATA, 0x8C);                  // Non-RST, 13-line inversion
    Write(COMMAND,0xBD);                // Display Compensation Step
    Write(DATA,0x04);                   // based on module
    Write(COMMAND,0x3A);                // Color Mode Setting
    Write(DATA,0x05);                   // 65k Color
    Write(COMMAND,0x36);                // Memory Access Control
    Write(DATA,0x00);                   // Setting by LCD module
    Write(COMMAND,0xB0);                // Duty Setting
    Write(DATA,0X9F);                   // 160 duty
    Write(COMMAND,0x20);                // Display Inversion OFF
```

1. Set Gamma table for Module

2. Set Temp compensation for Module.

```
    Write(COMMAND,0x2A);                // Col
    Write(DATA,0x00);                   // 0~127
    Write(DATA,0x00);
    Write(DATA,0x00);
    Write(DATA,0x7F);

    Write(COMMAND,0x2B);                // Page
    Write(DATA,0x00);                   // 0~159
    Write(DATA,0x00);
    Write(DATA,0x00);
    Write(DATA,0x9F);

    Write(COMMAND, 0x29 );              // Display On
}
```

```
void Set_PROM_Register(void)
{
//--------------------------------Set PROM register--------------------------------------
        Write(COMMAND, 0xCD );                  // Set ID code, depend on customer
        Write(DATA, 0xF1 );                     //

        Write(COMMAND, 0xB5 );                  // N-Line Setting
        Write(DATA, 0x8C);                      // Non-RST, 13-line inversion

        Write(COMMAND,0xBD);                    // Display Compensation Step
        Write(DATA,0x04);                       // Step 5

}

void Fine_Tune_Vop(void)
{
//------------------------------------ Show Map ------------------------------------------
        Show_Image();                           // Display a image
//------------------------------------ Display ON ----------------------------------------
        Write(COMMAND, 0x29 );                  // Display On
//--------------------------------Fine tune Vop offset-----------------------------------
        Write( COMMAND, 0xC1);                  // Fine tuning Vop here by command
        or                                      // 0xC1 (VopOffsetInc), 0xC2 (VopOffsetDec).
        Write( COMMAND, 0xC2);
        Note#1
}
```

```
void PROM_Writing(void)
{
//--------------------------------Display OFF-------------------------------------
      Write(COMMAND, 0x28 );                  // Display Off
      delayms(50);                            // delay 50ms
//---------------------------------PROM writing-------------------------------------
      Write( COMMAND, 0xF0 );                 // Keep frame rate at 77Hz
      Write( DATA, 0x12 );
      Write( DATA, 0x12 );
      Write( DATA, 0x12 );
      Write( DATA, 0x12 );

      Write( COMMAND, 0xE4 );                 // PROM selection
      Write( DATA, 0x59 );                    // Select PROM
      Write( COMMAND, 0xE5 );                 // Set PROM writing setup
      Write( DATA, 0x0F );
      Write( COMMAND, 0xE0 );                 // Read/write mode setting
      Write( DATA, 0x20 );                    // Set Write mode
      delayms(100);                           // Delay 100ms
      Write( COMMAND, 0xE2 );                 // Write active
      delayms(100);                           // Delay 100ms
      Write( COMMAND, 0xE1 );                 // Cancel control
}
```

Note:

#1 In this section"+" & "-" key button, please execute Write(COMMAND,0xC1) to increase one step at Vop and execute Write(COMMAND,0xC2) to decrease one step at Vop, if necessary.

#2 The TC is turn on in burning flow. If LCD module is too dark or bright, it's an effect of backlight.

17. REVISION HISTORY

ST7689 Serial Specification Revision History		
Version	**Date**	**Description**
0.0	2008/08	● First Issue
0.1	2008/08	● Modify Vop suggestion
0.2	2008/09	● Add Application Note. ● Modify PROM description. ● Modify I/O Pin ITO Resister Limitation. ● Modify description of command MADCTL.
0.3	2009/03	● Add the value of DC CHARACTERISTICS ● Add the value of TIMING CHARACTERISTICS. ● Modify the default value of ID is 80H. ● Modify bias and booster setting.
1.0	2009/10	● Modify TIMING CHARACTERISTICS ● Add the Command ECH(DispCompStep2) ● Add Application Note