

# Sitronix

## ST7773

### 262K Color Single-Chip TFT Controller/Driver

## 1. Introduction

ST7773 is a single-chip controller/driver for 262K-color, graphic type TFT-LCD. It consists of 528 source line and 220 gate line driver circuits. This chip can be connected to a microprocessor direct through Serial Peripheral Interface (SPI) or 8-bits/9-bits/16-bits/18-bits parallel interface. The display data is stored in the on-chip Display Data RAM (DDRAM) of 176x220x18 bits. It can perform display data RAM read/write operation with no external operation clock to minimize power consumption. In addition, because of the integrated power supply circuits necessary to drive liquid crystal, it is possible to make a display system with fewer components.

## 2. Features

### Single chip TFT-LCD Controller/Driver with RAM

#### On-chip Display Data RAM (i.e. Frame Memory)

- 176 x 220 x 18 = 696,960 bits

#### LCD Driver Output Circuits:

- Source Outputs: 176 RGB channels
- Gate Outputs: 220 channels

#### Display Resolution

- 176 (RGB) x 220

#### Display Colors (Color Mode)

- Full Color: 262K, RGB=(666) max., Idle Mode OFF
- Color Reduce: 8-color, RGB=(111), Idle Mode ON

#### Programmable Pixel Color Format (Color Depth) for

#### Various Display Data input Format

- 12-bit/pixel: RGB=(444) using whole frame memory
- 16-bit/pixel: RGB=(565) using whole frame memory
- 18-bit/pixel: RGB=(666) using whole frame memory

#### Various Interfaces

- Parallel 8080-series MCU Interface (8-bit, 9-bit, 16-bit & 18-bit)
- 3-line serial interface

#### Display Features

- Programmable partial display duty
- Line inversion, frame inversion
- Supporting MVA type LC
- Support both normal-black & normal-white LC

#### Built-in Circuits

- DC/DC converter
- Adjustable VCOM
- 4 preset gamma curves (1.0, 1.8, 2.2 & 2.5)
- Oscillator for display clock generation
- Timing controller

#### Built-in NV Memory for LCD Initial Register Setting

- 7-bits for ID2
- 7-bits for VCOM adjustment

#### Wide Supply Voltage Range

- I/O Voltage (VDDI to DGND): 1.6V~3.3V
- Analog Voltage (VDD to AGND): 2.7V~3.3V

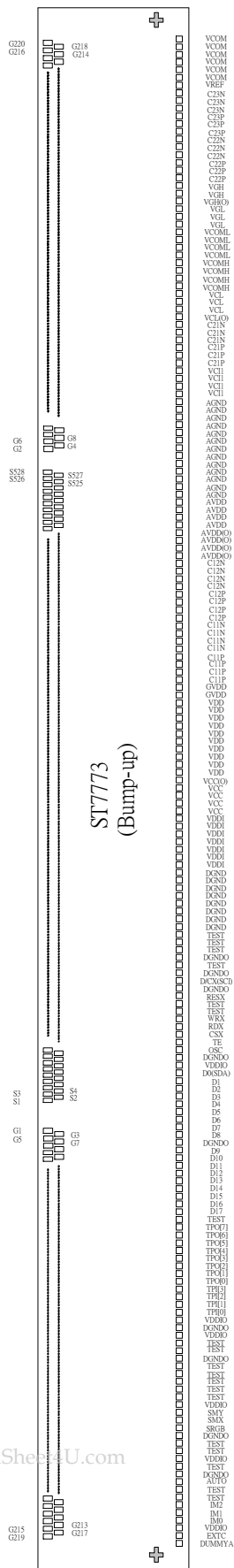
#### On-Chip Power System

- Source Voltage (GVDD to AGND): 3.0V~5.0V
- VCOM HIGH level (VCOMH to AGND): 2.5V to 5.0V
- VCOM LOW level (VCOML to AGND): -2.5V to 0.0V
- Gate driver HIGH level (VGH to AGND): +10.0V to 16V
- Gate driver LOW level (VGL to AGND): -13V to -5.5V

#### Operating Temperature: -30°C to +85°C

<b>ST7773</b>	<b>8080 MCU Interface: 8-bit/9-bit/16-bit/18-bit Serial Peripheral Interface : 3-line</b>	
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## 3. Pad arrangement



View point: bump view

Chip size (um): 17370x820

PAD coordinate: pad center

Coordinate origin: chip center

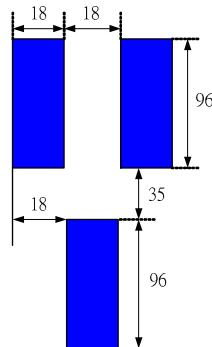
Chip thickness (um): 300(typical)

Bump height (um): 15(typical)

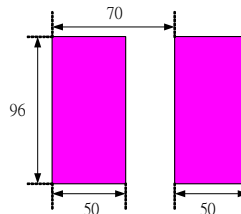
Bump hardness (HV): 75(typical)

Pad arrangement (Unit: um):

Output: pad No. 1 ~ 751 = 18 x 96



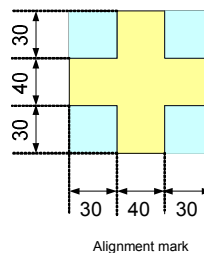
Input: pad No. 752 ~ 947 = 50 x 96



Alignment mark (unit: um):

Left align mark (-8120.58, -300)

Left align mark (8080.6, -300)



Alignment mark

## 4. Pad Center Coordinates

Unit: um

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1	G220	7028	299	41	G140	6308	299
2	G218	7010	168	42	G138	6290	168
3	G216	6992	299	43	G136	6272	299
4	G214	6974	168	44	G134	6254	168
5	G212	6956	299	45	G132	6236	299
6	G210	6938	168	46	G130	6218	168
7	G208	6920	299	47	G128	6200	299
8	G206	6902	168	48	G126	6182	168
9	G204	6884	299	49	G124	6164	299
10	G202	6866	168	50	G122	6146	168
11	G200	6848	299	51	G120	6128	299
12	G198	6830	168	52	G118	6110	168
13	G196	6812	299	53	G116	6092	299
14	G194	6794	168	54	G114	6074	168
15	G192	6776	299	55	G112	6056	299
16	G190	6758	168	56	DUMMYA	6038	168
17	G188	6740	299	57	G110	6020	299
18	G186	6722	168	58	G108	6002	168
19	G184	6704	299	59	G106	5984	299
20	G182	6686	168	60	G104	5966	168
21	G180	6668	299	61	G102	5948	299
22	G178	6650	168	62	G100	5930	168
23	G176	6632	299	63	G98	5912	299
24	G174	6614	168	64	G96	5894	168
25	G172	6596	299	65	G94	5876	299
26	G170	6578	168	66	G92	5858	168
27	G168	6560	299	67	G90	5840	299
28	G166	6542	168	68	G88	5822	168
29	G164	6524	299	69	G86	5804	299
30	G162	6506	168	70	G84	5786	168
31	G160	6488	299	71	G82	5768	299
32	G158	6470	168	72	G80	5750	168
33	G156	6452	299	73	G78	5732	299
34	G154	6434	168	74	G76	5714	168
35	G152	6416	299	75	G74	5696	299
36	G150	6398	168	76	G72	5678	168
37	G148	6380	299	77	G70	5660	299
38	G146	6362	168	78	G68	5642	168
39	G144	6344	299	79	G66	5624	299
40	G142	6326	168	80	G64	5606	168

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PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
81	G62	5588	299	121	S519	4275	168
82	G60	5570	168	122	S518	4257	299
83	G58	5552	299	123	S517	4239	168
84	G56	5534	168	124	S516	4221	299
85	G54	5516	299	125	S515	4203	168
86	G52	5498	168	126	S514	4185	299
87	G50	5480	299	127	S513	4167	168
88	G48	5462	168	128	S512	4149	299
89	G46	5444	299	129	S511	4131	168
90	G44	5426	168	130	S510	4113	299
91	G42	5408	299	131	S509	4095	168
92	G40	5390	168	132	S508	4077	299
93	G38	5372	299	133	S507	4059	168
94	G36	5354	168	134	S506	4041	299
95	G34	5336	299	135	S505	4023	168
96	G32	5318	168	136	S504	4005	299
97	G30	5300	299	137	S503	3987	168
98	G28	5282	168	138	S502	3969	299
99	G26	5264	299	139	S501	3951	168
100	G24	5246	168	140	S500	3933	299
101	G22	5228	299	141	S499	3915	168
102	G20	5210	168	142	S498	3897	299
103	G18	5192	299	143	S497	3879	168
104	G16	5174	168	144	S496	3861	299
105	G14	5156	299	145	S495	3843	168
106	G12	5138	168	146	S494	3825	299
107	G10	5120	299	147	S493	3807	168
108	G8	5102	168	148	S492	3789	299
109	G6	5084	299	149	S491	3771	168
110	G4	5066	168	150	S490	3753	299
111	G2	5048	299	151	S489	3735	168
112	S528	4437	299	152	S488	3717	299
113	S527	4419	168	153	S487	3699	168
114	S526	4401	299	154	S486	3681	299
115	S525	4383	168	155	S485	3663	168
116	S524	4365	299	156	S484	3645	299
117	S523	4347	168	157	S483	3627	168
118	S522	4329	299	158	S482	3609	299
119	S521	4311	168	159	S481	3591	168
120	S520	4293	299	160	S480	3573	299

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PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
161	S479	3555	168	201	S439	2835	168
162	S478	3537	299	202	S438	2817	299
163	S477	3519	168	203	S437	2799	168
164	S476	3501	299	204	S436	2781	299
165	S475	3483	168	205	S435	2763	168
166	S474	3465	299	206	S434	2745	299
167	S473	3447	168	207	S433	2727	168
168	S472	3429	299	208	S432	2709	299
169	S471	3411	168	209	S431	2691	168
170	S470	3393	299	210	S430	2673	299
171	S469	3375	168	211	S429	2655	168
172	S468	3357	299	212	S428	2637	299
173	S467	3339	168	213	S427	2619	168
174	S466	3321	299	214	S426	2601	299
175	S465	3303	168	215	S425	2583	168
176	S464	3285	299	216	S424	2565	299
177	S463	3267	168	217	S423	2547	168
178	S462	3249	299	218	S422	2529	299
179	S461	3231	168	219	S421	2511	168
180	S460	3213	299	220	S420	2493	299
181	S459	3195	168	221	S419	2475	168
182	S458	3177	299	222	S418	2457	299
183	S457	3159	168	223	S417	2439	168
184	S456	3141	299	224	S416	2421	299
185	S455	3123	168	225	S415	2403	168
186	S454	3105	299	226	S414	2385	299
187	S453	3087	168	227	S413	2367	168
188	S452	3069	299	228	S412	2349	299
189	S451	3051	168	229	S411	2331	168
190	S450	3033	299	230	S410	2313	299
191	S449	3015	168	231	S409	2295	168
192	S448	2997	299	232	S408	2277	299
193	S447	2979	168	233	S407	2259	168
194	S446	2961	299	234	S406	2241	299
195	S445	2943	168	235	S405	2223	168
196	S444	2925	299	236	S404	2205	299
197	S443	2907	168	237	S403	2187	168
198	S442	2889	299	238	S402	2169	299
199	S441	2871	168	239	S401	2151	168
200	S440	2853	299	240	S400	2133	299

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PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
241	S399	2115	168	281	S359	1395	168
242	S398	2097	299	282	S358	1377	299
243	S397	2079	168	283	S357	1359	168
244	S396	2061	299	284	S356	1341	299
245	S395	2043	168	285	S355	1323	168
246	S394	2025	299	286	S354	1305	299
247	S393	2007	168	287	S353	1287	168
248	S392	1989	299	288	S352	1269	299
249	S391	1971	168	289	S351	1251	168
250	S390	1953	299	290	S350	1233	299
251	S389	1935	168	291	S349	1215	168
252	S388	1917	299	292	S348	1197	299
253	S387	1899	168	293	S347	1179	168
254	S386	1881	299	294	S346	1161	299
255	S385	1863	168	295	S345	1143	168
256	S384	1845	299	296	S344	1125	299
257	S383	1827	168	297	S343	1107	168
258	S382	1809	299	298	S342	1089	299
259	S381	1791	168	299	S341	1071	168
260	S380	1773	299	300	S340	1053	299
261	S379	1755	168	301	S339	1035	168
262	S378	1737	299	302	S338	1017	299
263	S377	1719	168	303	S337	999	168
264	S376	1701	299	304	S336	981	299
265	S375	1683	168	305	S335	963	168
266	S374	1665	299	306	S334	945	299
267	S373	1647	168	307	S333	927	168
268	S372	1629	299	308	S332	909	299
269	S371	1611	168	309	S331	891	168
270	S370	1593	299	310	S330	873	299
271	S369	1575	168	311	S329	855	168
272	S368	1557	299	312	S328	837	299
273	S367	1539	168	313	S327	819	168
274	S366	1521	299	314	S326	801	299
275	S365	1503	168	315	S325	783	168
276	S364	1485	299	316	S324	765	299
277	S363	1467	168	317	S323	747	168
278	S362	1449	299	318	S322	729	299
279	S361	1431	168	319	S321	711	168
280	S360	1413	299	320	S320	693	299

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PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
321	S319	675	168	361	S279	-45	168
322	S318	657	299	362	S278	-63	299
323	S317	639	168	363	S277	-81	168
324	S316	621	299	364	S276	-99	299
325	S315	603	168	365	S275	-117	168
326	S314	585	299	366	S274	-135	299
327	S313	567	168	367	S273	-153	168
328	S312	549	299	368	S272	-171	299
329	S311	531	168	369	S271	-189	168
330	S310	513	299	370	S270	-207	299
331	S309	495	168	371	S269	-225	168
332	S308	477	299	372	S268	-243	299
333	S307	459	168	373	S267	-261	168
334	S306	441	299	374	S266	-279	299
335	S305	423	168	375	S265	-297	168
336	S304	405	299	376	DUMMYA	-315	299
337	S303	387	168	377	S264	-333	168
338	S302	369	299	378	S263	-351	299
339	S301	351	168	379	S262	-369	168
340	S300	333	299	380	S261	-387	299
341	S299	315	168	381	S260	-405	168
342	S298	297	299	382	S259	-423	299
343	S297	279	168	383	S258	-441	168
344	S296	261	299	384	S257	-459	299
345	S295	243	168	385	S256	-477	168
346	S294	225	299	386	S255	-495	299
347	S293	207	168	387	S254	-513	168
348	S292	189	299	388	S253	-531	299
349	S291	171	168	389	S252	-549	168
350	S290	153	299	390	S251	-567	299
351	S289	135	168	391	S250	-585	168
352	S288	117	299	392	S249	-603	299
353	S287	99	168	393	S248	-621	168
354	S286	81	299	394	S247	-639	299
355	S285	63	168	395	S246	-657	168
356	S284	45	299	396	S245	-675	299
357	S283	27	168	397	S244	-693	168
358	S282	9	299	398	S243	-711	299
359	S281	-9	168	399	S242	-729	168
360	S280	-27	299	400	S241	-747	299

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PAD No.	PIN Name	X	Y
401	S240	-765	168
402	S239	-783	299
403	S238	-801	168
404	S237	-819	299
405	S236	-837	168
406	S235	-855	299
407	S234	-873	168
408	S233	-891	299
409	S232	-909	168
410	S231	-927	299
411	S230	-945	168
412	S229	-963	299
413	S228	-981	168
414	S227	-999	299
415	S226	-1017	168
416	S225	-1035	299
417	S224	-1053	168
418	S223	-1071	299
419	S222	-1089	168
420	S221	-1107	299
421	S220	-1125	168
422	S219	-1143	299
423	S218	-1161	168
424	S217	-1179	299
425	S216	-1197	168
426	S215	-1215	299
427	S214	-1233	168
428	S213	-1251	299
429	S212	-1269	168
430	S211	-1287	299
431	S210	-1305	168
432	S209	-1323	299
433	S208	-1341	168
434	S207	-1359	299
435	S206	-1377	168
436	S205	-1395	299
437	S204	-1413	168
438	S203	-1431	299
439	S202	-1449	168
440	S201	-1467	299

PAD No.	PIN Name	X	Y
441	S200	-1485	168
442	S199	-1503	299
443	S198	-1521	168
444	S197	-1539	299
445	S196	-1557	168
446	S195	-1575	299
447	S194	-1593	168
448	S193	-1611	299
449	S192	-1629	168
450	S191	-1647	299
451	S190	-1665	168
452	S189	-1683	299
453	S188	-1701	168
454	S187	-1719	299
455	S186	-1737	168
456	S185	-1755	299
457	S184	-1773	168
458	S183	-1791	299
459	S182	-1809	168
460	S181	-1827	299
461	S180	-1845	168
462	S179	-1863	299
463	S178	-1881	168
464	S177	-1899	299
465	S176	-1917	168
466	S175	-1935	299
467	S174	-1953	168
468	S173	-1971	299
469	S172	-1989	168
470	S171	-2007	299
471	S170	-2025	168
472	S169	-2043	299
473	S168	-2061	168
474	S167	-2079	299
475	S166	-2097	168
476	S165	-2115	299
477	S164	-2133	168
478	S163	-2151	299
479	S162	-2169	168
480	S161	-2187	299

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PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
481	S160	-2205	168	521	S120	-2925	168
482	S159	-2223	299	522	S119	-2943	299
483	S158	-2241	168	523	S118	-2961	168
484	S157	-2259	299	524	S117	-2979	299
485	S156	-2277	168	525	S116	-2997	168
486	S155	-2295	299	526	S115	-3015	299
487	S154	-2313	168	527	S114	-3033	168
488	S153	-2331	299	528	S113	-3051	299
489	S152	-2349	168	529	S112	-3069	168
490	S151	-2367	299	530	S111	-3087	299
491	S150	-2385	168	531	S110	-3105	168
492	S149	-2403	299	532	S109	-3123	299
493	S148	-2421	168	533	S108	-3141	168
494	S147	-2439	299	534	S107	-3159	299
495	S146	-2457	168	535	S106	-3177	168
496	S145	-2475	299	536	S105	-3195	299
497	S144	-2493	168	537	S104	-3213	168
498	S143	-2511	299	538	S103	-3231	299
499	S142	-2529	168	539	S102	-3249	168
500	S141	-2547	299	540	S101	-3267	299
501	S140	-2565	168	541	S100	-3285	168
502	S139	-2583	299	542	S99	-3303	299
503	S138	-2601	168	543	S98	-3321	168
504	S137	-2619	299	544	S97	-3339	299
505	S136	-2637	168	545	S96	-3357	168
506	S135	-2655	299	546	S95	-3375	299
507	S134	-2673	168	547	S94	-3393	168
508	S133	-2691	299	548	S93	-3411	299
509	S132	-2709	168	549	S92	-3429	168
510	S131	-2727	299	550	S91	-3447	299
511	S130	-2745	168	551	S90	-3465	168
512	S129	-2763	299	552	S89	-3483	299
513	S128	-2781	168	553	S88	-3501	168
514	S127	-2799	299	554	S87	-3519	299
515	S126	-2817	168	555	S86	-3537	168
516	S125	-2835	299	556	S85	-3555	299
517	S124	-2853	168	557	S84	-3573	168
518	S123	-2871	299	558	S83	-3591	299
519	S122	-2889	168	559	S82	-3609	168
520	S121	-2907	299	560	S81	-3627	299

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PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
561	S80	-3645	168	601	S40	-4365	168
562	S79	-3663	299	602	S39	-4383	299
563	S78	-3681	168	603	S38	-4401	168
564	S77	-3699	299	604	S37	-4419	299
565	S76	-3717	168	605	S36	-4437	168
566	S75	-3735	299	606	S35	-4455	299
567	S74	-3753	168	607	S34	-4473	168
568	S73	-3771	299	608	S33	-4491	299
569	S72	-3789	168	609	S32	-4509	168
570	S71	-3807	299	610	S31	-4527	299
571	S70	-3825	168	611	S30	-4545	168
572	S69	-3843	299	612	S29	-4563	299
573	S68	-3861	168	613	S28	-4581	168
574	S67	-3879	299	614	S27	-4599	299
575	S66	-3897	168	615	S26	-4617	168
576	S65	-3915	299	616	S25	-4635	299
577	S64	-3933	168	617	S24	-4653	168
578	S63	-3951	299	618	S23	-4671	299
579	S62	-3969	168	619	S22	-4689	168
580	S61	-3987	299	620	S21	-4707	299
581	S60	-4005	168	621	S20	-4725	168
582	S59	-4023	299	622	S19	-4743	299
583	S58	-4041	168	623	S18	-4761	168
584	S57	-4059	299	624	S17	-4779	299
585	S56	-4077	168	625	S16	-4797	168
586	S55	-4095	299	626	S15	-4815	299
587	S54	-4113	168	627	S14	-4833	168
588	S53	-4131	299	628	S13	-4851	299
589	S52	-4149	168	629	S12	-4869	168
590	S51	-4167	299	630	S11	-4887	299
591	S50	-4185	168	631	S10	-4905	168
592	S49	-4203	299	632	S9	-4923	299
593	S48	-4221	168	633	S8	-4941	168
594	S47	-4239	299	634	S7	-4959	299
595	S46	-4257	168	635	S6	-4977	168
596	S45	-4275	299	636	S5	-4995	299
597	S44	-4293	168	637	S4	-5013	168
598	S43	-4311	299	638	S3	-5031	299
599	S42	-4329	168	639	S2	-5049	168
600	S41	-4347	299	640	S1	-5067	299

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PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
641	G1	-5678	299	681	G81	-6398	299
642	G3	-5696	168	682	G83	-6416	168
643	G5	-5714	299	683	G85	-6434	299
644	G7	-5732	168	684	G87	-6452	168
645	G9	-5750	299	685	G89	-6470	299
646	G11	-5768	168	686	G91	-6488	168
647	G13	-5786	299	687	G93	-6506	299
648	G15	-5804	168	688	G95	-6524	168
649	G17	-5822	299	689	G97	-6542	299
650	G19	-5840	168	690	G99	-6560	168
651	G21	-5858	299	691	G101	-6578	299
652	G23	-5876	168	692	G103	-6596	168
653	G25	-5894	299	693	G105	-6614	299
654	G27	-5912	168	694	G107	-6632	168
655	G29	-5930	299	695	G109	-6650	299
656	G31	-5948	168	696	DUMMYA	-6668	168
657	G33	-5966	299	697	G111	-6686	299
658	G35	-5984	168	698	G113	-6704	168
659	G37	-6002	299	699	G115	-6722	299
660	G39	-6020	168	700	G117	-6740	168
661	G41	-6038	299	701	G119	-6758	299
662	G43	-6056	168	702	G121	-6776	168
663	G45	-6074	299	703	G123	-6794	299
664	G47	-6092	168	704	G125	-6812	168
665	G49	-6110	299	705	G127	-6830	299
666	G51	-6128	168	706	G129	-6848	168
667	G53	-6146	299	707	G131	-6866	299
668	G55	-6164	168	708	G133	-6884	168
669	G57	-6182	299	709	G135	-6902	299
670	G59	-6200	168	710	G137	-6920	168
671	G61	-6218	299	711	G139	-6938	299
672	G63	-6236	168	712	G141	-6956	168
673	G65	-6254	299	713	G143	-6974	299
674	G67	-6272	168	714	G145	-6992	168
675	G69	-6290	299	715	G147	-7010	299
676	G71	-6308	168	716	G149	-7028	168
677	G73	-6326	299	717	G151	-7046	299
678	G75	-6344	168	718	G153	-7064	168
679	G77	-6362	299	719	G155	-7082	299
680	G79	-6380	168	720	G157	-7100	168

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PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
721	G159	-7118	299	761	DGND0	-7398.58	-299
722	G161	-7136	168	762	TEST	-7328.58	-299
723	G163	-7154	299	763	VDDIO	-7258.58	-299
724	G165	-7172	168	764	TEST	-7188.58	-299
725	G167	-7190	299	765	TEST	-7118.58	-299
726	G169	-7208	168	766	DGND0	-7048.58	-299
727	G171	-7226	299	767	SRGB	-6978.58	-299
728	G173	-7244	168	768	SMX	-6908.58	-299
729	G175	-7262	299	769	SMY	-6838.58	-299
730	G177	-7280	168	770	VDDIO	-6768.58	-299
731	G179	-7298	299	771	TEST	-6698.58	-299
732	G181	-7316	168	772	TEST	-6628.58	-299
733	G183	-7334	299	773	TEST	-6558.58	-299
734	G185	-7352	168	774	TEST	-6488.58	-299
735	G187	-7370	299	775	TEST	-6418.58	-299
736	G189	-7388	168	776	DGND0	-6348.58	-299
737	G191	-7406	299	777	TEST	-6278.58	-299
738	G193	-7424	168	778	TEST	-6208.58	-299
739	G195	-7442	299	779	VDDIO	-6138.58	-299
740	G197	-7460	168	780	DGND0	-6068.58	-299
741	G199	-7478	299	781	VDDIO	-5998.58	-299
742	G201	-7496	168	782	TPI[0]	-5928.58	-299
743	G203	-7514	299	783	TPI[1]	-5858.58	-299
744	G205	-7532	168	784	TPI[2]	-5788.58	-299
745	G207	-7550	299	785	TPI[3]	-5718.58	-299
746	G209	-7568	168	786	TPO[0]	-5648.58	-299
747	G211	-7586	299	787	TPO[1]	-5578.58	-299
748	G213	-7604	168	788	TPO[2]	-5508.58	-299
749	G215	-7622	299	789	TPO[3]	-5438.58	-299
750	G217	-7640	168	790	TPO[4]	-5368.58	-299
751	G219	-7658	299	791	TPO[5]	-5298.58	-299
752	DUMMYA	-8028.58	-299	792	TPO[6]	-5228.58	-299
753	EXTC	-7958.58	-299	793	TPO[7]	-5158.58	-299
754	VDDIO	-7888.58	-299	794	TEST	-5088.58	-299
755	IM0	-7818.58	-299	795	D17	-5018.58	-299
756	IM1	-7748.58	-299	796	D16	-4948.58	-299
757	IM2	-7678.58	-299	797	D15	-4878.58	-299
758	TEST	-7608.58	-299	798	D14	-4808.58	-299
759	TEST	-7538.58	-299	799	D13	-4738.58	-299
760	AUTO	-7468.58	-299	800	D12	-4668.58	-299

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PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
801	D11	-4598.58	-299	841	VDDI	-1798.58	-299
802	D10	-4528.58	-299	842	VDDI	-1728.58	-299
803	D9	-4458.58	-299	843	VDDI	-1658.58	-299
804	DGND0	-4388.58	-299	844	VDDI	-1588.58	-299
805	D8	-4318.58	-299	845	VDDI	-1518.58	-299
806	D7	-4248.58	-299	846	VDDI	-1448.58	-299
807	D6	-4178.58	-299	847	VCC	-673.45	-299
808	D5	-4108.58	-299	848	VCC	-603.45	-299
809	D4	-4038.58	-299	849	VCC	-533.45	-299
810	D3	-3968.58	-299	850	VCC	-463.45	-299
811	D2	-3898.58	-299	851	VCCO	-393.45	-299
812	D1	-3828.58	-299	852	VDD	88.26	-299
813	D0(SDA)	-3758.58	-299	853	VDD	158.26	-299
814	VDDIO	-3688.58	-299	854	VDD	228.26	-299
815	DGND0	-3618.58	-299	855	VDD	298.26	-299
816	OSCP	-3548.58	-299	856	VDD	368.26	-299
817	TEP	-3478.58	-299	857	VDD	438.26	-299
818	CSX	-3408.58	-299	858	VDD	508.26	-299
819	RDX	-3338.58	-299	859	VDD	578.26	-299
820	WRX	-3268.58	-299	860	VDD	648.26	-299
821	TEST	-3198.58	-299	861	VDD	718.26	-299
822	TEST	-3128.58	-299	862	GVDD	788.26	-299
823	RESX	-3058.58	-299	863	GVDD	858.26	-299
824	DGND0	-2988.58	-299	864	C11P	2232.71	-299
825	D/CX(SCI)	-2918.58	-299	865	C11P	2302.71	-299
826	DGND0	-2848.58	-299	866	C11P	2372.71	-299
827	TEST	-2778.58	-299	867	C11P	2442.71	-299
828	DGND0	-2708.58	-299	868	C11N	2512.71	-299
829	TEST	-2638.58	-299	869	C11N	2582.71	-299
830	TEST	-2568.58	-299	870	C11N	2652.71	-299
831	TEST	-2498.58	-299	871	C11N	2722.71	-299
832	DGND	-2428.58	-299	872	C12P	2792.71	-299
833	DGND	-2358.58	-299	873	C12P	2862.71	-299
834	DGND	-2288.58	-299	874	C12P	2932.71	-299
835	DGND	-2218.58	-299	875	C12P	3002.71	-299
836	DGND	-2148.58	-299	876	C12N	3072.71	-299
837	DGND	-2078.58	-299	877	C12N	3142.71	-299
838	DGND	-2008.58	-299	878	C12N	3212.71	-299
839	DGND	-1938.58	-299	879	C12N	3282.71	-299
840	VDDI	-1868.58	-299	880	AVDDO	3352.71	-299

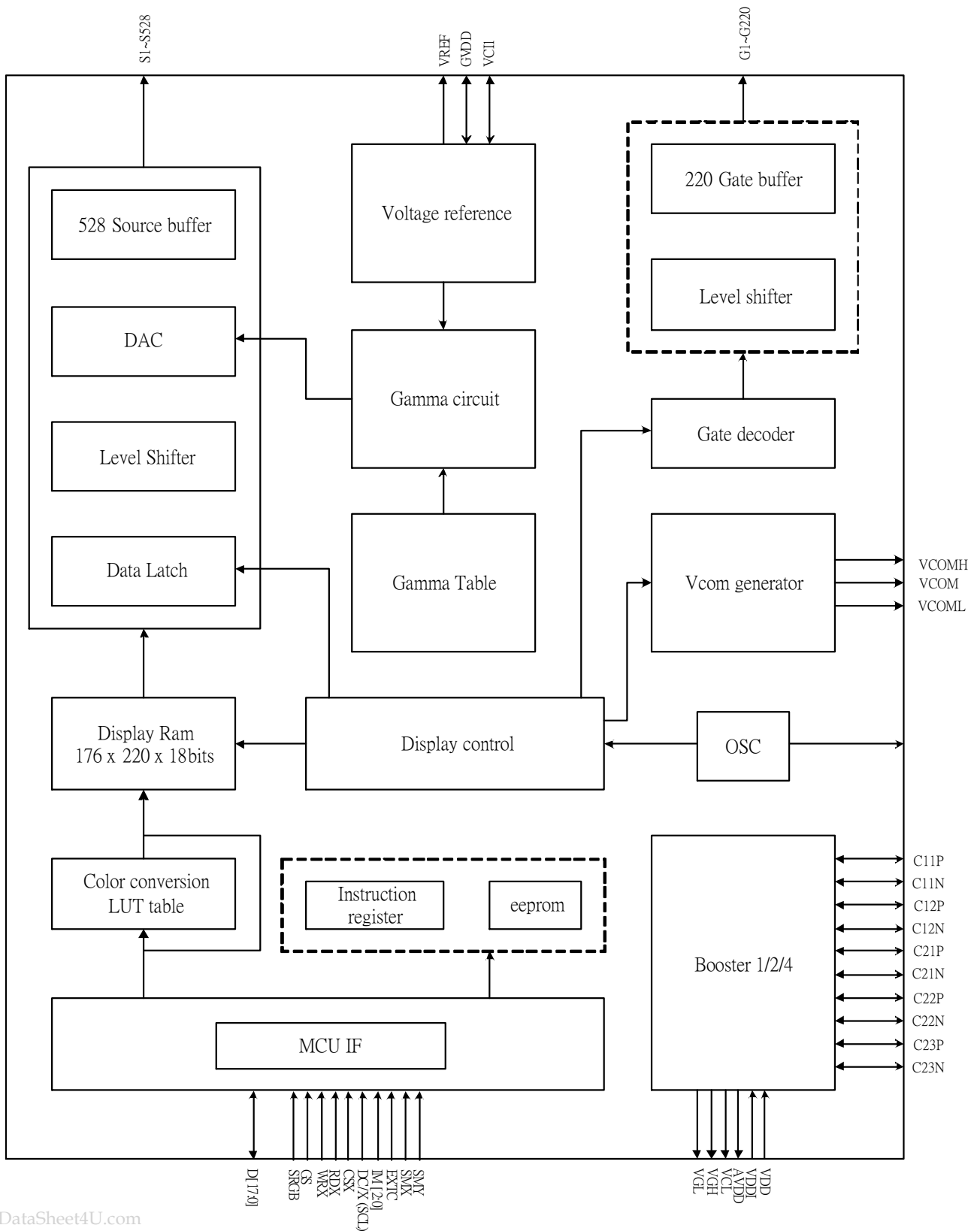
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PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
881	AVDDO	3422.71	-299	921	VCOML	6222.71	-299
882	AVDDO	3492.71	-299	922	VCOML	6292.71	-299
883	AVDDO	3562.71	-299	923	VGL	6362.71	-299
884	AVDD	3632.71	-299	924	VGL	6432.71	-299
885	AVDD	3702.71	-299	925	VGL	6502.71	-299
886	AVDD	3772.71	-299	926	VGHO	6572.71	-299
887	AVDD	3842.71	-299	927	VGH	6642.71	-299
888	AGND	3912.71	-299	928	VGH	6712.71	-299
889	AGND	3982.71	-299	929	C22P	6782.71	-299
890	AGND	4052.71	-299	930	C22P	6852.71	-299
891	AGND	4122.71	-299	931	C22P	6922.71	-299
892	AGND	4192.71	-299	932	C22N	6992.71	-299
893	AGND	4262.71	-299	933	C22N	7062.71	-299
894	AGND	4332.71	-299	934	C22N	7132.71	-299
895	AGND	4402.71	-299	935	C23P	7202.71	-299
896	AGND	4472.71	-299	936	C23P	7272.71	-299
897	AGND	4542.71	-299	937	C23P	7342.71	-299
898	AGND	4612.71	-299	938	C23N	7412.71	-299
899	AGND	4682.71	-299	939	C23N	7482.71	-299
900	AGND	4752.71	-299	940	C23N	7552.71	-299
901	VCI1	4822.71	-299	941	VREF	8172.06	-299
902	VCI1	4892.71	-299	942	VCOM	8242.06	-299
903	VCI1	4962.71	-299	943	VCOM	8312.06	-299
904	VCI1	5032.71	-299	944	VCOM	8382.06	-299
905	C21P	5102.71	-299	945	VCOM	8452.06	-299
906	C21P	5172.71	-299	946	VCOM	8522.06	-299
907	C21P	5242.71	-299	947	VCOM	8592.06	-299
908	C21N	5312.71	-299				
909	C21N	5382.71	-299				
910	C21N	5452.71	-299				
911	VCLO	5522.71	-299				
912	VCL	5592.71	-299				
913	VCL	5662.71	-299				
914	VCL	5732.71	-299				
915	VCOMH	5802.71	-299				
916	VCOMH	5872.71	-299				
917	VCOMH	5942.71	-299				
918	VCOMH	6012.71	-299				
919	VCOML	6082.71	-299				
920	VCOML	6152.71	-299				

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5. Block diagram



## 6. Pin description

### 6.1 Power supply pin

Name	I/O	Description	Count	Connect pin
VDD	I	Power supply for analog, digital system and booster circuit.		VDD
VDDI	I	Power supply for I/O system.		VDDI
AGND	I	System ground for analog system and booster circuit.		GND
DGND	I	System ground for I/O system and digital system.		GND

### 6.2 Interface logic pin

Name	I/O	Description	Count	Connect pin															
IM2	I	MCU Parallel interface bus and Serial interface select IM2='1', Parallel interface IM2='0', Serial interface.	1	DGND/VDDI															
IM1,IM0	I	- MCU parallel interface type selection -If not used, please fix this pin at VDDI or DGND level.	2	DGND/VDDI															
		<table border="1"> <thead> <tr> <th>IM1</th> <th>IM0</th> <th>Parallel interface</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>MCU 8-bit parallel</td> </tr> <tr> <td>0</td> <td>1</td> <td>MCU 16-bit parallel</td> </tr> <tr> <td>1</td> <td>0</td> <td>MCU 9-bit parallel</td> </tr> <tr> <td>1</td> <td>1</td> <td>MCU 18-bit parallel</td> </tr> </tbody> </table>			IM1	IM0	Parallel interface	0	0	MCU 8-bit parallel	0	1	MCU 16-bit parallel	1	0	MCU 9-bit parallel	1	1	MCU 18-bit parallel
		IM1			IM0	Parallel interface													
		0			0	MCU 8-bit parallel													
		0			1	MCU 16-bit parallel													
1	0	MCU 9-bit parallel																	
1	1	MCU 18-bit parallel																	
RESX	I	-This signal will reset the device and it must be applied to properly initialize the chip. -Signal is active low.	1	MCU															
CSX	I	-Chip selection pin ("Low" is enable).	1	MCU															
D/CX (SCI)	I	-Display data/command selection pin in MCU interface. -D/CX='1': display data or parameter. -D/CX='0': command data. -In serial interface, this is used as SCL.	1	MCU															
RDX	I	-Read enable in 8080 MCU parallel interface. -If not used, please connect this pin to VDDI or DGND.	1	MCU															
WRX	I	-Write enable in MCU parallel interface. -If not used, please connect this pin to VDDI or DGND.	1	MCU															
OSC	O	-Monitoring pin of internal oscillator clock and is turned ON/OFF by S/W command. -When this pin is inactive (function OFF), this pin is DGND level. -If not used, please open this pin.	1	-															
D[17:0]	I/O	-D[17:0] are used as MCU parallel interface data bus. -D0 is the serial input/output signal in serial interface mode. -In serial interface, D[17:1] are not used and should be connected to VDDI or DGND.	18	MCU															
TE	O	-Tearing effect output pin to synchronies MCU to frame rate, activated by S/W command. -When this pin is inactive, this pin is DGND level. -If not used, please open this pin.	1	MCU															

Note1. When in parallel mode, no use data pin must be connected to "1" or "0".

Note2. When CSX="1", there is no influence to the parallel and serial interface.

Note3. "1"="HIGH"= VDDI level, "0"="LOW"= DGND level.



## 6.3 Mode selection pin

Name	I/O	Description	Count	Connect pin
EXTC	I	-To use extended command set, please connect this pin to VDDI. -During normal operation, please open this pin (internal $R_{pull-down}=2M\Omega$ ).	1	VDDI/DGND
		<b>EXTC</b> Enable/disable modification of extend command		
		0                      Only use default command set		
1                      Use extended command set				
SRGB	I	-RGB arrangement selection pin for color filter design.	1	VDDI/DGND
		<b>SRGB</b> RGB arrangement		
		0                      S1, S2, S3 filter order = 'R', 'G', 'B'		
1                      S1, S2, S3 filter order = 'B', 'G', 'R'				
SMX	I	-Scanning direction of source output selection pin.	1	VDDI/DGND
		<b>SMX</b> Scanning direction of source output		
		0                      S1->S528		
1                      S528->S1				
SMY	I	-Scanning direction of gate output selection pin.	1	VDDI/DGND
		<b>SMY</b> Scanning direction of gate output		
		0                      G1->G220		
1                      G220->G1				
AUTO	I	-Please connect this pin to VDDI.	1	VDDI

## 6.4 Driver output pin

Name	I/O	Description	Count	Connect pin
S1 to S528	O	- Source driver output pins.	528	-
G1 to G220	O	- Gate driver output pins.	220	-
VCI1	I/O	- A reference voltage for step-up circuit 1. - Connect a capacitor for stabilization.	4	Capacitor
AVDD	I	- Power input pin for analog circuits. - In normal usage, connect it to AVDDO.	4	AVDDO
AVDDO	O	- Output of step-up circuit 1 - Connect a capacitor for stabilization.	4	Capacitor
VCL	I	- Power input pin for VCOM circuit. - In normal usage, connect it to VCLO.	3	VCLO
VCLO	O	- A power output pin of step-up circuit 4. - When VCOML is higher than AGND, VCLO=AGND. - Connect a capacitor for stabilization.	1	Capacitor
VGH	I	- Power input pin for gate driver circuit. - In normal usage, connect it to VGHO.	2	VGHO
VGHO	O	- Positive output pin of the step-up circuit 2. - Connect a capacitor for stabilization.	1	Capacitor
VGL	I	- Power input pin for gate driver circuit. - Negative output of the step-up circuit 2 is connected inside the driver. - Connect a capacitor for stabilization.	3	VGLO
VREF	O	- A reference voltage for power system. - Connect a capacitor for stabilization.	1	Capacitor
GVDD	O	- A power output of grayscale voltage generator. - Connect a capacitor for stabilization. - When internal GVDD generator is not used, connect an external power supply (AVDD-0.5V) to this pin.	2	Capacitor
VCOMH	O	- Positive voltage output of VCOM. - Connect a capacitor for stabilization.	4	Capacitor
VCOML	O	- Negative voltage output of VCOM. - Connect a capacitor for stabilization.	4	Capacitor
VCOM	O	- A power supply for the TFT-LCD common electrode.	6	Common electrode
C11P, C11N, C12P, C12N	O	- Capacitor connecting pins for step-up circuit 1 (for AVDDO)	16	Step-up Capacitor
C21P, C21N, C22P, C22N, C23P, C23N	O	- Capacitor connecting pins for step-up circuit 2 and 4 (for VGHO, VGLO, VCLO)	18	Step-up Capacitor
VDDIO	O	-VDDI voltage output level for monitoring.	6	-
DGND0	O	-DGND voltage output level for monitoring.	9	-
VCCO	O	-Monitoring pin of internal digital reference voltage. -Connect a capacitor for stabilization.	5	Capacitor

## 6.5 Test pin

Name	I/O	Description	Count	Connect pin
TEST	I	-Please connect this pin to DGND	19	DGND
TPI[3]~[0]	I	-Please open these pins.	4	Open
TPO[7]~[0]	O	-Please open these pins.	8	Open
Dummy	-	-These pins are dummy (have no function inside). -Can allow signal traces pass through these pads on TFT glass.	4	Open

## 7. Driver electrical characteristics

### 7.1 Absolute operation range

Item	Symbol	Rating	Unit
Supply voltage	VDD	- 0.3 ~ +4.6	V
Supply voltage (Logic)	VDDI	- 0.3 ~ +4.6	V
Supply voltage (Digital)	VCC	-0.3 ~ +4.6	V
Driver supply voltage	VGH-VGL	-0.3 ~ +30.0	V
Logic input voltage range	V <sub>IN</sub>	0.3 ~ VDDI + 0.3	V
Logic output voltage range	V <sub>O</sub>	0.3 ~ VDDI + 0.3	V
Operating temperature range	T <sub>OPR</sub>	-30 ~ +85	°C
Storage temperature range	T <sub>STG</sub>	-40 ~ +125	°C

Note: If one of the above items is exceeded its maximum limitation momentarily, the quality of the product may be degraded. Absolute maximum limitation, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range.

### 7.2 DC characteristic

Parameter	Symbol	Condition	Specification			Unit	Related Pins
			Min	TYP	Max		
<b>Power &amp; operation voltage</b>							
System voltage	VDD	Operating voltage	2.7	2.8	3.3	V	
Interface operation voltage	VDDI	I/O supply voltage	1.6	1.8	3.3	V	
Gate driver high voltage	VGH		10		16	V	
Gate driver low voltage	VGL		-13		-5.5	V	
Gate driver supply voltage		VGH-VGL	15.5		29.0	V	
<b>Input / Output</b>							
Logic-high input voltage	V <sub>IH</sub>		0.7VDDI		VDDI	V	Note 1
Logic-low input voltage	V <sub>IL</sub>		VSS		0.3VDDI	V	Note 1
Logic-high output voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1.0mA	0.8VDDI		VDDI	V	Note 1
Logic-low output voltage	V <sub>OL</sub>	I <sub>OL</sub> = +1.0mA	VSS		0.2VDDI	V	Note 1
Input leakage current	I <sub>IL</sub>	I <sub>OH</sub> = -1.0mA	-1		+1	uA	Note 1
<b>VCOM voltage</b>							
VCOM high voltage	VCOMH	Ccom=22nF	2.5		5.0	V	
VCOM low voltage	VCOML	Ccom=22nF	-2.5		0.0	V	
VCOM amplitude	VCOMAC	VCOMH-VCOML	4.0		6.0	V	
<b>Source driver</b>							
Gamma reference voltage	GVDD		3.0		5.0	V	
Source output settling time	T <sub>r</sub>	Below with 99% precision		25	30	us	Note 2
Output offset voltage	V <sub>OFSET</sub>				35	mV	Note 3

Note 1: VDDI=1.6 to 3.3V, VDD=2.7 to 3.3V, AGND=DGND=0V, T<sub>A</sub>=-25 °C

Note 2, Source channel loading= 10pF/channel, Gate channel loading=50pF/channel.

Note 3, The Max. value is between measured point of gamma setting value.

### 7.3 Power consumption

T<sub>a</sub>=25°C, Frame rate = 60Hz, the registers setting are IC default setting.

Operation mode	Inversion mode	Image	Current consumption	
			Typical	Maximum
			IDD+IDDI (mA)	IDD+IDDI (mA)
-Normal mode	One Line	Note 1	2.2	3.0
	One Line	Note 2	2.2	3.0
-Partial + Idle mode (40 lines)	One Line	Note 1	1.3	1.6
		Note 2	1.3	1.6
-Sleep-in mode	N/A	N/A	0.015	0.025

Notes:

1. All pixels black.
2. All pixels white.

Typical case:  
T<sub>A</sub> = 25 °C  
VDD = 2.8 V  
VDDI = 1.8 V

Worst case:  
T<sub>A</sub> = 25 °C  
VDD = 2.7~3.3V  
VDDI = 1.6~3.3V

## 8. Timing chart

### 8.1 Parallel interface characteristics(8080-series MCU interface): 18, 16, 9 or 8-bits bus

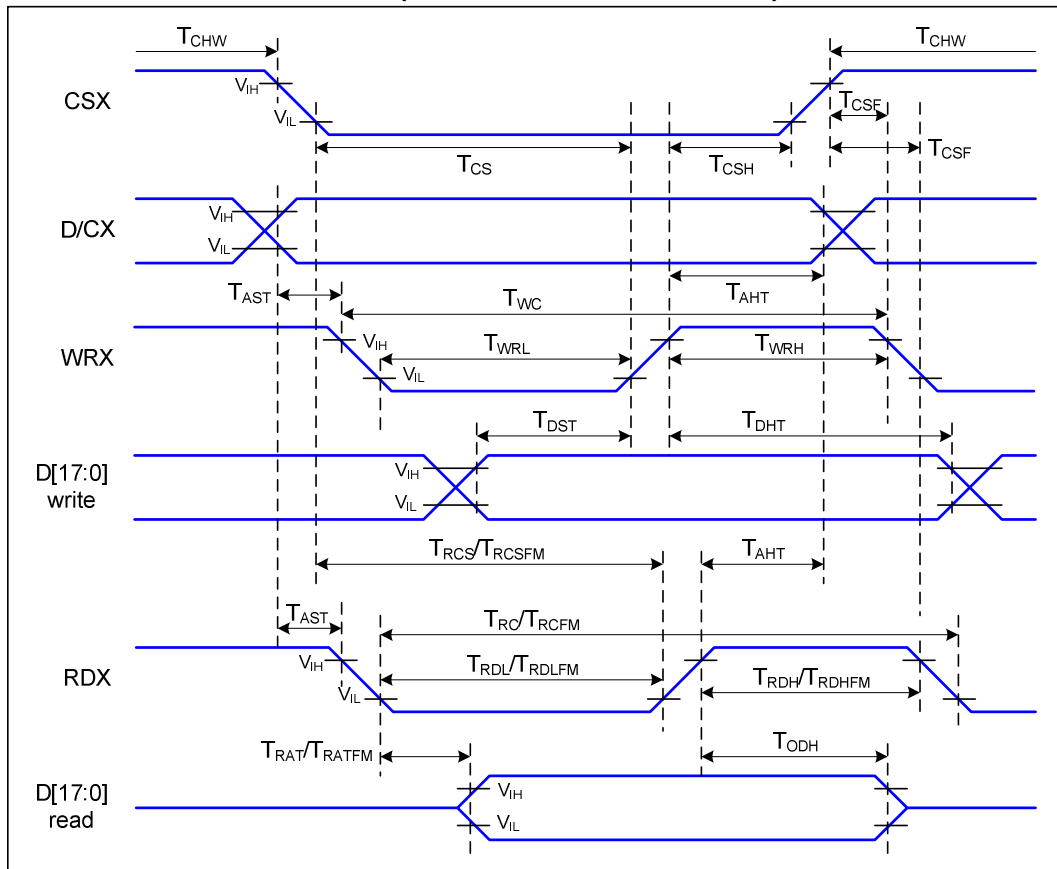


Fig. 8.1.1 Parallel interface timing characteristics (8080-series MCU interface)

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	$T_{AST}$	Address setup time	10		ns	-
	$T_{AHT}$	Address hold time (Write/Read)	15		ns	
CSX	$T_{CHW}$	Chip select "H" pulse width	0		ns	-(3-transfer for one pixel)
	$T_{CS}$	Chip select setup time (Write)	30		ns	
	$T_{RCS}$	Chip select setup time (Read ID)	150		ns	
	$T_{RCSFM}$	Chip select setup time (Read FM)	250		ns	
	$T_{CSF}$	Chip select wait time (Write/Read)	10		ns	
	$T_{CSH}$	Chip select hold time	10		ns	
WRX	$T_{WC}$	Write cycle	100		ns	10MHz
	$T_{WRH}$	Control pulse "H" duration	40		ns	
	$T_{WRL}$	Control pulse "L" duration	30		ns	
RDX (ID)	$T_{RC}$	Read cycle (ID)	160		ns	When read ID data
	$T_{RDH}$	Control pulse "H" duration (ID)	40		ns	
	$T_{RDL}$	Control pulse "L" duration (ID)	100		ns	
RDX (FM)	$T_{RCFM}$	Read cycle (FM)	400		ns	When read from frame memory
	$T_{RDHFM}$	Control pulse "H" duration (FM)	40		ns	
	$T_{RDLFM}$	Control pulse "L" duration (FM)	300		ns	
D[17:0]	$T_{DST}$	Data setup time	10		ns	For maximum $C_L=30pF$
	$T_{DHT}$	Data hold time	15		ns	
	$T_{RAT}$	Read access time (ID)		100	ns	
	$T_{RATFM}$	Read access time (FM)		100	ns	
	$T_{ODH}$	Output disable time	45	80	ns	

Note 1:  $V_{DD1}=1.6$  to  $3.3V$ ,  $V_{DD}=2.7$  to  $3.3V$ ,  $AGND=DGND=0V$ ,  $T_a=25^\circ C$

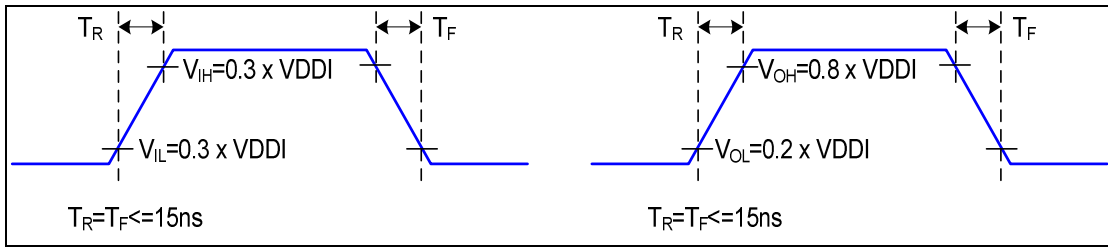


Fig. 8.1.2 Rising and falling timing for input and output signal

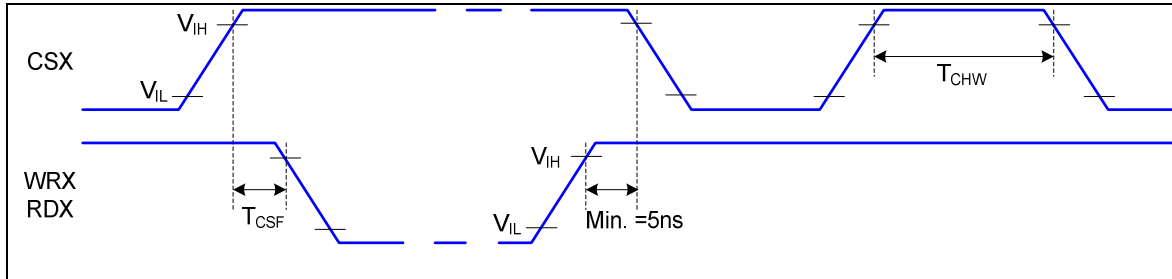


Fig.8.1.3 Chip selection (CSX) timing

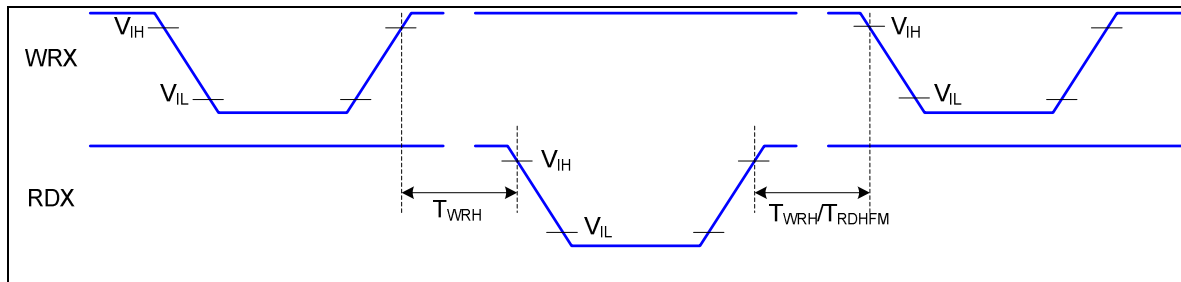


Fig. 8.1.4 Write-to-read and read-to-write timing

NOTE: The rising time and falling time ( $T_r$ ,  $T_f$ ) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

## 8.3 Serial interface characteristics (3-line serial)

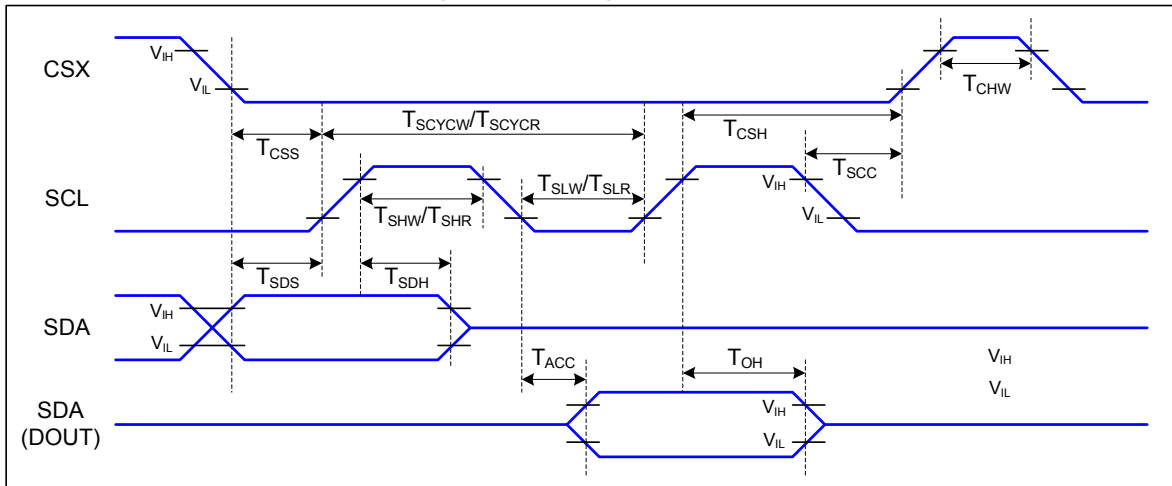


Fig. 8.3.1 3-line serial interface timing

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T <sub>CSS</sub>	Chip select setup time	60		ns	
	T <sub>CSH</sub>	Chip select hold time	60		ns	
	T <sub>SCC</sub>	Chip select setup time	10		ns	
	T <sub>CHW</sub>	Chip select hold time	10		ns	
SCL	T <sub>SCYCW</sub>	Serial clock cycle (Write)	65		ns	
	T <sub>SHW</sub>	SCL "H" pulse width (Write)	20		ns	
	T <sub>SLW</sub>	SCL "L" pulse width (Write)	40		ns	
	T <sub>SCYCR</sub>	Serial clock cycle (Read)	150		ns	
	T <sub>SHR</sub>	SCL "H" pulse width (Read)	60		ns	
	T <sub>SLR</sub>	SCL "L" pulse width (Read)	80		ns	
SDA (DIN) (DOUT)	T <sub>SDS</sub>	Data setup time	10		ns	For maximum CL=30pF
	T <sub>SDH</sub>	Data hold time	15		ns	
	T <sub>ACC</sub>	Access time		80	ns	
	T <sub>OH</sub>	Output disable time	45	80	ns	

Table 8.3: 3-line Serial Interface Characteristics

Note 1: VDDI=1.6 to 3.3V, VDD=2.7 to 3.3V, AGND=DGND=0V, Ta=25°C

Note 2: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

## 9. Function description

### 9.1 Interface type selection

The selection of given interfaces are done by setting IM2, IM1, and IM0 pins as shown in following table.

Table 9.1.1 Selection of MCU interface

IM2	IM1	IM0	Interface	Read back selection
0	-	-	3-line serial interface	Via the read instruction
1	0	0	8080 MCU 8-bit parallel	RDX strobe (8-bit read data and 8-bit read parameter)
1	0	1	8080 MCU 16-bit parallel	RDX strobe (16-bit read data and 8-bit read parameter)
1	1	0	8080 MCU 9-bit parallel	RDX strobe (9-bit read data and 8-bit read parameter)
1	1	1	8080 MCU 18-bit parallel	RDX strobe (18-bit read data and 8-bit read parameter)

Table 9.1.2 Pin connection according to various MCU interface

IM2	IM1	IM0	Interface	RDX	WRX	D/CX	Read back selection
0	-	-	3-line serial interface	Note1	Note1	SCL	D[17:1]: unused, D0: SDA
1	0	0	8080 8-bit parallel	RDX	WRX	D/CX	D[17:8]: unused, D7-D0: 8-bit data
1	0	1	8080 16-bit parallel	RDX	WRX	D/CX	D[17:16]: unused, D15-D0: 16-bit data
1	1	0	8080 9-bit parallel	RDX	WRX	D/CX	D[17:9]: unused, D8-D0: 9-bit data
1	1	1	8080 18-bit parallel	RDX	WRX	D/CX	D17-D0: 18-bit data

Note 1. Unused pins must be connected to DGND or VDDI.

### 9.2 Write cycle sequence

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control signals (D/CX, RDX, WRX) and data signals (D[17:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (=‘0’) and vice versa it is data (=‘1’).

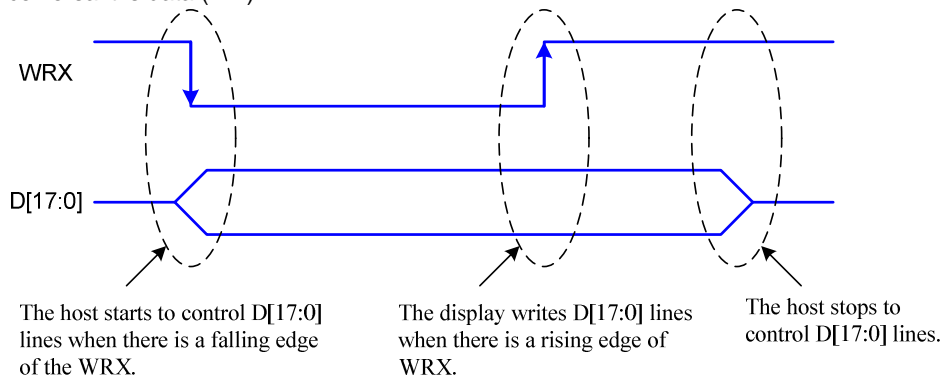


Fig. 9.2.1 8080-series WRX protocol

Note: WRX is an unsynchronized signal (It can be stopped).

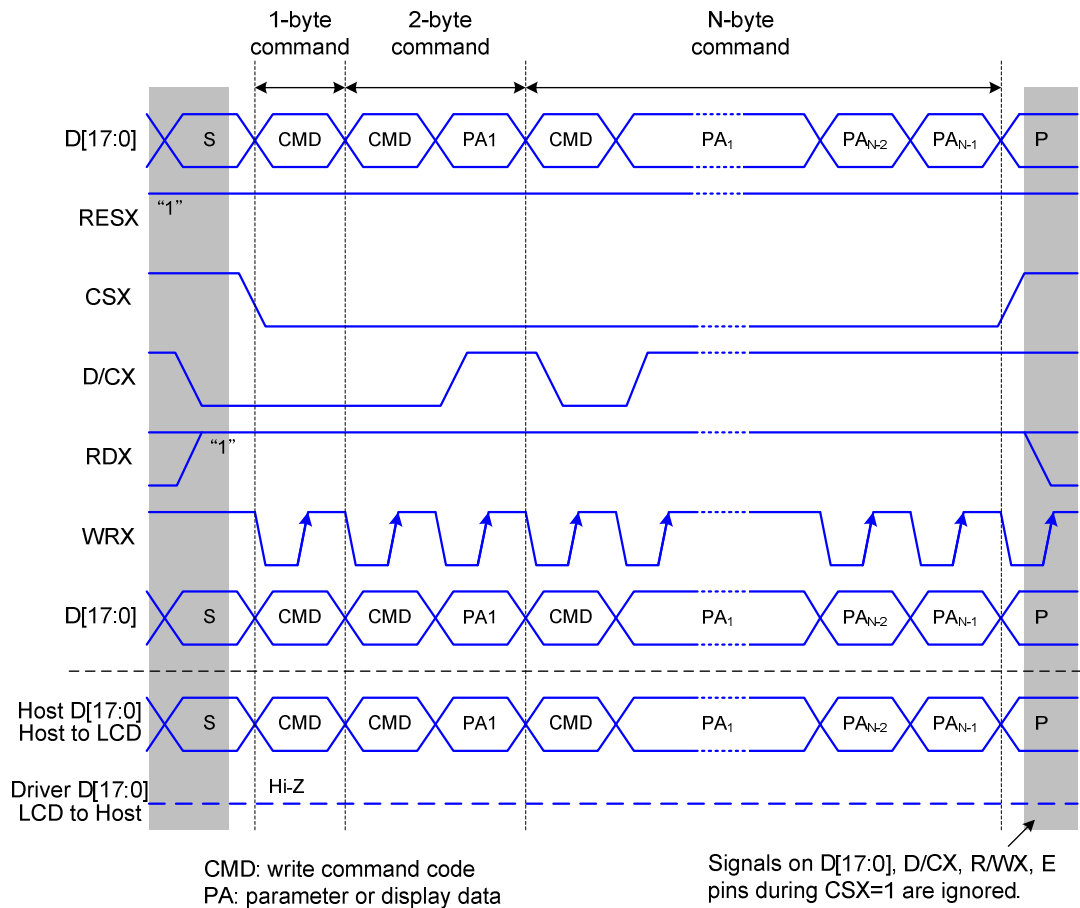


Fig. 9.2.2 8080-series parallel bus protocol, write to register or display RAM

### 9.3 Read cycle sequence

The read cycle (RDX high-low-high sequence) means that the host reads information from LCD driver via interface. The driver sends data (D[17:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

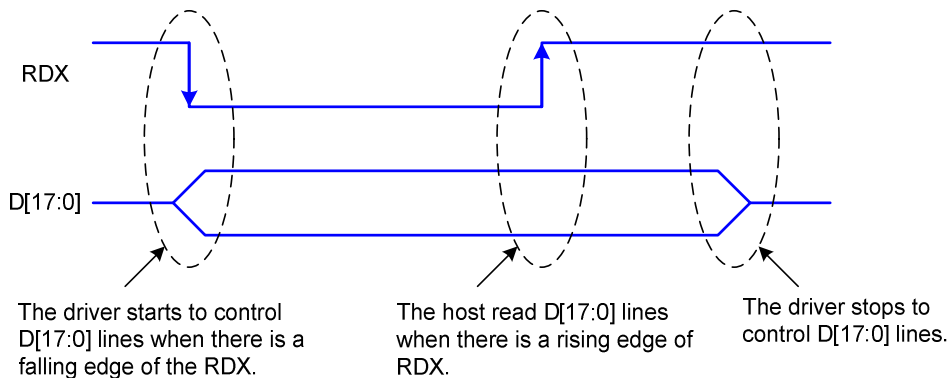


Fig. 9.2.3 8080-series RDX protocol

Note: RDX is an unsynchronized signal (It can be stopped).



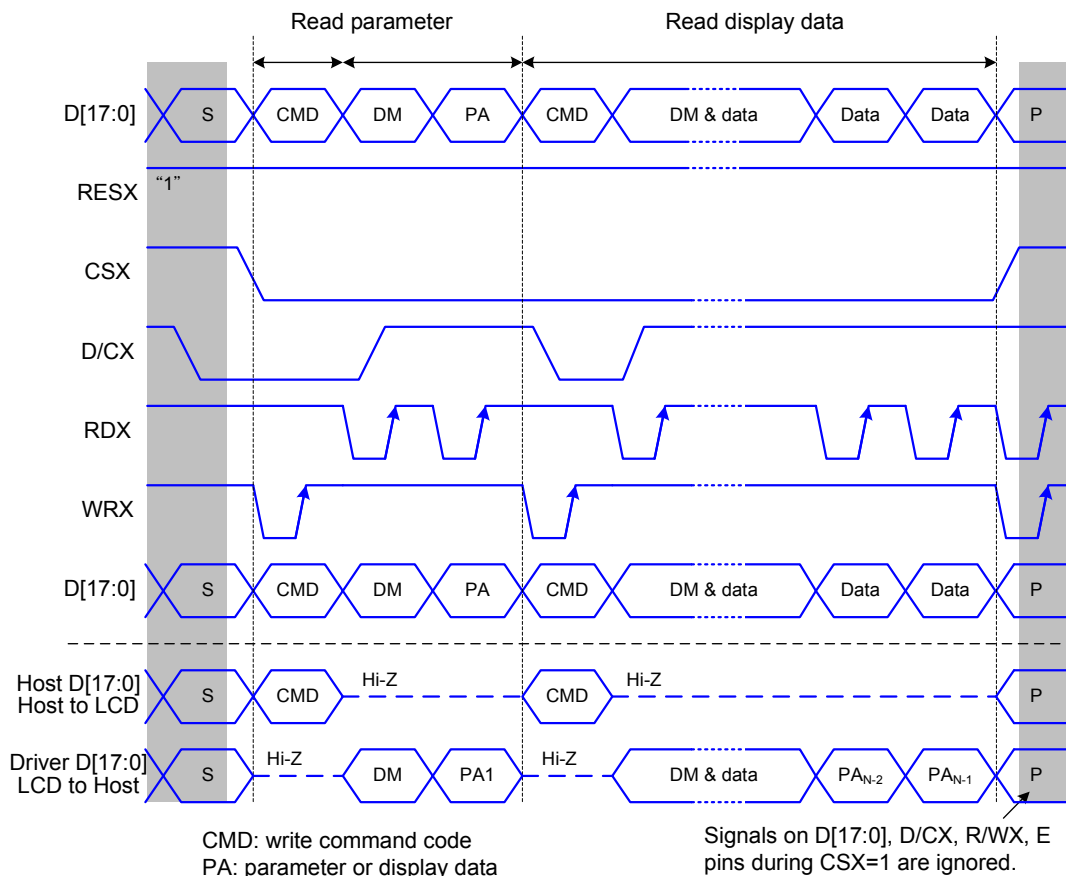


Fig. 9.2.4 8080-series parallel bus protocol, read data from register or display RAM

## 9.4 Serial interface

The selection of this interface is done by IM2="Low".

The serial interface is either 3-lines/9-bits bi-directional interface for communication between the micro controller and the LCD driver. The 3-lines serial interface use: CSX (chip enable), SCL (serial clock) and SDA (serial data input/output), Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

### 9.4.1 Command Write Mode

The write mode of the interface means the micro controller writes commands and data to the LCD driver. 3-lines serial data packet contains a control bit D/CX and a transmission byte. Any instruction can be sent in any order to the driver. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

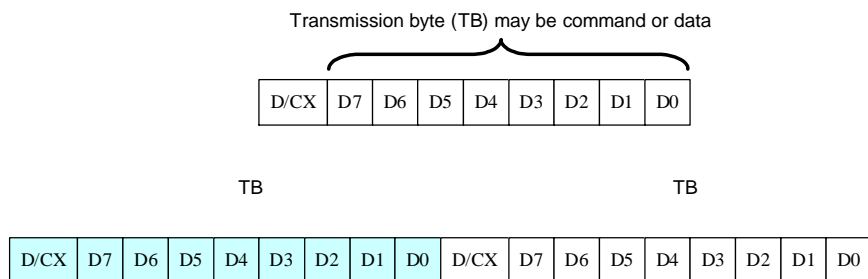


Fig. 9.4.1 Serial interface data stream format

When CSX is "high", SCL clock is ignored. During the high period of CSX the serial interface is initialized. At the falling edge of CSX, SCL can be high or low (see Fig 9.4.2). SDA is sampled at the rising edge of SCL. D/CX indicates whether the byte is command (D/CX='0') or parameter/RAM data (D/CX='1'). D/CX is sampled when first rising edge of SCL. If CSX stays low after the last bit of command/data byte, the serial interface expects the D/CX bit of the next byte at the next rising edge of SCL.

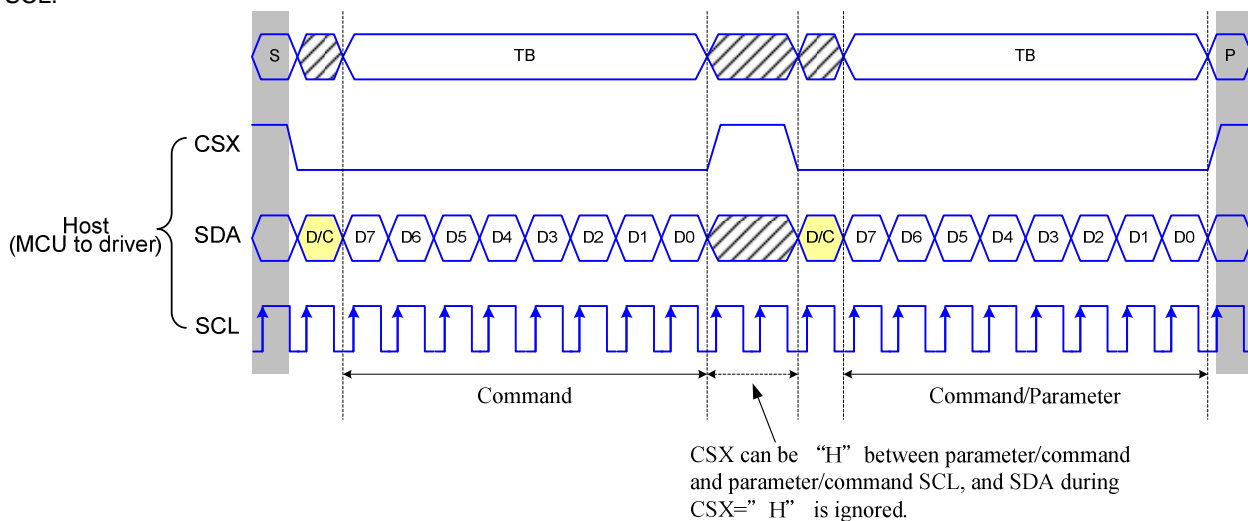


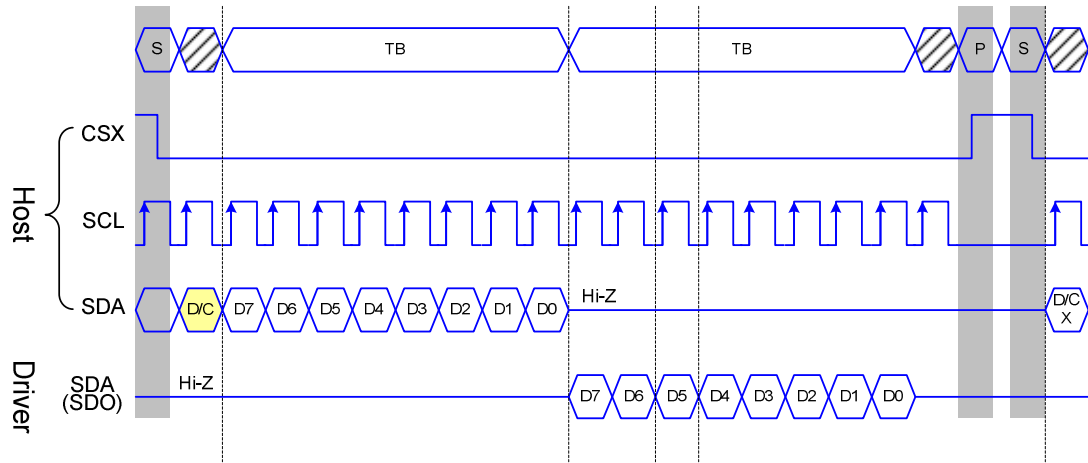
Fig. 9.4.2 3-line serial interface write protocol (write to register with control bit in transmission)

### 9.4.2 Read Functions

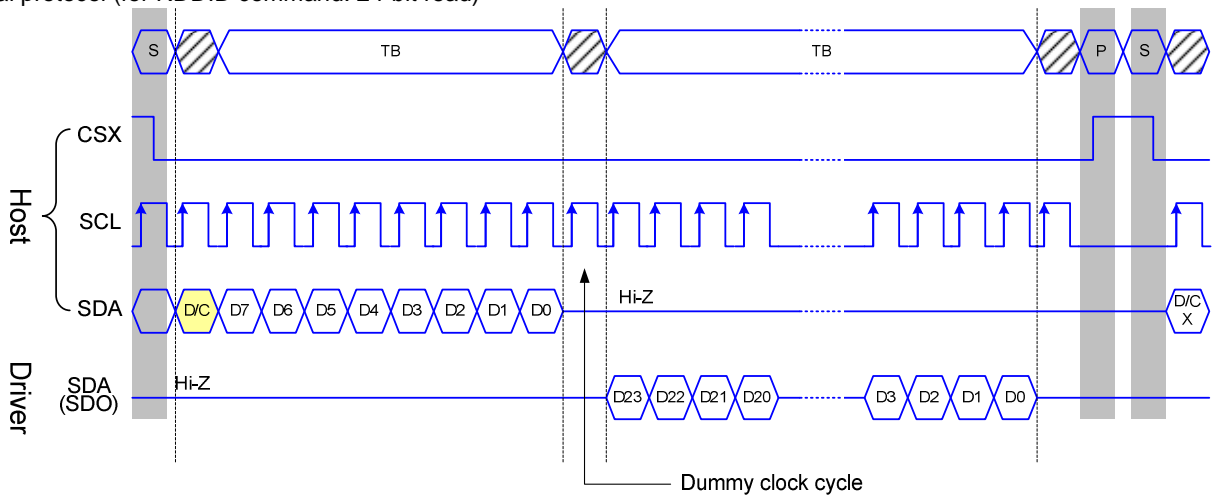
The read mode of the interface means that the micro controller reads register value from the driver. To achieve read function, the micro controller first has to send a command (read ID or register command) and then the following byte is transmitted in the opposite direction. After that CSX is required to go to high before a new command is send (see the below figure). The driver samples the SDA (input data) at rising edge of SCL, but shifts SDA (output data) at the falling edge of SCL. Thus the micro controller is supported to read at the rising edge of SCL.

After the read status command has been sent, the SDA line must be set to tri-state no later than at the falling edge of SCL of the last bit.

Serial protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read):



Serial protocol (for RDDID command: 24-bit read)



Serial Protocol (for RDDST command: 32-bit read)

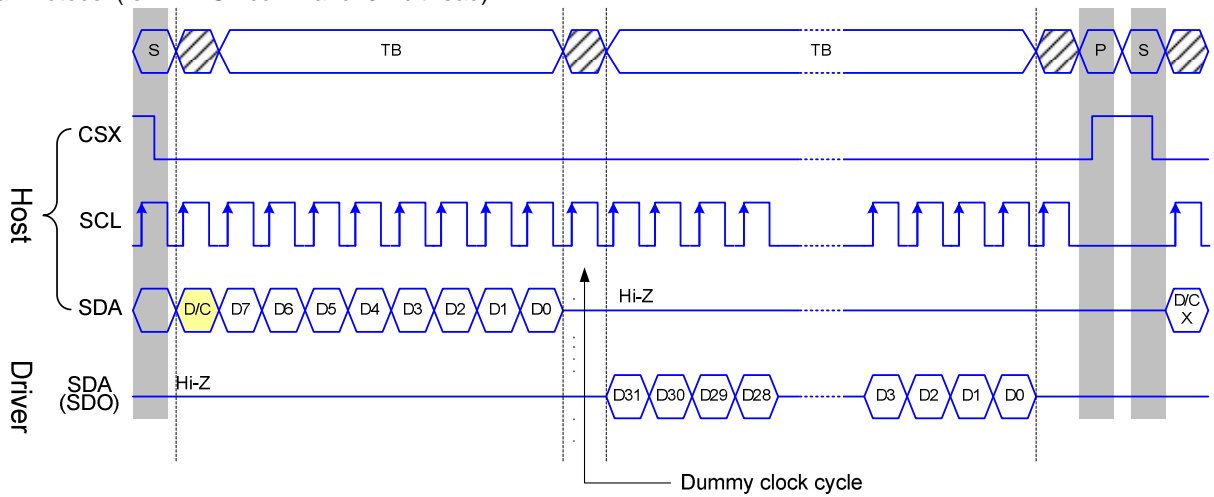


Fig. 9.4.4 3-line serial interface read protocol

9.5 Data Transfer Break and Recovery

If there is a break in data transmission by RESX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select line (CSX) is next activated after RESX have been HIGH state. See the following example

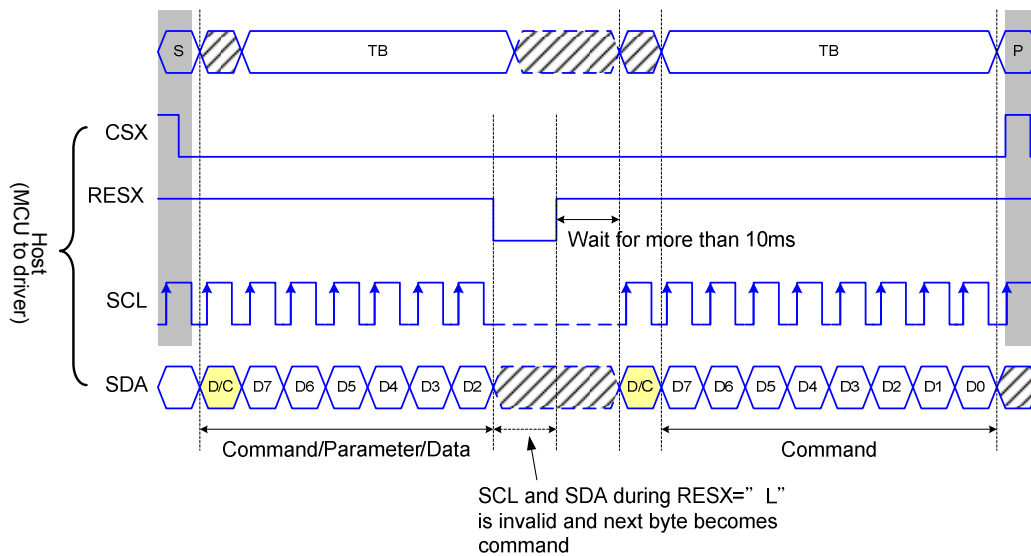


Fig. 9.5.1 Serial bus protocol, write mode - interrupted by RESX

If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated. See the following example

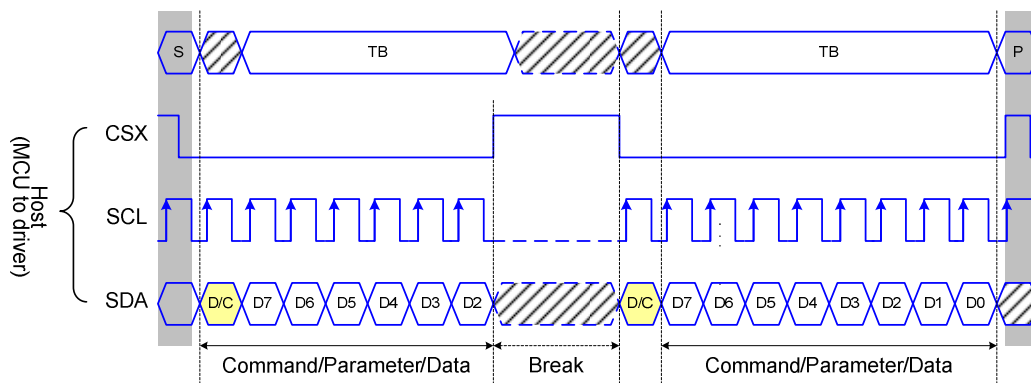


Fig. 9.5.2 Serial bus protocol, write mode - interrupted by CSX

If 1, 2 or more parameter commands are being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.

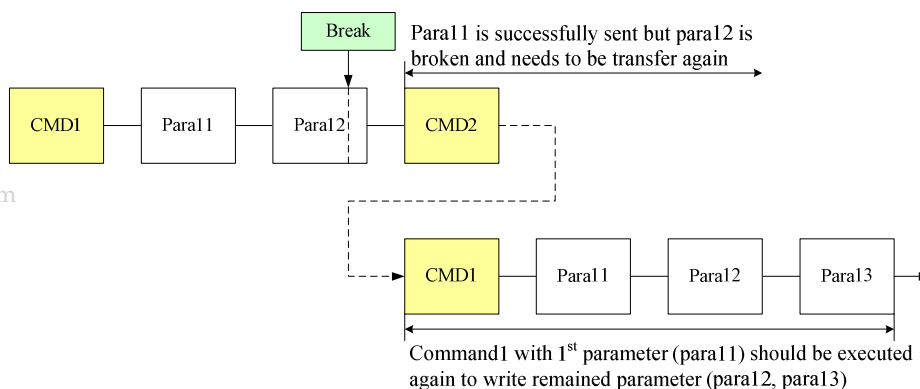


Fig.9.5.3 Write interrupts recovery (serial interface)

If a 2 or more parameter commands are being sent and a break occurs by the other command before the last one is sent, then the parameters that were successfully sent are stored and the other parameter of that command remains previous value.

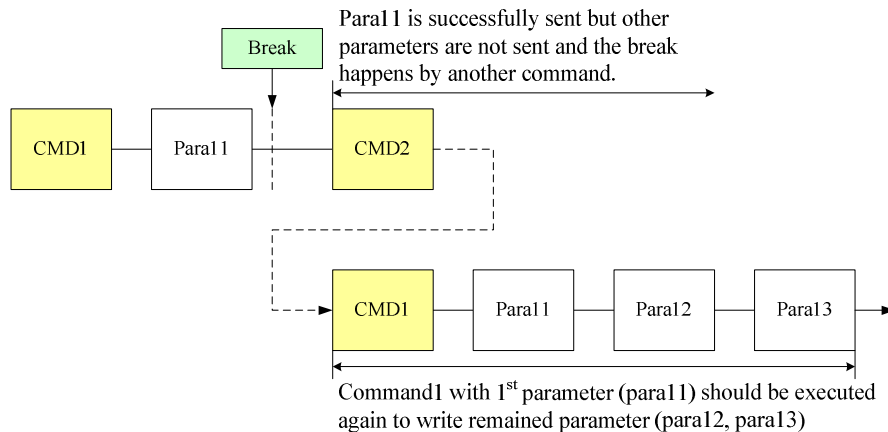


Fig. 9.5.4 Write interrupts recovery (both serial and parallel Interface)

### 9.6 Data transfer pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select line is released after a whole byte of a frame memory data or multiple parameter data has been completed, then driver will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select Line is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters (if appropriate) or a new command when the chip select line is next enabled as shown below.

This applies to the following 4 conditions:

- 1) Command-Pause-Command
- 2) Command-Pause-Parameter
- 3) Parameter-Pause-Command
- 4) Parameter-Pause-Parameter

#### 9.6.1 Serial interface pause

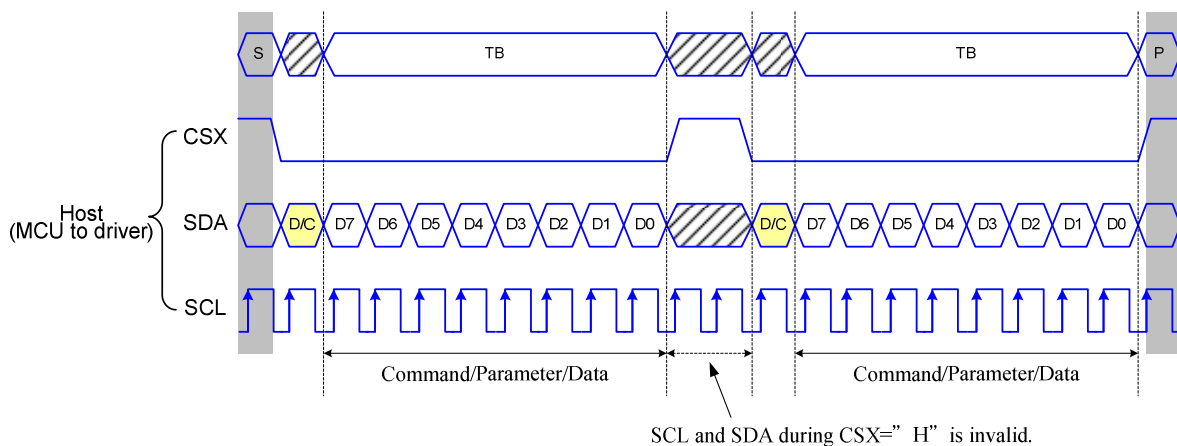


Fig. 9.6.1 Serial interface pause protocol (pause by CSX)

## 9.6.2 Parallel interface pause

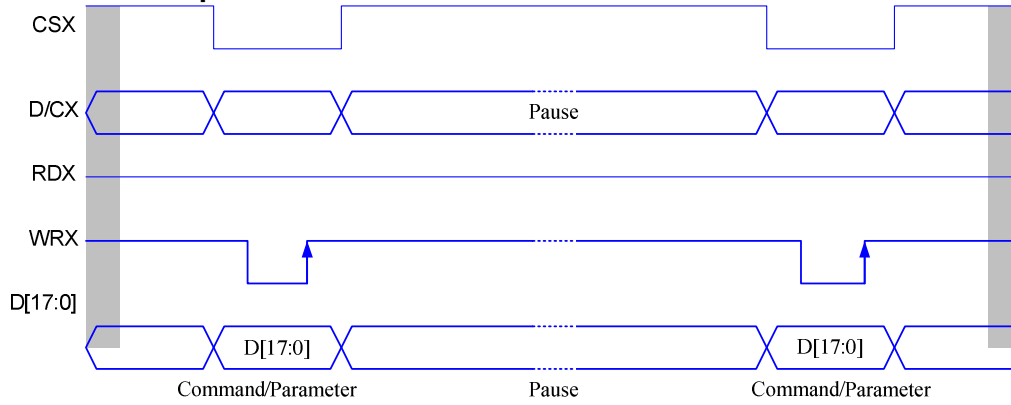


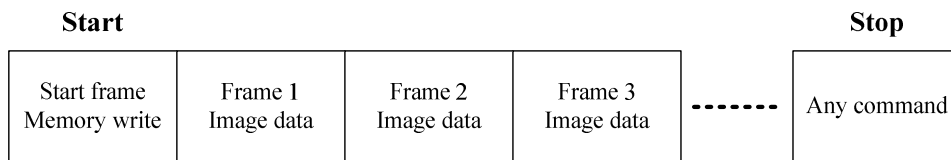
Fig. 9.6.2 Parallel bus pause protocol (paused by CSX)

## 9.7 Data Transfer Modes

The module has three kinds color modes for transferring data to the display RAM. These are 12-bits color per pixel, 16-bits color per pixel and 18-bits color per pixel. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

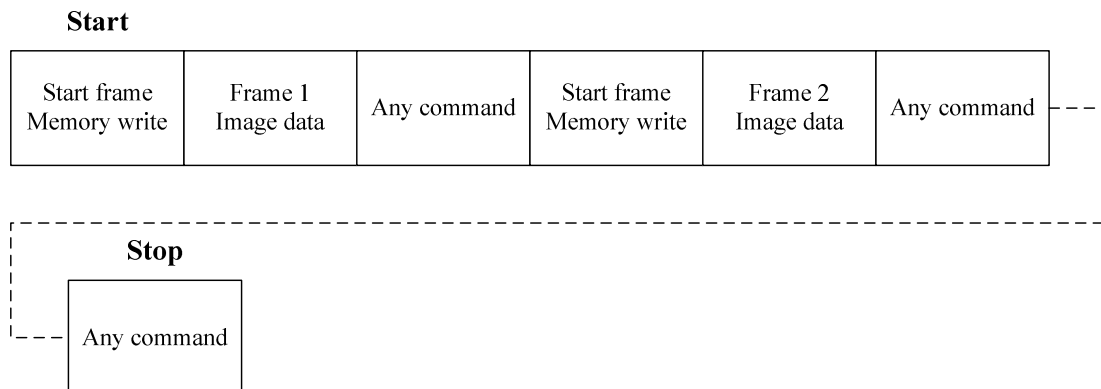
### 9.7.1 Method 1

The Image data is sent to the frame memory in successive frame writes, each time the frame memory is filled, the frame memory pointer is reset to the start point and the next frame is written.



### 9.7.2 Method 2

Image data is sent and at the end of each frame memory download, a command is sent to stop frame memory write. Then start memory write command is sent, and a new frame is downloaded.



Note:

- 1) These apply to all data transfer Color modes on both serial and parallel interfaces.
- 2) The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

## 9.8 Data Color Coding

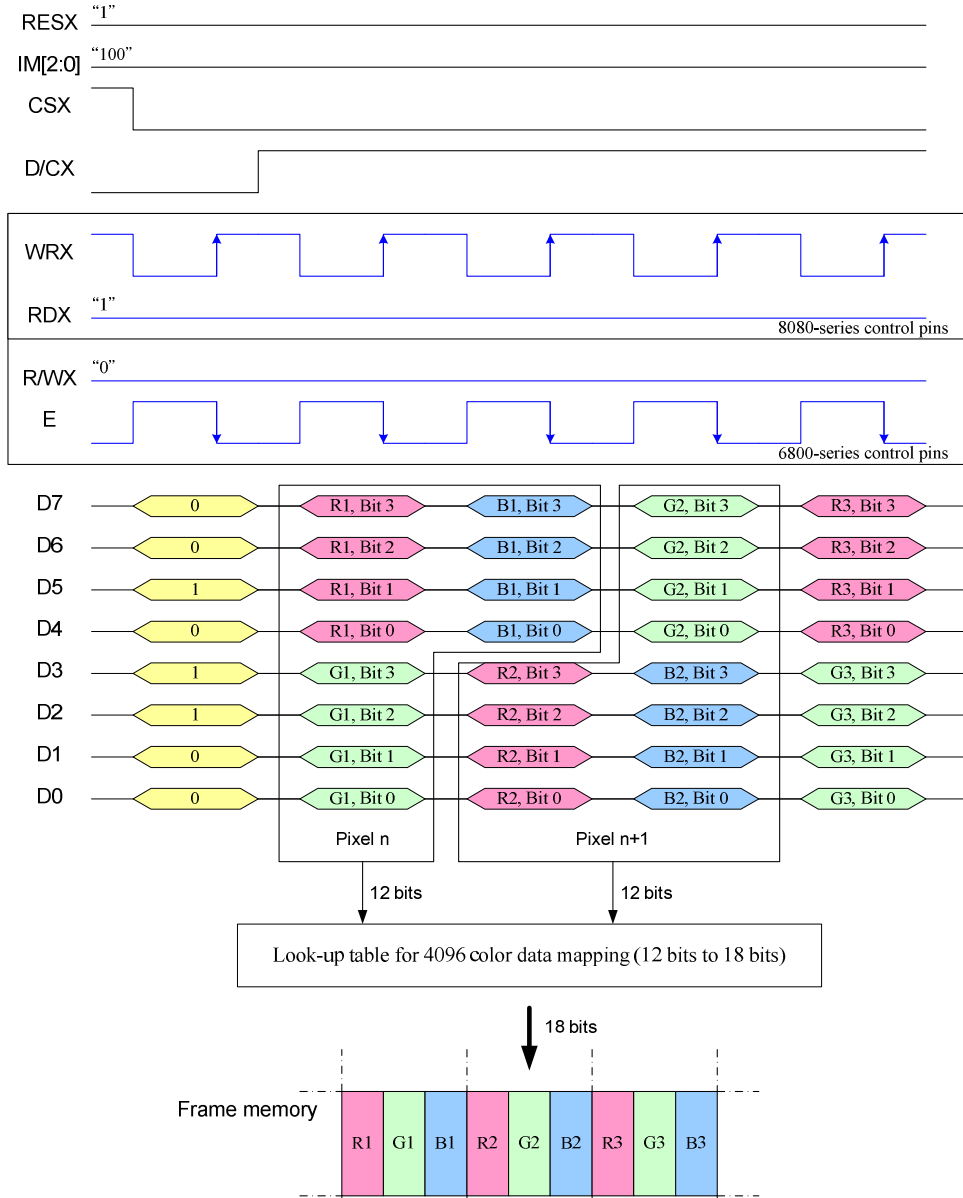
### 9.8.1 8-bit Parallel Interface (IM2, IM1, IM0= "100")

Different display data formats are available for three Colors depth supported by listed below.

- 4k Colors, RGB 4,4,4-bit input,
- 65k Colors, RGB 5,6,5-bit input,
- 262k Colors, RGB 6,6,6-bit input,

#### 9.8.1.1 8-bit data bus for 12-bit/pixel (RGB 4-4-4-bit input), 4K-Colors, 3AH= "03h"

There are 2 pixels (6 sub-pixels) per 3-bytes.



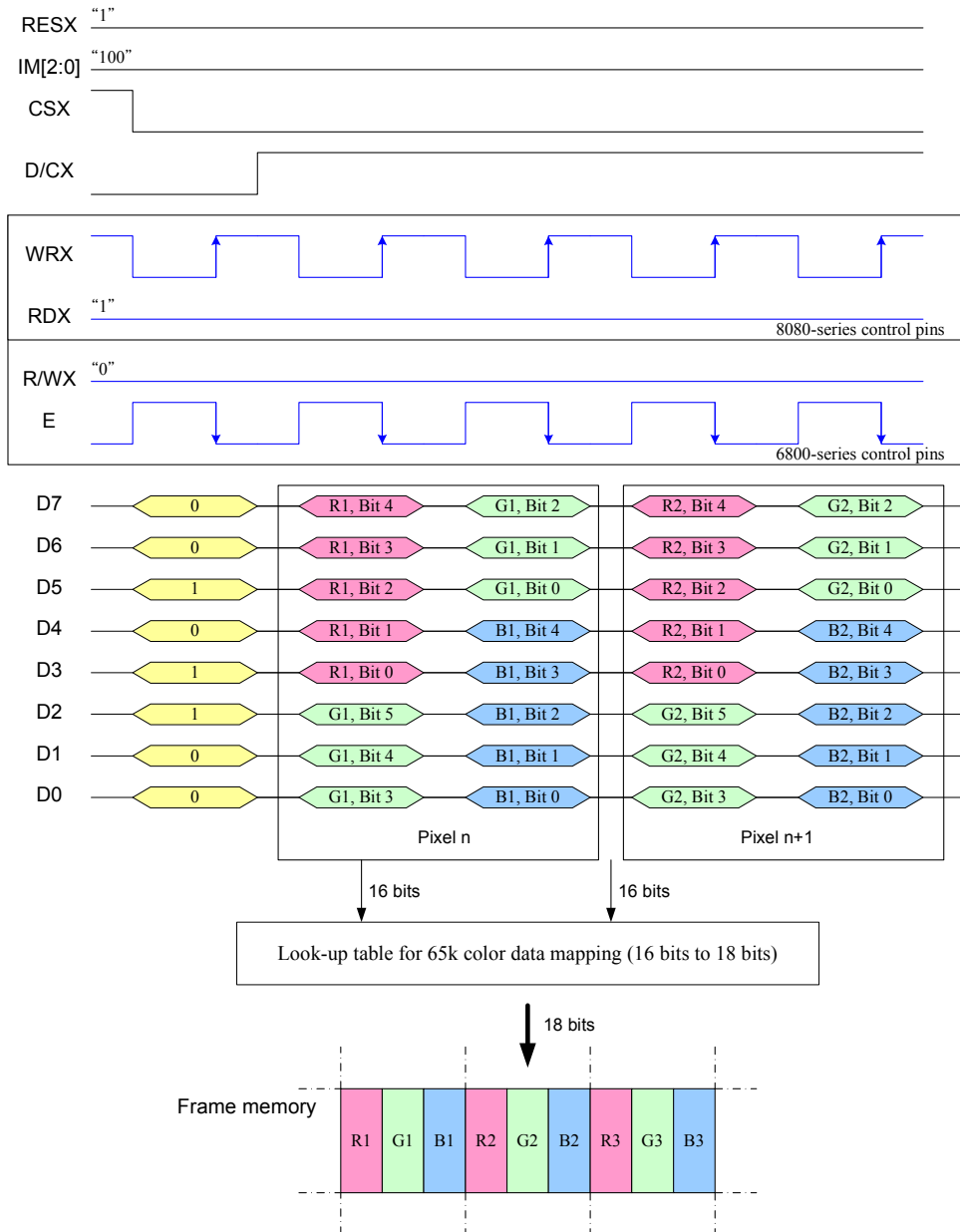
Note 1. The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.

Note 2. 3-time transfer is used to transmit 1 pixel data with the 12-bit color depth information.

Note 3. '-' = Don't care - Can be set to '0' or '1'

## 9.8.1.2 8-bit data bus for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3AH= "05h"

There is 1 pixel (3 sub-pixels) per 2-bytes.



Note 1. The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

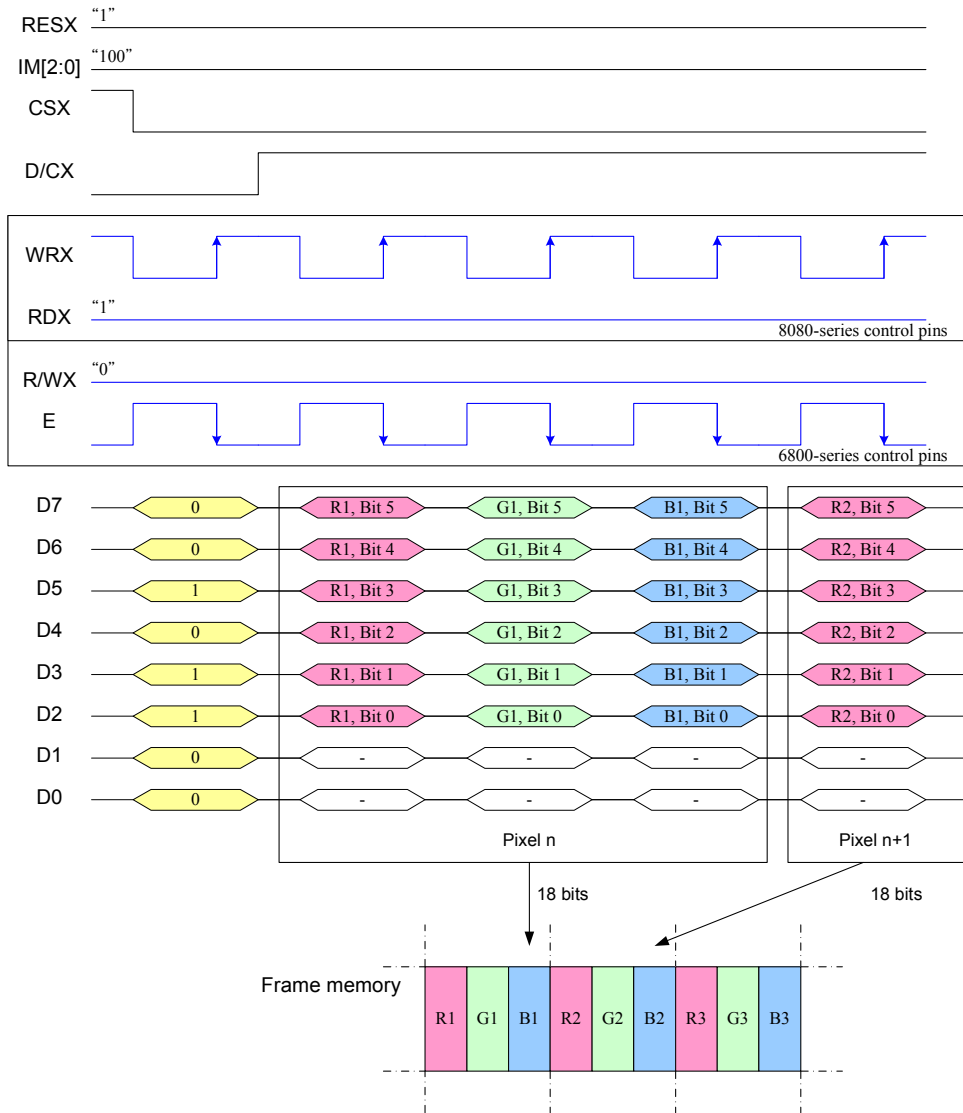
Note 2. 2-times transfer is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3. '-' = Don't care - Can be set to '0' or '1'



## 9.8.1.3 8-bit data bus for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3AH= "06h"

There is 1 pixel (3 sub-pixels) per 3-bytes.



Note 1. The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2. 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3. '-' = Don't care - Can be set to '0' or '1'

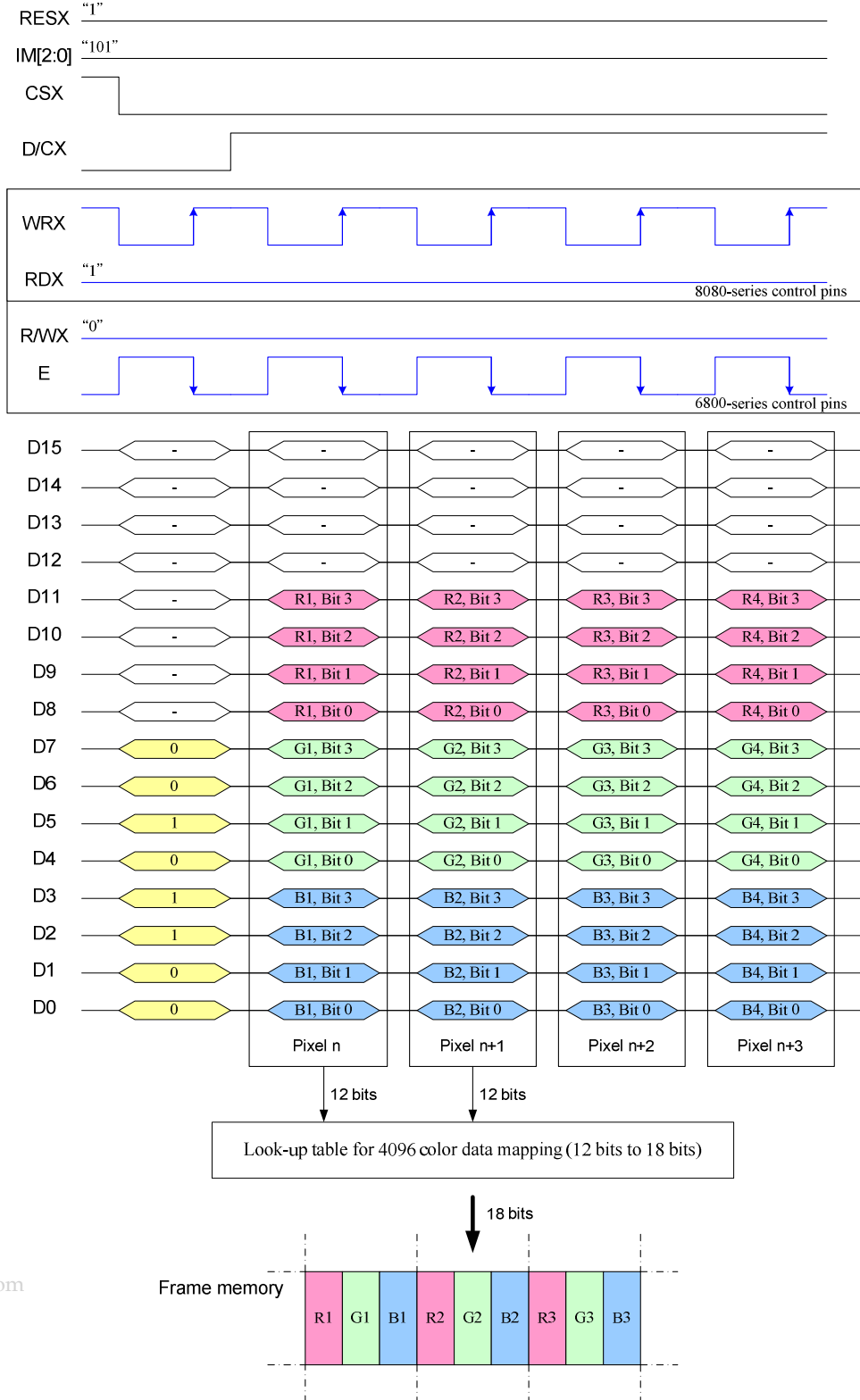
## 9.8.2 16-Bit Parallel Interface (IM2,IM1, IM0= "101")

Different display data formats are available for three colors depth supported by listed below.

- 4k colors, RGB 4,4,4-bit input
- 65k colors, RGB 5,6,5-bit input
- 262k colors, RGB 6,6,6-bit input

### 9.8.2.1 16-bit data bus for 12-bit/pixel (RGB 4-4-4-bit input), 4K-Colors, 3AH= "03h"

There is 1 pixel (3 sub-pixels) per 1 bytes, 12-bit/pixel.

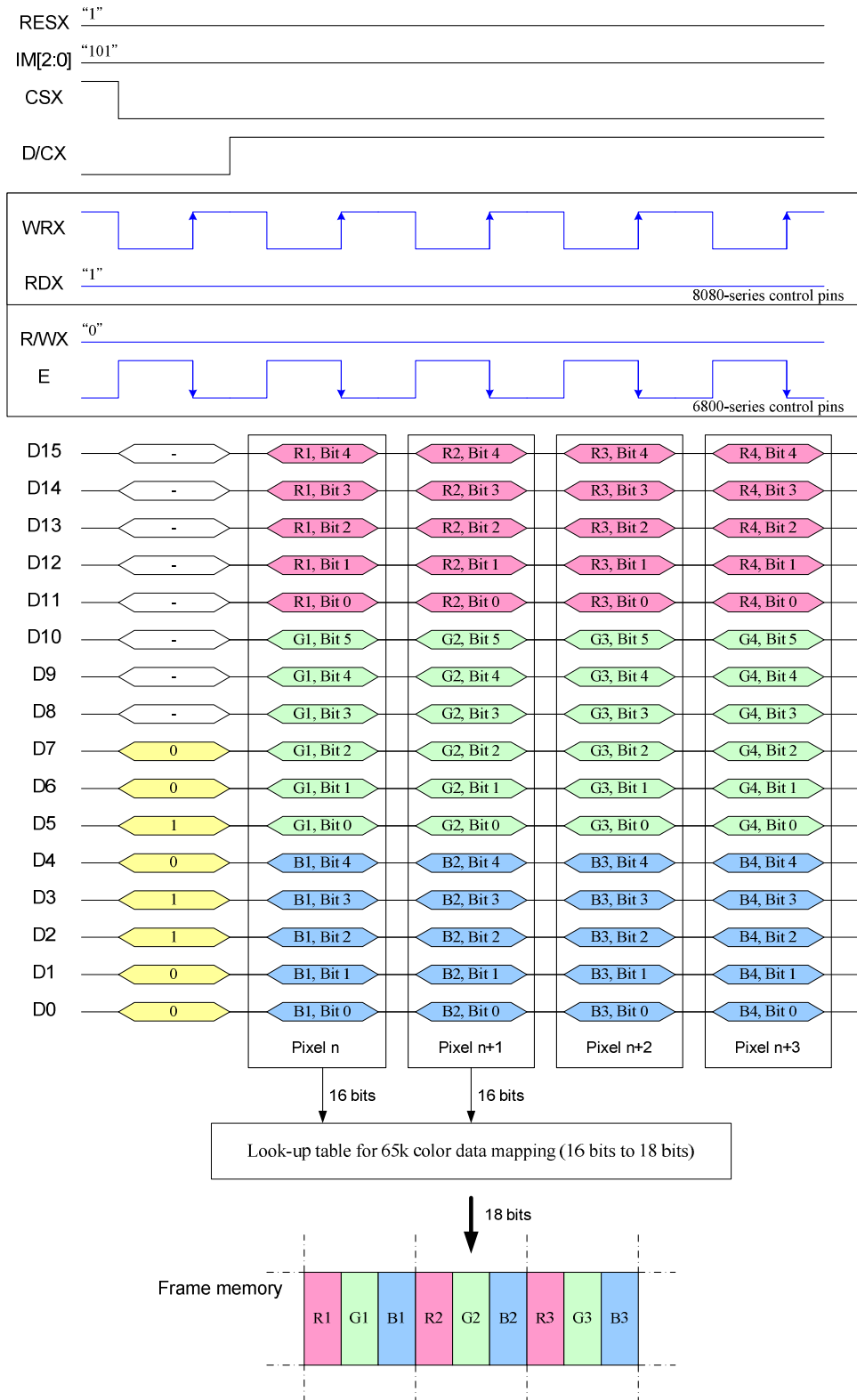


Note1. The data order is as follows, MSB=D11, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.

Note 2. 1-times transfer (D11 to D0) is used to transmit 1 pixel data with the 12-bit color depth information.

## 9.8.2.2 16-bit data bus for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3AH= "05h"

There is 1 pixel (3 sub-pixels) per 1 bytes, 16-bit/pixel.



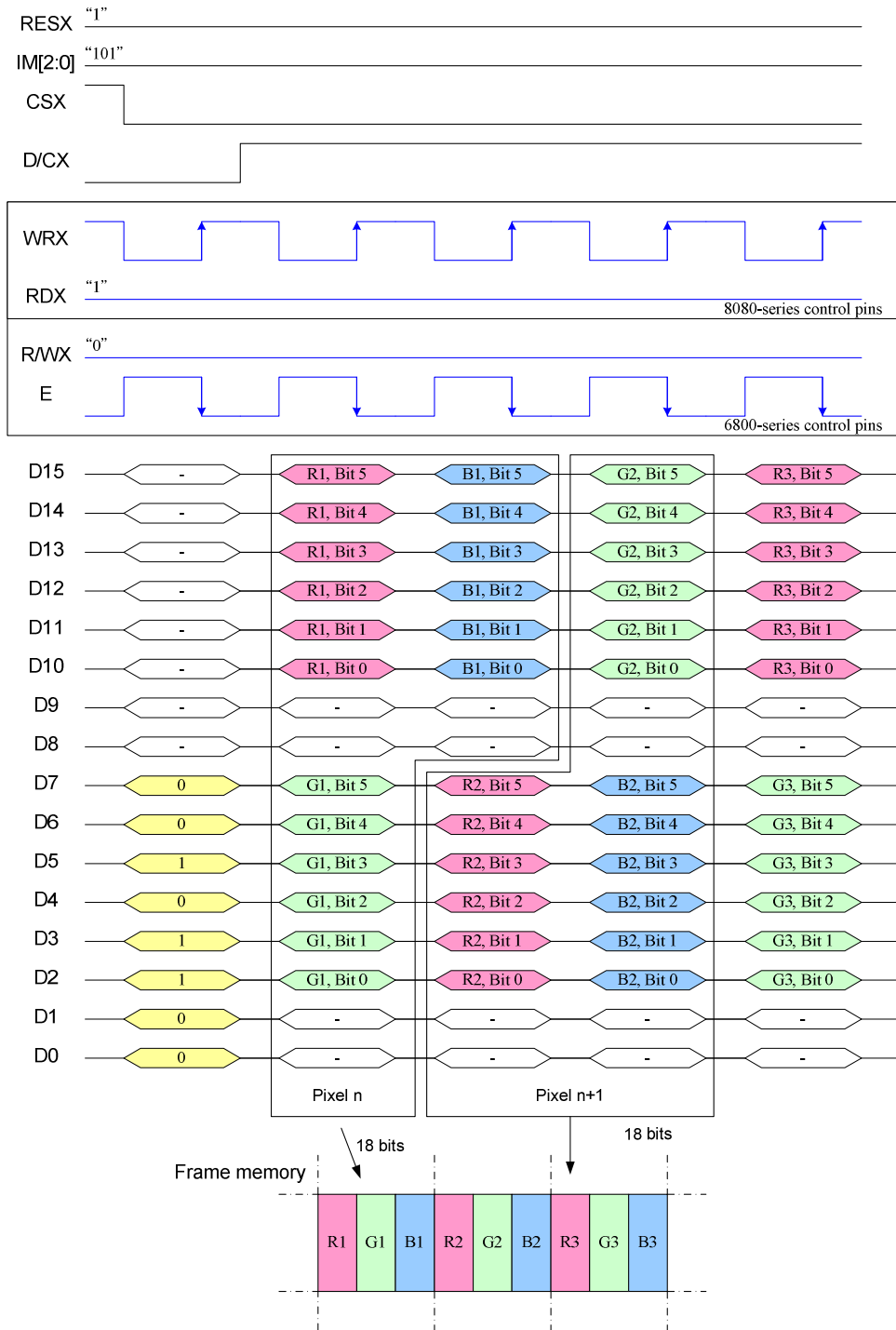
*Note 1. The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.*

*Note 2. 1-times transfer (D15 to D0) is used to transmit 1 pixel data with the 16-bit color depth information.*

*Note 3. '-' = Don't care - Can be set to '0' or '1'*

## 9.8.2.3 16-bit data bus for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3AH= "06h"

There are 2 pixel (6 sub-pixels) per 3 bytes, 18-bit/pixel.



Note 1. The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

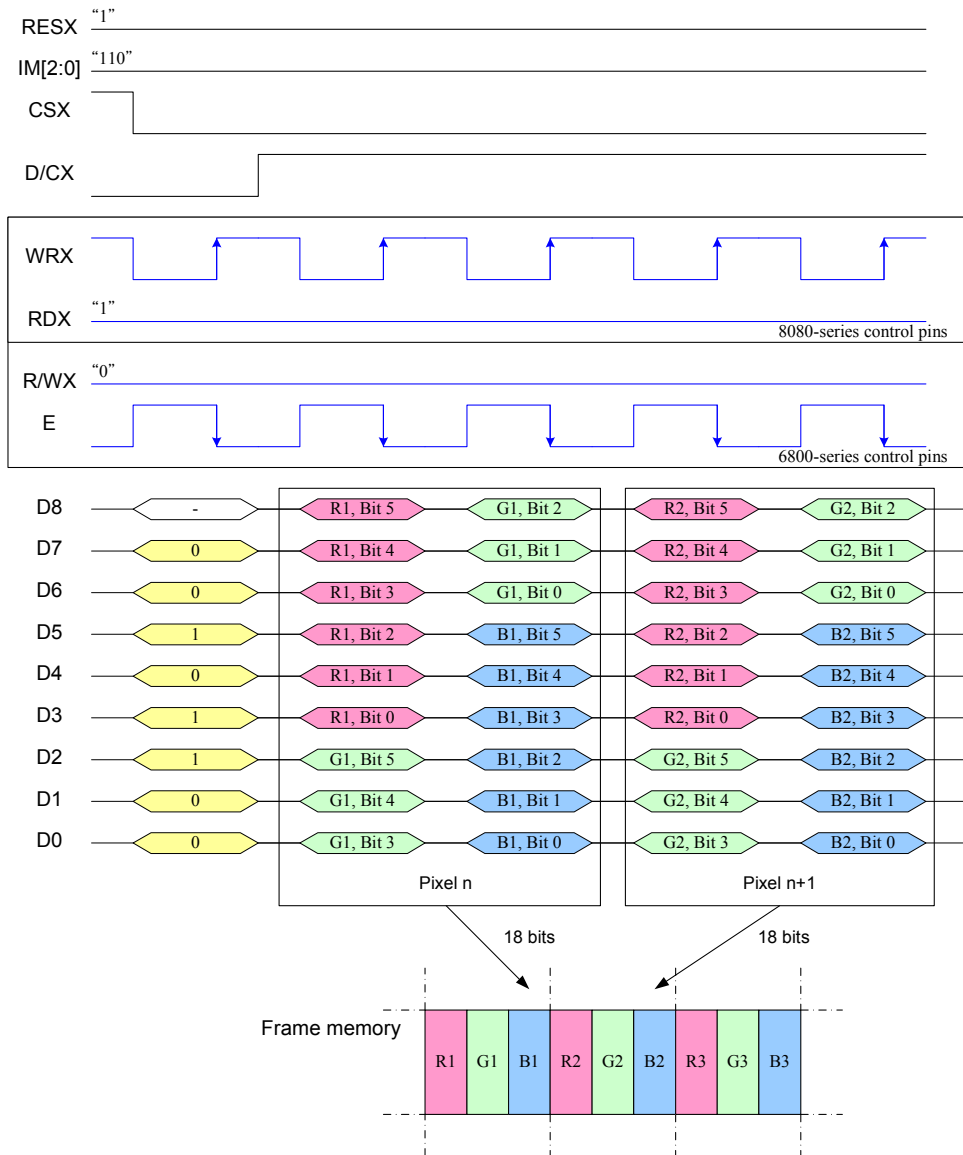
Note 2. 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3. '-' = Don't care - Can be set to '0' or '1'

## 9.8.3 9-Bit Parallel Interface (IM2, IM1, IM0="110")

Different display data formats are available for three colors depth supported by listed below.

- 262k colors, RGB 6,6,6-bit input



Note 1. The data order is as follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2. 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3. '-' = Don't care - Can be set to '0' or '1'

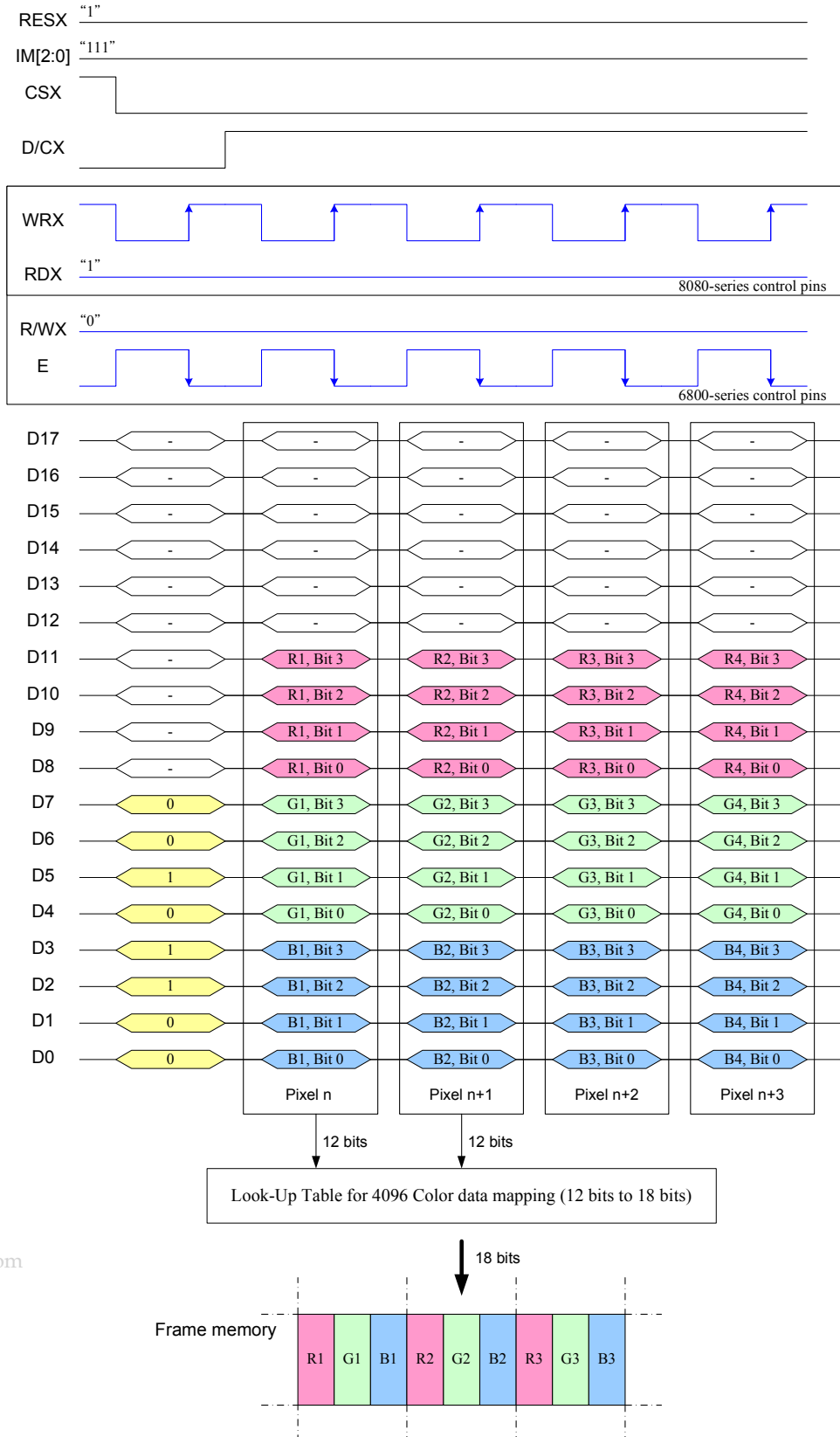
## 9.8.4 18-Bit Parallel Interface (IM2, IM1, IM0="111")

Different display data formats are available for three colors depth supported by listed below.

- 4k colors, RGB 4,4,4-bit input
- 65k colors, RGB 5,6,5-bit input
- 262k colors, RGB 6,6,6-bit input.

### 9.8.4.1 18-bit data bus for 12-bit/pixel (RGB 4-4-4-bit input), 4K-Colors, 3AH="03h"

There are 1 pixel (3 sub-pixels) per 1 byte, 12-bit/pixel.

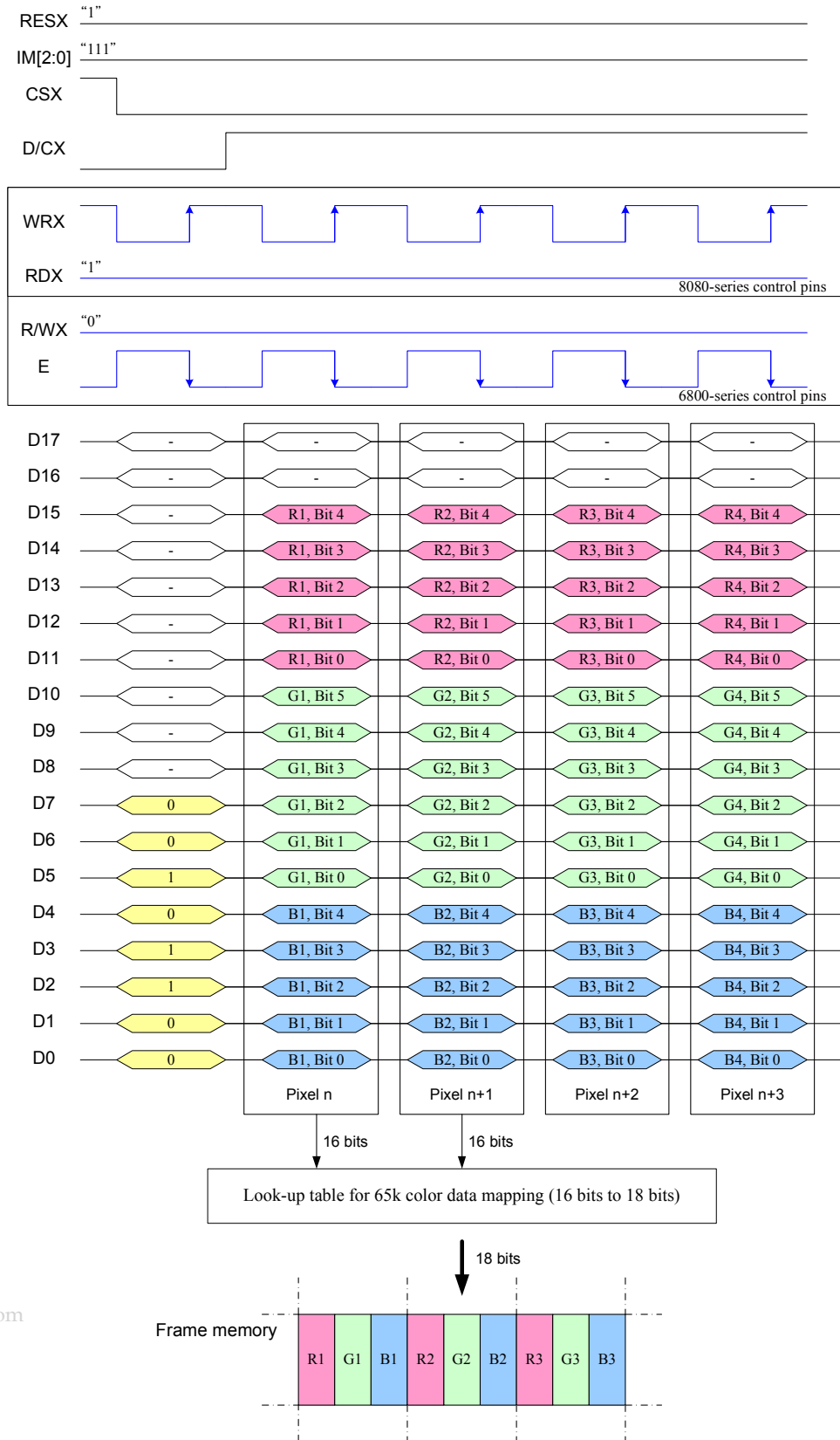


Note1. The data order is as follows, MSB=D11, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.

Note 2. 1-times transfer is used to transmit 1 pixel data with the 12-bit color depth information.

## 9.8.4.2 18-bit data bus for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3AH="05h"

There are 1 pixel (3 sub-pixels) per 1 byte, 16-bit/pixel.

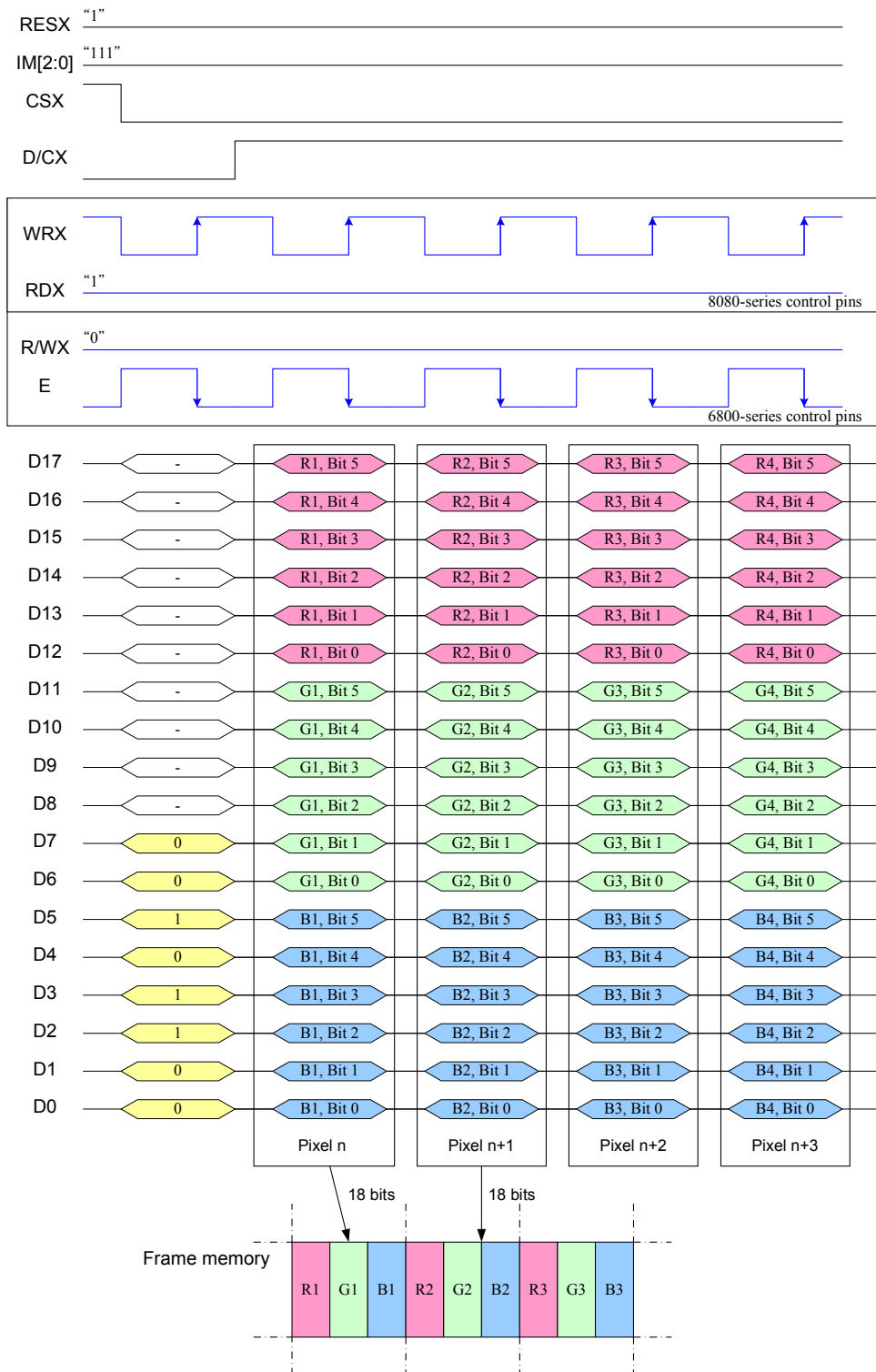


Note1. The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2.1-times transfer is used to transmit 1 pixel data with the 16-bit color depth information.

### 9.8.4.3 18-bit data bus for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3AH="06h"

There are 1 pixel (3 sub-pixels) per 1 bytes, 18-bit/pixel.



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Note1. The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Read, Green and Blue data.

Note 2.1-times transfer (D17o D0) is used to transmit 1 pixel data with the 18-bit color depth information.

N



## 9.8.5 3-line serial Interface

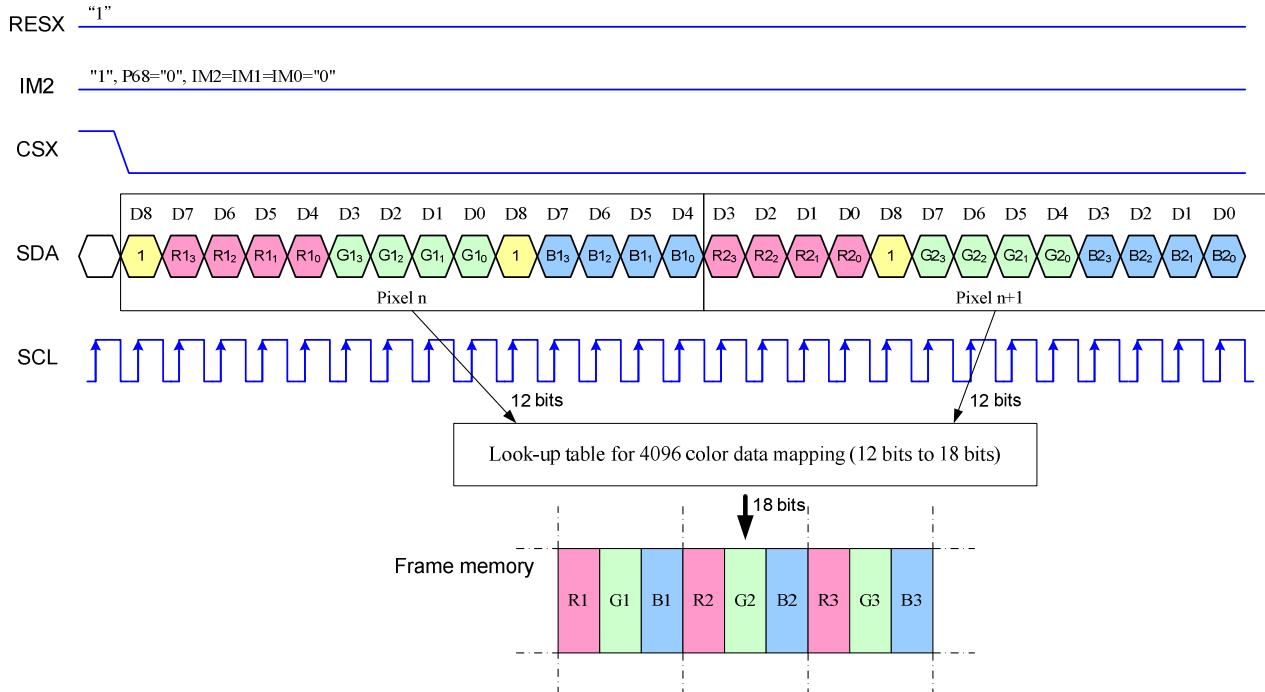
Different display data formats are available for three colors depth supported by the LCM listed below.

4k colors, RGB 4-4-4-bit input

65k colors, RGB 5-6-5-bit input

262k colors, RGB 6-6-6-bit input

### 9.8.5.1 Write data for 12-bit/pixel (RGB 4-4-4-bit input), 4K-Colors, 3AH="03h"

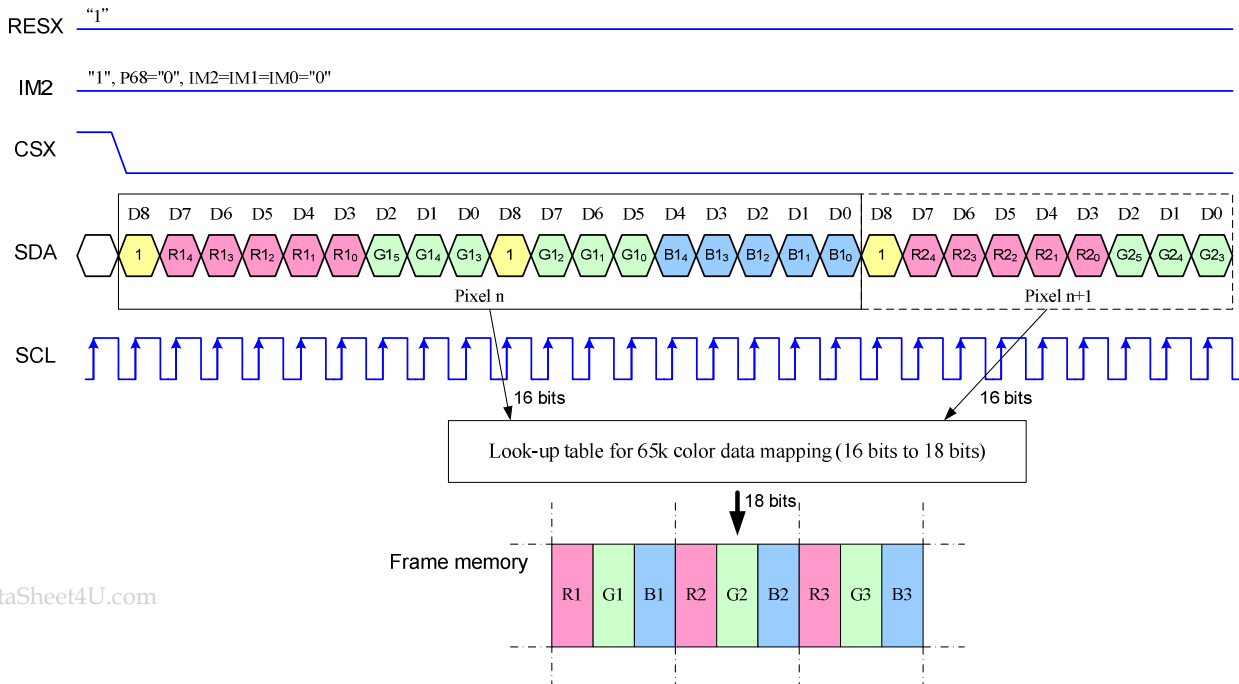


Note 1. pixel data with the 12-bit color depth information

Note 2. The most significant bits are: Rx3, Gx3 and Bx3

Note 3. The least significant bits are: Rx0, Gx0 and Bx0

### 9.8.5.2 Write data for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3AH="05h"



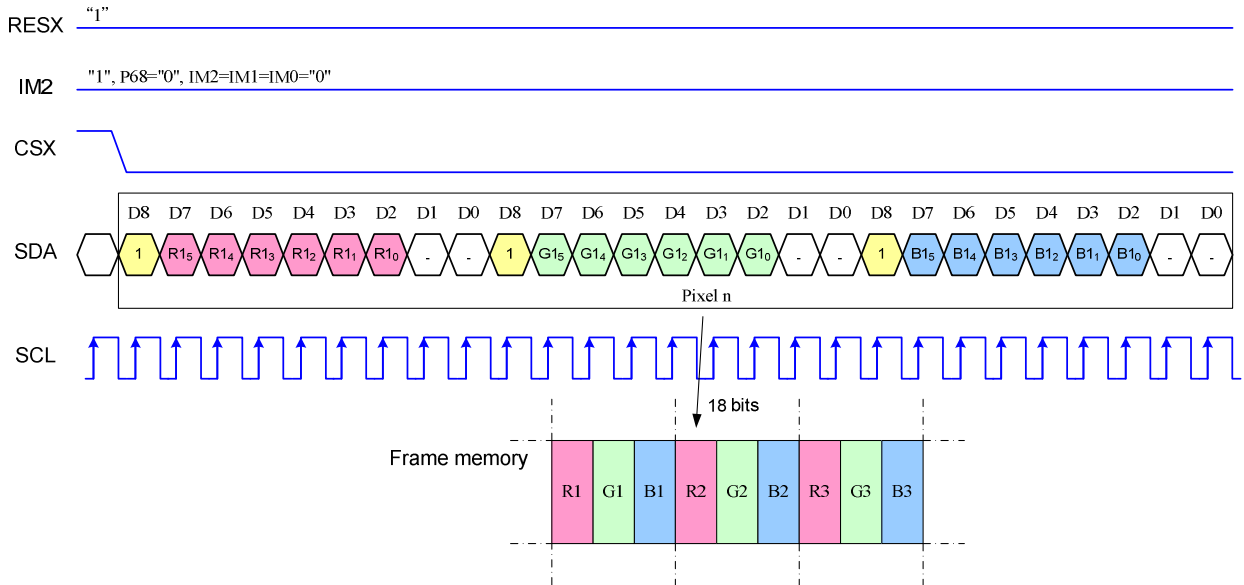
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Note 1. pixel data with the 16-bit color depth information

Note 2. The most significant bits are: Rx4, Gx5 and Bx4

Note 3. The least significant bits are: Rx0, Gx0 and Bx0

## 9.8.5.3 Write data for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3AH="06h"



Note 1. pixel data with the 18-bit color depth information

Note 2. The most significant bits are: Rx5, Gx5 and Bx5

Note 3. The least significant bits are: Rx0, Gx0 and Bx0

## 9.9 Display Data RAM

### 9.9.1 Configuration

The display module has an integrated 176x220x18-bit graphic type static RAM. This 696,960-bit memory allows to store on-chip a 176xRGBx220 image with an 18-bpp resolution (262K-color).

There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

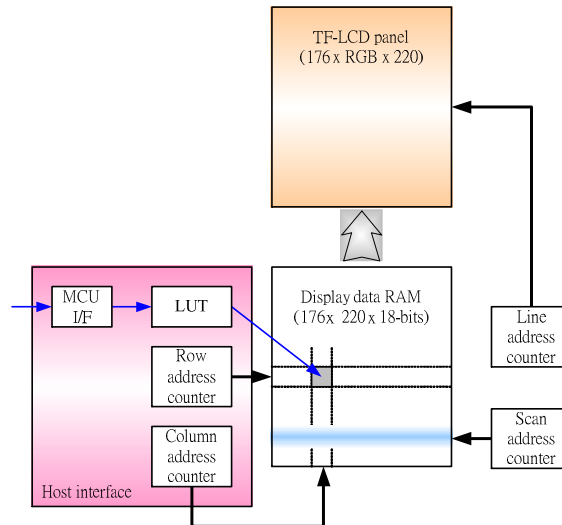
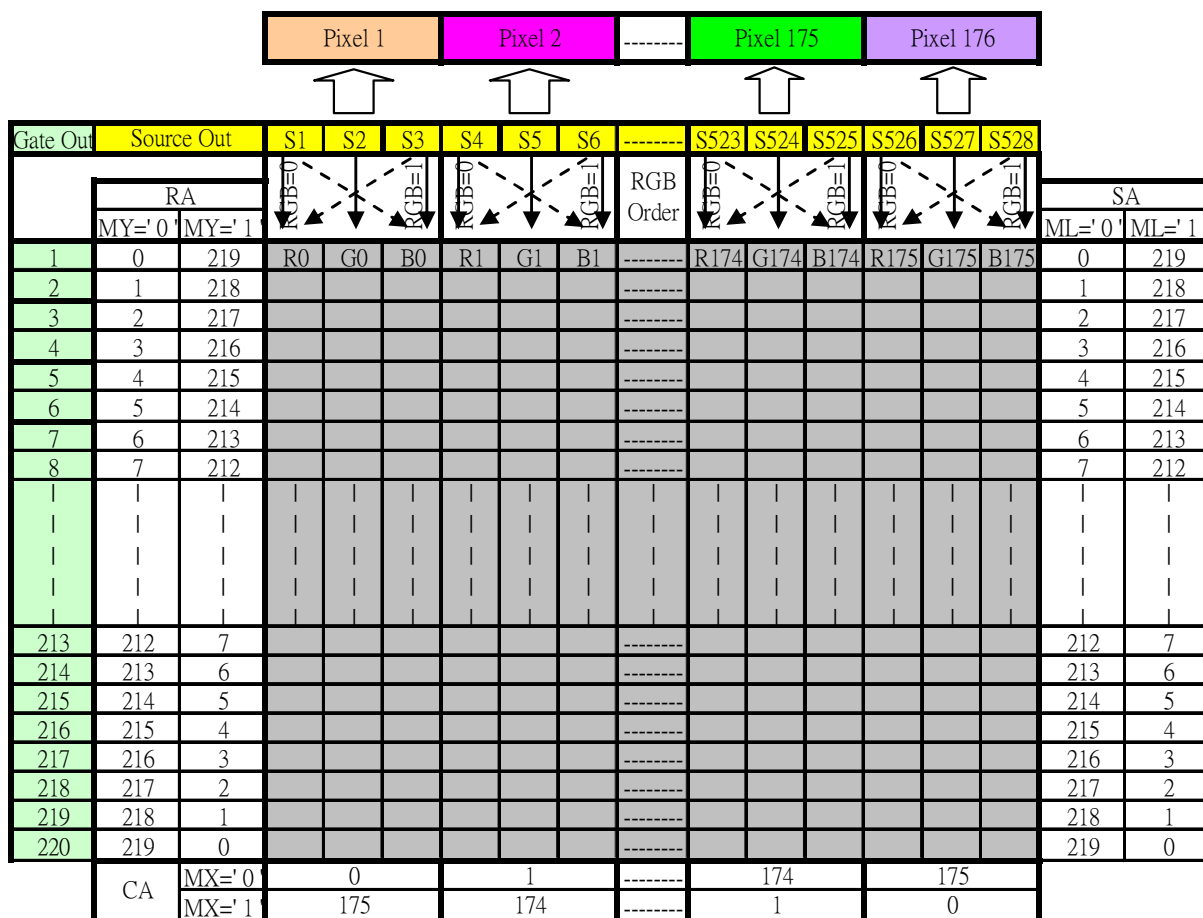


Fig. 9.9.1 Display data RAM organization

## 9.9.2 Memory to Display Address Mapping



**Note**

RA = Row Address,

CA = Column Address

SA = Scan Address

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

MY = Mirror Y-axis (Row address direction parameter), D7 parameter of MADCTL command

MX = Scan direction parameter, D4 parameter of MADCTL command

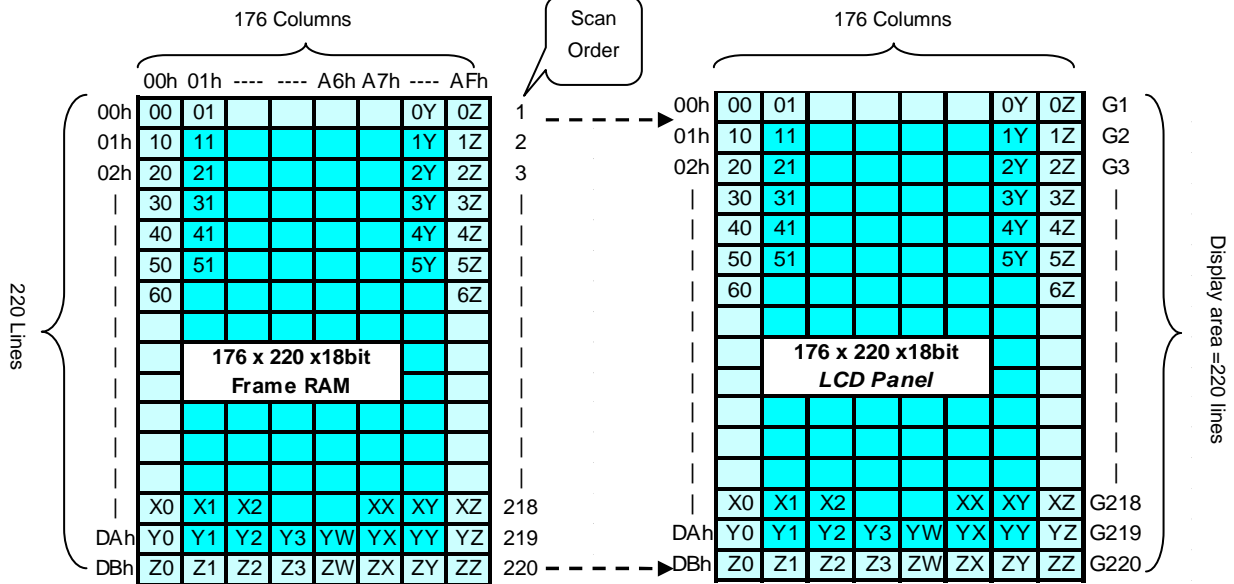
RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

## 9.9.3 Normal Display On or Partial Mode On, Vertical Scroll Off

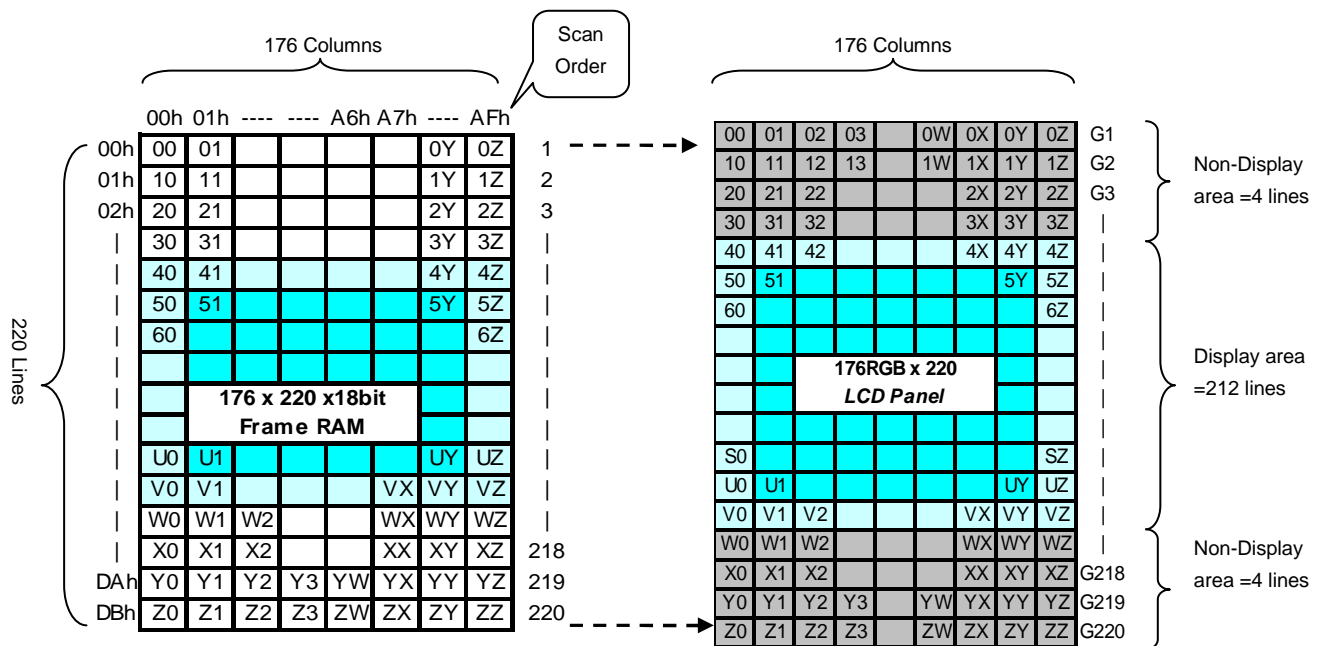
In this mode, contents of the frame memory within an area where column pointer is 00h to AFh and page pointer is 00h to DBh is displayed.

To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

1). Example for Normal Display On (MX=MY=ML='0', SMX=SMY='0')



2). Example for Partial Display On (PSL[7:0]=04h, PEL[7:0]=D7h, MX=MV=ML='0', SMX=SMY='0')



## 9.9.4 Vertical Scroll Mode

There is vertical scrolling, which are determined by the commands “Vertical Scrolling Definition” (33h) and Vertical Scrolling Start Address” (37h).

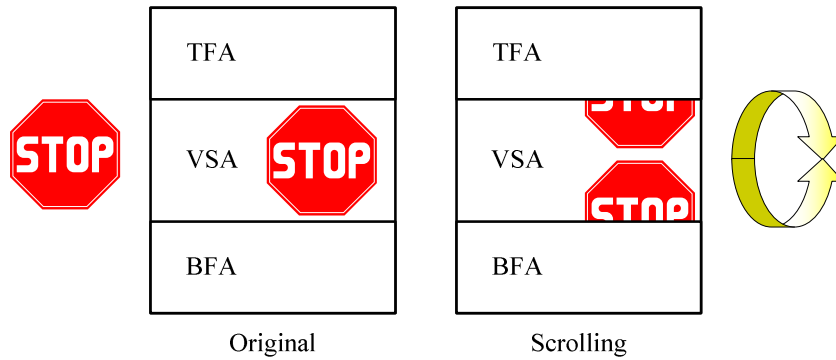
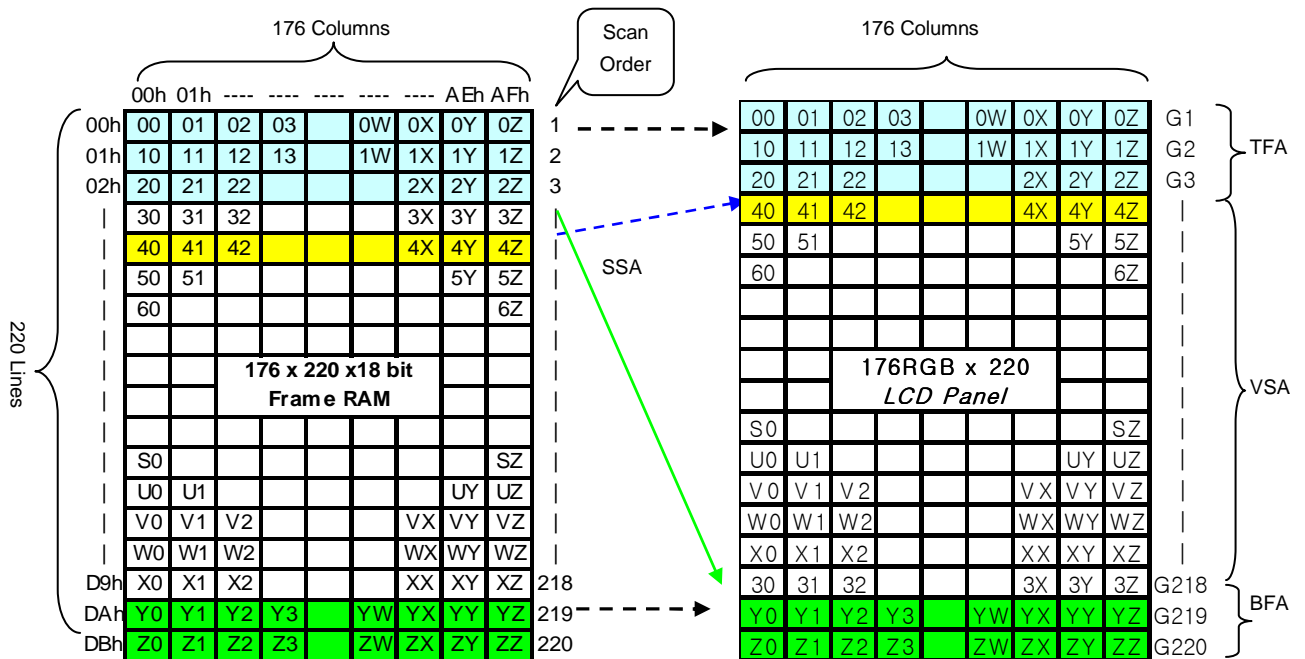


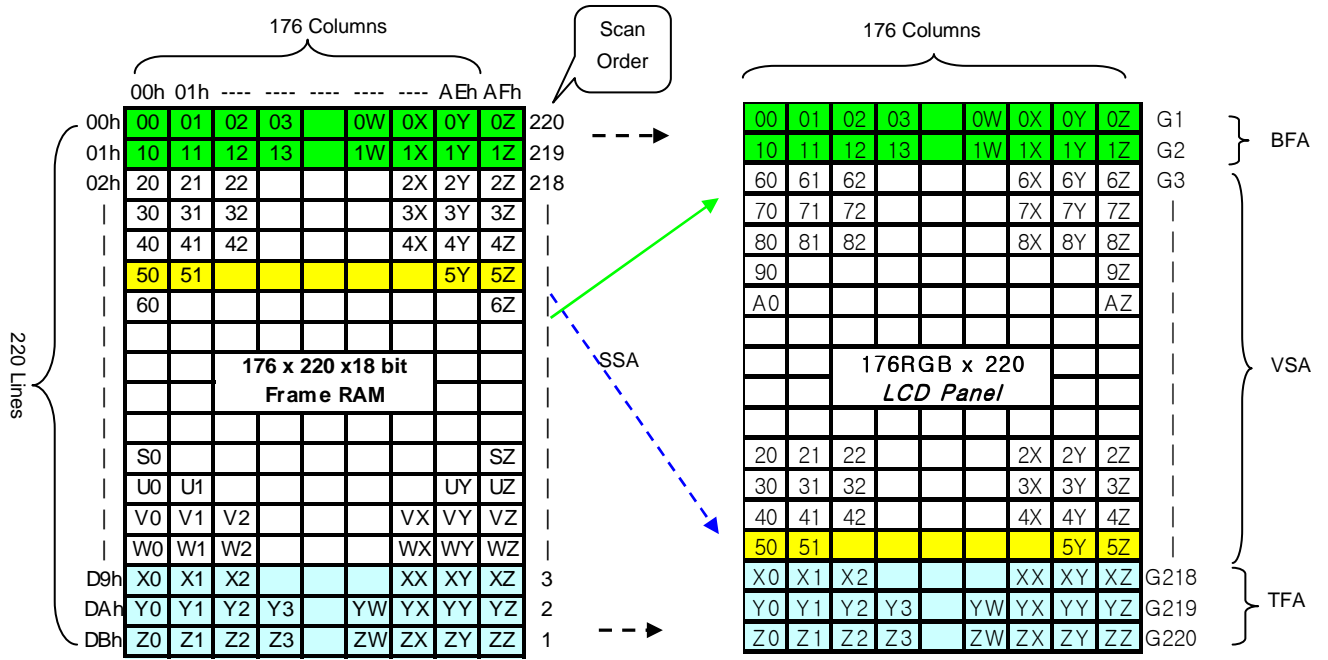
Fig. 9.9.2 Difference between Scrolling and original

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA)=220. In this case, scrolling is applied as shown below.

1). Example for TFA =3, VSA=215, BFA=2, SSA=4, ML=0: Scrolling



2). Example for TFA=3, VSA=215, BFA=2, SSA=215, ML=1: Scrolling: TFA and BFT are exchanged



## 9.9.5 Vertical Scroll Example

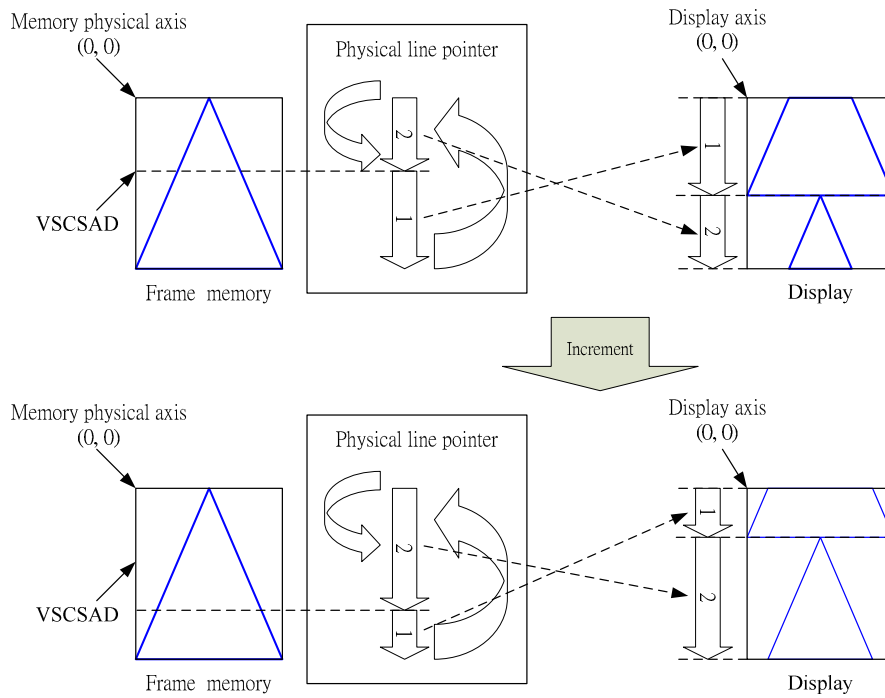
There are 2 types of vertical scrolling, which are determined by the commands "Vertical Scrolling Definition" (33h) and "Vertical Scrolling Start Address" (37h).

### Case 1: TFA + VSA + BFA#220

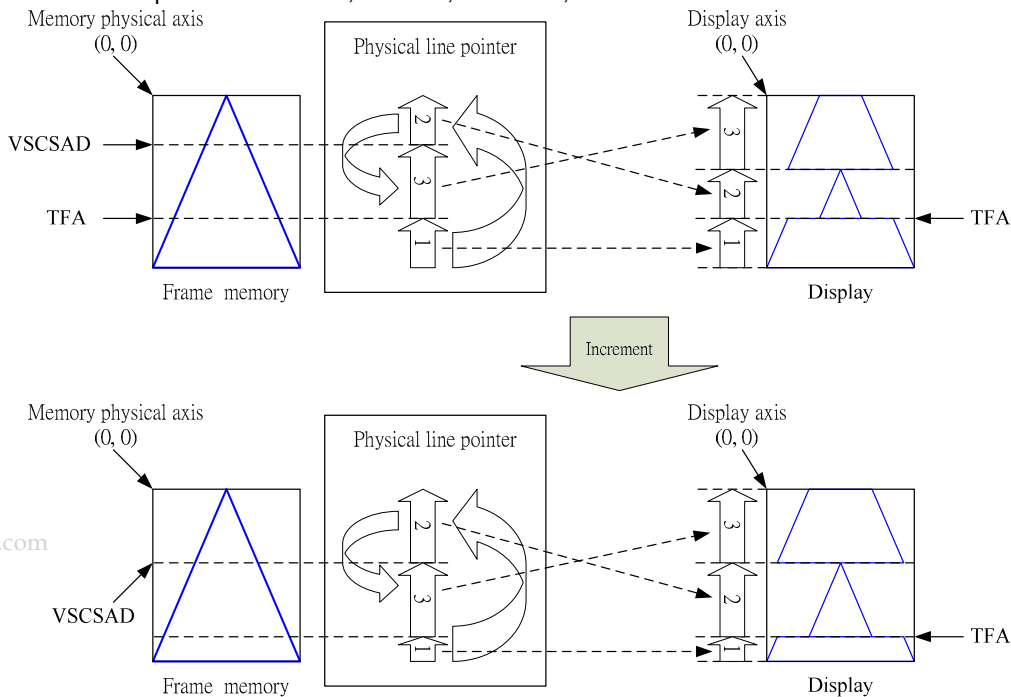
N/A. Do not set TFA + VSA + BFA#220. In that case, unexpected picture will be shown.

### Case 2: TFA + VSA + BFA=220 (Scrolling)

Example1) When MADCTL parameter ML="0", TFA=0, VSA=220, BFA=0 and VSCSAD=80.



Example2) When MADCTL parameter ML="1", TFA=30, VSA=190, BFA=0 and VSCSAD=80.





## 9.10 Address Counter

The address counter sets the addresses of the display data RAM for writing and reading.

Data is written pixel-wise into the RAM matrix of DRIVER. The data for one pixel or two pixels is collected (RGB 6-6-6-bit), according to the data formats. As soon as this pixel-data information is complete the "Write access" is activated on the RAM. The locations of RAM are addressed by the address pointers. The address ranges are X=0 to X=175 (AFh) and Y=0 to Y=219 (DBh). Addresses outside these ranges are not allowed. Before writing to the RAM, a window must be defined that will be written. The window is programmable via the command registers XS, YS designating the start address and XE, YE designating the end address.

For example the whole display contents will be written, the window is defined by the following values: XS=0 (0h) YS=0 (0h) and XE=175(AFh), YE=219 (DBh).

In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (V=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to XS and Y increments to address the next row. After the every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS).

For flexibility in handling a wide variety of display architectures, the commands "CASET, RASET" and "MADCTL" (see section 10 command list), define flags MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Section 9.12 show the available combinations of writing to the display RAM. When MX, MY and MV will be changed the data must be rewritten to the display RAM.

For each image condition, the controls for the column and row counters apply as section 9.11 below:

Condition	Column Counter	Row Counter
When RAMWR/RAMRD command is accepted	Return to "Start Column (XS)"	Return to "Start Row (YS)"
Complete Pixel Read / Write action	Increment by 1	No change
The Column counter value is larger than "End Column (XE)"	Return to "Start Column (XS)"	Increment by 1
The Column counter value is larger than "End Column (XE)" and the Row counter value is larger than "End Row (YE)"	Return to "Start Column (XS)"	Return to "Start Row (YS)"

## 9.11. Memory Data Write/ Read Direction

The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by "Memory Data Access Control" Command, bits B5 (MV), B6 (MX), B7 (MY) as described below.

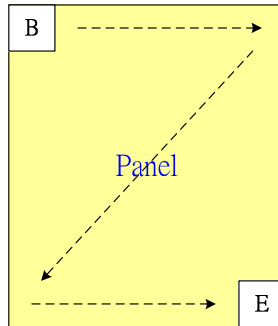
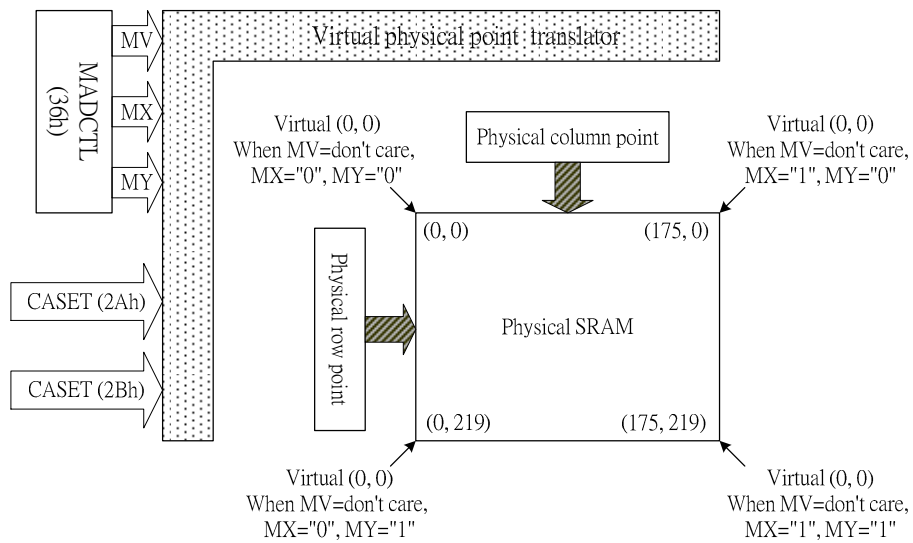


Fig. 9.11.1 Data streaming order



MV	MX	MY	CASET	RASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Row Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (219-Physical Row Pointer)
0	1	0	Direct to (175-Physical Column Pointer)	Direct to Physical Row Pointer
0	1	1	Direct to (175-Physical Column Pointer)	Direct to (219-Physical Row Pointer)
1	0	0	Direct to Physical Row Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (219-Physical Row Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Row Pointer	Direct to (175-Physical Column Pointer)
1	1	1	Direct to (219-Physical Row Pointer)	Direct to (175-Physical Column Pointer)

Note: Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MADCTL bits B7 (MY), B6 (MX), B5 (MV). The write order for each pixel unit is

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

One pixel unit represents 1 column and 1page counter value on the Frame Memory.

9.11.2 Frame Data Write Direction According to the MADCTL parameters (MV, MX and MY)

Display Data Direction	MADCTL Parameter			Image in the Host (MPU)	Image in the Driver (DDRAM)	
	MV	MX	MY			
Normal	0	0	0		H/W position (0,0) →	 X-Y address (0,0) X: CASET Y: RASET
Y-Mirror	0	0	1		H/W position (0,0) →	 X-Y address (0,0) X: CASET Y: RASET
X-Mirror	0	1	0		H/W position (0,0) →	 X-Y address (0,0) X: CASET Y: RASET
X-Mirror Y-Mirror	0	1	1		H/W position (0,0) →	 X-Y address (0,0) X: CASET Y: RASET
X-Y Exchange	1	0	0		H/W position (0,0) →	 X-Y address (0,0) X: RASET Y: CASET
X-Y Exchange Y-Mirror	1	0	1		H/W position (0,0) →	 X-Y address (0,0) X: RASET Y: CASET
X-Y Exchange X-Mirror	1	1	0		H/W position (0,0) →	 X-Y address (0,0) X: RASET Y: CASET
X-Y Exchange X-Mirror Y-Mirror	1	1	1		H/W position (0,0) →	 X-Y address (0,0) X: RASET Y: CASET

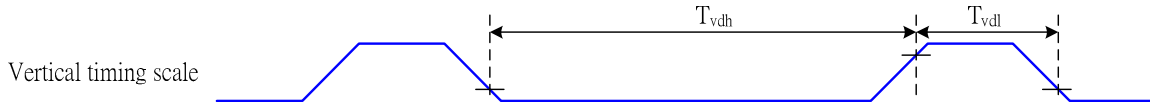
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## 9.12 Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

### 9.12.1 Tearing Effect Line Modes

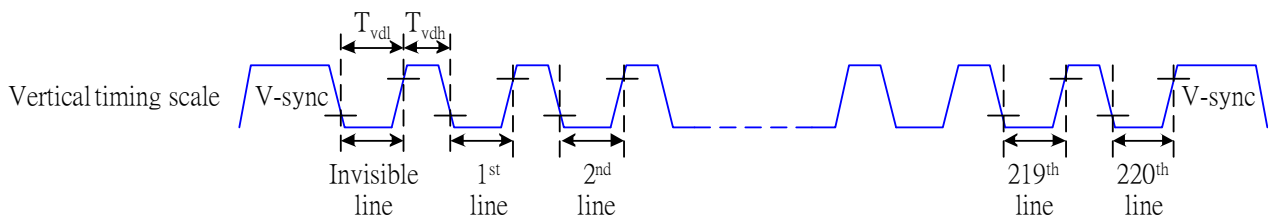
**Mode 1**, the Tearing Effect Output signal consists of V-Blanking Information only:



$tvdh$ = The LCD display is not updated from the Frame Memory

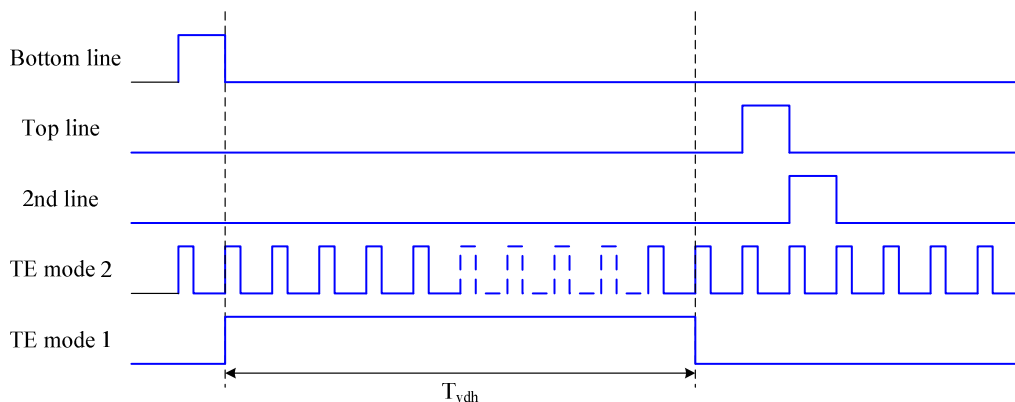
$tvdI$ = The LCD display is updated from the Frame Memory (except Invisible Line – see below)

**Mode 2**, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 220 H-sync pulses per field.



$thdh$ = The LCD display is not updated from the Frame Memory

$thdl$ = The LCD display is updated from the Frame Memory (except Invisible Line – see above)



Note: During Sleep In Mode, the Tearing Output Pin is active Low.

## 9.12.2 Tearing Effect Line Timings

The Tearing Effect signal is described below:

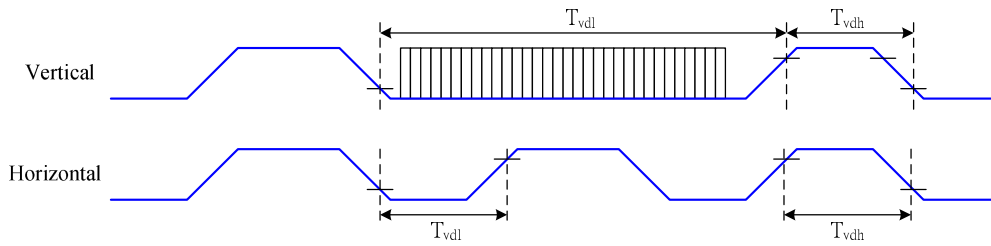
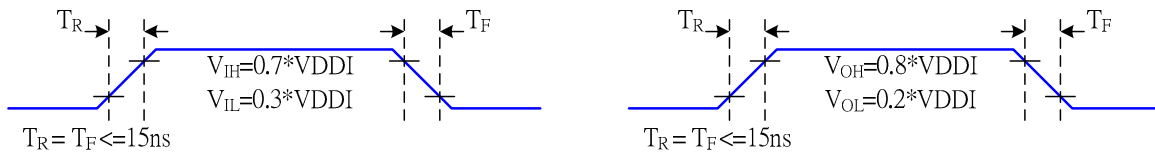


Table 9.12.1 AC characteristics of Tearing Effect Signal Idle Mode Off (Frame Rate = 58.9 Hz)

Symbol	Parameter	min	max	unit	description
t <sub>vdl</sub>	Vertical Timing Low Duration	13	-	ms	
t <sub>vdh</sub>	Vertical Timing High Duration	1000	-	μs	
t <sub>hdl</sub>	Horizontal Timing Low Duration	33	-	μs	
t <sub>hdh</sub>	Horizontal Timing High Duration	25	500	μs	

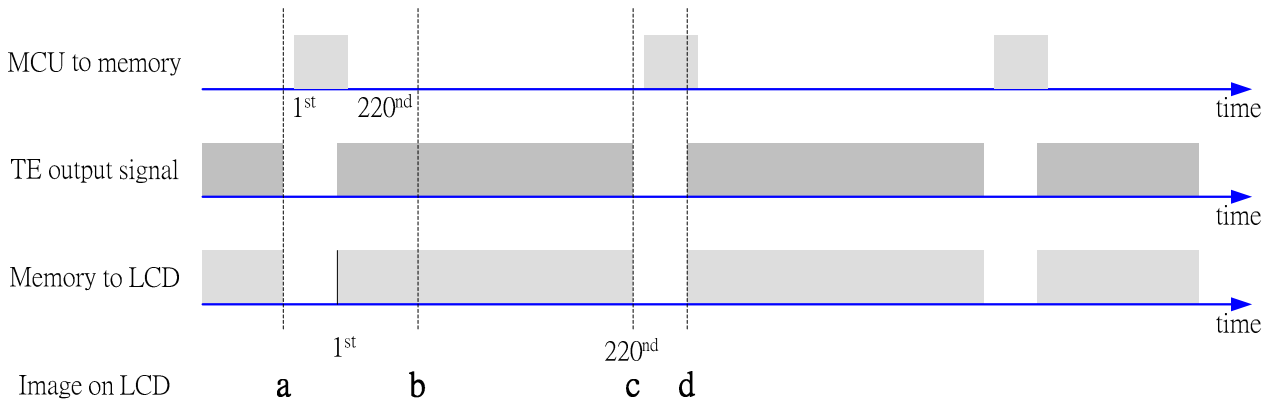
NOTE: The timings in Table 9.3.1 apply when MADCTL ML=0 and ML=1

The signal's rise and fall times (t<sub>f</sub>, t<sub>r</sub>) are stipulated to be equal to or less than 15ns.

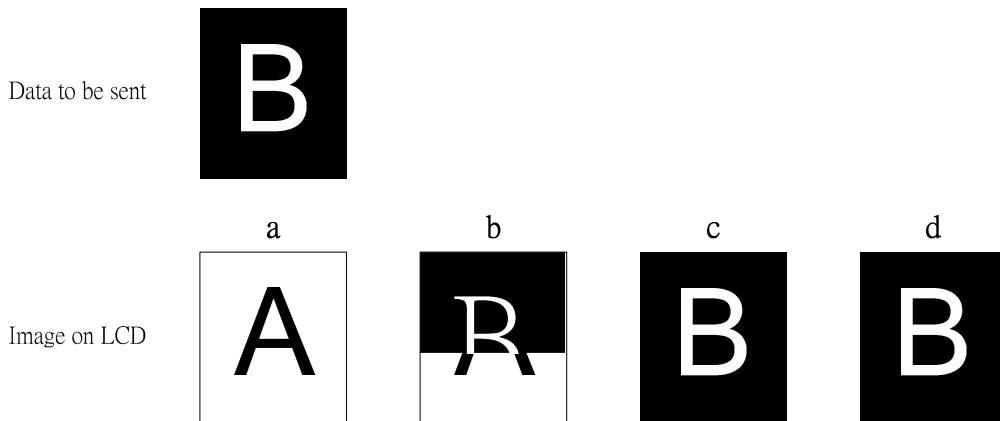


The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

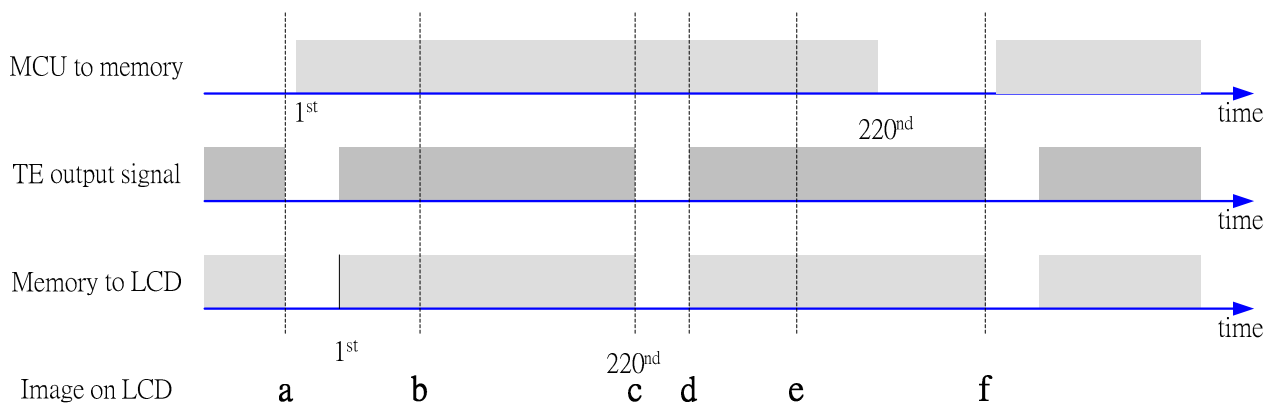
## 9.12.3 Example 1: MPU Write is faster than panel read



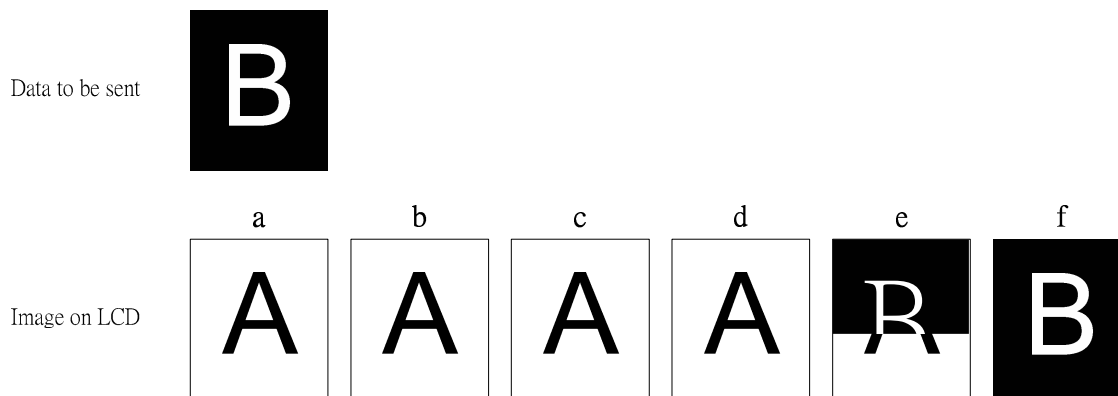
Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:



## 9.12.4 Example 2: MPU write is slower than panel read.



The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MPU to Frame memory write position.

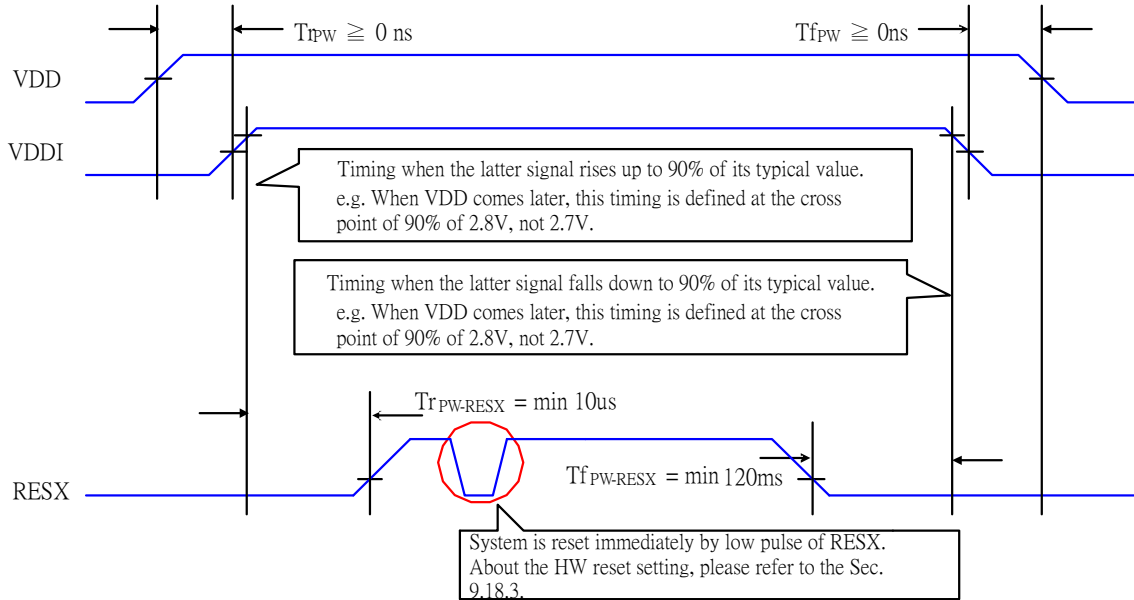


## 9.13 Preset Values

ST7773 will set preset values on our production line for each display module. Any of these preset values do not need customer's SW support.

## 9.14 Power ON/OFF Sequence

The power on/off sequence is illustrated below: (VDD must be powered on then VDDI)



## 9.15.3 Uncontrolled Power Off

The uncontrolled power-off means a situation which removed a battery without the controlled power off sequence. It will neither damage the module or the host interface

If uncontrolled power-off happened, the display will go blank and there will not be any visible effects on the display (blank display) and remains blank until "Power On Sequence" powers it up.



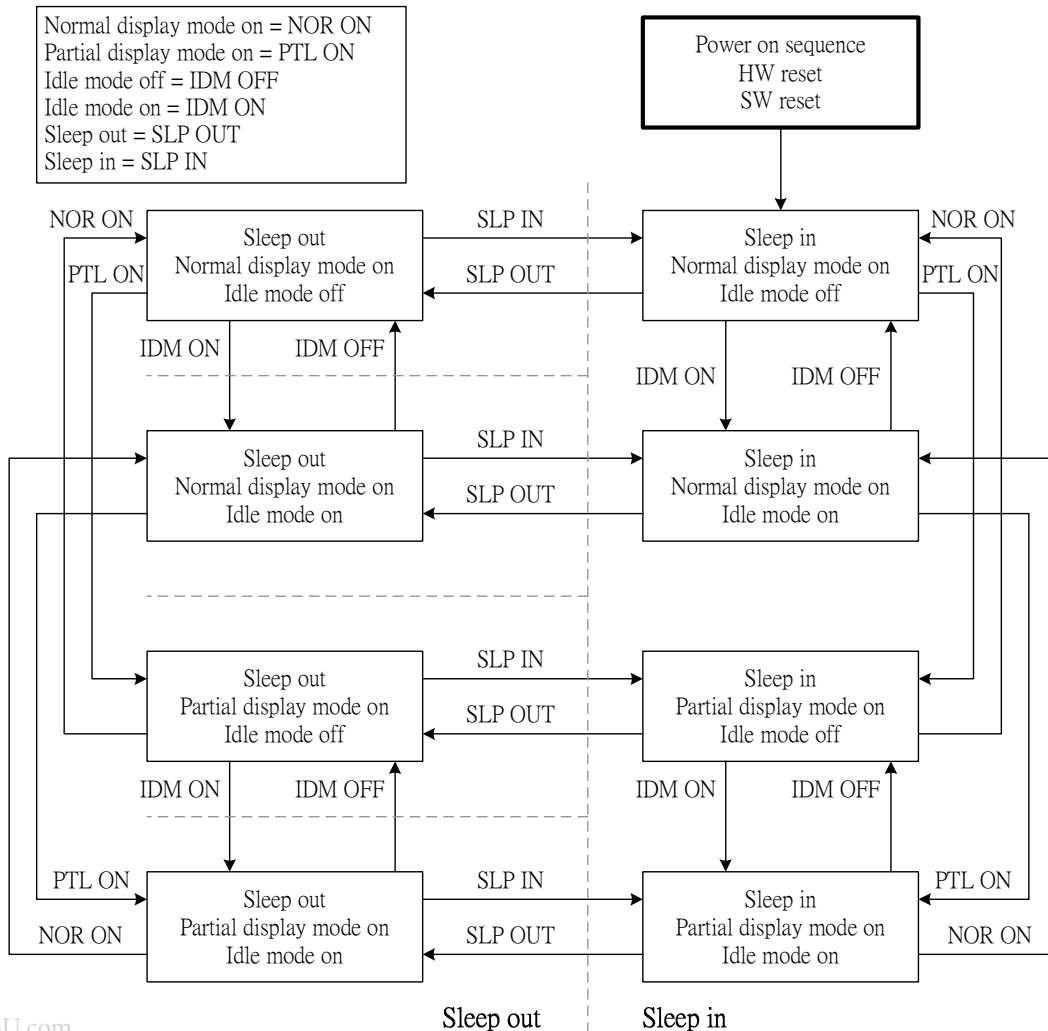
## 9.16 Power Level Definition

### 9.16.1 Power Level

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

- 1. Normal Mode On (full display), Idle Mode Off, Sleep Out.**  
In this mode, the display is able to show maximum 262,144 colors.
- 2. Partial Mode On, Idle Mode Off, Sleep Out.**  
In this mode part of the display is used with maximum 262,144 colors.
- 3. Normal Mode On (full display), Idle Mode On, Sleep Out.**  
In this mode, the full display area is used but with 8 colors.
- 4. Partial Mode On, Idle Mode On, Sleep Out.**  
In this mode, part of the display is used but with 8 colors.
- 5. Sleep In Mode**  
In this mode, the DC: DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDDI power supply. Contents of the memory are safe.
- 6. Power Off Mode**  
In this mode, both VDD and VDDI are removed.

### 9.16.2 Power Flow Chart



## 9.17 Reset Table

Item	After Power On	After Hardware Reset	After Software Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display On/Off	Off	Off	Off
Display mode (normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column: Start Address (XS)	0000h	0000h	0000h
Column: End Address (XE)	00AFh	00AFh	00AFh (175d) (when MV=0) 00DBh (219d) (when MV=1)
Row: Start Address (YS)	0000h	0000h	0000h
Row: End Address (YE)	00DBh	00DBh	00DBh (219d) (when MV=0) 00AFh (175d) (when MV=1)
Gamma setting	GC0	GC0	GC0
RGB for 256, 4k and 65k Color Mode	See Section 9.19	See Section 9.19	No Change
Partial: Start Address (PSL)	0000h	0000h	0000h
Partial: End Address (PEL)	00DBh	00DBh	00DBh
Scroll: Vertical scrolling	Off	Off	Off
Scroll: Top Fixed Area (TFA)	0000h	0000h	0000h
Scroll: Scroll Area (VSA)	00DCh	00DCh	00DCh
Scroll: Bottom Fixed Area (BFA)	0000h	0000h	0000h
Scroll Start Address (SSA)	0000h	0000h	0000h
Tearing: On/Off	Off	Off	Off
Tearing Effect Mode *3)	0 (Mode1)	0 (Mode1)	0 (Mode1)
Memory Data Access Control (MY/MX/MV/ML/RGB)	0/0/0/0/0	0/0/0/0/0	No Change
Interface Pixel Color Format	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDPM	08h	08h	08h
RDDMADCTL	00h	00h	No Change
RDDCOLMOD	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
RDDSDR	00h	00h	00h
ID1	29h	29h	29h
ID2	-	-	-

Note1. TE Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

### 9.18.1 Module Input/Output Pins

#### 9.18.1.1 Output or Bi-directional (I/O) Pins

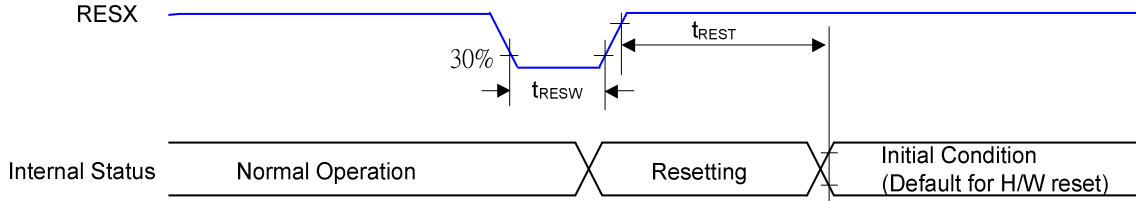
Output or Bi-directional pins	After Power On	After Hardware Reset	After Software Reset
TE	Low	Low	Low
D17 to D0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)

Note: There will be no output from D7-D0 during Power On/Off sequence, Hardware Reset and Software Reset.

#### 9.18.1.2 Input Pins

Input pins	During Power On Process	After Power On	After Hardware Reset	After Software Reset	During Power Off Process
RESX	See 9.15	Input valid	Input valid	Input valid	See 9.15
CSX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D/CX	Input invalid	Input valid	Input valid	Input valid	Input invalid
WRX	Input invalid	Input valid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D17 to D0	Input invalid	Input valid	Input valid	Input valid	Input invalid
P/SX	Input invalid	Input valid	Input valid	Input valid	Input invalid

## 9.18.2 Reset Timing



VSS=0V, VDDI=1.6 to 3.3V, VDD=2.7 to 3.3V, Ta = 25°C)

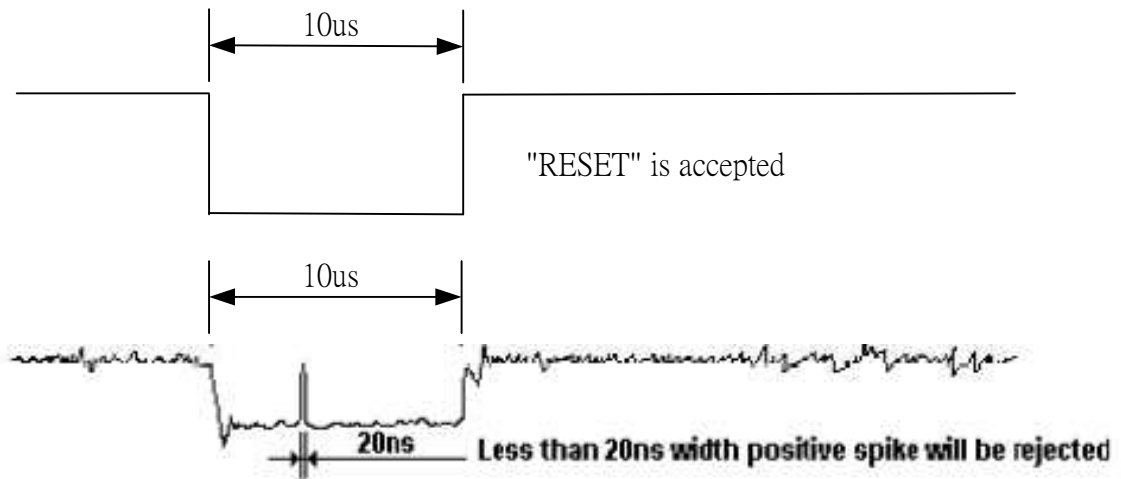
Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t <sub>RESW</sub>	*1) Reset low pulse width	RESX	10	-	-	-	us
t <sub>REST</sub>	Reset complete time	-	120	-	-		ms

Note 1 Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

Note 2. During Reset Complete Time, ID2 and VCOMOF value in EEPROM will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (t<sub>REST</sub>) within 5ms after a rising edge of RESX.

Note 3. Spike Rejection also applies during a valid reset pulse as shown below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts (It depends on voltage and temperature condition.)



## 9.19 External Light Source

The operation of the module can meet customer's Environmental reliability requirements.

## 9.20 Oscillator

The chip has on-chip oscillator that does not require external components. This oscillator output signal is used for system clock generation for internal display operation.

## 9.21 System Clock Generator

The timing generator produces the various signals to driver the internal circuitry. Internal chip operation is not affected by operations on the data bus.

## 9.22 Instruction Decoder and Register

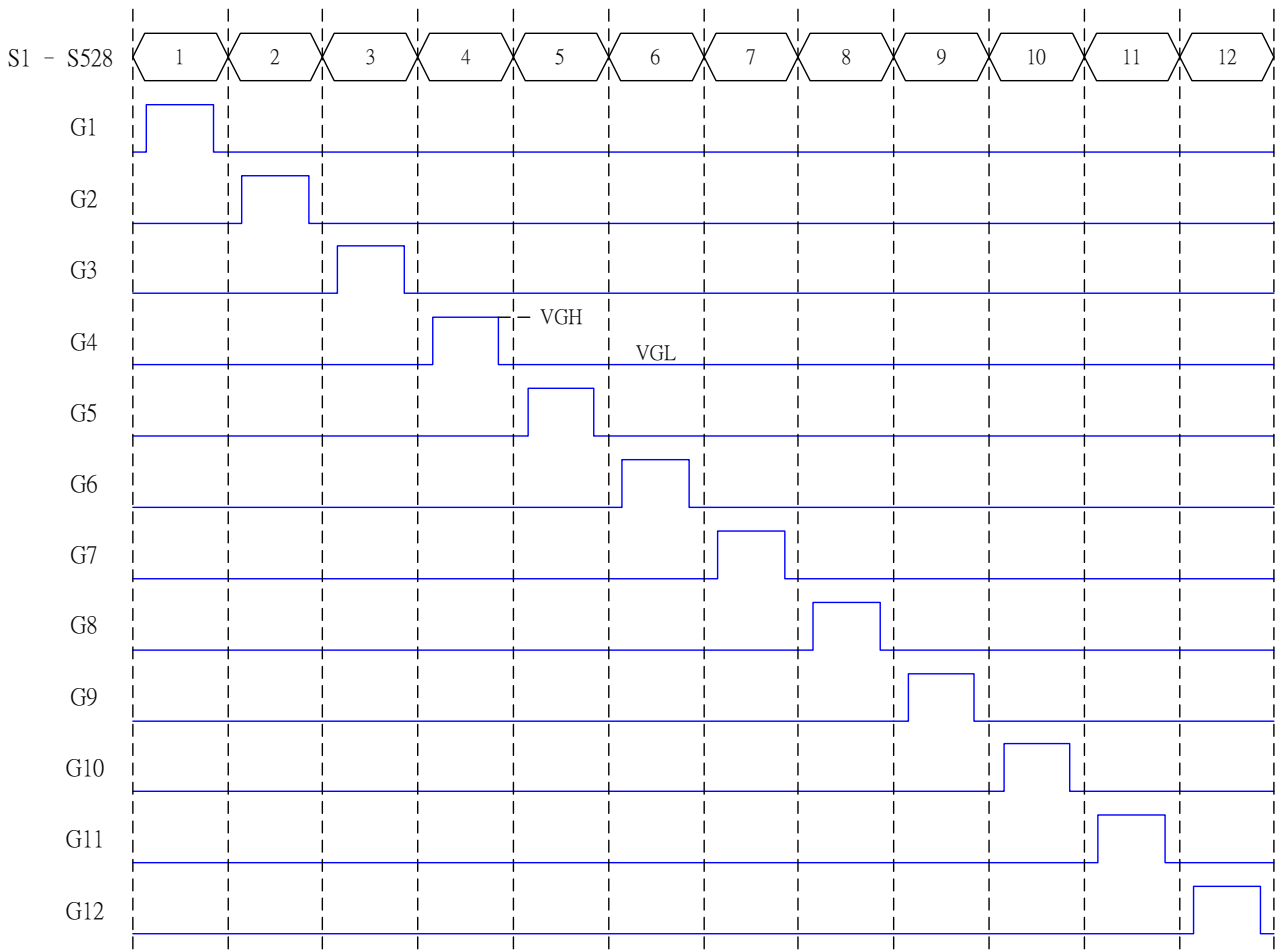
The instruction decoder identifies command words arriving at the interface and routes the following data bytes to their destination. The command set can be found in "Command" section.

## 9.23 Source Driver

The source driver block includes 176x3 source outputs (S1 to S528), which should be connected directly to the TFT-LCD. The source output signals are generated in the data processing block after the data is read out of the RAM and latched, which represent the simulatance selected rows.

## 9.24 Gate Driver

The gate driver block includes 220 channel gate output (G0 to G219) which should be connected directly to the TFT-LCD.



# ST7773

## 10. Command

### 10.1 System function Command List and Description

Table 10.1.1 System Function command List (1)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function	
NOP	10.1.1	0	↑	1	-	0	0	0	0	0	0	0	0	(00h)	No Operation	
SWRESET	10.1.2	0	↑	1	-	0	0	0	0	0	0	0	1	(01h)	Software reset	
RDDID	10.1.3	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)	Read Display ID	
		1	1	↑	-	-	-	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	-	-	ID1 read
		1	1	↑	-	'1'	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-	-	ID2 read
RDDST	10.1.4	0	↑	1	-	0	0	0	0	1	0	0	1	(09h)	Read Display Status	
		1	1	↑	-	-	-	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	-	BSTON	MY	MX	MV	ML	RGB	MH	ST24	-	-	-
		1	1	↑	-	ST23	IFPF2	IFPF1	IFPF0	IDMON	PTLON	SLOUT	NORON	-	-	-
		1	1	↑	-	VSSON	ST14	INVON	ST21	ST11	DISON	TEON	GCS2	-	-	-
		1	1	↑	-	GCS1	GCS0	TELON	HSON	VSON	PCKON	DEON	ST0	-	-	-
RDDPM	10.1.5	0	↑	1	-	0	0	0	0	1	0	1	0	(0Ah)	Read Display Power Mode	
		1	1	↑	-	-	-	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	-	BSTON	IDMON	PTLON	SLPOUT	NORON	DISON	D1	D0	-	-	-
RDD MADCTL	10.1.6	0	↑	1	-	0	0	0	0	1	0	1	1	(0Bh)	Read Display MADCTL	
		1	1	↑	-	-	-	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	-	MY	MX	MV	ML	RGB	MH	D1	D0	-	-	-
RDD COLMOD	10.1.7	0	↑	1	-	0	0	0	0	1	1	0	0	(0Ch)	Read Display Pixel Format	
		1	1	↑	-	-	-	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	-	D7	D6	D5	D4	D3	IFPF2	IFPF1	IFPF0	-	-	-
RDDIM	10.1.8	0	↑	1	-	0	0	0	0	1	1	0	1	(0Dh)	Read Display Image Mode	
		1	1	↑	-	-	-	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	-	VSSON	D6	INVON	D4	D3	GCS2	GCS1	GCS0	-	-	-
RDDSM	10.1.9	0	↑	1	-	0	0	0	0	1	1	1	0	(0Eh)	Read Display Signal Mode	
		1	1	↑	-	-	-	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	-	TEON	TELON	HSON	VSON	PCKON	DEON	D1	D0	-	-	-

"-": Don't care

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Table 10.1.2 System Function command List (2)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
SLPIN	10.1.11	0	↑	1	-	0	0	0	1	0	0	0	0	(10h)	Sleep in & booster off
SLPOUT	10.1.12	0	↑	1	-	0	0	0	1	0	0	0	1	(11h)	Sleep out & booster on
PTLON	10.1.13	0	↑	1	-	0	0	0	1	0	0	1	0	(12h)	Partial mode on
NORON	10.1.14	0	↑	1	-	0	0	0	1	0	0	1	1	(13h)	Partial mode off (Normal)
INVOFF	10.1.15	0	↑	1	-	0	0	1	0	0	0	0	0	(20h)	Display inversion off (normal)
INVON	10.1.16	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)	Display inversion on
GAMSET	10.1.17	0	↑	1	-	0	0	1	0	0	1	1	0	(26h)	Gamma curve select
		1	↑	1	-	-	-	-	-	GC3	GC2	GC1	GC0		-
DISPOFF	10.1.18	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)	Display off
DISPON	10.1.19	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)	Display on
CASET	10.1.20	0	↑	1	-	0	0	1	0	1	0	1	0	(2Ah)	Column address set
		1	↑	1	-	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8		X address start: $0 \leq S \leq X$
		1	↑	1	-	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0		
		1	↑	1	-	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8		X address end: $XS \leq XE \leq X$
RASET	10.1.21	0	↑	1	-	0	0	1	0	1	0	1	1	(2Bh)	Row address set
		1	↑	1	-	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8		Y address start: $0 \leq YS \leq Y$
		1	↑	1	-	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0		
		1	↑	1	-	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8		Y address end: $YS \leq YE \leq Y$
RAMWR	10.1.22	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)	Memory write
		1	↑	1	-	D7	D6	D5	D4	D3	D2	D1	D0		Write data
RAMRD	10.1.23	0	↑	1	-	0	0	1	0	1	1	1	0	(2Eh)	Memory read
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	D7	D6	D5	D4	D3	D2	D1	D0		Read data

“-”: Don't care

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Table 10.1.3 System Function command List (3)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
PTLAR	10.1.24	0	↑	1	-	0	0	1	1	0	0	0	0	(30h)	Partial start/end address set
		1	↑	1	-	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8		Partial start address (0,1,2, ..P)
		1	↑	1	-	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8		Partial end address (0,1,2, ..., P)
		1	↑	1	-	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0		
SCRLAR	10.1.25	0	↑	1	-	0	0	1	1	0	0	1	1	(33h)	Scroll area set
		1	↑	1	-	TFA15	TFA14	TFA13	TFA12	TFA11	TFA10	TFA9	TFA8		Top fixed area (0,1,2, ..., S)
		1	↑	1	-	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0		
		1	↑	1	-	VSA15	VSA14	VSA13	VSA12	VSA11	VSA10	VSA9	VSA8		Vertical scroll area (0,1,2, ..., S)
		1	↑	1	-	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0		
		1	↑	1	-	BFA15	BFA14	BFA13	BFA12	BFA11	BFA10	BFA9	BFA8		Bottom fixed area (0,1,2, ..., S)
1	↑	1	-	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0				
TEOFF	10.1.26	0	↑	1	-	0	0	1	1	0	1	0	0	(34h)	Tearing effect line off
TEON	10.1.27	0	↑	1	-	0	0	1	1	0	1	0	1	(35h)	Tearing effect mode set & on
		1	↑	1	-	-	-	-	-	-	-	-	M		M="0": Mode1, M="1": Mode2
MADCTL	10.1.28	0	↑	1	-	0	0	1	1	0	1	1	0	(36h)	Memory data access control
		1	↑	1	-	MY	MX	MV	ML	RGB	MH	0	0		-
VSCSAD	10.1.29	0	↑	1	-	0	0	1	1	0	1	1	1	(37h)	Scroll start address of RAM
		1	↑	1	-	-	-	-	-	-	-	-	SSA8		SSA = 0, 1, 2, ..., 175
		1	↑	1	-	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0		
IDMOFF	10.1.30	0	↑	1	-	0	0	1	1	1	0	0	0	(38h)	Idle mode off
IDMON	10.1.31	0	↑	1	-	0	0	1	1	1	0	0	1	(39h)	Idle mode on
COLMOD	10.1.32	0	↑	1	-	0	0	1	1	1	0	1	0	(3Ah)	Interface pixel format
		1	↑	1	-	-	-	-	-	0	IFPF2	IFPF1	IFPF0		Interface format
RDID1	10.1.33	0	↑	1	-	1	1	0	1	1	0	1	0	(DAh)	Read ID1
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		Read parameter
RDID2	10.1.34	0	↑	1	-	1	1	0	1	1	0	1	1	(DBh)	Read ID2
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		Read parameter
RDID3	10.1.35	0	↑	1	-	1	1	0	1	1	1	0	0	(DCh)	Read ID3
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		Read parameter

"-": Don't care

Note 1: After the H/W reset by RESX pin or S/W reset by SWRESET command, each internal register becomes default state (Refer "RESET TABLE" section)

Note 2: Undefined commands are treated as NOP (00 h) command.

Note 3: DE to FF are for factory use of driver supplier.

Note 4: Commands 10h, 12h, 13h, 20h, 21h, 26h, 28h, 29h, 30h, 33h, 36h (ML parameter only), 37h, 38h and 39h are updated during V-sync when Module is in Sleep Out Mode to avoid abnormal visual effects. During Sleep In mode, these commands are updated immediately. Read status (09h), Read Display Power Mode (0Ah), Read Display MADCTL (0Bh), Read Display Pixel Format (0Ch), Read Display Image Mode (0Dh), Read Display Signal Mode (0Eh) of these commands are updated immediately both in Sleep In mode and Sleep Out mode.

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## 10.2 Panel Function Command List and Description

Table 10.2.1 Panel Function Command List (1)

Instruction	Refer	D/CX	WRX	RDX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function	
FRMCTR1	10.2.2	0	↑	1	-	1	0	1	1	0	0	0	1	(B1h)	In normal mode (Full colors)	
		1	↑	1	RTNA[7:0]											RTNA_VSYNC setting for VSYNC mode
					-	0	0	1	1	1	0	1	1			
					FPA[4:0]											
					-	0	0	0	0	0	1	0	0			
					BPA[4:0]											
RTNA_VSYNC[7:0]																
					0	0	1	1	1	0	0	0				
FRMCTR2	10.2.3	0	↑	1	-	1	0	1	1	0	0	1	0	(B2h)	In Idle mode (8 colors)	
		1	↑	1	RTNB[7:0]											
					-	0	0	1	1	1	0	1	1			
					FPB[4:0]											
					-	0	0	0	0	0	1	0	0			
					BPB[4:0]											
RTNB_VSYNC[7:0]																
					0	0	0	0	1	1						
FRMCTR3	10.2.4	0	↑	1	-	1	0	1	1	0	0	1	0	(B3h)	In partial mode (Full colors)	
		1	↑	1	RTNC[7:0]											
					-	0	0	1	1	1	0	1	1			
					FPC[4:0]											
					-	0	0	0	0	0	1	0	0			
					BPC[4:0]											
RTNC_VSYNC[7:0]																
					0	0	0	0	1	1						
INVCTR	10.2.5	0	↑	1	-	1	0	1	1	0	1	0	0	(B4h)	Display inversion control	
		1	↑	1	-	0	0	0	0	0	NLA	NLB	NLC		NLA;NLB,NLC set inversion	
					-	0	0	0	0	0	0	0				
DISSET5	10.2.7	0	↑	1	-	1	0	1	1	0	1	1	0	(B6h)	Display function setting	
		1	↑	1	-	0	0	NO1	NO0	SDT1	SDT0	EQ1	EQ0		NO: the amount of non-overlap SDT: set amount of source delay PT: No display area source/ VCOM/ Gate output control EQ: set EQ period	
					-	0	0	0	1	0	1	0	1			
					PTG[4:0]											
					0	0	0	0	0	0	0	0				



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Table 10.2.2 Panel Function Command List (2)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
PWCTR1	10.2.10	0	↑	1	-	1	1	0	0	0	0	0	0	(C0h)	Power control setting
		1	↑	1	-	0	0	0	VRH4	VRH3	VRH2	VRH1	VRH0		VRH: Set the GVDD voltage
PWCTR2	10.2.11	0	↑	1	-	1	1	0	0	0	0	0	1	(C1h)	Power control setting
		1	↑	1	-	VGH3	VGH2	VGH1	VGH0	VGL3	VGL2	VGL1	VGL0		VGH: set VGH voltage VGL: set VGL voltage
PWCTR3	10.2.12	0	↑	1	-	1	1	0	0	0	0	1	0	(C2h)	In normal mode (Full colors)
		1	↑	1	-	0	0	0	0	0	APA2	APA1	APA0		AP: adjust the operational amplifier DC: adjust the booster circuit for Idle mode
PWCTR4	10.2.13	0	↑	1	-	1	1	0	0	0	0	1	1	(C3h)	In Idle mode (8-colors)
		1	↑	1	-	0	0	0	0	0	APB2	APB1	APB0		AP: adjust the operational amplifier DCT: adjust the booster circuit for Idle mode
PWCTR5	10.2.14	0	↑	1	-	1	1	0	0	0	1	0	0	(C4h)	In partial mode + Full colors
		1	↑	1	-	0	0	0	0	0	APC2	APC1	APC0		AP: adjust the operational amplifier DCT: adjust the booster circuit for Idle mode
VMCTR1	10.2.15	0	↑	1	-	1	1	0	0	0	1	0	1	(C5h)	VCOM control 1
		1	↑	1	-	0	VMH6	VMH5	VMH4	VMH3	VMH2	VMH1	VMH0		VMH: VCOMH voltage control VML: VCOML voltage control
		1	↑	1	-	0	VML6	VML5	VML4	VML3	VML2	VML1	VML0		
VMOFCTR	10.2.16	0	↑	1	-	1	1	0	0	0	1	1	1	(C7h)	VCOM offset control
		1	↑	1	-	nVM*	VMF6	VMF5	VMF4	VMF3	VMF2	VMF1	VMF0		
STEP CTR	10.2.17	0	1	↑	-	1	1	0	0	1	0	0	1	(C9h)	Step124 setup
		1	↑	↑	-	DUAL_EN	STEP_DIV_EN	1	0	0	CP1_FREQ_SEL[2:0]				Adjust step1/2/4 booster frequency
					-	NW_MODE	0	0	0	0	CP2_FREQ_SEL[2:0]				
					-	0	0	0	0	0	1	0	0		
					-	0	0	0	0	0	CP4_FREQ_SEL[2:0]				
-	1	1	1	1	0	1	0	0	(F4h)						
-	0	1	0	1	0	0	0	1	0	1		Adjust read GRAM timing control function			
-	0	0	0	0	0	0	0	0	1	0	0				
8-color CTR	10.2.18	0	↑	1	-	1	1	1	1	1	0	0	0	(F8h)	
		1	↑	1	-	0	0	0	0	0	8-color	0	0		8-color detect function
PWCTR6	10.2.19	0	↑	1	-	1	1	1	1	1	1	0	0	(FCh)	Gate operational amplifier control
		1	↑	1	-	0	0	1	1	1	SAPA[2:0]				SAPA.: Normal mode SAPB: Idle mode SAPC: Partial mode
					-	0	0	1	1	1	1	0	0		
					-	0	1	1	1	1	SAPB[2:0]				
					-	0	1	1	1	1	1	0	0		
-	0	0	0	0	0	SAPC[2:0]									
-	0	0	0	0	0	0	0	0	1	0	0				

"-": Don't care

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Table 10.2.3 Panel Function Command List (3)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
WRID2	10.2.20	0	↑	1	-	1	1	0	1	0	0	0	1	(D1h)	LCM version code
		1	↑	1	-	1	0	ID26	ID25	ID24	ID23	ID22	ID21	ID20	
NVCTR2	10.2.23	0	↑	1	-	1	1	0	1	1	1	1	0	(DEh)	MTP read command
		1	↑	1	-	1	0	1	0	1	0	1	0	75	
NVCTR3	10.2.24	0	↑	1	-	1	1	0	1	1	1	1	1	(DFh)	MTP write command
		1	↑	1	-	0	1	0	1	0	1	0	1	55	
		1	↑	1	-	1	1	1	1	0	0	0	0	F0	
		1	↑	1	-	0	1	0	1	1	0	1	0	5A	

"-": Don't care

Note 1: The D1h to D3h registers are fixed for about ID code setting.

Note 2: The DEh and DFh registers are used for NV Memory function controller. (Ex: write, clear, etc.)

Table 10.2.4 Panel Function Command List (4)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function		
GAMCTRP1		0	↑	1	-	1	1	1	0	0	0	0	0	(E0h)	Set Gamma correction		
		1	↑	1	-	---	---	VRF0P[5:0]									Positive Polarity
		1	↑	1	-	---	---	VOS0P[5:0]									
		1	↑	1	-	---	---	PK0P[5:0]									
		1	↑	1	-	---	---	PK1P[5:0]									
		1	↑	1	-	---	---	PK2P[5:0]									
		1	↑	1	-	---	---	PK3P[5:0]									
		1	↑	1	-	---	---	PK4P[5:0]									
		1	↑	1	-	---	---	PK5P[5:0]									
		1	↑	1	-	---	---	PK6P[5:0]									
		1	↑	1	-	---	---	PK7P[5:0]									
		1	↑	1	-	---	---	PK8P[5:0]									
		1	↑	1	-	---	---	PK9P[5:0]									
		1	↑	1	-	---	---	SELV0P[5:0]									
		1	↑	1	-	---	---	SELV1P[5:0]									
		1	↑	1	-	---	---	SELV62P[5:0]									
		1	↑	1	-	---	---	SELV63P[5:0]									
GAMCTRN1		0	↑	1	-	1	1	1	0	0	0	0	1	(E1h)	Set Gamma correction		
		1	↑	1	-	---	---	VRF0N[5:0]									Negative Polarity
		1	↑	1	-	---	---	VOS0N[5:0]									
		1	↑	1	-	---	---	PK0N[5:0]									
		1	↑	1	-	---	---	PK1N[5:0]									
		1	↑	1	-	---	---	PK2N[5:0]									
		1	↑	1	-	---	---	PK3N[5:0]									
		1	↑	1	-	---	---	PK4N[5:0]									
		1	↑	1	-	---	---	PK5N[5:0]									
		1	↑	1	-	---	---	PK6N[5:0]									
		1	↑	1	-	---	---	PK7N[5:0]									
		1	↑	1	-	---	---	PK8N[5:0]									
		1	↑	1	-	---	---	PK9N[5:0]									
		1	↑	1	-	---	---	SELV0N[5:0]									
		1	↑	1	-	---	---	SELV1N[5:0]									
		1	↑	1	-	---	---	SELV1N[5:0]									

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GAMCTRN1	1	↑	1	-	---	---	SELV62N[5:0]							Negative Polariy
				-	0	0	0	0	0	0	0	0		
	1	↑	1	-	---	---	SELV63N[5:0]							
				-	0	0	0	0	0	0	0	0		

"-": Don't care

Note 1: E0-E1 registers are fixed for about Gamma adjusting.

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## 10.1.1 NOP (00h)

00H	NOP (No Operation)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
NOP	0	↑	1	-	0	0	0	0	0	0	0	0	(00h)
Parameter	No Parameter												-

NOTE: "-" Don't care

Description	-This command is empty command.
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## 10.1.2 SWRESET (01h): Software Reset

01H	SWRESET (Software Reset)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SWRESET	0	↑	1	-	0	0	0	0	0	0	0	1	(01h)
Parameter	No Parameter												-

NOTE: "-" Don't care

Description	<ul style="list-style-type: none"> <li>-When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values and all source &amp; gate outputs are set to VSS (display off).</li> <li>-It will be necessary to wait 5msec before sending new command following software reset.</li> <li>-The display module loads all default values to the registers during 5msec.</li> <li>-If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep Out command.</li> <li>-Software Reset command cannot be sent during Sleep Out sequence.</li> </ul>
-------------	---

## 10.1.3 RDDID (04h): Read Display ID

04H	RDDID (Read Display ID)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDID	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)
1 <sup>st</sup> Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2 <sup>nd</sup> Parameter	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	
3 <sup>rd</sup> Parameter	1	1	↑	-	'1'	ID26	ID25	ID24	ID23	ID22	ID21	ID20	

NOTE: "-" Don't care

Description	<ul style="list-style-type: none"> <li>-This read byte returns 24-bit display identification information.</li> <li>-The 1st parameter is dummy data</li> <li>-The 2nd parameter (ID17 to ID10): LCD module's manufacturer ID.</li> <li>-The 3rd parameter (ID27 to ID20): LCD module/driver version ID</li> </ul> <p>NOTE: Commands RDID1/2(DAh, DBh) read data correspond to the parameters 2,3, of the command 04h, respectively.</p>														
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="2">Default Value</th> </tr> <tr> <th>ID1</th> <th>ID2</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>-</td> <td>-</td> </tr> <tr> <td>S/W Reset</td> <td>29h</td> <td>29h</td> </tr> <tr> <td>H/W Reset</td> <td>81h</td> <td>81h</td> </tr> </tbody> </table>	Status	Default Value		ID1	ID2	Power On Sequence	-	-	S/W Reset	29h	29h	H/W Reset	81h	81h
Status	Default Value														
	ID1	ID2													
Power On Sequence	-	-													
S/W Reset	29h	29h													
H/W Reset	81h	81h													

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## 10.1.4 RDDST (09h): Read Display Status

09H	RDDST (Read Display Status)												(Code)
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDST	0	↑	1	-	0	0	0	0	1	0	0	1	(09h)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	BSTON	MY	MX	MV	ML	RGB	MH	ST24	
3rd Parameter	1	1	↑	-	ST23	IFPF2	IFPF1	IFPF0	IDMON	PTLON	SLOUT	NORON	
4th Parameter	1	1	↑	-	VSSON	ST14	INVON	ST12	ST11	DISON	TEON	GCS2	
5th Parameter	1	1	↑		GCS1	GCS0	TELOM	HSON	VSON	PCKON	DEON	ST0	

NOTE: "-" Don't care

Description	This command indicates the current status of the display as described in the table below:		
	Bit	Description	Value
	BSTON	Booster Voltage Status	'1' =Booster on, '0' =Booster off
	MY	Row Address Order (MY)	'1' =Decrement, (Bottom to Top, when MADCTL (36h) D7='1') '0' =Increment, (Top to Bottom, when MADCTL (36h) D7='0')
	MX	Column Address Order (MX)	'1' =Decrement, (Right to Left, when MADCTL (36h) D6='1') '0' =Increment, (Left to Right, when MADCTL (36h) D6='0')
	MV	Row/Column Exchange (MV)	'1' = Row/column exchange, (when MADCTL (36h) D5='1') '0' = Normal, (when MADCTL (36h) D5='0')
	ML	Scan Address Order (ML)	'1' =Decrement, (LCD refresh Top to Bottom, when MADCTL (36h) D4='1') '0' =Increment, (LCD refresh Bottom to Top, when MADCTL (36h) D4='0')
	RGB	RGB/ BGR Order (RGB)	'1' =BGR, (When MADCTL (36h) D3='1') '0' =RGB, (When MADCTL (36h) D3='0')
	MH	Horizontal Order	'1' =Decrement, (LCD refresh Left to Right, when MADCTL (36h) D2='1') '0' =Increment, (LCD refresh Right to Left, when MADCTL (36h) D2='0')
	ST24	For Future Use	'0'
	ST23	For Future Use	'0'
	IFPF2	Interface Color Pixel Format Definition	"011" = 12-bit / pixel,
	IFPF1		"101" = 16-bit / pixel,
	IFPF0		"110" = 18-bit / pixel, others are no define
	IDMON	Idle Mode On/Off	'1' = On, "0" = Off
	PTLON	Partial Mode On/Off	'1' = On, "0" = Off
	SLPOUT	Sleep In/Out	'1' = Out, "0" = In
	NORON	Display Normal Mode On/Off	'1' = Normal Display, '0' = Partial Display
	VSSON	Vertical Scrolling Status	'1' = Scroll on, "0" = Scroll off
	ST14	Horizontal Scroll Status	'0'
	INVON	Inversion Status	'1' = On, "0" = Off
	ST12	All Pixels On (Not Used)	'0'
	ST11	All Pixels Off (Not Used)	'0'
	DISON	Display On/Off	'1' = On, "0" = Off
	TEON	Tearing effect line on/off	'1' = On, "0" = Off
	GCSEL2	Gamma Curve Selection	"000" = GC0
	GCSEL1		"001" = GC1
	GCSEL0		"010" = GC2
			"011" = GC3
	TELOM	Tearing effect line mode	'0' = mode1, '1' = mode2
	HSON	Horizontal Sync. (HS, RGB I/F)	'1' = On, '0' = Off
	VSON	Vertical Sync. (VS, RGB I/F)	'1' = On, '0' = Off
	PCLKON	Pixel Clock (PCLK, RGB I/F)	'1' = On, '0' = Off
	DEON	Data Enable (DE, RGB I/F)	'1' = On, '0' = Off
	ST0	For Future Use	'0'

Note: ST0, ST5, ST9, ST11-ST15, ST19, ST23, ST24 are set to '0', when RGB I/F.

Default	Status	Default Value (ST31 to ST0)			
		ST[31-24]	ST[23-16]	ST[15-8]	ST[7-0]
	Power On Sequence	0000-0000	0110-0001	0000-0000	0000-0000
	S/W Reset	0xxx0xx00	0xxx-0001	0000-0000	0000-0000
	H/W Reset	0000-0000	0110-0001	0000-0000	0000-0000

## 10.1.5 RDDPM (0Ah): Read Display Power Mode

0AH	RDDPM (Read Display Power Mode)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDPM	0	↑	1	-	0	0	0	0	1	0	1	0	(0Ah)
1 <sup>st</sup> Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2 <sup>nd</sup> Parameter	1	1	↑		BSTON	IDMON	PTLON	SLPOUT	NORON	DISON	D1	D0	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	This command indicates the current status of the display as described in the table below:		
	Bit	Description	Value
	BSTON	Booster Voltage Status	'1' =Booster on, '0' =Booster off
	IDMON	Idle Mode On/Off	'1' = Idle Mode On, '0' = Idle Mode Off
	PTLON	Partial Mode On/Off	'1' = Partial Mode On, '0' = Partial Mode Off
	SLPON	Sleep In/Out	'1' = Sleep Out, '0' = Sleep In
	NORON	Display Normal Mode On/Off	'1' = Normal Display, '0' = Partial Display
	DISON	Display On/Off	'1' = Display On, '0' = Display Off
	D1	Not Used	'0'
	D0	Not Used	'0'
Default	Status		Default Value (D7 to D0)
	Power On Sequence		0000_1000(08h)
	S/W Reset		0000_1000(08h)
	H/W Reset		0000_1000(08h)

## 10.1.6 RDDMADCTL (0Bh): Read Display MADCTL

0BH	RDDMADCTL (Read Display MADCTL)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDMADCTL	0	↑	1	-	0	0	0	0	1	0	1	1	(0Bh)
1 <sup>st</sup> Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2 <sup>nd</sup> Parameter	1	1	↑		MY	MX	MV	ML	RGB	MH	D1	D0	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	This command indicates the current status of the display as described in the table below:		
	Bit	Description	Value
	MX	Row Address Order	'1' = Bottom to Top (When MADCTL B7='1') '0' = Top to Bottom (When MADCTL B7='0')
	MY	Column Address Order	'1' = Right to Left (When MADCTL B6='1') '0' = Left to Right (When MADCTL B6='0')
	MV	Row/Column Order (MV)	'1' = Row/column exchange (MV=1) '0' = Normal (MV=0)
	ML	Vertical Refresh Order	'1' =LCD Refresh Bottom to Top '0' =LCD Refresh Top to Bottom
	RGB	RGB/BGR Order	'1' =BGR, "0"=RGB
	MH	Horizontal order	'1' =LCD Refresh Right to Left '0' =LCD Refresh Left to Right
	D1	Not Used	'0'
	D0	Not Used	'0'
Default	Status		Default Value (D7 to D0)
	Power On Sequence		0000_0000 (00h)
	S/W Reset		No change
	H/W Reset		0000_0000 (00h)

## 10.1.7 RDDCOLMOD (0Ch): Read Display Pixel Format

0Ch	RDDCOLMOD (Read Display Pixel Format)												(Code)
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDCOLMOD	0	↑	1	-	0	0	0	0	1	1	0	0	(0Ch)
1 <sup>st</sup> Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2 <sup>nd</sup> Parameter	1	1	↑	-	VIPF3	VIPF2	VIPF1	VIPF0	D3	IFPF2	IFPF1	IFPF0	-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	This command indicates the current status of the display as described in the table below:		
	IFPF[2:0]		MCU Interface Color Format
	011	3	12-bit/pixel
	101	5	16-bit/pixel
	110	6	18-bit/pixel
	111	7	No used
	Others are no define and invalid		
	VIFPF[2:0]		RGB Interface Color Format
	0101	5	16-bit/pixel (1-times data transfer)
	0110	6	18-bit/pixel (1-times data transfer)
0111	7	No used	
1110	14	18-bit/pixel (3-times data transfer)	
Others are no define and invalid			
Default	Status		Default Value
			IFPF[2:0]      VIPF[3:0]
	Power On Sequence		0110 (18 bits/pixel)      0110 (18 bits/pixel)
	S/W Reset		No Change      No Change
	H/W Reset		0110 (18 bits/pixel)      0110 (18 bits/pixel)

## 10.1.8 RDDDIM (0Dh): Read Display Image Mode

0Dh	RDDIM (0Dh): Read Display Image Mode												(Code)
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDIM	0	↑	1	-	0	0	0	0	1	1	0	1	(0Dh)
1 <sup>st</sup> Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2 <sup>nd</sup> Parameter	1	1	↑	-	VSSON	D6	INVON	D4	D3	GCS2	GCS1	GCS0	-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	This command indicates the current status of the display as described in the table below:		
	Bit	Description	Value
	VSSON	Vertical Scrolling On/Off	"1" = Vertical scrolling is On, "0" = Vertical scrolling is Off
	D6	Horizontal Scrolling On/Off	"0" (Not used)
	INVON	Inversion On/Off	"1" = Inversion is On, "0" = Inversion is Off
	D4	All Pixels On	"0" (Not used)
	D3	All Pixels Off	"0" (Not used)
	GCS2	Gamma Curve Selection	"000" = GC0, "001" = GC1, "010" = GC2, "011" = GC3, "100" to "111" = Not defined
	GCS1		
	GCS0		
Default	Status		Default Value(D7 to D0)
	Power On Sequence		0000_0000 (00h)
	S/W Reset		0000_0000 (00h)
	H/W Reset		0000_0000 (00h)



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## 10.1.9 RDDSM (0Eh): Read Display Signal Mode

0EH	RDDSM (0Eh): Read Display Signal Mode												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDSM	0	↑	1	-	0	0	0	0	1	1	1	0	(0Eh)
1 <sup>st</sup> Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2 <sup>nd</sup> Parameter	1	1	↑	-	TEON	TELOM	HSON	VSON	PCKON	DEON	D1	D0	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	This command indicates the current status of the display as described in the table below:		
	Bit	Description	Value
	TEON	Tearing Effect Line On/Off	"1" = On, "0" = Off
	TELOM	Tearing effect line mode	"1" = mode1, "0" = mode2
	HSON	Horizontal Sync. (RGB I/F) On/Off	"1" = On, "0" = Off
	VSON	Vertical Sync. (RGB I/F) On/Off	"1" = On, "0" = Off
	PCKON	Pixel Clock (PCLK, RGB I/F) On/Off	"1" = On, "0" = Off
	DEON	Data Enable (DE, RGB I/F) On/Off	"1" = On, "0" = Off
	D1	Not Used	"1" = On, "0" = Off
D0	Not Used	"1" = On, "0" = Off	
Default	Status		Default Value(D7~D0)
	Power On Sequence		0000_0000 (00h)
	S/W Reset		0000_0000 (00h)
	H/W Reset		0000_0000 (00h)

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## 10.1.10 SLPIN (10h): Sleep In

10H	SLPIN (Sleep In)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SLPIN	0	↑	1	-	0	0	0	1	0	0	0	0	(10h)
1 <sup>st</sup> Parameter	No parameter												-

NOTE: “-” Don't care, can be set to VDDI or DGND level

Description	<p>-This command causes the LCD module to enter the minimum power consumption mode. -In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped.</p> <p>* Note: complete 1 frame display (ex: continue 2-falling edges of VS)</p>								
	<p>-This command has no effect when module is already in sleep in mode. Sleep In Mode can only be exit by the Sleep Out Command (11h). -It will be necessary to wait <u>5msec</u> before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. -It will be necessary to wait <u>120msec</u> after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.</p>								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Sleep in mode</td> </tr> <tr> <td>S/W Reset</td> <td>Sleep in mode</td> </tr> <tr> <td>H/W Reset</td> <td>Sleep in mode</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Sleep in mode	S/W Reset	Sleep in mode	H/W Reset	Sleep in mode
Status	Default Value								
Power On Sequence	Sleep in mode								
S/W Reset	Sleep in mode								
H/W Reset	Sleep in mode								

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## 10.1.11 SLPOUT (11h): Sleep Out

11H	SLPOUT (Sleep Out)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SLPOUT	0	↑	1	-	0	0	0	1	0	0	0	1	(11h)
1st Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	<p>-This command turns off sleep mode. -In this mode the DC/DC converter is enabled, Internal display oscillator is started, and panel scanning is started.</p> <p>* Note: complete 1 frame display (ex: continue 2-falling edges of VS)</p>								
	<p>-This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be exit by the Sleep In Command (10h). -It will be necessary to wait <u>5msec</u> before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. -DRIVER loads all default values of extended and test command to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if those default and register values are same when this load is done and when the DRIVER is already Sleep Out mode. -DRIVER is doing self-diagnostic functions during this 5msec. See also section 9.20. -It will be necessary to wait <u>120msec</u> after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent</p>								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Sleep in mode</td> </tr> <tr> <td>S/W Reset</td> <td>Sleep in mode</td> </tr> <tr> <td>H/W Reset</td> <td>Sleep in mode</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Sleep in mode	S/W Reset	Sleep in mode	H/W Reset	Sleep in mode
Status	Default Value								
Power On Sequence	Sleep in mode								
S/W Reset	Sleep in mode								
H/W Reset	Sleep in mode								

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## 10.1.12 PTLON (12h): Partial Display Mode On

12H	PTLON (12h): Partial Display Mode On												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PTLON	0	↑	1	-	0	0	0	1	0	0	1	0	(12h)
1 <sup>st</sup> Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	-This command turns on Partial mode. The partial mode window is described by the Partial Area command (30h)	
	-To leave Partial mode, the Normal Display Mode On command (13H) should be written.	
Default	Status	
	Power On Sequence	
	S/W Reset	
	H/W Reset	
		Default Value
		Normal Mode On
		Normal Mode On
		Normal Mode On

## 10.1.13 NORON (13h): Normal Display Mode On

13H	NORON (Normal Display Mode On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
NORON	0	↑	1	-	0	0	0	1	0	0	1	1	(13h)
1 <sup>st</sup> Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	-This command returns the display to normal mode.	
	-Normal display mode on means <u>Partial mode off</u> , <u>Scroll mode Off</u> .	
		-Exit from NORON by the Partial mode On command (12h)
Default	Status	
	Power On Sequence	
	S/W Reset	
	H/W Reset	
		Default Value
		Normal Mode On
		Normal Mode On
		Normal Mode On

## 10.1.14 INVOFF (20h): Display Inversion Off

20H	INVOFF (Normal Display Mode Off)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
INVOFF	0	↑	1	-	0	0	1	0	0	0	0	0	(20h)
1 <sup>st</sup> Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	-This command is used to recover from display inversion mode.	
	<p>(Example)</p>	
Default	Status	
	Power On Sequence	
	S/W Reset	
	H/W Reset	
		Default Value
		Display Inversion off
		Display Inversion off
		Display Inversion off

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## 10.1.15 INVON (21h): Display Inversion On

21H		IVNOFF (Display Inversion On)											
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
INVON	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)
1 <sup>st</sup> Parameter	No Parameter												-

NOTE: “-” Don't care, can be set to VDDI or DGND level

Description	<p>-This command is used to enter into display inversion mode -To exit from Display Inversion On, the Display Inversion Off command (20h) should be written.</p>									
	<p>(Example)</p>									
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display Inversion off</td> </tr> <tr> <td>S/W Reset</td> <td>Display Inversion off</td> </tr> <tr> <td>H/W Reset</td> <td>Display Inversion off</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	Display Inversion off	S/W Reset	Display Inversion off	H/W Reset	Display Inversion off
	Status	Default Value								
	Power On Sequence	Display Inversion off								
	S/W Reset	Display Inversion off								
H/W Reset	Display Inversion off									

## 10.1.16 GAMSET (26h): Gamma Set

26H		GAMSET (Gamma Set)											
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GAMSET	0	↑	1	-	0	0	1	0	0	1	1	0	(26h)
1 <sup>st</sup> Parameter	1	↑	1	-	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	

NOTE: “-” Don't care, can be set to VDDI or DGND level

Description	<p>-This command is used to select the desired Gamma curve for the current display. A maximum of 4 curves can be selected. The curves are defined in section 9.17 The curve is selected by setting the appropriate bit in the parameter as described in the Table.</p>																			
	<table border="1"> <thead> <tr> <th>GC [7:0]</th> <th>Parameter</th> <th>Curve Selected</th> </tr> </thead> <tbody> <tr> <td></td> <td></td> <td>GS=1</td> </tr> <tr> <td>01h</td> <td>GC0</td> <td>Gamma Curve 1 (G2.2)</td> </tr> <tr> <td>02h</td> <td>GC1</td> <td>Gamma Curve 2 (G1.8)</td> </tr> <tr> <td>04h</td> <td>GC2</td> <td>Gamma Curve 3 (G2.5)</td> </tr> <tr> <td>08h</td> <td>GC3</td> <td>Gamma Curve 4 (G1.0)</td> </tr> </tbody> </table>		GC [7:0]	Parameter	Curve Selected			GS=1	01h	GC0	Gamma Curve 1 (G2.2)	02h	GC1	Gamma Curve 2 (G1.8)	04h	GC2	Gamma Curve 3 (G2.5)	08h	GC3	Gamma Curve 4 (G1.0)
	GC [7:0]	Parameter	Curve Selected																	
			GS=1																	
	01h	GC0	Gamma Curve 1 (G2.2)																	
02h	GC1	Gamma Curve 2 (G1.8)																		
04h	GC2	Gamma Curve 3 (G2.5)																		
08h	GC3	Gamma Curve 4 (G1.0)																		
<p>Note: All other values are undefined.</p>																				
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>01h</td> </tr> <tr> <td>S/W Reset</td> <td>01h</td> </tr> <tr> <td>H/W Reset</td> <td>01h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	01h	S/W Reset	01h	H/W Reset	01h										
	Status	Default Value																		
	Power On Sequence	01h																		
	S/W Reset	01h																		
H/W Reset	01h																			

# ST7773

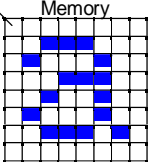
## 10.1.17 DISPOFF (28h): Display Off

28H	DISPOFF (Display Off)												(Code)
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DISPOFF	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)
1 <sup>st</sup> Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

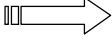
-This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted.  
 -Exit from this command by Display On (29h)

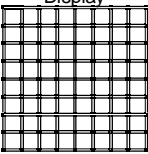
Top-Left (0,0)



Memory

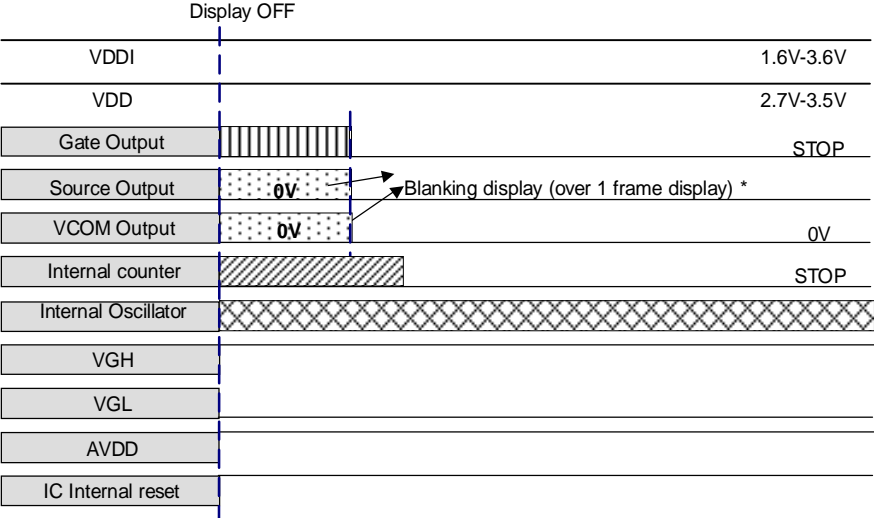
(Example)





Display

**Timing Diagram for Display OFF:**



\* Note: complete 1 frame display (ex: continue 2-falling edges of VS)

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

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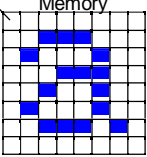
## 10.1.18 DISPON (29h): Display On

29H	DISPON (Display On)												(Code)
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DISPON	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)
1 <sup>st</sup> Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

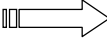
-This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled.

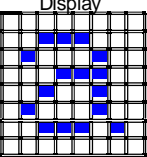
Top-Left (0,0)



Memory

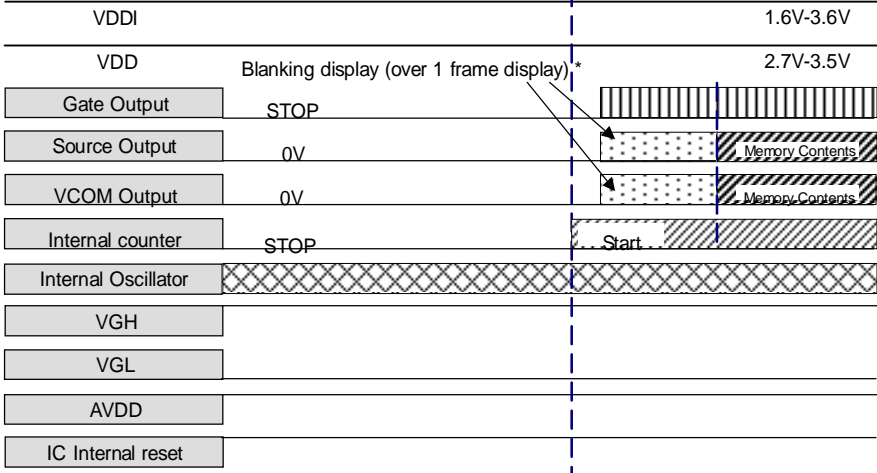
(Example)





Display

Display ON



\* Note: complete 1 frame display (ex: continue 2-falling edges of VS)

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

## 10.1.19 CASET (2Ah): Column Address Set

2AH	CASET(Colume Address Set)_												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GAMSET	0	↑	1	-	0	0	1	0	0	1	1	0	(2Ah)
1 <sup>st</sup> Parameter	1	↑	1	-	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8	
2 <sup>nd</sup> Parameter	1	↑	1		XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	
3 <sup>rd</sup> Parameter	1	↑	1		XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8	
4 <sup>th</sup> Parameter	1	↑	1		XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	<p>-The value of XS [15:0] and XE [15:0] are referred when RAMWR command comes.                      -Each value represents one column line in the Frame Memory.</p> <p style="text-align: center;">(Example)</p> <div style="text-align: center;"> </div>																	
Restriction	<p>XS [15:0] always must be equal to or less than XE [15:0]                      When XS [15:0] or XE [15:0] is greater than maximum address like below, data of out of range will be ignored.                      (Parameter range: <math>0 \leq XS [15:0] \leq XE [15:0] \leq 175</math> (00AFh)): MV="0"                      (Parameter range: <math>0 \leq XS [15:0] \leq XE [15:0] \leq 219</math> (00DBh)): MV="1"</p>																	
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="3">Default Value</th> </tr> <tr> <th>XS [15:0]</th> <th>XE [15:0] (MV='0')</th> <th>XE [15:0] (MV='1')</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td rowspan="3" style="text-align: center;">0000h</td> <td colspan="2" style="text-align: center;">00AFh (175)</td> </tr> <tr> <td>S/W Reset</td> <td style="text-align: center;">00AFh (175)</td> <td style="text-align: center;">00DBh (219)</td> </tr> <tr> <td>H/W Reset</td> <td colspan="2" style="text-align: center;">00AFh (175)</td> </tr> </tbody> </table>	Status	Default Value			XS [15:0]	XE [15:0] (MV='0')	XE [15:0] (MV='1')	Power On Sequence	0000h	00AFh (175)		S/W Reset	00AFh (175)	00DBh (219)	H/W Reset	00AFh (175)	
Status	Default Value																	
	XS [15:0]	XE [15:0] (MV='0')	XE [15:0] (MV='1')															
Power On Sequence	0000h	00AFh (175)																
S/W Reset		00AFh (175)	00DBh (219)															
H/W Reset		00AFh (175)																



## 10.1.20 RASET (2Bh): Row Address Set

2BH	RASET (Row Address Set)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RASET (2Bh)	0	↑	1	-	0	0	1	0	1	0	1	1	(2Bh)
1st Parameter	1	↑	1	-	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8	
2nd Parameter	1	↑	1	-	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
3rd Parameter	1	↑	1	-	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8	
4th Parameter	1	↑	1	-	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	<p>The value of YS [15:0] and YE [15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.</p> <p style="text-align: center;">Example</p>																			
Restriction	<p>YS [15:0] always must be equal to or less than YE [15:0] When YS [15:0] or YE [15:0] are greater than maximum row address like below, data of out of range will be ignored.</p> <p>(Parameter range: <math>0 \leq YS [15:0] \leq YE [15:0] \leq 219</math> (00DBh)): MV="0" (Parameter range: <math>0 \leq YS [15:0] \leq YE [15:0] \leq 175</math> (009Fh)): MV="1"</p>																			
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="3">Default Value</th> </tr> <tr> <th>YS [15:0]</th> <th>YE [15:0] (MV='0')</th> <th>YE [15:0] (MV='1')</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>0000h</td> <td colspan="2" style="text-align: center;">00DBh (219)</td> </tr> <tr> <td>S/W Reset</td> <td>0000h</td> <td>00DBh (219)</td> <td>00AFh (175)</td> </tr> <tr> <td>H/W Reset</td> <td>0000h</td> <td colspan="2" style="text-align: center;">00DBh (219)</td> </tr> </tbody> </table>	Status	Default Value			YS [15:0]	YE [15:0] (MV='0')	YE [15:0] (MV='1')	Power On Sequence	0000h	00DBh (219)		S/W Reset	0000h	00DBh (219)	00AFh (175)	H/W Reset	0000h	00DBh (219)	
Status	Default Value																			
	YS [15:0]	YE [15:0] (MV='0')	YE [15:0] (MV='1')																	
Power On Sequence	0000h	00DBh (219)																		
S/W Reset	0000h	00DBh (219)	00AFh (175)																	
H/W Reset	0000h	00DBh (219)																		

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## 10.1.21 RAMWR (2Ch): Memory Write

2CH	RAMWR (Memory Write)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RAMWR	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)
1st Parameter	1	↑	1	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	-
	1	↑	1										
Nth Parameter	1	↑	1	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	<p>-When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions.                      -The Start Column/Start Row positions are different in accordance with MADCTL setting. (See section 9.12)                      -Sending any other command can stop Frame Write.</p> <p>In all color modes, there is no restriction on length of parameters.                      -1. 176x220 memory base (GM = '00')                      176x220x18-bit memory can be written by this command                      Memory range: (0000h,0000h) -&gt; (00AFh, 00DBh)</p>								
	Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Contents of memory is set randomly</td> </tr> <tr> <td>S/W Reset</td> <td>Contents of memory is not cleared</td> </tr> <tr> <td>H/W Reset</td> <td>Contents of memory is not cleared</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Contents of memory is set randomly	S/W Reset	Contents of memory is not cleared	H/W Reset
Status	Default Value								
Power On Sequence	Contents of memory is set randomly								
S/W Reset	Contents of memory is not cleared								
H/W Reset	Contents of memory is not cleared								

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## 10.1.22 RAMHD (2Eh): Memory Read

2EH	RAMHD (Memory Read)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RAMHD	0	↑	1	-	0	0	1	0	1	1	1	0	(2Eh)
1 <sup>st</sup> Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2 <sup>nd</sup> Parameter	1	1	↑	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	-
	1	1	↑										
(N+1) <sup>th</sup> Parameter	1	1	↑	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	-

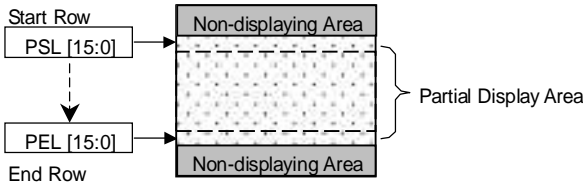

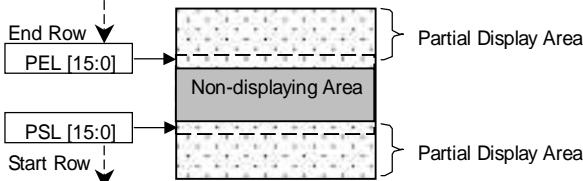
NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	<ul style="list-style-type: none"> <li>-This command is used to transfer data from frame memory to MCU.</li> <li>-When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions.</li> <li>-The Start Column/Start Row positions are different in accordance with MADCTL setting. (See section 9.12)</li> <li>-Then D[17:0] is read back from the frame memory and the column register and the row register incremented as section 9.10.2.</li> <li>-Frame Read can be cancelled by sending any other command.</li> <li>-See section 9.8 "Data color coding" for color coding (18-bit cases), when there is used 8, 9, 16 and 18-bit data lines for image data.</li> </ul>								
	Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Contents of memory is set randomly</td> </tr> <tr> <td>S/W Reset</td> <td>Contents of memory is not cleared</td> </tr> <tr> <td>H/W Reset</td> <td>Contents of memory is not cleared</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Contents of memory is set randomly	S/W Reset	Contents of memory is not cleared	H/W Reset
Status	Default Value								
Power On Sequence	Contents of memory is set randomly								
S/W Reset	Contents of memory is not cleared								
H/W Reset	Contents of memory is not cleared								

## 10.1.25 PTLAR (30h): Partial Area

30H	PTLAR (Partial Area)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PTLAR	0	↑	1	-	0	0	1	1	0	0	0	0	(30h)
1 <sup>st</sup> Parameter	1	↑	1	-	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8	
2 <sup>nd</sup> Parameter	1	↑	1	-	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	
3 <sup>rd</sup> Parameter	1	↑	1	-	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8	
4 <sup>th</sup> Parameter	1	↑	1	-	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0	

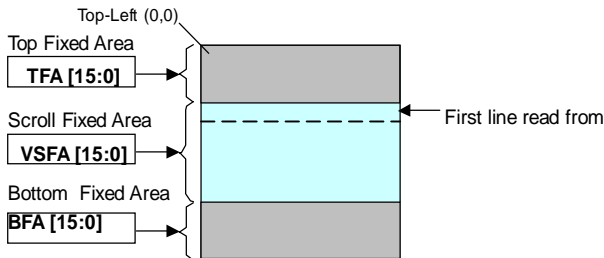
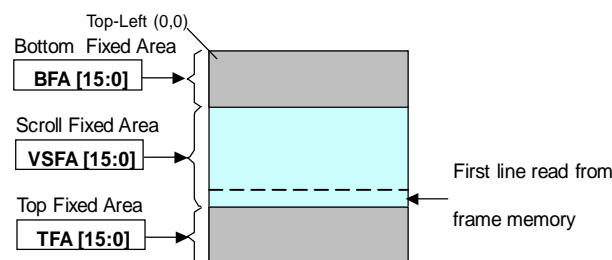
NOTE: "-" Don't care, can be set to VDDI or DGND level

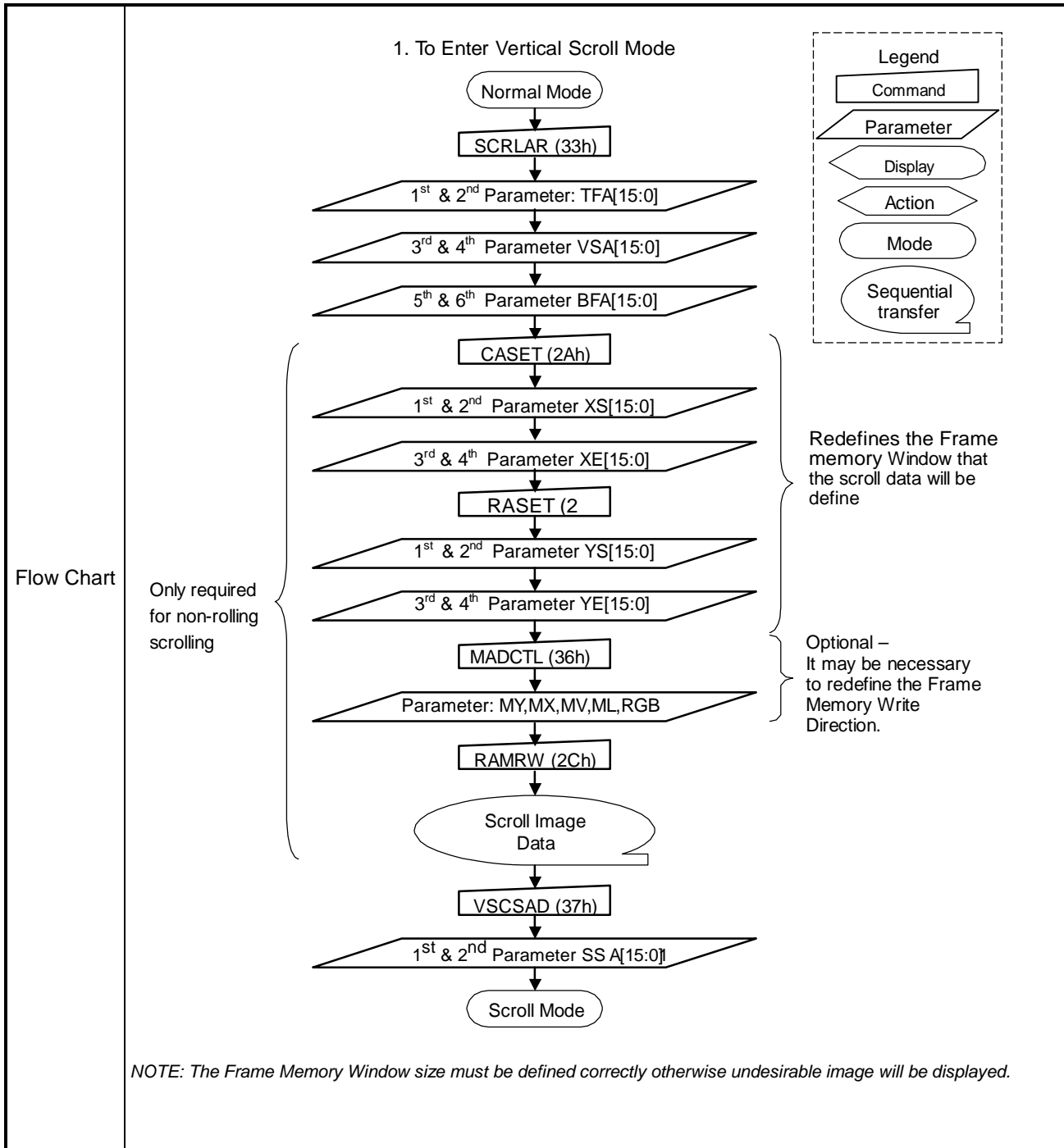
Description	<p>-This command defines the partial mode's display area.                  -There are 4 parameters associated with this command, the first defines the Start Row (PSL) and the second the End Row (PEL), as illustrated in the figures below. PSL and PEL refer to the Frame Memory row address counter.</p> <p>-If End Row &gt; Start Row, when MADCTL ML='0'</p>  <p>-If End Row &gt; Start Row, when MADCTL ML='1'</p>  <p>-If End Row &lt; Start Row, when MADCTL ML='0'</p>  <p>-If End Row = Start Row then the Partial Area will be one row deep.</p>									
	Default	<table border="1"> <thead> <tr> <th>Status</th> <th>PSL [15:0]</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td rowspan="3">0000h</td> <td>PEL [15:0]</td> </tr> <tr> <td>S/W Reset</td> <td rowspan="2">00DBh</td> </tr> <tr> <td>H/W Reset</td> </tr> </tbody> </table>	Status	PSL [15:0]	Default Value	Power On Sequence	0000h	PEL [15:0]	S/W Reset	00DBh
Status	PSL [15:0]	Default Value								
Power On Sequence	0000h	PEL [15:0]								
S/W Reset		00DBh								
H/W Reset										

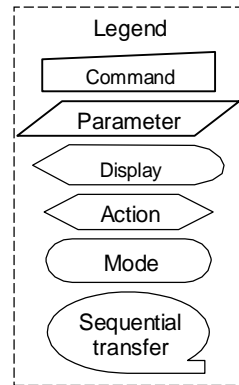
## 10.1.23 SCRLAR (33h): Scroll Area

33H	SCRLAR (Scroll Area)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PTLAR	0	↑	1	-	0	0	1	1	0	0	1	1	(33h)
1 <sup>st</sup> Parameter	1	↑	1	-	TFA15	TFA 14	TFA 13	TFA 12	TFA 11	TFA 10	TFA 9	TFA 8	00h
2 <sup>nd</sup> Parameter	1	↑	1	-	TFA 7	TFA 6	TFA 5	TFA 4	TFA 3	TFA 2	TFA 1	TFA 0	00h
3 <sup>rd</sup> Parameter	1	↑	1	-	VSA15	VSA 14	VSA 13	VSA 12	VSA 11	VSA 10	VSA 9	VSA 8	
4 <sup>th</sup> Parameter	1	↑	1	-	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0	
5 <sup>th</sup> Parameter	1	↑	1	-	BFA15	BFA 14	BFA 13	BFA 12	BFA 11	BFA 10	BFA 9	BFA 8	00h
6 <sup>th</sup> Parameter	1	↑	1	-	BFA 7	BFA 6	BFA 5	BFA 4	BFA 3	BFA 2	BFA 1	BFA 0	00h

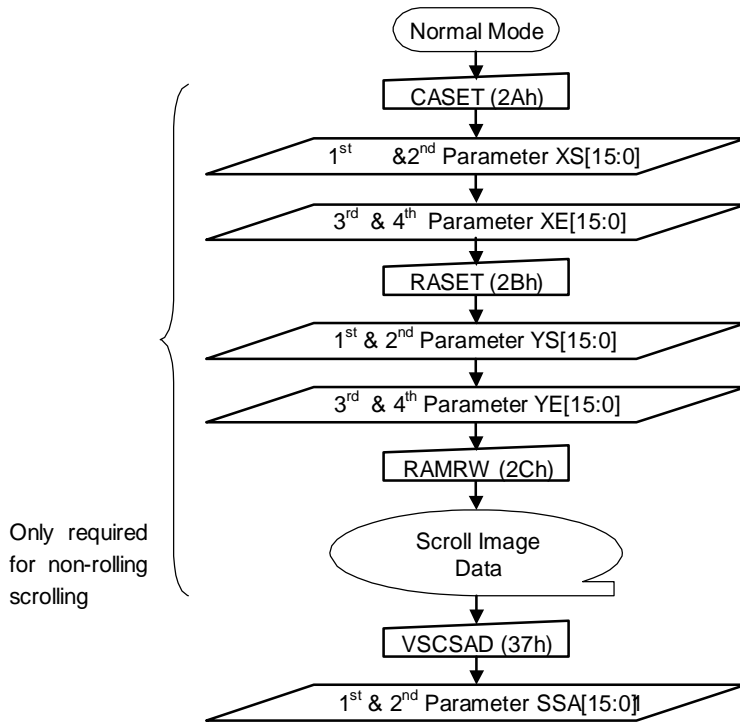
NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	<p>-This command defines the Vertical Scrolling Area of the display. When MADCTL ML=0</p> <ul style="list-style-type: none"> <li>- The 1<sup>st</sup> &amp; 2<sup>nd</sup> parameter TFA [15:0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).</li> <li>- The 3<sup>rd</sup> &amp; 4<sup>th</sup> parameter VSA [15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address)</li> <li>- The first line appears immediately after the bottom most line of the Top Fixed Area.</li> <li>- The 5<sup>th</sup> &amp; 6<sup>th</sup> parameter BFA [15:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).</li> <li>- TFA, VSA and BFA refer to the Frame Memory row address.</li> </ul> 													
	<p>When MADCTL ML=1</p> <ul style="list-style-type: none"> <li>- The 1<sup>st</sup> &amp; 2<sup>nd</sup> parameter TFA [15:0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).</li> <li>- The 3<sup>rd</sup> &amp; 4<sup>th</sup> parameter VSA [15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address)</li> <li>- The first line appears immediately after the top most line of the Top Fixed Area.</li> <li>- The 5<sup>th</sup> &amp; 6<sup>th</sup> parameter BFA [15:0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).</li> </ul> 													
Default	<p>See Section 9.10.1 for details of the Memory to Display Mapping.</p> <p>-The condition is <math>0 \leq (TFA+VSA+BFA) \leq 220</math>, otherwise Scrolling mode is undefined.</p> <p>-In Vertical Scroll Mode, MADCTL parameter MV should be set to '0'-this only affects the Frame Memory Write.</p> <table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="3">Default Value</th> </tr> <tr> <th>TFA [15:0]</th> <th>VSA [15:0]</th> <th>BFA [15:0]</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td rowspan="3">0000h</td> <td colspan="2" rowspan="3">00DBh</td> </tr> <tr> <td>S/W Reset</td> </tr> <tr> <td>H/W Reset</td> </tr> </tbody> </table>	Status	Default Value			TFA [15:0]	VSA [15:0]	BFA [15:0]	Power On Sequence	0000h	00DBh		S/W Reset	H/W Reset
Status	Default Value													
	TFA [15:0]	VSA [15:0]	BFA [15:0]											
Power On Sequence	0000h	00DBh												
S/W Reset														
H/W Reset														

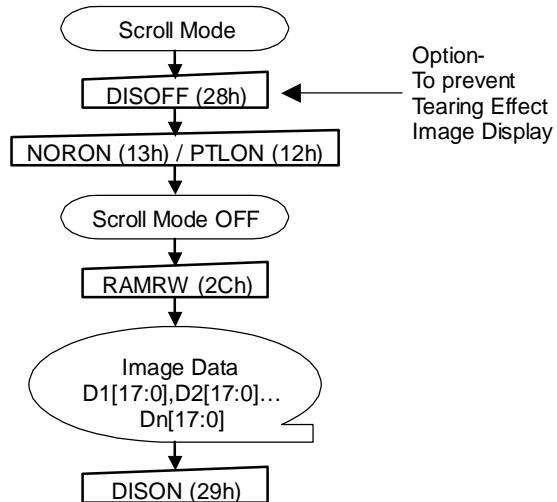




2. Continuous Scroll



3. To Exit Vertical Scroll Mode



NOTE: Scroll Mode can be exit by both the Normal Display Mode On (13h) and Partial Mode On (12h) commands.

## 10.1.24 TEOFF (34h): Tearing Effect Line OFF

34H	TEOFF (Tearing Effect Line OFF)												(Code)
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEOFF	0	↑	1	-	0	0	1	1	0	1	0	0	(34h)
1st Parameter	No Parameter												-

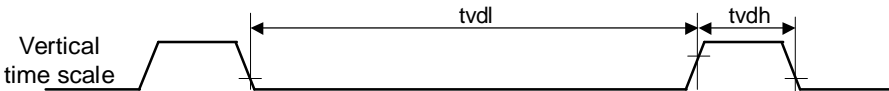
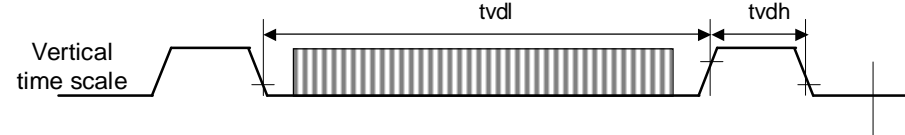
NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	-This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.		
Default	Status	Default Value	
		RCM1,RCM0 = "00","1x"	RCM1,RCM0 = "01"
	Power On Sequence	OFF	
	S/W Reset		
H/W Reset			

## 10.1.25 TEON (35h): Tearing Effect Line ON

35H	TEON (Tearing Effect Line ON)												(Code)
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEON	0	↑	1	-	0	0	1	1	0	1	0	1	(35h)
1st Parameter	1	↑	1	-	0	0	0	0	0	0	0	TELOM	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	<p>-This command is used to turn ON the Tearing Effect output signal from the TE signal line.</p> <p>-This output is not affected by changing MADCTL bit ML.</p> <p>-The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line. ("-="Don't Care).</p> <p>- When M='0':</p> <p style="text-align: center;">The Tearing Effect Output line consists of V-Blanking information only.</p>  <p>- When M='1':</p> <p style="text-align: center;">The Tearing Effect Output line consists of both V-Blanking and H-Blanking information.</p>  <p>Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.</p>									
	Default	<table border="1"> <thead> <tr> <th>Status</th> <th colspan="2">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td colspan="2" rowspan="3">Tearing effect off &amp; TELOM=0</td> </tr> <tr> <td>S/W Reset</td> </tr> <tr> <td>H/W Reset</td> </tr> </tbody> </table>		Status	Default Value		Power On Sequence	Tearing effect off & TELOM=0		S/W Reset
Status	Default Value									
Power On Sequence	Tearing effect off & TELOM=0									
S/W Reset										
H/W Reset										



10.1.26 MADCTL (36h): Memory Data Access Control

36H	MADCTL (Memory Data Access Control)												(Code)
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
MADCTL	0	↑	1	-	0	0	1	1	0	1	1	0	(36h)
1st Parameter	1	↑	1	-	MY	MX	MV	ML	RGB	MH	0	0	00h

NOTE: "-" Don't care, can be set to VDDI or DGND level

-This command defines read/ write scanning direction of frame memory.  
 -Bit Assignment

Bit	NAME	DESCRIPTION
MY	Row Address Order	These 3bits controls MCU to memory write/read direction. (See Section 9.12)
MX	Column Address Order	
MV	Row/Column Exchange	
ML	Vertical Refresh Order	LCD vertical refresh direction control '0' = LCD vertical refresh Top to Bottom '1' = LCD vertical refresh Bottom to Top
RGB	RGB-BGR ORDER	Color selector switch control '0' =RGB color filter panel, '1' =BGR color filter panel)
MH	Horizontal Refresh Order	LCD horizontal refresh direction control '0' = LCD horizontal refresh Left to right '1' = LCD horizontal refresh right to left

Description

**ML: Vertical Refresh Order**

**RGB: RGB-BGR Order**

Description	<p style="text-align: center;"><b>MH: Horizontal refresh Order</b></p> <p>The diagram illustrates the horizontal refresh order for two memory layout modes: ML=0 and ML=1. Each mode shows a 10x10 grid for 'Memory' and a corresponding 10x10 grid for 'Display'. The origin (0,0) is at the top-left corner. For ML=0, the refresh order is row-major, starting from the top-left and moving right across each row, then down to the next row. For ML=1, the refresh order is also row-major but starts from the top-right and moves left across each row, then down to the next row. Arrows and labels ('Sent First', 'Sent 2nd', 'Sent 3rd', 'Sent Last') indicate the direction of data flow from memory to display.</p>									
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Status</th> <th style="width: 50%;">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>MY=0, MX=0, MV=0, ML=0, RGB=0, MH=0</td> </tr> <tr> <td>S/W Reset</td> <td>No Change</td> </tr> <tr> <td>H/W Reset</td> <td>MY=0, MX=0, MV=0, ML=0, RGB=0, MH=0</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	MY=0, MX=0, MV=0, ML=0, RGB=0, MH=0	S/W Reset	No Change	H/W Reset	MY=0, MX=0, MV=0, ML=0, RGB=0, MH=0
Status	Default Value									
Power On Sequence	MY=0, MX=0, MV=0, ML=0, RGB=0, MH=0									
S/W Reset	No Change									
H/W Reset	MY=0, MX=0, MV=0, ML=0, RGB=0, MH=0									

10.1.27 VSCSAD (37h): Vertical Scroll Start Address of RAM

37H	VSCSAD (Vertical Scroll Start Address of RAM)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VSCSAD	0	↑	1	-	0	0	1	1	0	1	1	1	(37h)
1st Parameter	1	↑	1	-	0	0	0	0	0	0	0	SSA8	00h
2nd Parameter	1	↑	1		SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	00h

NOTE: “-” Don’t care, can be set to VDDI or DGND level

-This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode.  
 -The Vertical Scrolling Start Address command has one parameter which describes which line in the Frame Memory will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:  
 -This command Start the scrolling.  
 -Exit from V-scrolling mode by commands Partial mode On (12h) or Normal mode On (13h).

**When MADCTL ML= ‘0’**  
 Example:  
 –When Top Fixed Area=Bottom Fixed Area=00, Vertical Scrolling Area=220 and Vertical Scrolling Pointer SSA= ‘3’.

(Example)

Top-Left (0,0) Memory

SSA[15:0] → Scroll start address

Scan address

0  
1  
2  
3  
218  
219

Display

G1  
G2  
G3  
G4  
G219  
G220

**When MADCTL ML = ‘1’**  
 Example:  
 –When Top Fixed Area= Bottom Fixed Area=00, Vertical Scrolling Area=220 and SSA= ‘3’

(Example)

Top-Left (0,0) Memory

SSA[15:0] → Scroll start address

Scan address

219  
218  
3  
2  
1  
0

Display

G1  
G2  
G3  
G4  
G219  
G220

NOTE: -When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect.  
 -SSA refers to the Frame Memory scan address.

Default	Status	Default Value
	Power On Sequence	0000h
	S/W Reset	0000h
	H/W Reset	0000h

## 10.1.28 IDMOFF (38h): Idle Mode Off

38H	IDMOFF (Idle Mode Off)												(Code)
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
IDMOFF	0	↑	1	-	0	0	1	1	1	0	0	0	(38h)
1st Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	-This command is used to recover from Idle mode on. -In the idle off mode, 1. LCD can display 4096, 65k or 262k colors. 2. Normal frame frequency is applied.											
	Default	Status						Default Value				
Power On Sequence						Idle Mode Off						
S/W Reset						Idle Mode Off						
H/W Reset						Idle Mode Off						

## 10.1.29 IDMON (39h): Idle Mode On

39H	IDMON (Idle Mode On)												(Code)
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
IDMON	0	↑	1	-	0	0	1	1	1	0	0	1	(39h)
1st Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	-This command is used to enter into Idle mode on. -There will be no abnormal visible effect on the display mode change transition. -In the idle on mode, 1. Color expression is reduced. The primary and the secondary colors using MSB of each R,G and B in the Frame Memory, 8 color depth data is displayed. 2. 8-Color mode frame frequency is applied. 3. Exit from IDMON by Idle Mode Off (38h) command											
	<div style="display: flex; align-items: center; justify-content: center;"> <div style="text-align: center;"> <p>Top-Left (0,0)</p> <p>Memory</p> </div> <div style="margin: 0 20px;"> <p>(Example)</p> </div> <div style="text-align: center;"> <p>Display</p> </div> </div>											
Default	Color						Default Value					
	Black						0xxxxx					
	Blue						0xxxxx					
	Red						0xxxxx					
	Magenta						0xxxxx					
	Green						1xxxxx					
	Cyan						1xxxxx					
Yellow						1xxxxx						
White						1xxxxx						

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## 10.1.30 COLMOD (3Ah): Interface Pixel Format

3AH	COLMOD (3Ah): Interface Pixel Format												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
COLMOD	0	↑	1	-	0	0	1	1	1	0	1	0	(3Ah)
1st Parameter	1	↑	1	-	0	1	1	0	0	IFPF2	IFPF1	IFPF0	66h

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	This command is used to define the format of RGB picture data, which is to be transferred via the MCU interface and RGB interface. The formats are shown in the table:												
	IFPF[2:0]			MCU Interface Color Format									
	011	3	12-bit/pixel										
	101	5	16-bit/pixel										
	110	6	18-bit/pixel										
	111	7	No used										
	Others are no define and invalid												
	Note 1: In 12-bit/Pixel, 16-bit/Pixel or 18-bit/Pixel mode, the LUT is applied to transfer data into the Frame Memory.												
	Note 2: When VIPF[3:0]="1110", 6-bit data width of 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.												
Default	Status						Default Value						
							VIPF[3:0]						
	Power On Sequence						06H(18-bit/Pixel)						
	S/W Reset						No Change						
	H/W Reset						06H(18-bit/Pixel)						

## 10.1.31 RDID1 (DAh): Read ID1 Value

DAH	RDID1 (Read ID1 Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDID1	0	↑	1	-	1	1	0	1	1	0	1	0	(DAh)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	-This read byte returns 8-bit LCD module's manufacturer ID												
	-The 1 <sup>st</sup> parameter is dummy data												
	-The 2 <sup>nd</sup> parameter (ID17 to ID10): LCD module's manufacturer ID.												
	NOTE: See command RDDID (04h), 2 <sup>nd</sup> parameter.												
Default	Status						Default Value						
	Power On Sequence						-						
	S/W Reset						29h						
	H/W Reset						29h						

## 10.1.32 RDID2 (DBh): Read ID2 Value

DBH	RDID2 (Read ID2 Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDID2	0	↑	1	-	1	1	0	1	1	0	1	1	(DBh)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	'1'	ID26	ID25	ID24	ID23	ID22	ID21	ID20	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	<ul style="list-style-type: none"> <li>-This read byte returns 8-bit LCD module/driver version ID</li> <li>-The 1<sup>st</sup> parameter is dummy data</li> <li>-The 2<sup>nd</sup> parameter (ID26 to ID20): LCD module/driver version ID</li> <li>-Parameter Range: ID=80h to FFh</li> </ul>								
	Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Status</th> <th style="width: 50%;">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td style="text-align: center;">-</td> </tr> <tr> <td>S/W Reset</td> <td style="text-align: center;">81h</td> </tr> <tr> <td>H/W Reset</td> <td style="text-align: center;">81h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	-	S/W Reset	81h	H/W Reset
Status	Default Value								
Power On Sequence	-								
S/W Reset	81h								
H/W Reset	81h								

## 10.2.1 FRMCTR1 (B1h): Frame Rate Control (In normal mode/ Full colors)

B1H	FRMCTR1 (Frame Rate Control)												(Code)
Inst / Para	D/CX	WRX	RDX	D1 7-8	D7	D6	D5	D4	D3	D2	D1	D0	
FRMCTR1	0	↑	1	-	1	0	1	1	0	0	0	1	(B1h)
1st Parameter	1	↑	1	-	RTNA[7:0]							3Bh	
2nd Parameter	1	↑	1	-					FPA[4:0]				04h
3rd Parameter	1	↑	1	-					BPA[4:0]				03h
Nth Parameter	1	↑	1	-	RTNA_VSYNC[7:0]							38h	

NOTE: "-" Don't care

Description	-Set the frame frequency of the full colors normal mode, recommend to set under 110Hz.	
	-The frame frequency need to meet 60Hz±5% in this mode	
	$\text{Frame rate(Hz)} = \frac{\text{OSC}}{(\text{RTNA}) * (220 + \text{FPA} + \text{BPA})}$	
	RTNA[7:0]	Frame Rate
	0100000	32
	0100001	33
	0100010	34
	0100011	35
	0100100	36
	0100101	37
	0100110	38
	0100111	39
	0101000	40
	0101001	41
	0101010	42
	0101011	43
	0101100	44
	0101101	45
	0101110	46
	0101111	47
	0110000	48
	0110001	49
	0110010	50
	0110011	51
	0110100	52
0110101	53	
0110110	54	
0110111	55	
0111000	56	
0111001	57	
0111010	58	
0111011	59	
0111100	60	
0111101	61	
0111110	62	
0111111	63	
1000000	64	
1000001	65	
1000010	66	
1000011	67	
1000100	68	
1000101	69	
1000110	70	
1000111	71	
1001000	72	
1001001	73	
1001010	74	
1001011	75	
1001100	76	
1001101	77	
1001110	78	

1001111		79	45	1111111		127	28
<b>Note: OSC output fre. Is 800KHz, FPA=04H and BPA=03H</b>							
FPA[4:0]		Timing		BPA[4:0]		Timing	
0000	0	0 line		0000	0	0 line	
0001	1	1 line		0001	1	1 line	
0010	2	2 lines		0010	2	2 lines	
0011	3	3 lines		0011	3	3 lines	
00100	4	4 lines		00100	4	4 lines	
00101	5	5 lines		00101	5	5 lines	
00110	6	6 lines		00110	6	6 lines	
00111	7	7 lines		00111	7	7 lines	
01000	8	8 lines		01000	8	8 lines	
01001	9	9 lines		01001	9	9 lines	
01010	10	10 lines		01010	10	10 lines	
01011	11	11 lines		01011	11	11 lines	
01100	12	12 lines		01100	12	12 lines	
01101	13	13 lines		01101	13	13 lines	
01110	14	14 lines		01110	14	14 lines	
01111	15	15 lines		01111	15	15 lines	
10000	16	16 lines		10000	16	16 lines	
10001	17	17 lines		10001	17	17 lines	
10010	18	18 lines		10010	18	18 lines	
10011	19	19 lines		10011	19	19 lines	
10100	20	20 lines		10100	20	20 lines	
10101	21	21 lines		10101	21	21 lines	
10110	22	22 lines		10110	22	22 lines	
10111	23	23 lines		10111	23	23 lines	
11000	24	24 lines		11000	24	24 lines	
11001	25	25 lines		11001	25	25 lines	
11010	26	26 lines		11010	26	26 lines	
11011	27	27 lines		11011	27	27 lines	
11100	28	28 lines		11100	28	28 lines	
11101	29	29 lines		11101	29	29 lines	
11110	30	30 lines		11110	30	30 lines	
11111	31	31 lines		11111	31	31 lines	

Default	Status	Default Value
	Power On Sequence	3B/04/03/38 H
	S/W Reset	-
	H/W Reset	3B/04/03/38 H



10.2.2 FRMCTR2 (B2h): Frame Rate Control (In Idle mode/ 8-colors)

B2H	FRMCTR2 (Frame Rate Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
FRMCTR2	0	↑	1	-	1	0	1	1	0	0	1	0	(B2h)
1st Parameter	1	↑	1	-	RTNB[7:0]							3Bh	
2nd Parameter	1	↑	1	-	-	-	-	FPB[4:0]					04h
3rd Parameter	1	↑	1	-	-	-	-	BPB[4:0]					03h

NOTE: "-- Don't care

Description	-Set the frame frequency of the full colors idle mode, recommend to set under 110Hz.			
	-The frame frequency need to meet 60Hz±5% in this mode			
	$\text{Frame rate(Hz)} = \frac{\text{OSC}}{(\text{RTNB}) * (220+\text{FPB}+\text{BPB})}$			
	RTNB[7:0]	Frame Rate	RTNB[7:0]	Frame Rate
	0100000	32	110	44
	0100001	33	107	43
	0100010	34	104	43
	0100011	35	101	42
	0100100	36	98	42
	0100101	37	95	41
	0100110	38	93	41
	0100111	39	90	41
	0101000	40	88	40
	0101001	41	86	40
	0101010	42	84	39
	0101011	43	82	39
	0101100	44	80	38
	0101101	45	78	38
	0101110	46	77	37
	0101111	47	75	37
	0110000	48	73	37
	0110001	49	72	36
	0110010	50	70	36
	0110011	51	69	36
	0110100	52	68	35
0110101	53	66	35	
0110110	54	65	35	
0110111	55	64	34	
0111000	56	63	34	
0111001	57	62	34	
0111010	58	61	33	
0111011	59	60	33	
0111100	60	59	33	
0111101	61	58	32	
0111110	62	57	32	
0111111	63	56	32	
1000000	64	55	31	
1000001	65	54	31	
1000010	66	53	31	
1000011	67	52	31	
1000100	68	52	30	
1000101	69	51	30	
1000110	70	50	30	
1000111	71	49	30	
1001000	72	49	29	
1001001	73	48	29	
1001010	74	48	29	
1001011	75	47	29	
1001100	76	46	28	
1001101	77	46	28	
1001110	78	45	28	

1001111		79	45	1111111		127	28
<b>Note: OSC output fre. Is 800KHz, FPB=04H and BPB=03H</b>							
FPB[4:0]		Timing		BPB[4:0]		Timing	
0000	0	0 line		0000	0	0 line	
0001	1	1 line		0001	1	1 line	
0010	2	2 lines		0010	2	2 lines	
0011	3	3 lines		0011	3	3 lines	
00100	4	4 lines		00100	4	4 lines	
00101	5	5 lines		00101	5	5 lines	
00110	6	6 lines		00110	6	6 lines	
00111	7	7 lines		00111	7	7 lines	
01000	8	8 lines		01000	8	8 lines	
01001	9	9 lines		01001	9	9 lines	
01010	10	10 lines		01010	10	10 lines	
01011	11	11 lines		01011	11	11 lines	
01100	12	12 lines		01100	12	12 lines	
01101	13	13 lines		01101	13	13 lines	
01110	14	14 lines		01110	14	14 lines	
01111	15	15 lines		01111	15	15 lines	
10000	16	16 lines		10000	16	16 lines	
10001	17	17 lines		10001	17	17 lines	
10010	18	18 lines		10010	18	18 lines	
10011	19	19 lines		10011	19	19 lines	
10100	20	20 lines		10100	20	20 lines	
10101	21	21 lines		10101	21	21 lines	
10110	22	22 lines		10110	22	22 lines	
10111	23	23 lines		10111	23	23 lines	
11000	24	24 lines		11000	24	24 lines	
11001	25	25 lines		11001	25	25 lines	
11010	26	26 lines		11010	26	26 lines	
11011	27	27 lines		11011	27	27 lines	
11100	28	28 lines		11100	28	28 lines	
11101	29	29 lines		11101	29	29 lines	
11110	30	30 lines		11110	30	30 lines	
11111	31	31 lines		11111	31	31 lines	

Status	Default Value
Power On Sequence	3B/04/03 H
S/W Reset	-
H/W Reset	3B/04/03 H

## 10.2.3 FRMCTR3 (B3h): Frame Rate Control (In Partial mode/ full colors)

B3H	FRMCTR3 (Frame Rate Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
FRMCTR3	0	↑	1	-	1	0	1	1	0	0	1	1	(B3h)
1st Parameter	1	↑	1	-	RTNC[7:0]							3Bh	
2nd Parameter	1	↑	1	-	FPC[4:0]							04h	
3rd Parameter	1	↑	1	-	BPC[4:0]							03h	

NOTE: "-- Don't care

Description	<p>-Set the frame frequency of the full colors partial mode, recommend to set under 110Hz.                      -The frame frequency need to meet 60Hz±5% in this mode</p>																																																																																																																																																																																																				
	<p style="text-align: center;">OSC</p> <p style="text-align: center;">Frame rate(Hz) = <math>\frac{\text{OSC}}{(\text{RTNC}) * (220 + \text{FPC} + \text{BPC})}</math></p>																																																																																																																																																																																																				
	<table border="1"> <thead> <tr> <th>RTNC[7:0]</th> <th>Frame Rate</th> <th>RTNC[7:0]</th> <th>Frame Rate</th> </tr> </thead> <tbody> <tr><td>0100000</td><td>32</td><td>1010000</td><td>80</td></tr> <tr><td>0100001</td><td>33</td><td>1010001</td><td>81</td></tr> <tr><td>0100010</td><td>34</td><td>1010010</td><td>82</td></tr> <tr><td>0100011</td><td>35</td><td>1010011</td><td>83</td></tr> <tr><td>0100100</td><td>36</td><td>1010100</td><td>84</td></tr> <tr><td>0100101</td><td>37</td><td>1010101</td><td>85</td></tr> <tr><td>0100110</td><td>38</td><td>1010110</td><td>86</td></tr> <tr><td>0100111</td><td>39</td><td>1010111</td><td>87</td></tr> <tr><td>0101000</td><td>40</td><td>1011000</td><td>88</td></tr> <tr><td>0101001</td><td>41</td><td>1011001</td><td>89</td></tr> <tr><td>0101010</td><td>42</td><td>1011010</td><td>90</td></tr> <tr><td>0101011</td><td>43</td><td>1011011</td><td>91</td></tr> <tr><td>0101100</td><td>44</td><td>1011100</td><td>92</td></tr> <tr><td>0101101</td><td>45</td><td>1011101</td><td>93</td></tr> <tr><td>0101110</td><td>46</td><td>1011110</td><td>94</td></tr> <tr><td>0101111</td><td>47</td><td>1011111</td><td>95</td></tr> <tr><td>0110000</td><td>48</td><td>1100000</td><td>96</td></tr> <tr><td>0110001</td><td>49</td><td>1100001</td><td>97</td></tr> <tr><td>0110010</td><td>50</td><td>1100010</td><td>98</td></tr> <tr><td>0110011</td><td>51</td><td>1100011</td><td>99</td></tr> <tr><td>0110100</td><td>52</td><td>1100100</td><td>100</td></tr> <tr><td>0110101</td><td>53</td><td>1100101</td><td>101</td></tr> <tr><td>0110110</td><td>54</td><td>1100110</td><td>102</td></tr> <tr><td>0110111</td><td>55</td><td>1100111</td><td>103</td></tr> <tr><td>0111000</td><td>56</td><td>1101000</td><td>104</td></tr> <tr><td>0111001</td><td>57</td><td>1101001</td><td>105</td></tr> <tr><td>0111010</td><td>58</td><td>1101010</td><td>106</td></tr> <tr><td>0111011</td><td>59</td><td>1101011</td><td>107</td></tr> <tr><td>0111100</td><td>60</td><td>1101100</td><td>108</td></tr> <tr><td>0111101</td><td>61</td><td>1101101</td><td>109</td></tr> <tr><td>0111110</td><td>62</td><td>1101110</td><td>110</td></tr> <tr><td>0111111</td><td>63</td><td>1101111</td><td>111</td></tr> <tr><td>1000000</td><td>64</td><td>1110000</td><td>112</td></tr> <tr><td>1000001</td><td>65</td><td>1110001</td><td>113</td></tr> <tr><td>1000010</td><td>66</td><td>1110010</td><td>114</td></tr> <tr><td>1000011</td><td>67</td><td>1110011</td><td>115</td></tr> <tr><td>1000100</td><td>68</td><td>1110100</td><td>116</td></tr> <tr><td>1000101</td><td>69</td><td>1110101</td><td>117</td></tr> <tr><td>1000110</td><td>70</td><td>1110110</td><td>118</td></tr> <tr><td>1000111</td><td>71</td><td>1110111</td><td>119</td></tr> <tr><td>1001000</td><td>72</td><td>1111000</td><td>120</td></tr> <tr><td>1001001</td><td>73</td><td>1111001</td><td>121</td></tr> <tr><td>1001010</td><td>74</td><td>1111010</td><td>122</td></tr> <tr><td>1001011</td><td>75</td><td>1111011</td><td>123</td></tr> <tr><td>1001100</td><td>76</td><td>1111100</td><td>124</td></tr> <tr><td>1001101</td><td>77</td><td>1111101</td><td>125</td></tr> <tr><td>1001110</td><td>78</td><td>1111110</td><td>126</td></tr> <tr><td>1001111</td><td>79</td><td>1111111</td><td>127</td></tr> </tbody> </table>	RTNC[7:0]	Frame Rate	RTNC[7:0]	Frame Rate	0100000	32	1010000	80	0100001	33	1010001	81	0100010	34	1010010	82	0100011	35	1010011	83	0100100	36	1010100	84	0100101	37	1010101	85	0100110	38	1010110	86	0100111	39	1010111	87	0101000	40	1011000	88	0101001	41	1011001	89	0101010	42	1011010	90	0101011	43	1011011	91	0101100	44	1011100	92	0101101	45	1011101	93	0101110	46	1011110	94	0101111	47	1011111	95	0110000	48	1100000	96	0110001	49	1100001	97	0110010	50	1100010	98	0110011	51	1100011	99	0110100	52	1100100	100	0110101	53	1100101	101	0110110	54	1100110	102	0110111	55	1100111	103	0111000	56	1101000	104	0111001	57	1101001	105	0111010	58	1101010	106	0111011	59	1101011	107	0111100	60	1101100	108	0111101	61	1101101	109	0111110	62	1101110	110	0111111	63	1101111	111	1000000	64	1110000	112	1000001	65	1110001	113	1000010	66	1110010	114	1000011	67	1110011	115	1000100	68	1110100	116	1000101	69	1110101	117	1000110	70	1110110	118	1000111	71	1110111	119	1001000	72	1111000	120	1001001	73	1111001	121	1001010	74	1111010	122	1001011	75	1111011	123	1001100	76	1111100	124	1001101	77	1111101	125	1001110	78	1111110	126	1001111	79	1111111	127
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1001111	79	1111111	127																																																																																																																																																																																																		
	<p><b>Note: OSC output fre. Is 800KHz, FPC=04H and BPC=03H</b></p>																																																																																																																																																																																																				

FPC[4:0]		Timing	BPC[4:0]		Timing
0000	0	0 line	0000	0	0 line
0001	1	1 line	0001	1	1 line
0010	2	2 lines	0010	2	2 lines
0011	3	3 lines	0011	3	3 lines
0100	4	4 lines	0100	4	4 lines
0101	5	5 lines	0101	5	5 lines
0110	6	6 lines	0110	6	6 lines
0111	7	7 lines	0111	7	7 lines
1000	8	8 lines	1000	8	8 lines
1001	9	9 lines	1001	9	9 lines
1010	10	10 lines	1010	10	10 lines
1011	11	11 lines	1011	11	11 lines
1100	12	12 lines	1100	12	12 lines
1101	13	13 lines	1101	13	13 lines
1110	14	14 lines	1110	14	14 lines
1111	15	15 lines	1111	15	15 lines
10000	16	16 lines	10000	16	16 lines
10001	17	17 lines	10001	17	17 lines
10010	18	18 lines	10010	18	18 lines
10011	19	19 lines	10011	19	19 lines
10100	20	20 lines	10100	20	20 lines
10101	21	21 lines	10101	21	21 lines
10110	22	22 lines	10110	22	22 lines
10111	23	23 lines	10111	23	23 lines
11000	24	24 lines	11000	24	24 lines
11001	25	25 lines	11001	25	25 lines
11010	26	26 lines	11010	26	26 lines
11011	27	27 lines	11011	27	27 lines
11100	28	28 lines	11100	28	28 lines
11101	29	29 lines	11101	29	29 lines
11110	30	30 lines	11110	30	30 lines
11111	31	31 lines	11111	31	31 lines

Status	Default Value
Power On Sequence	3B/04/03 H
S/W Reset	-
H/W Reset	3B/04/03 H

## 10.2.4 INVCTR (B4h): Display Inversion Control

B4H	INVCTR (Display Inversion Control)												(Code)
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
INVCTR	0	↑	1	-	1	0	1	1	0	1	0	0	(B4h)
1st Parameter	1	↑	1	-	0	0	0	0	0	NLA	NLB	NLC	

NOTE: "-" Don't care

Description	-Display Inversion mode control					
	-NLA: Inversion setting in full colors normal mode (Normal mode on)					
	<b>NLA</b>		<b>Inversion setting in full Colors normal mode</b>			
	0		<b>Line Inversion</b>			
	1		Frame Inversion			
	-NLB: Inversion setting in Idle mode (Idle mode on)					
	<b>NLB</b>		<b>Inversion setting in Idle mode</b>			
	0		Line Inversion			
	1		<b>Frame Inversion</b>			
	-NLC: Inversion setting in full colors partial mode (Partial mode on / Idle mode off)					
<b>NLC</b>		<b>Inversion setting in full Colors partial mode</b>				
0		<b>Line Inversion</b>				
1		Frame Inversion				
Default	Status		Default Value			
			NLA	NLB	NLC	B4h
	Power On Sequence		0d	1d	0d	02h
	S/W Reset		No Change	No Change	No Change	No Change
	H/W Reset		0d	1d	0d	02h

## 10.2.5 DISSET5 (B6h): Display Function set 5

B6H	DISSET (Display Function set 5)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DISSET5	0	↑	1	-	1	0	1	1	0	1	1	0	(B6h)
1st Parameter	1	↑	1	-	0	0	NO1	NO0	SDT1	SDT0	EQ1	EQ0	15h
2nd Parameter	1	↑	1	-	0	0	0	0	PTG1	PTG0	PT1	PT0	00h

NOTE: “-“ Don't care

Description	-1 <sup>st</sup> parameter: Set output waveform relation.				
	-NO[1:0]: Set the amount of non-overlap of the gate output				
	<b>NO[1:0]</b>	<b>Amount of non-overlap of the gate output</b>			
		Refer the Internal oscillator			
	00	0			
		No			
	01	1			
		1 clock cycle			
	10	2			
		4 clock cycle			
11	3				
	6 clock cycle				
		Refer the PCLK			
		4 clock cycle			
		16 clock cycle			
		24 clock cycle			
		32 clock cycle			
-SDT[1:0]: Set delay amount from gate signal falling edge of the source output.					
<b>SDT[1:0]</b>	<b>Amount of non-overlap of the gate output</b>				
	Refer the Internal oscillator				
	No				
00	0				
	4 clock cycle				
01	1				
	1 clock cycle				
10	2				
	2 clock cycle				
11	3				
	3 clock cycle				
		Refer the PCLK			
		4 clock cycle			
		8 clock cycle			
		12clock cycle			
		16 clock cycle			
-EQ[1:0]: Set the Equalizing period					
<b>EQ[1:0]</b>	<b>Amount of non-overlap of the gate output</b>				
	Refer the Internal oscillator				
	No EQ				
00	0				
	No EQ				
01	1				
	2 clock cycle				
10	2				
	4 clock cycle				
11	3				
	6 clock cycle				
		Refer the PCLK			
		No EQ			
		4 clock cycle			
		16 clock cycle			
		24 clock cycle			
<p>The diagram shows four signals: Gn, Gn+1, Sn, and VCOM. Gn and Gn+1 are gate signals that transition from high to low. Sn is a source signal that transitions from low to high. VCOM is a common voltage signal that transitions from high to low. The Gate Non-overlap period is the time between the falling edge of Gn and the falling edge of Gn+1. The Delay time for source output is the time between the falling edge of Gn and the rising edge of Sn. The EQ period is the time between the falling edge of Gn and the falling edge of VCOM.</p>					
-2 <sup>nd</sup> parameter: Set the output waveform in non-display area.					
-PTG[1:0]: Determine gate output in a non-display area in the partial mode					
<b>PTG[1:0]</b>	<b>Gate output in a non-display area</b>				
00	0				
	Normal scan				
01	1				
	Fix on VGL				
10	2				
	Fix on VGL				
11	3				
	Fix on VGL				
-PT[1:0]: Determine Source /VCOM output in a non-display area in the partial mode					
<b>PT[1:0]</b>	<b>Source output on non-display area</b>	<b>VCOM output on non-display area</b>			
	Positive	Negative	Positive	Negative	
00	0	V63	V0	VCOML	VCOMH
01	1	V0	V63	VCOML	VCOMH
10	2	AGND	AGND	AGND	AGND
11	3	Hi-z	Hi-z	AGND	AGND

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Default	Status	Default Value				
		NO[1:0]	STD[1:0]	EQ[1:0]	PTG[1:0]	PT[1:0]
	Power On Sequence	01H	01H	01H	01H	10H
	S/W Reset	01H	01H	01H	01H	10H
	H/W Reset	01H	01H	01H	01H	10H

## 10.2.8 PWCTR1 (C0h): Power Control 1

C0H	PWCTR1 (Power Control 1)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWCTR1	0	↑	1	-	1	1	0	0	0	0	0	0	(C0h)
1st Parameter	1	↑	1	-	0	0	0	VRH4	VRH3	VRH2	VRH1	VRH0	

NOTE: “-“ Don't care

Description	-Set the GVDD and VC11 voltage		
	VRH[4:0]	GVDD	
	00000	0	5.00
	00001	1	4.75
	00010	2	4.70
	00011	3	4.65
	00100	4	4.60
	00101	5	4.55
	00110	6	4.50
	00111	7	4.45
	01000	8	4.40
	01001	9	4.35
	01010	10	4.30
	01011	11	4.25
	01100	12	4.20
	01101	13	4.15
	01110	14	4.10
	01111	15	4.05
	10000	16	4.00
	10001	17	3.95
	10010	18	3.90
	10011	19	3.85
	10100	20	3.80
	10101	21	3.75
	10110	22	3.70
	10111	23	3.65
	11000	24	3.60
	11001	25	3.55
	11010	26	3.50
	11011	27	3.45
	11100	28	3.40
	11101	29	3.35
	11110	30	3.25
	11111	31	3.00

Default	Status	Default Value
		TM LC type
		VRH[4:0]
	Power On Sequence	05H
	S/W Reset	05H
H/W Reset	05H	



## 10.2.9 PWCTR2 (C1h): Power Control 2

C1H	PWCTR2 (Power Control 2)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWCTR2	0	↑	1	-	1	1	0	0	0	0	0	1	(C1h)
1st Parameter	1	↑	1		VGH3	VGH2	VGH1	VGH0	VGL3	VGL2	VGL1	VGL0	BBh

NOTE: “-“ Don't care

Description	-Set the VGH and VGL supply power level			
	VGH[3:0]/VGL[3:0]		VGH	VGL
	0000	0	10	-5.5
	0001	1	10.5	-6
	0010	2	11	-7.5
	0011	3	11.5	-8
	0100	4	12	-8.5
	0101	5	12.5	-9
	0110	6	13	-9.5
	0111	7	13.5	-10
	1000	8	14	-10.5
	1001	9	14.5	-11
	1010	10	15	-11.5
	1011	11	15.5	-12
	1100	12	16	-12.5
	1101	13	16.5	-13
	1110	14	X	-13.5
	1111	15	X	X
	Unit(V)			
Default	Status		Default Value	
		VGH[3:0]	VGL[3:0]	
	Power On Sequence	-	-	
	S/W Reset	0Bh	0Bh	
	H/W Reset	0Bh	0Bh	

## 10.2.10 PWCTR3 (C2h): Power Control 3 (in Normal mode/ Full colors)

C2H		PWCTR3 (Power Control 3)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)	
PWCTR3	0	↑	1	-	1	1	0	0	0	0	1	0	(C2h)	
1st Parameter	1	↑	1	-	0	0	0	0	0	0	APA2	APA1	APA0	04h

NOTE: "-" Don't care

Description	-Set the amount of current in Operational amplifier in normal mode/full colors.																											
	-Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.																											
	<table border="1"> <thead> <tr> <th>APA[2:0]</th> <th>Amount of Current in Operational Amplifier</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>0</td> <td>Operation of the operational amplifier stops</td> </tr> <tr> <td>001</td> <td>1</td> <td>Small</td> </tr> <tr> <td>010</td> <td>2</td> <td>Medium Low</td> </tr> <tr> <td>011</td> <td>3</td> <td>Medium</td> </tr> <tr> <td>100</td> <td>4</td> <td>Medium High</td> </tr> <tr> <td>101</td> <td>5</td> <td>Large</td> </tr> <tr> <td>110</td> <td>6</td> <td>Reserved</td> </tr> <tr> <td>111</td> <td>7</td> <td>Reserved</td> </tr> </tbody> </table>		APA[2:0]	Amount of Current in Operational Amplifier	000	0	Operation of the operational amplifier stops	001	1	Small	010	2	Medium Low	011	3	Medium	100	4	Medium High	101	5	Large	110	6	Reserved	111	7	Reserved
	APA[2:0]	Amount of Current in Operational Amplifier																										
	000	0	Operation of the operational amplifier stops																									
	001	1	Small																									
	010	2	Medium Low																									
	011	3	Medium																									
	100	4	Medium High																									
	101	5	Large																									
110	6	Reserved																										
111	7	Reserved																										
Default	Status		Default Value																									
			APA[2:0]																									
	Power On Sequence		-																									
	S/W Reset		04h																									
	H/W Reset		04h																									

## 10.2.11 PWCTR4 (C3h): Power Control 4 (in Idle mode/ 8-colors)

C3H		PWCTR4 (Power Control 4)											
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWCTR4	0	↑	1	-	1	1	0	0	0	0	1	1	(C3h)
1st Parameter	1	↑	1	-	0	0	0	0	0	0	APB2	APB1	APB0

NOTE: "-" Don't care

Description	-Set the amount of current in Operational amplifier in Idle mode/8 colors.																											
	-Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.																											
	<table border="1"> <thead> <tr> <th>APB[2:0]</th> <th>Amount of Current in Operational Amplifier</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>0</td> <td>Operation of the operational amplifier stops</td> </tr> <tr> <td>001</td> <td>1</td> <td>Small</td> </tr> <tr> <td>010</td> <td>2</td> <td>Medium Low</td> </tr> <tr> <td>011</td> <td>3</td> <td>Medium</td> </tr> <tr> <td>100</td> <td>4</td> <td>Medium High</td> </tr> <tr> <td>101</td> <td>5</td> <td>Large</td> </tr> <tr> <td>110</td> <td>6</td> <td>Reserved</td> </tr> <tr> <td>111</td> <td>7</td> <td>Reserved</td> </tr> </tbody> </table>		APB[2:0]	Amount of Current in Operational Amplifier	000	0	Operation of the operational amplifier stops	001	1	Small	010	2	Medium Low	011	3	Medium	100	4	Medium High	101	5	Large	110	6	Reserved	111	7	Reserved
	APB[2:0]	Amount of Current in Operational Amplifier																										
	000	0	Operation of the operational amplifier stops																									
	001	1	Small																									
	010	2	Medium Low																									
	011	3	Medium																									
	100	4	Medium High																									
	101	5	Large																									
110	6	Reserved																										
111	7	Reserved																										
Default	Status		Default Value																									
			APB[2:0]																									
	Power On Sequence		-																									
	S/W Reset		04h																									
	H/W Reset		04h																									

## 10.2.12 PWCTR5 (C4h): Power Control 5 (in Partial mode/ full-colors)

C4H		PWCTR5 (Power Control 5)											
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWCTR5	0	↑	1	-	1	1	0	0	0	1	0	0	(C4h)
1st Parameter	1	↑	1	-	0	0	0	0	0	APC2	APC1	APC0	04h

NOTE: "-" Don't care

Description	-Set the amount of current in Operational amplifier in Partial mode/ full-colors.		
	-Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.		
	<b>APC[2:0]</b>		<b>Amount of Current in Operational Amplifier</b>
	000	0	Operation of the operational amplifier stops
	001	1	Small
	010	2	Medium Low
	011	3	Medium
	100	4	Medium High
	101	5	Large
	110	6	Reserved
111	7	Reserved	
Default	Status		Default Value
			APC[2:0]
	Power On Sequence		-
	S/W Reset		04h
	H/W Reset		04h

10.2.13 VMCTR1 (C5h): VCOM Control 1

C5H	VMCTR1 (VCOM Control 1)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VMCTR1	0	↑	1	-	1	1	0	0	0	1	0	1	(C5h)
1st Parameter	1	↑	1	-	0	VMH6	VMH5	VMH 4	VMH 3	VMH 2	VMH 1	VMH 0	3Ch
2nd Parameter	1	↑	1	-	0	VML 6	VML 5	VML 4	VML 3	VML 2	VML 1	VML 0	3Ch

NOTE: “-“ Don't care

Description	-Set VCOMH Voltage												
	VMH[6:0]	VCOMH	VMH[6:0]	VCOMH	VMH[6:0]	VCOMH	VMH[6:0]	VCOMH	VMH[6:0]	VCOMH	VMH[6:0]	VCOMH	
0000000	0	2.500	0011011	27	3.175	0110110	54	3.850	1010001	81	4.525		
0000001	1	2.525	0011100	28	3.200	0110111	55	3.875	1010010	82	4.550		
0000010	2	2.550	0011101	29	3.225	0111000	56	3.900	1010011	83	4.575		
0000011	3	2.575	0011110	30	3.250	0111001	57	3.925	1010100	84	4.600		
0000100	4	2.600	0011111	31	3.275	0111010	58	3.950	1010101	85	4.625		
0000101	5	2.625	0100000	32	3.300	0111011	59	3.975	1010110	86	4.650		
0000110	6	2.650	0100001	33	3.325	0111100	60	4.000	1010111	87	4.675		
0000111	7	2.675	0100010	34	3.350	0111101	61	4.025	1011000	88	4.700		
0001000	8	2.700	0100011	35	3.375	0111110	62	4.050	1011001	89	4.725		
0001001	9	2.725	0100100	36	3.400	0111111	63	4.075	1011010	90	4.750		
0001010	10	2.750	0100101	37	3.425	1000000	64	4.100	1011011	91	4.775		
0001011	11	2.775	0100110	38	3.450	1000001	65	4.125	1011100	92	4.800		
0001100	12	2.800	0100111	39	3.475	1000010	66	4.150	1011101	93	4.825		
0001101	13	2.825	0101000	40	3.500	1000011	67	4.175	1011110	94	4.850		
0001110	14	2.850	0101001	41	3.525	1000100	68	4.200	1011111	95	4.875		
0001111	15	2.875	0101010	42	3.550	1000101	69	4.225	1100000	96	4.900		
0010000	16	2.900	0101011	43	3.575	1000110	70	4.250	1100001	97	4.925		
0010001	17	2.925	0101100	44	3.600	1000111	71	4.275	1100010	98	4.950		
0010010	18	2.950	0101101	45	3.625	1001000	72	4.300	1100011	99	4.975		
0010011	19	2.975	0101110	46	3.650	1001001	73	4.325	1100100	100	5.000		
0010100	20	3.000	0101111	47	3.675	1001010	74	4.350	1100101	101		Not Permitted	
0010101	21	3.025	0110000	48	3.700	1001011	75	4.375					
0010110	22	3.050	0110001	49	3.725	1001100	76	4.400	1111111	127			
0010111	23	3.075	0110010	50	3.750	1001101	77	4.425					
0011000	24	3.100	0110011	51	3.775	1001110	78	4.450					
0011001	25	3.125	0110100	52	3.800	1001111	79	4.475					
0011010	26	3.150	0110101	53	3.825	1010000	80	4.500					
Description	-Set VCOML Voltage												
	VML[6:0]	VCOML	VML[6:0]	VCOML	VML[6:0]	VCOML	VML[6:0]	VCOML	VML[6:0]	VCOML	VML[6:0]	VCOML	
0000000	0	-2.500	0011011	27	-1.825	0110110	54	-1.150	1010001	81	-0.475		
0000001	1	-2.475	0011100	28	-1.800	0110111	55	-1.125	1010010	82	-0.450		
0000010	2	-2.450	0011101	29	-1.775	0111000	56	-1.100	1010011	83	-0.425		
0000011	3	-2.425	0011110	30	-1.750	0111001	57	-1.075	1010100	84	-0.400		
0000100	4	-2.400	0011111	31	-1.725	0111010	58	-1.050	1010101	85	-0.375		
0000101	5	-2.375	0100000	32	-1.700	0111011	59	-1.025	1010110	86	-0.350		
0000110	6	-2.350	0100001	33	-1.675	0111100	60	-1.000	1010111	87	-0.325		
0000111	7	-2.325	0100010	34	-1.650	0111101	61	-0.975	1011000	88	-0.300		
0001000	8	-2.300	0100011	35	-1.625	0111110	62	-0.950	1011001	89	-0.275		
0001001	9	-2.275	0100100	36	-1.600	0111111	63	-0.925	1011010	90	-0.250		
0001010	10	-2.250	0100101	37	-1.575	1000000	64	-0.900	1011011	91	-0.225		
0001011	11	-2.225	0100110	38	-1.550	1000001	65	-0.875	1011100	92	-0.200		
0001100	12	-2.200	0100111	39	-1.525	1000010	66	-0.850	1011101	93	-0.175		
0001101	13	-2.175	0101000	40	-1.500	1000011	67	-0.825	1011110	94	-0.150		
0001110	14	-2.150	0101001	41	-1.475	1000100	68	-0.800	1011111	95	-0.125		
0001111	15	-2.125	0101010	42	-1.450	1000101	69	-0.775	1100000	96	-0.100		
0010000	16	-2.100	0101011	43	-1.425	1000110	70	-0.750	1100001	97	-0.075		
0010001	17	-2.075	0101100	44	-1.400	1000111	71	-0.725	1100010	98	-0.050		
0010010	18	-2.050	0101101	45	-1.375	1001000	72	-0.700	1100011	99	-0.025		
0010011	19	-2.025	0101110	46	-1.350	1001001	73	-0.675	1100100	100	0.000		
0010100	20	-2.000	0101111	47	-1.325	1001010	74	-0.650	1100101	101		Not Permitted	
0010101	21	-1.975	0110000	48	-1.300	1001011	75	-0.625					
0010110	22	-1.950	0110001	49	-1.275	1001100	76	-0.600	1111111	127			
0010111	23	-1.925	0110010	50	-1.250	1001101	77	-0.575					
0011000	24	-1.900	0110011	51	-1.225	1001110	78	-0.550					
0011001	25	-1.875	0110100	52	-1.200	1001111	79	-0.525					
0011010	26	-1.850	0110101	53	-1.175	1010000	80	-0.500					

Default	Status	Default Value
		LCM = "01"
		TM LC type
		VMH[6:0] / VML[6:0]
	Power On Sequence	-
S/W Reset	3Ch / 3C h	
H/W Reset	3Ch / 3Ch	

10.2.14 VMOFCTR (C7h): VCOM Offset Control

C7H	VMOFCTR (VCOM Offset Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VMOFCTR	0	↑	1	-	1	1	0	0	0	1	1	1	(C7h)
1st Parameter	1	↑	1	-	0	VMF6	VMF5	VMF4	VMF3	VMF2	VMF1	VMF0	3Ch

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	-Set VCOM Voltage level for reduce the flicker issue		
	<b>VMF[6:0]</b>	<b>VCOMH Output Level</b>	<b>VCOML Output Level</b>
	4	"VMH"-64d	"VML"-60d
	5	"VMH"-63d	"VML"-59d
	6	"VMH"-62d	"VML"-58d
	58	"VMH"-2d	"VML"-2d
	59	"VMH"-1d	"VML"-1d
	60	"VMH"	"VML"
	61	"VMH"+1d	"VML"+1d
	62	"VMH"+2d	"VML"+2d
	126	"VMH"+62d	"VML"+62d
	127	"VMH"+63d	"VML"+63d
	-IF "VMH"-xd or "VML"-xd is less than 0d, it becomes 0d.		
	-IF"VMH"+xd or "VML"+xd is large than 100d, it becomes 100d.		
-VMF[6:0] are stored in NV memory to contrast.			
-The nVM need be used in 1 <sup>st</sup> parameter of VMOFCTR (C7h)			
Default	Status		Default Value VMF[5:0]
	Power Mode On Sequence		3Ch
	S/W Reset		3Ch
	H/W Reset		3Ch

## 10.2.15 STEP CTR (C9h): step1/2/4 booster frequency control

BEH	RDVMOF (Read the VCOM Offset Value NV memory)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDVMOF	0	↑	1	-	1	1	0	0	1	0	0	1	(C9h)
1st Parameter	1	↑	1	-	DUAL_EN	STEP_DIV_EN	1	0	0	CP1_FREQ_SEL[2:0]			A4h
2nd Parameter	1	↑	1	-	NW_MODE	0	0	0	0	CP2_FREQ_SEL[2:0]			04h
2nd Parameter	1	↑	1	-	0	0	0	0	0	CP4_FREQ_SEL[2:0]			04h

NOTE: “-“ Don't care

Description	DUAL_EN : STEP1/2/4 booster mode select, default : 1(Dual mode)												
	STEP_DIV_EN : STEP1/2/3 CLK select OSC frequency divid 4 enable,0(default),1 : divid 4												
	NW_MODE : select panel type,0=Normally White,1=Normally Black												
	STEP_DIV_EN	CP1_FREQ_SEL[2:0]			Step-up cycle in Booster circuit1				CP2_FREQ_SEL[2:0]		Step-up cycle in Booster circuit 2		
	0/1	000	0	OSC/1024, OSC/4096				000	0	OSC/1024, OSC/4096			
	0/1	001	1	OSC/512, OSC/2048				001	1	OSC/512, OSC/2048			
	0/1	010	2	OSC/256, OSC/1024				010	2	OSC/256, OSC/1024			
	0/1	011	3	OSC/128, OSC/512				011	3	OSC/128, OSC/512			
	0/1	100	4	OSC/64, OSC/256				100	4	OSC/64, OSC/256			
	0/1	101	5	OSC/32, OSC/128				101	5	OSC/32, OSC/128			
0/1	110	6	OSC/16, OSC/64				110	6	OSC/16, OSC/64				
0/1	111	7	OSC/8, OSC/32				111	7	OSC/8, OSC/32				
Default	STEP_DIV_EN	CP4_FREQ_SEL[2:0]			Step-up cycle in Booster circuit4								
	0/1	000	0	OSC/1024, OSC/4096									
	0/1	001	1	OSC/512, OSC/2048									
	0/1	010	2	OSC/256, OSC/1024									
	0/1	011	3	OSC/128, OSC/512									
	0/1	100	4	OSC/64, OSC/256									
	0/1	101	5	OSC/32, OSC/128									
	0/1	110	6	OSC/16, OSC/64									
	0/1	111	7	OSC/8, OSC/32									
	Status						Default Value						
Power On Sequence						-							
S/W Reset						A4h/04h/04h							
H/W Reset						A4h/04h/04h							

## 10.2.16 RD PULSE CTR (F4h): Adjust read GRAM timing control function

F8H	VMOFCTR (VCOM Offset Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
8-color detect	0	↑	1	-	1	1	1	1	1	0	0	0	(F4h)
1st Parameter	1	↑	1	-	0	1	0	1	RD_PULSE_WIDTH[3:0]			55h	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	-This command is used to adjust read GRAM timing control function	
Default	Status	
	Power On Sequence	55h
	S/W Reset	55h
	H/W Reset	55h

## 10.2.17 8-color (F8h): 8 color detect function

F8H	VMOFCTR (VCOM Offset Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
8-color detect	0	↑	1	-	1	1	1	1	1	0	0	0	(F8h)
1st Parameter	1	↑	1	-	0	0	0	0	0	8-color	0	0	04h

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	-This command is used to turn on/off 8-color detect function 1 : enable 8-color detect function 0 : disable 8-color detect function	
Default	Status	
	Power On Sequence	04h
	S/W Reset	04h
	H/W Reset	04h

## 10.2.18 PWCTR6 (FCh): Power Control 6

FCH	RDVMOF (Read the VCOM Offset Value NV memory)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWCTR6	0	↑	1	-	1	1	1	1	1	1	0	0	(FCh)
1st Parameter	1	↑	1	-	0	0	1	1	1	SAPA[2:0]			3Ch
2nd Parameter	1	↑	1	-	0	1	1	1	1	SAPB[2:0]			7Ch
2nd Parameter	1	↑	1	-	0	0	0	0	0	SAPC[2:0]			04h

NOTE: "-- Don't care

Description	-Adjust the amount of fixed current from the fixed current source in the operational amplifier for the gate driver.	
	-SAPA[2:0] : Set the amount of current in Operational amplifier in Normal mode.	
	<b>SAPA[2:0]</b>	<b>Amount of Current in Operational Amplifier</b>
	000	0 Operation of the operational amplifier stops
	001	1 Small
	010	2 Medium Low
	011	3 Medium
	100	4 Medium High
	101	5 Large Low
	110	6 Large
	111	7 Large High
	-SAPB[2:0] : Set the amount of current in Operational amplifier in Idle mode.	
	<b>SAPB[2:0]</b>	<b>Amount of Current in Operational Amplifier</b>
	000	0 Operation of the operational amplifier stops
	001	1 Small
010	2 Medium Low	
011	3 Medium	
100	4 Medium High	
101	5 Large Low	
110	6 Large	
111	7 Large High	
-SAPC[2:0] : Set the amount of current in Operational amplifier in Partial/Full color mode.		
<b>SAPC[2:0]</b>	<b>Amount of Current in Operational Amplifier</b>	
000	0 Operation of the operational amplifier stops	
001	1 Small	
010	2 Medium Low	
011	3 Medium	
100	4 Medium High	
101	5 Large Low	
110	6 Large	
111	7 Large High	
Default	Status	
	Default Value	
	SAPA[2:0]/ SAPB[2:0]/SAPC[2:0]	
	Power On Sequence	-
	S/W Reset	3C/7C/04h
H/W Reset	3C/7C/04h	



## 10.2.19 WRID2 (D1h): Write ID2 Value

D1H	WRID2 (Write ID2 Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
WRID2	0	↑	1	-	1	1	0	1	0	0	0	1	(D1h)
1st Parameter	1	↑	1	-	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-

NOTE: “-“ Don't care

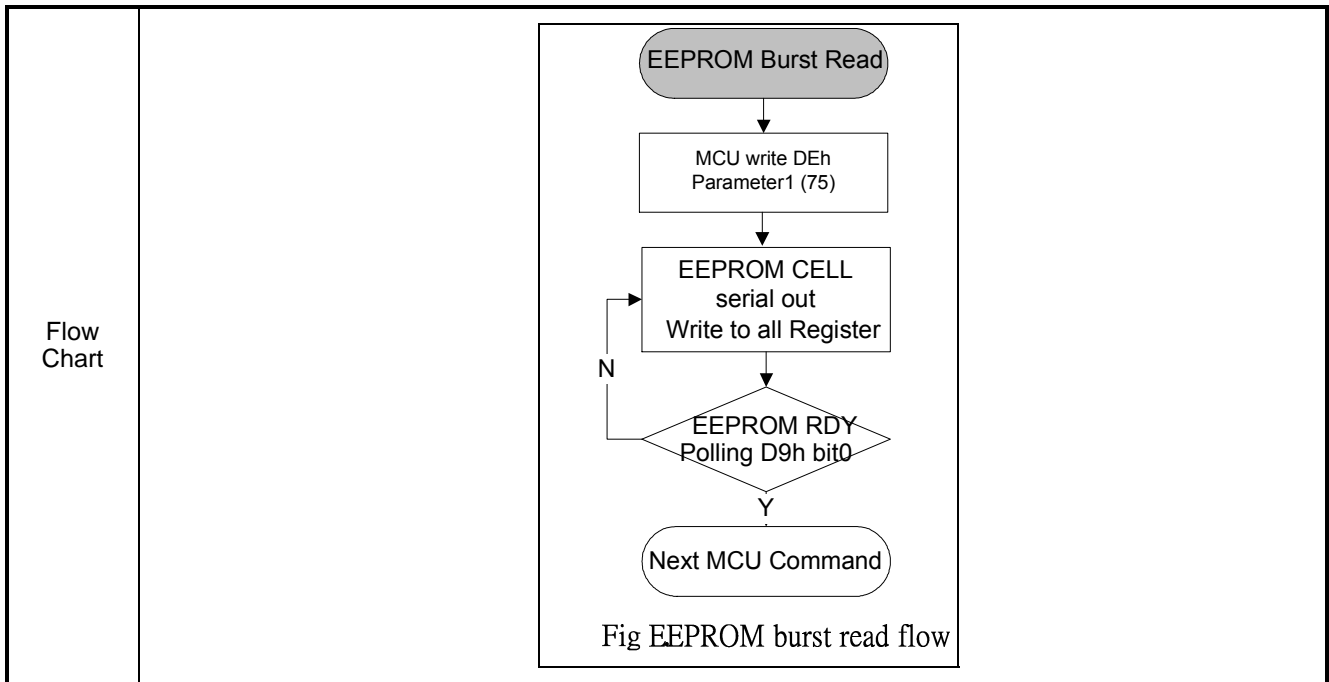
Description	-Write 7-bit data of LCD module version to save it to NV memory. -The 1 <sup>st</sup> parameter ID2[6:0] is LCD Module version ID.	
Default	Status	Default Value
	Power On Sequence	-
	S/W Reset	-
	H/W Reset	-

## 10.2.20 NVFCTR2 (DEh): NV Memory Function Controller 2

DEH	NVFCTR1 (NV Memory Function Controller 2)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
NVFCTR1	0	↑	1	-	1	1	0	1	1	1	1	0	(DEh)
1 <sup>st</sup> Parameter	1	↑	1		0	1	0	1	0	1	0	1	75

NOTE: “-“ Don't care

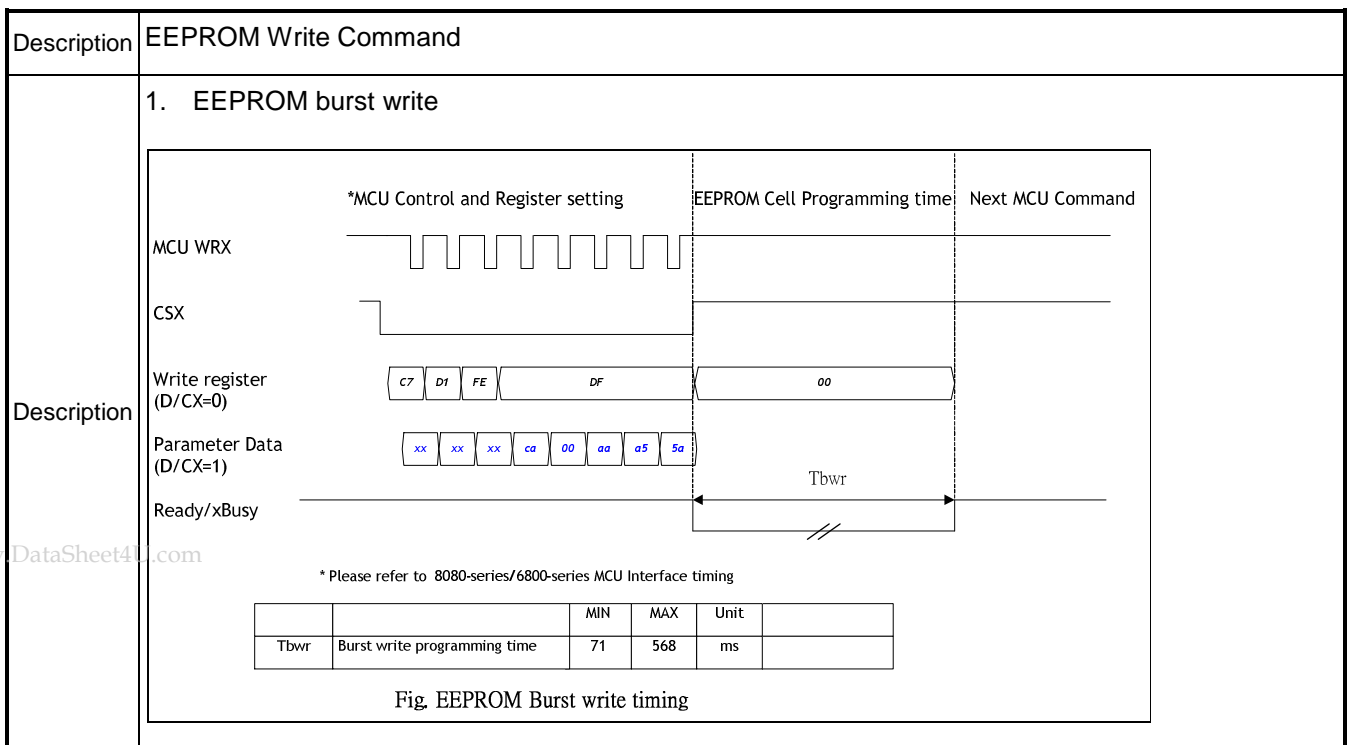
Description	1. EEPROM burst read												
	<p>* Please refer to 8080-series/6800-series MCU Interface timing</p> <table border="1"> <thead> <tr> <th></th> <th></th> <th>MIN</th> <th>MAX</th> <th>Unit</th> <th></th> </tr> </thead> <tbody> <tr> <td>Tbrd</td> <td>Burst read waiting time</td> <td>58</td> <td>464</td> <td>us</td> <td></td> </tr> </tbody> </table> <p>Fig. EEPROM Burst read timing</p>				MIN	MAX	Unit		Tbrd	Burst read waiting time	58	464	us
		MIN	MAX	Unit									
Tbrd	Burst read waiting time	58	464	us									
Default	Status	Default Value											
	Power On Sequence	Not Fixed											
	S/W Reset	Not Fixed											
	H/W Reset	Not Fixed											



10.2.21 NVFCTR3 (DFh): NV Memory Function Controller 3

DFH	NVFCTR1 (NV Memory Function Controller 3)												(Code)
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	
NVFCTR1	0	↑	1	-	1	1	0	1	1	1	1	1	(DFh)
1 <sup>st</sup> Parameter	1	↑	1	-	1	1	0	0	1	0	1	0	CA
2 <sup>nd</sup> Parameter	1	↑	1	-	0	0	0	0	0	0	0	0	00
3 <sup>rd</sup> Parameter	1	↑	1	-	1	0	1	0	1	0	1	0	AA
4 <sup>rd</sup> Parameter	1	↑	1	-	1	0	1	0	0	1	0	1	A5
5 <sup>rd</sup> Parameter	1	↑	1	-	0	1	0	1	1	0	1	0	5A

NOTE: "-" Don't care



Default	Status	Default Value
	Power On Sequence	Not Fixed
	S/W Reset	Not Fixed
	H/W Reset	Not Fixed
Flow Chart	<pre> graph TD     Start([EEPROM Burst Write]) --&gt; Reg[MCU write reg (C7 D1 FE)]     Reg --&gt; Param[MCU write DFh Parameter1 (CA) Parameter2 (00) Parameter3 (AA) Parameter4 (A5) Parameter5 (5A)]     Param --&gt; Program[Program EEPROM CELL]     Program --&gt; Poll{EEPROM RDY Polling D9h bit0}     Poll -- N --&gt; Program     Poll -- Y --&gt; Next([Next MCU Command])     </pre> <p>FigEEPROM burst write flow</p>	

10.2.22 GMCTRP1 (E0h): Gamma ('+'polarity) Correction Characteristics Setting

E0H	GMCTRP0 (Gamma '+'polarity Correction Characteristics Setting)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GMCTRP1	0	↑	1	-	1	1	1	0	0	0	0	0	(E0h)
1 <sup>st</sup> Parameter	1	↑	1	-	-	-	VRF0P[5]	VRF0P[4]	VF0P[3]	VRF0P[2]	VRF0P[1]	VRF0P[0]	
2 <sup>nd</sup> Parameter	1	↑	1	-	-	-	VOS0P[5]	VOS0P[4]	VOS0P[3]	VOS0P[2]	VOS0P[1]	VOS0P[0]	
3 <sup>rd</sup> Parameter	1	↑	1	-	-	-	PK0P[5]	PK0P[4]	PK0P[3]	PK0P[2]	PK0P[1]	PK0P[0]	
4 <sup>th</sup> Parameter	1	↑	1	-	-	-	PK1P[5]	PK1P[4]	PK1P[3]	PK1P[2]	PK1P[1]	PK1P[0]	
5 <sup>th</sup> Parameter	1	↑	1	-	-	-	PK2P[5]	PK2P[4]	PK2P[3]	PK2P[2]	PK2P[1]	PK2P[0]	
6 <sup>th</sup> Parameter	1	↑	1	-	-	-	PK3P[5]	PK3P[4]	PK3P[3]	PK3P[2]	PK3P[1]	PK3P[0]	
7 <sup>th</sup> Parameter	1	↑	1	-	-	-	PK4P[5]	PK4P[4]	PK4P[3]	PK4P[2]	PK4P[1]	PK4P[0]	
8 <sup>th</sup> Parameter	1	↑	1	-	-	-	PK5P[5]	PK5P[4]	PK5P[3]	PK5P[2]	PK5P[1]	PK5P[0]	
9 <sup>th</sup> Parameter	1	↑	1	-	-	-	PK6P[5]	PK6P[4]	PK6P[3]	PK6P[2]	PK6P[1]	PK6P[0]	
10 <sup>th</sup> Parameter	1	↑	1	-	-	-	PK7P[5]	PK7P[4]	PK7P[3]	PK7P[2]	PK7P[1]	PK7P[0]	
11 <sup>th</sup> Parameter	1	↑	1	-	-	-	PK8P[5]	PK8P[4]	PK8P[3]	PK8P[2]	PK8P[1]	PK8P[0]	
12 <sup>th</sup> Parameter	1	↑	1	-	-	-	PK9P[5]	PK9P[4]	PK9P[3]	PK9P[2]	PK9P[1]	PK9P[0]	
13 <sup>th</sup> Parameter	1	↑	1	-	-	-	SELV0P[5]	SELV0P[4]	SELV0P[3]	SELV0P[2]	SELV0P[1]	SELV0P[0]	
14 <sup>th</sup> Parameter	1	↑	1	-	-	-	SELV1P[5]	SELV1P[4]	SELV1P[3]	SELV1P[2]	SELV1P[1]	SELV1P[0]	
15 <sup>th</sup> Parameter	1	↑	1	-	-	-	SELV62P[5]	SELV62P[4]	SELV62P[3]	SELV62P[2]	SELV62P[1]	SELV62P[0]	
16 <sup>th</sup> Parameter	1	↑	1	-	-	-	SELV63P[5]	SELV63P[4]	SELV63P[3]	SELV63P[2]	SELV63P[1]	SELV63P[0]	

NOTE: "-" Don't care

Description	Register Group	Negative Polarity	Set-up Contents	
	High level adjustment	VRF0P[5:0]		Variable resistor VRHP
Mid level adjustment		SELV0P[5:0]		The voltage of grayscale number 0 is selected by the 64 to 1 selector
		SELV1P[5:0]		The voltage of grayscale number 1 is selected by the 64 to 1 selector
		PK0P[5:0]		The voltage of grayscale number 3 is selected by the 64 to 1 selector
		PK1P[5:0]		The voltage of grayscale number 6 is selected by the 64 to 1 selector
		PK2P[5:0]		The voltage of grayscale number 11 is selected by the 64 to 1 selector
		PK3P[5:0]		The voltage of grayscale number 19 is selected by the 64 to 1 selector
		PK4P[5:0]		The voltage of grayscale number 27 is selected by the 64 to 1 selector
		PK5P[5:0]		The voltage of grayscale number 36 is selected by the 64 to 1 selector
		PK6P[5:0]		The voltage of grayscale number 44 is selected by the 64 to 1 selector
		PK7P[5:0]		The voltage of grayscale number 52 is selected by the 64 to 1 selector
		PK8P[5:0]		The voltage of grayscale number 57 is selected by the 64 to 1 selector
		PK9P[5:0]		The voltage of grayscale number 60 is selected by the 64 to 1 selector
		SELV62P[5:0]		The voltage of grayscale number 62 is selected by the 64 to 1 selector
SELV63P[5:0]			The voltage of grayscale number 63 is selected by the 64 to 1 selector	
Low level adjustment	VOS0P[5:0]		Variable resistor VRLP	

10.2.23 GMCTR1 (E1h): Gamma '-'polarity Correction Characteristics Setting

E0H	GMCTRP0 (Gamma '+'polarity Correction Characteristics Setting)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GMCTR1	0	↑	1	-	1	1	1	0	0	0	0	1	(E1h)
1 <sup>st</sup> Parameter	1	↑	1	-	-	-	VRF0N[5]	VRF0N[4]	VF0N[3]	VRF0N[2]	VRF0N[1]	VRF0N[0]	
2 <sup>nd</sup> Parameter	1	↑	1	-	-	-	VOS0N[5]	VOS0N[4]	VOS0N[3]	VOS0N[2]	VOS0N[1]	VOS0N[0]	
3 <sup>rd</sup> Parameter	1	↑	1	-	-	-	PK0N[5]	PK0N[4]	PK0N[3]	PK0N[2]	PK0N[1]	PK0N[0]	
4 <sup>th</sup> Parameter	1	↑	1	-	-	-	PK1N[5]	PK1N[4]	PK1N[3]	PK1N[2]	PK1N[1]	PK1N[0]	
5 <sup>th</sup> Parameter	1	↑	1	-	-	-	PK2N[5]	PK2N[4]	PK2N[3]	PK2N[2]	PK2N[1]	PK2N[0]	
6 <sup>th</sup> Parameter	1	↑	1	-	-	-	PK3N[5]	PK3N[4]	PK3N[3]	PK3N[2]	PK3N[1]	PK3N[0]	
7 <sup>th</sup> Parameter	1	↑	1	-	-	-	PK4N[5]	PK4N[4]	PK4N[3]	PK4N[2]	PK4N[1]	PK4N[0]	
8 <sup>th</sup> Parameter	1	↑	1	-	-	-	PK5N[5]	PK5N[4]	PK5N[3]	PK5N[2]	PK5N[1]	PK5N[0]	
9 <sup>th</sup> Parameter	1	↑	1	-	-	-	PK6N[5]	PK6N[4]	PK6N[3]	PK6N[2]	PK6N[1]	PK6N[0]	
10 <sup>th</sup> Parameter	1	↑	1	-	-	-	PK7N[5]	PK7N[4]	PK7N[3]	PK7N[2]	PK7N[1]	PK7N[0]	
11 <sup>th</sup> Parameter	1	↑	1	-	-	-	PK8N[5]	PK8N[4]	PK8N[3]	PK8N[2]	PK8N[1]	PK8N[0]	
12 <sup>th</sup> Parameter	1	↑	1	-	-	-	PK9N[5]	PK9N[4]	PK9N[3]	PK9N[2]	PK9N[1]	PK9N[0]	
13 <sup>th</sup> Parameter	1	↑	1	-	-	-	SELV0N[5]	SELV0N[4]	SELV0N[3]	SELV0N[2]	SELV0N[1]	SELV0N[0]	
14 <sup>th</sup> Parameter	1	↑	1	-	-	-	SELV1N[5]	SELV1N[4]	SELV1N[3]	SELV1N[2]	SELV1N[1]	SELV1N[0]	
15 <sup>th</sup> Parameter	1	↑	1	-	-	-	SELV62N[5]	SELV62N[4]	SELV62N[3]	SELV62N[2]	SELV62N[1]	SELV62N[0]	
16 <sup>th</sup> Parameter	1	↑	1	-	-	-	SELV63N[5]	SELV63N[4]	SELV63N[3]	SELV63N[2]	SELV63N[1]	SELV63N[0]	

NOTE: "-" Don't care

Description	Register Group	Negative Polarity	Set-up Contents
	Description	High level adjustment	VRF0N[5:0]
Mid level adjustment		SELV0N[5:0]	The voltage of grayscale number 0 is selected by the 64 to 1 selector
		SELV1N[5:0]	The voltage of grayscale number 1 is selected by the 64 to 1 selector
		PK0N[5:0]	The voltage of grayscale number 3 is selected by the 64 to 1 selector
		PK1N[5:0]	The voltage of grayscale number 6 is selected by the 64 to 1 selector
		PK2N[5:0]	The voltage of grayscale number 11 is selected by the 64 to 1 selector
		PK3N[5:0]	The voltage of grayscale number 19 is selected by the 64 to 1 selector
		PK4N[5:0]	The voltage of grayscale number 27 is selected by the 64 to 1 selector
		PK5N[5:0]	The voltage of grayscale number 36 is selected by the 64 to 1 selector
		PK6N[5:0]	The voltage of grayscale number 44 is selected by the 64 to 1 selector
		PK7N[5:0]	The voltage of grayscale number 52 is selected by the 64 to 1 selector
		PK8N[5:0]	The voltage of grayscale number 57 is selected by the 64 to 1 selector
		PK9N[5:0]	The voltage of grayscale number 60 is selected by the 64 to 1 selector
		SELV62N[5:0]	The voltage of grayscale number 62 is selected by the 64 to 1 selector
		SELV63N[5:0]	The voltage of grayscale number 63 is selected by the 64 to 1 selector
Low level adjustment	VOS0N[5:0]	Variable resistor VRLN	

## 11. Power structure

### 11.1. Driver IC Operating voltages Specification

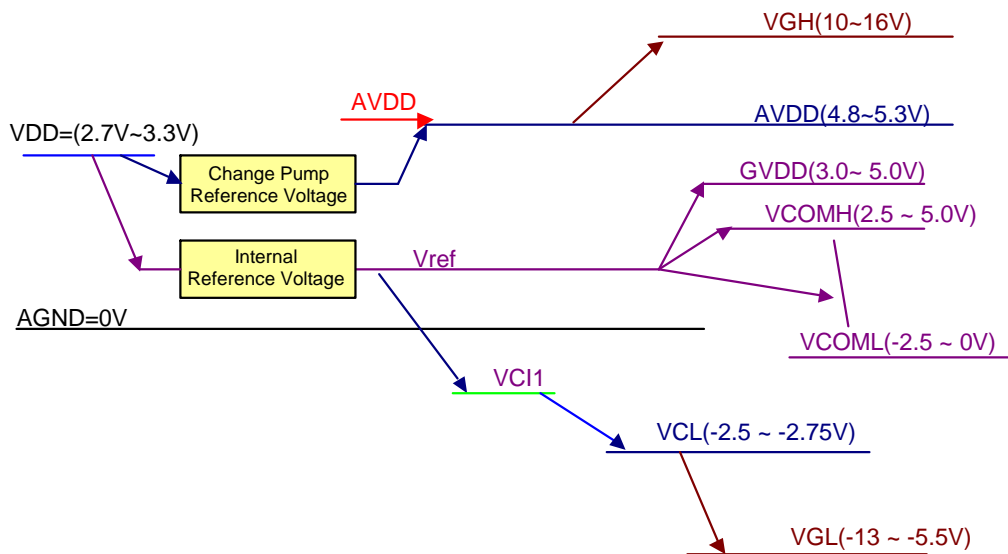


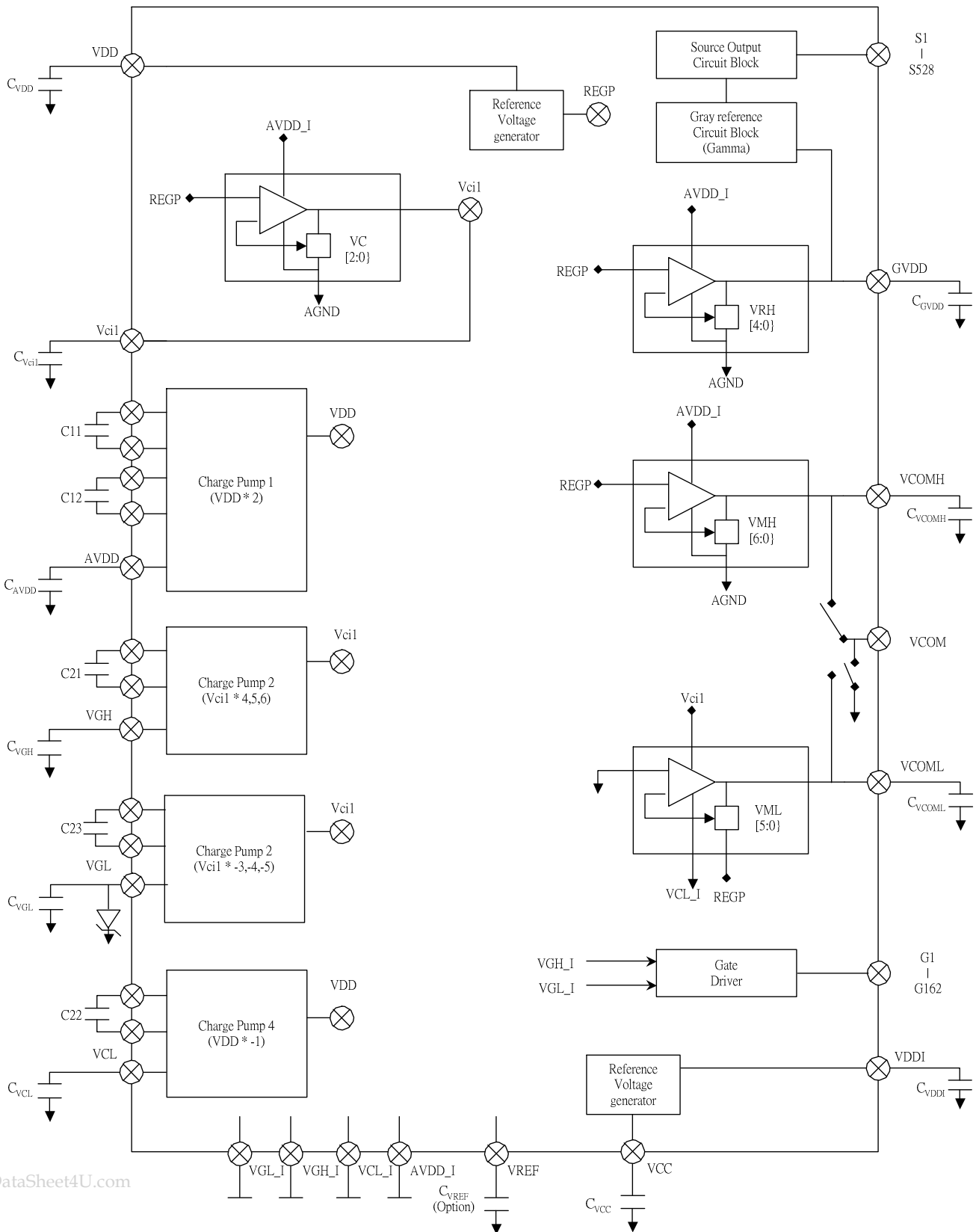
Fig 11.1.1 Power Booster Level

#### Remark

1. AVDD supply to all power source (exclude VGH, VGL)
2. Linear Range: 0.2V ~ AVDD-0.1V (For all output voltage, but exclude VGH, VGL)
3. Above operating voltages is min range.

11.2 Power Step1/2/4 Circuit

11.2.1 VCI1 generate from Vref



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Fig. 11.2.1 Power Booster Structure (1)

## 11.2.2 EXTERNAL COMPONENTS CONNECTION

Pad Name	Connection	Rated (Min) Voltage	Typical capacitance value
VDDI	VDDI (Logic Power)	6.3V	1.0 uF
VDD	VDD (Analog Power)	6.3V	1.0 uF
VCC	Connect to Capacitor (Max 3V): VCC -----  ----- GND	6.3V	1.0 uF
AGND	Analog ground (Connect to GND)		
DGND	Digital ground (Connect to GND)		
C23P, C23N	Connect to Capacitor: C23P -----  -----C23N	16.0V	1.0 uF
C22P, C22N	Connect to Capacitor: C22P -----  -----C22N	25.0V	1.0 uF
C21P, C22N	Connect to Capacitor: C21P -----  -----C21N	6.3V	1.0 uF
C12P, C12N	Connect to Capacitor: C12P -----  -----C12N	6.3V	1.0 uF
C11P, C11N	Connect to Capacitor: C11P -----  -----C11N	6.3V	1.0 uF
AVDD	Connect to Capacitor: AVDD -----  ----- GND	6.3V	1.0 uF
VCI1	Connect to Capacitor: AVDD -----  ----- GND	6.3V	1.0 uF
VGH	Connect to Capacitor: VGH -----  ----- GND	25.0V	1.0 uF
VGL	Connect to Capacitor: VGL -----  ----- GND	16.0V	1.0 uF
VCL	Connect to Capacitor: VCL -----  ----- GND	6.3V	1.0 uF
VREF	Connect to Capacitor: VREF -----  ----- GND(Optional)	6.3V	1.0 uF
GVDD	Connect to Capacitor: GVDD -----  ----- GND(Optional)	6.3V	1.0 uF
VCOMH	Connect to Capacitor: VCOMH-----  ----- GND	6.3V	1.0 uF
VCOML	Connect to Capacitor: VCOML -----  ----- GND	6.3V	1.0 uF
VGL	Connect to Schottky diode: VGL ----->  ----- GND	30V	Schottky diode(note1)

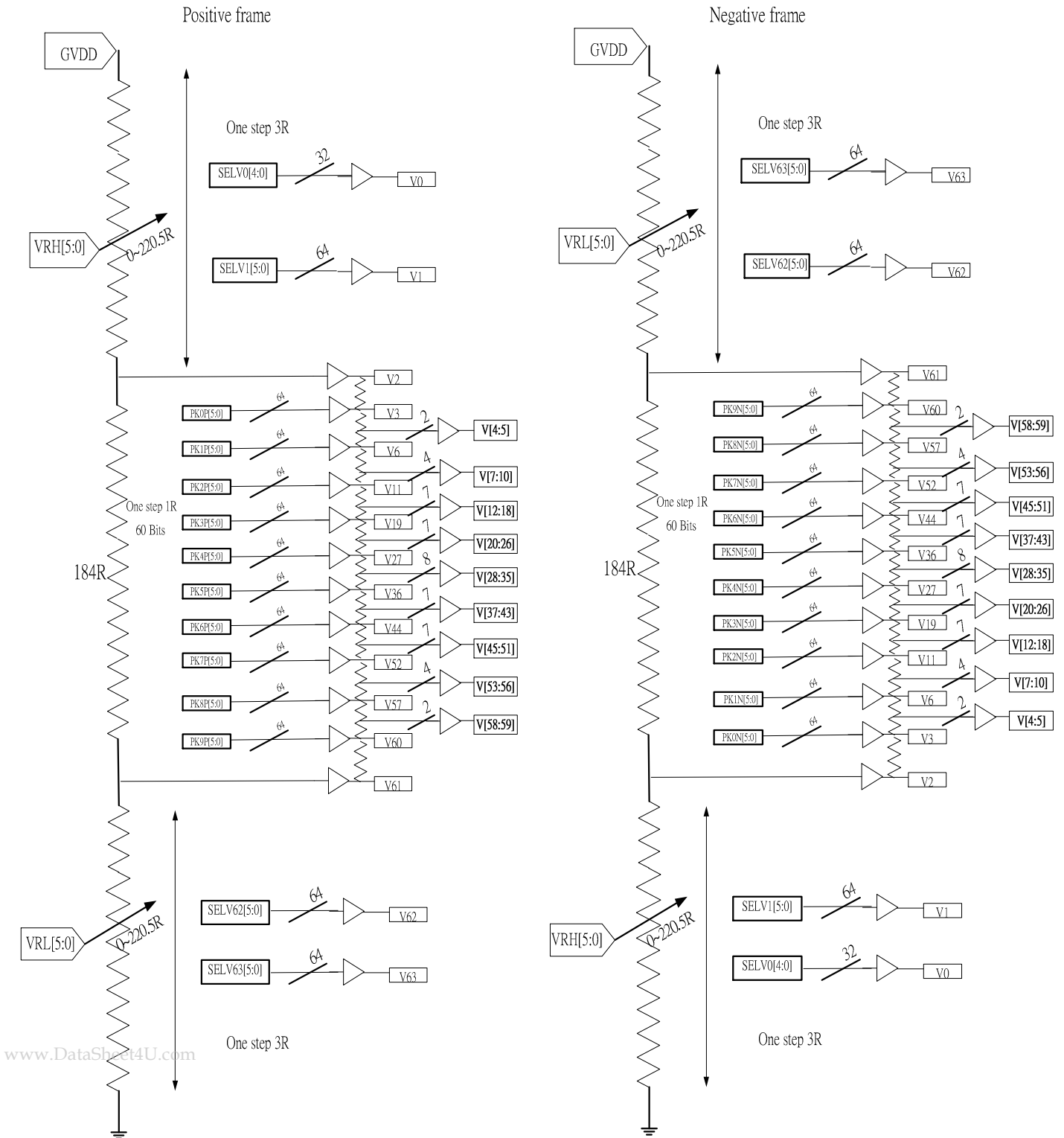
Note1: Leakage current must to be smaller than 20uA when the schottky diode operates at -30~85°C .



12. Gamma structure

12.1 STRUCTURE OF GRAYSCALE AMPLIFIER

The structure of grayscale amplifier is shown as below. 16 voltage levels (VIN0-VIN15) between GVDD and VGS are determined by the high/ mid/ low level adjustment registers. Each mid-adjustment level is split into 64 levels again by the internal ladder resistor network. As a result, grayscale amplifier generates 64 voltage levels ranging from V0 to V63 and outputs one of 64 levels.



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## 12.2 ST7773 Gamma Voltage Formula (Positive/ Negative Polarity)

Grayscale	Voltage Formula(Positive)	Voltage Formula(Negative)
0	VINP0	VINN0
1	VINP1	VINN1
2	VINP2	VINN2
3	VINP3	VINN3
4	$V3-(V3-V6)*(11/30)$	$V3-(V3-V6)*(11/30)$
5	$V3-(V3-V6)*(21/30)$	$V3-(V3-V6)*(21/30)$
6	VINP4	VINN4
7	$V6-(V6-V11)*(7/30)$	$V6-(V6-V11)*(7/30)$
8	$V6-(V6-V11)*(14/30)$	$V6-(V6-V11)*(14/30)$
9	$V6-(V6-V11)*(20/30)$	$V6-(V6-V11)*(20/30)$
10	$V6-(V6-V11)*(25/30)$	$V6-(V6-V11)*(25/30)$
11	VINP5	VINN5
12	$V11-(V11-V19)*(4/32)$	$V11-(V11-V19)*(4/32)$
13	$V11-(V11-V19)*(8/32)$	$V11-(V11-V19)*(8/32)$
14	$V11-(V11-V19)*(12/32)$	$V11-(V11-V19)*(12/32)$
15	$V11-(V11-V19)*(16/32)$	$V11-(V11-V19)*(16/32)$
16	$V11-(V11-V19)*(20/32)$	$V11-(V11-V19)*(20/32)$
17	$V11-(V11-V19)*(24/32)$	$V11-(V11-V19)*(24/32)$
18	$V11-(V11-V19)*(28/32)$	$V11-(V11-V19)*(28/32)$
19	VINP6	VINN6
20	$V19-(V19-V27)*(4/32)$	$V19-(V19-V27)*(4/32)$
21	$V19-(V19-V27)*(8/32)$	$V19-(V19-V27)*(8/32)$
22	$V19-(V19-V27)*(12/32)$	$V19-(V19-V27)*(12/32)$
23	$V19-(V19-V27)*(16/32)$	$V19-(V19-V27)*(16/32)$
24	$V19-(V19-V27)*(20/32)$	$V19-(V19-V27)*(20/32)$
25	$V19-(V19-V27)*(24/32)$	$V19-(V19-V27)*(24/32)$
26	$V19-(V19-V27)*(28/32)$	$V19-(V19-V27)*(28/32)$
27	VINP7	VINN7
28	$V27-(V27-V36)*(4/36)$	$V27-(V27-V36)*(4/36)$
29	$V27-(V27-V36)*(8/36)$	$V27-(V27-V36)*(8/36)$
30	$V27-(V27-V36)*(12/36)$	$V27-(V27-V36)*(12/36)$
31	$V27-(V27-V36)*(16/36)$	$V27-(V27-V36)*(16/36)$
32	$V27-(V27-V36)*(20/36)$	$V27-(V27-V36)*(20/36)$
33	$V27-(V27-V36)*(24/36)$	$V27-(V27-V36)*(24/36)$
34	$V27-(V27-V36)*(28/36)$	$V27-(V27-V36)*(28/36)$
35	$V27-(V27-V36)*(32/36)$	$V27-(V27-V36)*(32/36)$
36	VINP8	VINN8
37	$V36-(V36-V44)*(4/32)$	$V36-(V36-V44)*(4/32)$
38	$V36-(V36-V44)*(8/32)$	$V36-(V36-V44)*(8/32)$
39	$V36-(V36-V44)*(12/32)$	$V36-(V36-V44)*(12/32)$
40	$V36-(V36-V44)*(16/32)$	$V36-(V36-V44)*(16/32)$
41	$V36-(V36-V44)*(20/32)$	$V36-(V36-V44)*(20/32)$
42	$V36-(V36-V44)*(24/32)$	$V36-(V36-V44)*(24/32)$
43	$V36-(V36-V44)*(28/32)$	$V36-(V36-V44)*(28/32)$
44	VINP9	VINN9
45	$V44-(V44-V52)*(4/32)$	$V44-(V44-V52)*(4/32)$
46	$V44-(V44-V52)*(8/32)$	$V44-(V44-V52)*(8/32)$
47	$V44-(V44-V52)*(12/32)$	$V44-(V44-V52)*(12/32)$
48	$V44-(V44-V52)*(16/32)$	$V44-(V44-V52)*(16/32)$
49	$V44-(V44-V52)*(20/32)$	$V44-(V44-V52)*(20/32)$
50	$V44-(V44-V52)*(24/32)$	$V44-(V44-V52)*(24/32)$
51	$V44-(V44-V52)*(28/32)$	$V44-(V44-V52)*(28/32)$
52	VINP10	VINN10
53	$V52-(V52-V57)*(5/30)$	$V52-(V52-V57)*(5/30)$
54	$V52-(V52-V57)*(11/30)$	$V52-(V52-V57)*(11/30)$

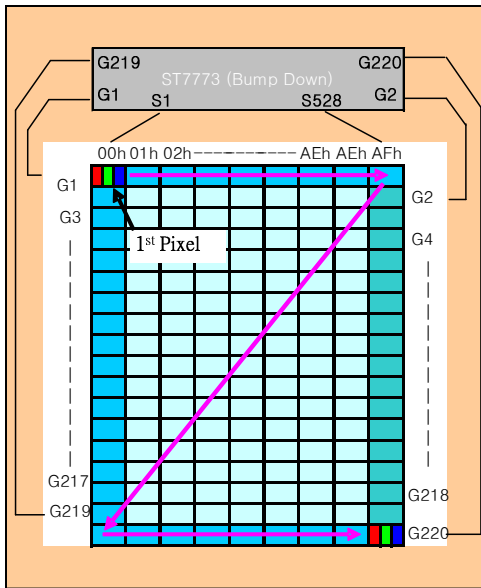
## ST7773

55	V52-(V52-V57)*(17/30)	V52-(V52-V57)*(17/30)
56	V52-(V52-V57)*(23/30)	V52-(V52-V57)*(23/30)
57	VINP11	VINN11
58	V57-(V57-V60)*(8/30)	V57-(V57-V60)*(8/30)
59	V57-(V57-V60)*(18/30)	V57-(V57-V60)*(18/30)
60	VINP12	VINN12
61	VINP13	VINN13
62	VINP14	VINN14
63	VINP15	VINN15

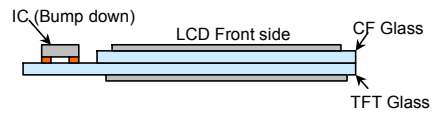
## 13. Example Connection with Panel direction and Different Resolution

Case 1: (This is default case)

- 1<sup>st</sup> Pixel is at *Left Top* of the panel
- RGB filter order = **RGB**

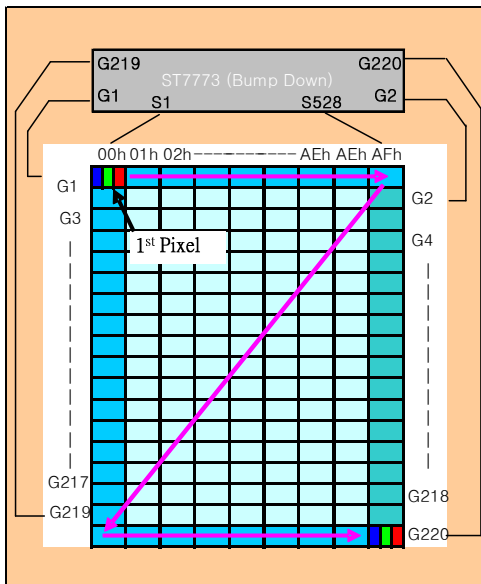


- Direction default setting (H/W)
  - SMX = '0'
  - SMY = '0'
  - SRGB = '0'
- S1 = Filter **R**
- S2 = Filter **G**
- S3 = Filter **B**
- Display direction control (S/W)
  - X-Mirror control by MX
  - Y-Mirror control by MY
  - XY-Exchange control by MV

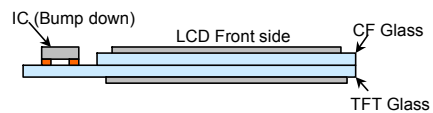


Case 2:

- 1<sup>st</sup> Pixel is at *Left Top* of the panel
- RGB filter order = **BGR**



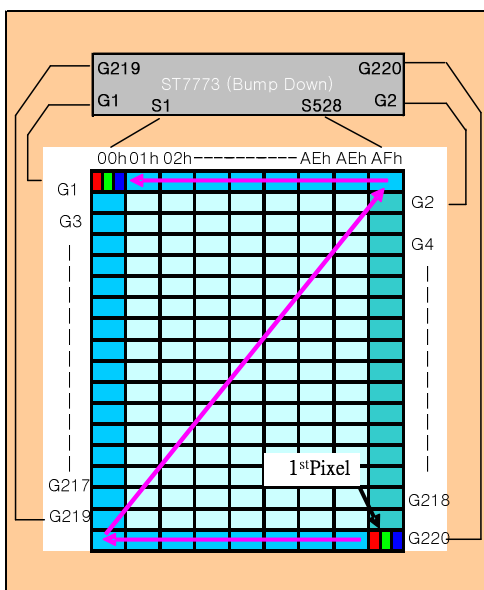
- Direction default setting (H/W)
  - SMX = '0'
  - SMY = '0'
  - SRGB = '1'
- S1 = Filter **B**
- S2 = Filter **G**
- S3 = Filter **R**
- Display direction control (S/W)
  - X-Mirror control by MX
  - Y-Mirror control by MY
  - XY-Exchange control by MV



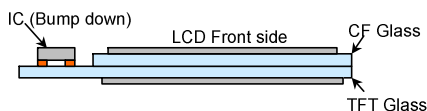
# ST7773

## Case 3:

- 1<sup>st</sup> Pixel is at *Right Bottom* of the panel
- RGB filter order = **RGB**

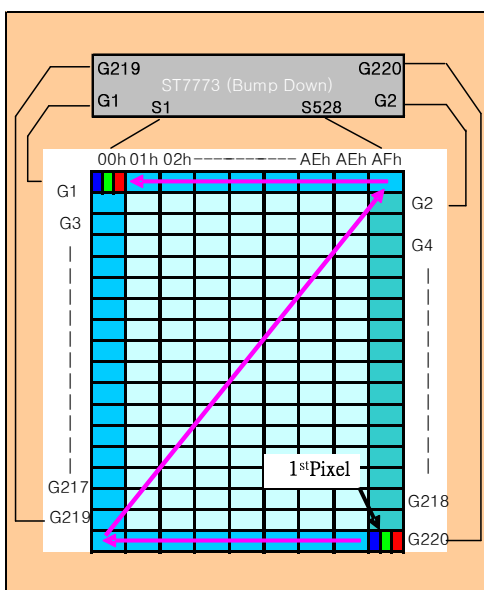


- Direction default setting (H/W)
  - SMX = '1'
  - SMY = '1'
  - SRGB = '0'
- S1 = Filter **R**
- S2 = Filter **G**
- S3 = Filter **B**
- Display direction control (S/W)
  - X-Mirror control by MX
  - Y-Mirror control by MY
  - XY-Exchange control by MV

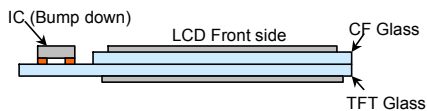


## Case 4:

- 1<sup>st</sup> Pixel is at *Right Bottom* of the panel
- RGB filter order = **BGR**



- Direction default setting (H/W)
  - SMX = '1'
  - SMY = '1'
  - SRGB = '1'
- S1 = Filter **B**
- S2 = Filter **G**
- S3 = Filter **R**
- Display direction control (S/W)
  - X-Mirror control by MX
  - Y-Mirror control by MY
  - XY-Exchange control by MV



## 13.3 MicroProcessor Interface applications

### 13.3.1 8080-Series MCU Interface for 8-bit data bus (IM1, IM0="00")

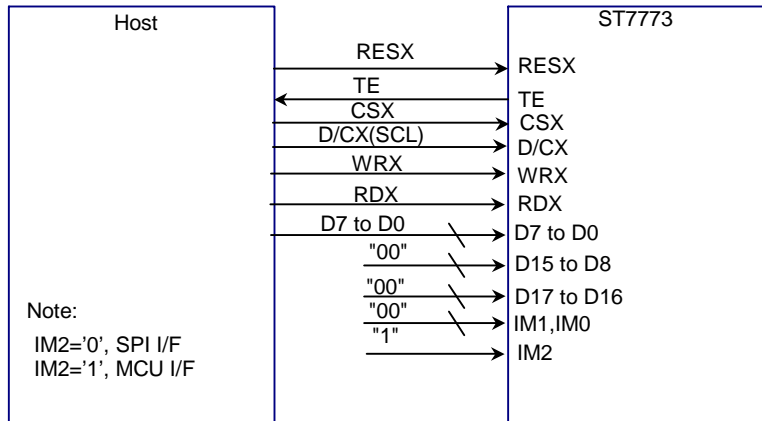


Fig.13.3.1 8080-Series MCU Interface for 8-bit data bus

### 13.3.2 8080-Series MCU Interface for 16-bit data bus (IM1, IM0="01")

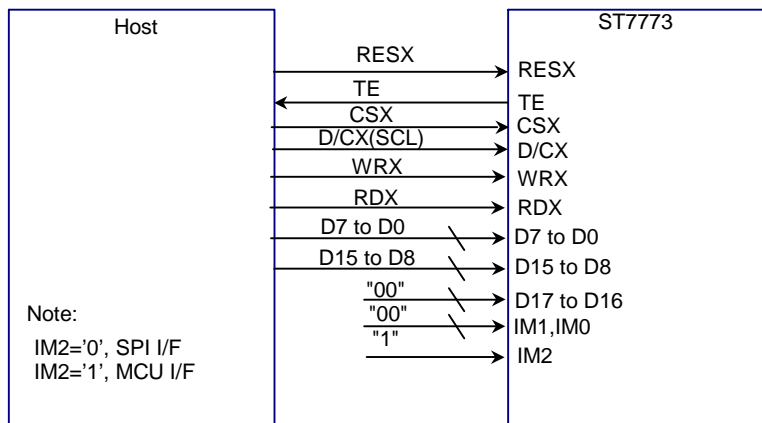


Fig.13.3.2 8080-Series MCU Interface for 16-bit data bus

## 13.3.3 8080-Series MCU Interface for 9-bit data bus (IM1, IM0="10")

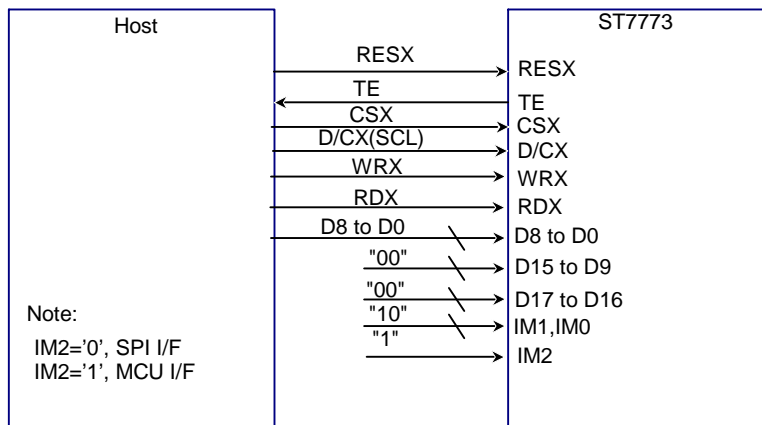


Fig.13.3.3 8080-Series MCU Interface for 9-bit data bus

## 13.3.4 8080-Series MCU Interface for 18-bit data bus (IM1, IM0="11")

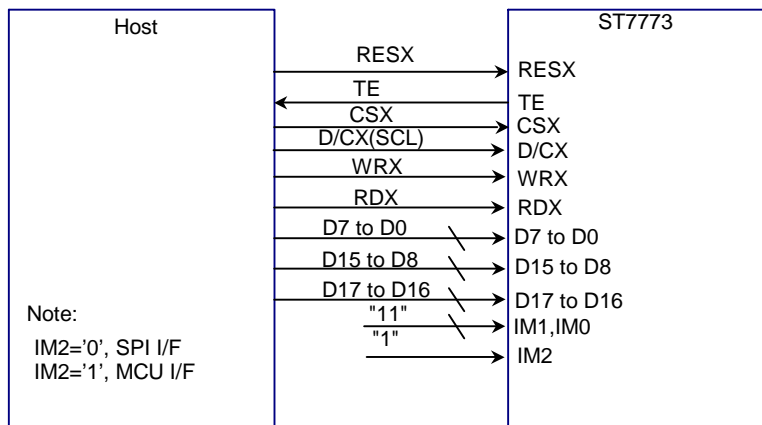


Fig.13.3.4 8080-Series MCU Interface for 18-bit data bus

## 13.3.5 3-line Series Interface(IM2="0")

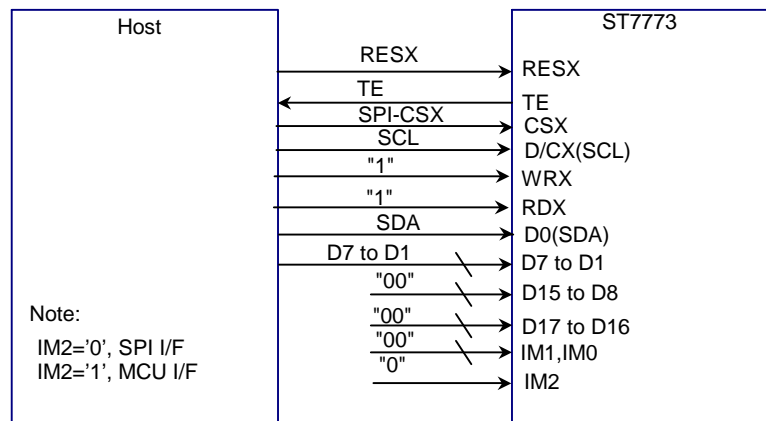


Fig.13.3.5 SPI 3-line Interface

<b>ST7773 Serial Specification Revision History</b>		
<b>Version</b>	<b>Date</b>	<b>Description</b>
1.x	2008/01/--	Preliminary
2.0	2008/07/04	Mass Production release