



# Sitronix

## ST7787

### 262K Color Single-Chip TFT Controller/Driver

#### 1. Introduction

The ST7787 is a single-chip controller/driver for 262K-color, graphic type TFT-LCD. It consists of 720 source line and 320 gate line driving circuits. This chip is capable of connecting directly to an external microprocessor, and accepts Serial Peripheral Interface (SPI), 8-bits/9-bits/16-bits/18-bits parallel interface. Display data can be stored in the on-chip display data RAM of 240x320x18 bits. It can perform display data RAM read/write operation with no external operation clock to minimize power consumption. In addition, because of the integrated power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

#### 2. Features

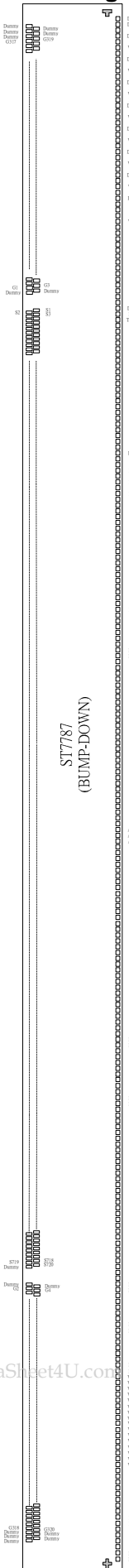
- ◆ Single chip TFT-LCD controller/driver with display data RAM
- ◆ Display resolution: 240(H) x RGB x 320(V)
- ◆ Display data RAM (frame memory): 240 x 320 x 18-bits = 1,382,400 bits
- ◆ Operation Frequency: DC~30MHz (30MHz for 6 bits, 10MHz for 18 bits)
- ◆ Output:
  - 240ch source outputs (240RGB)
  - 320ch gate outputs
  - Common electrode output
- ◆ Display mode (color mode)
  - Full color mode (idle mode off): 262K-colors
  - Reduce color mode (idle mode on): 8-colors (1-bit for individual R, G, B color depth)
- ◆ Display resolution option
  - 240 x 320 Display with 240 x 18-bits x 320 display RAM
- ◆ Supported LC type option
  - MVA LC type (When LCM[1]=0,LCM[0]=0 )
  - Transflective LC type (When LCM[1]=0,LCM[0]=1 )
  - Transmissive LC type (When LCM[1]=1,LCM[0]=0 )
- ◆ Supported data format on display host interface
  - 12-bits/pixel: RGB= (444) using the 1382k bits frame memory and LUT
  - 16-bits/pixel: RGB= (565) using the 1382k bits frame memory and LUT
  - 18-bits/pixel: RGB= (666) using the 1382k bits frame memory
- ◆ Supported MCU Interface
  - 3-line serial interface
  - 8-bits, 9-bits, 16-bits, 18-bits interface with 8080-series MCU
  - 8-bits, 9-bits, 16-bits, 18-bits interface with 6800-series MCU
  - 6-bits, 16-bits, 18-bits RGB interface with graphic controller
- ◆ Display features
  - Area scrolling
  - Partial display mode
  - Software programmable color depth mode
- ◆ Build-in circuit
  - DC/DC converter
  - Adjustable VCOM generation
  - Non-volatile (NV) memory to store initial register setting
  - Oscillator for display clock generation
  - Timing controller
  - 4 preset gamma curve for  $\gamma = 1.0/1.8/2.2/2.5$  (supporting Transflective) and 1 preset gamma curve for  $\gamma = 2.2$  (supporting MVA, Transmissive type LC)
  - Factory default value (contrast, module ID, module version, etc) are stored in NV memory
  - Line inversion, frame inversion
- ◆ NV Memory
  - 8-bits for ID1
  - 7-bits for ID2
  - 8-bits for ID3
  - 8-bits for VCOM adjustment
- ◆ Supply voltage range
  - Analog supply voltage range (VDD to AGND): 2.45V – 3.3V
  - I/O supply voltage range (VDDI to DGND): 1.65V – 3.3V

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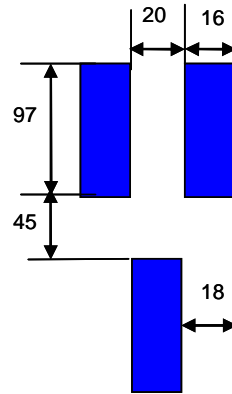
- ◆ Output voltage level
  - Source output voltage range (GVDD to AGND): 3.0V to 5.0V
  - Power supply range for driver circuit (AVDD to AGND): 5.2V (VDD=2.6V) to 6.0V (VDD=3.0V)
  - Output range of HIGH level of VCOM (VCOMH to AGND): 2.5V to 5.0V
  - Output range of LOW level of VCOM (VCOML to AGND): -2.5V to 0.0V
  - Output range of HIGH level of gate driver (VGH to AGND): +12V to +16.5V
  - Output range of LOW level of gate driver (VGL to AGND): -14V to -5V
- ◆ Lower power consumption, suitable for battery operated systems
  - CMOS compatible inputs
  - Optimized layout for COG assembly
  - Operate temperature range: -30 °C to +70°C

3. Pad arrangement

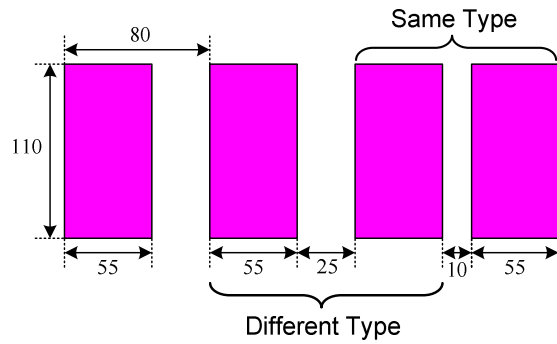


**View point: bump view**  
**Chip size (um): 19384 x 1170**  
**PAD coordinate: pad center**  
**Coordinate origin: chip center**  
**Chip thickness (um): 300**  
**Bump height (um): 15**  
**Bump hardness (HV): 75±25**

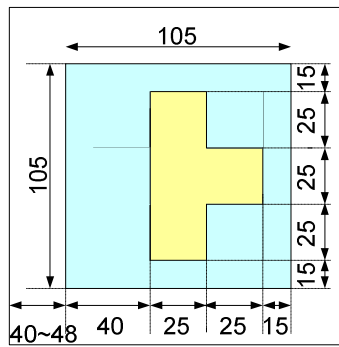
**Pad arrangement (Unit: um):**  
**Output: pad No. 1 ~ 1069 = 16 x 97**



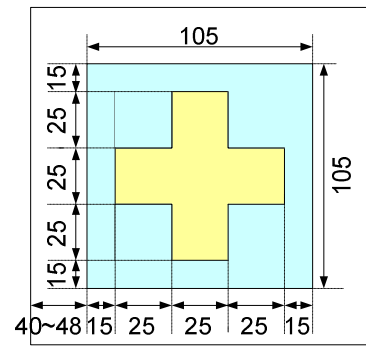
**Input: pad No. 1070 ~ 1335 = 55 x 110**



**Alignment mark (unit: um):**  
 (-9533,-248.77)



(9544,-248.77)



## 4. Pad Center Coordinates

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1	DUMMY	9612	486.72	41	G250	8892	486.72
2	DUMMY	9594	344.72	42	G248	8874	344.72
3	DUMMY	9576	486.72	43	G246	8856	486.72
4	DUMMY	9558	344.72	44	G244	8838	344.72
5	DUMMY	9540	486.72	45	G242	8820	486.72
6	G320	9522	344.72	46	G240	8802	344.72
7	G318	9504	486.72	47	G238	8784	486.72
8	G316	9486	344.72	48	G236	8766	344.72
9	G314	9468	486.72	49	G234	8748	486.72
10	G312	9450	344.72	50	G232	8730	344.72
11	G310	9432	486.72	51	G230	8712	486.72
12	G308	9414	344.72	52	G228	8694	344.72
13	G306	9396	486.72	53	G226	8676	486.72
14	G304	9378	344.72	54	G224	8658	344.72
15	G302	9360	486.72	55	G222	8640	486.72
16	G300	9342	344.72	56	G220	8622	344.72
17	G298	9324	486.72	57	G218	8604	486.72
18	G296	9306	344.72	58	G216	8586	344.72
19	G294	9288	486.72	59	G214	8568	486.72
20	G292	9270	344.72	60	G212	8550	344.72
21	G290	9252	486.72	61	G210	8532	486.72
22	G288	9234	344.72	62	G208	8514	344.72
23	G286	9216	486.72	63	G206	8496	486.72
24	G284	9198	344.72	64	G204	8478	344.72
25	G282	9180	486.72	65	G202	8460	486.72
26	G280	9162	344.72	66	G200	8442	344.72
27	G278	9144	486.72	67	G198	8424	486.72
28	G276	9126	344.72	68	G196	8406	344.72
29	G274	9108	486.72	69	G194	8388	486.72
30	G272	9090	344.72	70	G192	8370	344.72
31	G270	9072	486.72	71	G190	8352	486.72
32	G268	9054	344.72	72	G188	8334	344.72
33	G266	9036	486.72	73	G186	8316	486.72
34	G264	9018	344.72	74	G184	8298	344.72
35	G262	9000	486.72	75	G182	8280	486.72
36	G260	8982	344.72	76	G180	8262	344.72
37	G258	8964	486.72	77	G178	8244	486.72
38	G256	8946	344.72	78	G176	8226	344.72
39	G254	8928	486.72	79	G174	8208	486.72
40	G252	8910	344.72	80	G172	8190	344.72

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PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
81	G170	8172	486.72	121	G90	7452	486.72
82	G168	8154	344.72	122	G88	7434	344.72
83	G166	8136	486.72	123	G86	7416	486.72
84	G164	8118	344.72	124	G84	7398	344.72
85	G162	8100	486.72	125	G82	7380	486.72
86	G160	8082	344.72	126	G80	7362	344.72
87	G158	8064	486.72	127	G78	7344	486.72
88	G156	8046	344.72	128	G76	7326	344.72
89	G154	8028	486.72	129	G74	7308	486.72
90	G152	8010	344.72	130	G72	7290	344.72
91	G150	7992	486.72	131	G70	7272	486.72
92	G148	7974	344.72	132	G68	7254	344.72
93	G146	7956	486.72	133	G66	7236	486.72
94	G144	7938	344.72	134	G64	7218	344.72
95	G142	7920	486.72	135	G62	7200	486.72
96	G140	7902	344.72	136	G60	7182	344.72
97	G138	7884	486.72	137	G58	7164	486.72
98	G136	7866	344.72	138	G56	7146	344.72
99	G134	7848	486.72	139	G54	7128	486.72
100	G132	7830	344.72	140	G52	7110	344.72
101	G130	7812	486.72	141	G50	7092	486.72
102	G128	7794	344.72	142	G48	7074	344.72
103	G126	7776	486.72	143	G46	7056	486.72
104	G124	7758	344.72	144	G44	7038	344.72
105	G122	7740	486.72	145	G42	7020	486.72
106	G120	7722	344.72	146	G40	7002	344.72
107	G118	7704	486.72	147	G38	6984	486.72
108	G116	7686	344.72	148	G36	6966	344.72
109	G114	7668	486.72	149	G34	6948	486.72
110	G112	7650	344.72	150	G32	6930	344.72
111	G110	7632	486.72	151	G30	6912	486.72
112	G108	7614	344.72	152	G28	6894	344.72
113	G106	7596	486.72	153	G26	6876	486.72
114	G104	7578	344.72	154	G24	6858	344.72
115	G102	7560	486.72	155	G22	6840	486.72
116	G100	7542	344.72	156	G20	6822	344.72
117	G98	7524	486.72	157	G18	6804	486.72
118	G96	7506	344.72	158	G16	6786	344.72
119	G94	7488	486.72	159	G14	6768	486.72
120	G92	7470	344.72	160	G12	6750	344.72

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PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
161	G10	6732	486.72	201	S691	6012	486.72
162	G8	6714	344.72	202	S690	5994	344.72
163	G6	6696	486.72	203	S689	5976	486.72
164	G4	6678	344.72	204	S688	5958	344.72
165	G2	6660	486.72	205	S687	5940	486.72
166	DUMMY	6642	344.72	206	S686	5922	344.72
167	DUMMY	6624	486.72	207	S685	5904	486.72
168	DUMMY	6606	344.72	208	S684	5886	344.72
169	DUMMY	6588	486.72	209	S683	5868	486.72
170	DUMMY	6570	344.72	210	S682	5850	344.72
171	DUMMY	6552	486.72	211	S681	5832	486.72
172	S720	6534	344.72	212	S680	5814	344.72
173	S719	6516	486.72	213	S679	5796	486.72
174	S718	6498	344.72	214	S678	5778	344.72
175	S717	6480	486.72	215	S677	5760	486.72
176	S716	6462	344.72	216	S676	5742	344.72
177	S715	6444	486.72	217	S675	5724	486.72
178	S714	6426	344.72	218	S674	5706	344.72
179	S713	6408	486.72	219	S673	5688	486.72
180	S712	6390	344.72	220	S672	5670	344.72
181	S711	6372	486.72	221	S671	5652	486.72
182	S710	6354	344.72	222	S670	5634	344.72
183	S709	6336	486.72	223	S669	5616	486.72
184	S708	6318	344.72	224	S668	5598	344.72
185	S707	6300	486.72	225	S667	5580	486.72
186	S706	6282	344.72	226	S666	5562	344.72
187	S705	6264	486.72	227	S665	5544	486.72
188	S704	6246	344.72	228	S664	5526	344.72
189	S703	6228	486.72	229	S663	5508	486.72
190	S702	6210	344.72	230	S662	5490	344.72
191	S701	6192	486.72	231	S661	5472	486.72
192	S700	6174	344.72	232	S660	5454	344.72
193	S699	6156	486.72	233	S659	5436	486.72
194	S698	6138	344.72	234	S658	5418	344.72
195	S697	6120	486.72	235	S657	5400	486.72
196	S696	6102	344.72	236	S656	5382	344.72
197	S695	6084	486.72	237	S655	5364	486.72
198	S694	6066	344.72	238	S654	5346	344.72
199	S693	6048	486.72	239	S653	5328	486.72
200	S692	6030	344.72	240	S652	5310	344.72

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PAD No.	PIN Name	X	Y
241	S651	5292	486.72
242	S650	5274	344.72
243	S649	5256	486.72
244	S648	5238	344.72
245	S647	5220	486.72
246	S646	5202	344.72
247	S645	5184	486.72
248	S644	5166	344.72
249	S643	5148	486.72
250	S642	5130	344.72
251	S641	5112	486.72
252	S640	5094	344.72
253	S639	5076	486.72
254	S638	5058	344.72
255	S637	5040	486.72
256	S636	5022	344.72
257	S635	5004	486.72
258	S634	4986	344.72
259	S633	4968	486.72
260	S632	4950	344.72
261	S631	4932	486.72
262	S630	4914	344.72
263	S629	4896	486.72
264	S628	4878	344.72
265	S627	4860	486.72
266	S626	4842	344.72
267	S625	4824	486.72
268	S624	4806	344.72
269	S623	4788	486.72
270	S622	4770	344.72
271	S621	4752	486.72
272	S620	4734	344.72
273	S619	4716	486.72
274	S618	4698	344.72
275	S617	4680	486.72
276	S616	4662	344.72
277	S615	4644	486.72
278	S614	4626	344.72
279	S613	4608	486.72
280	S612	4590	344.72

PAD No.	PIN Name	X	Y
281	S611	4572	486.72
282	S610	4554	344.72
283	S609	4536	486.72
284	S608	4518	344.72
285	S607	4500	486.72
286	S606	4482	344.72
287	S605	4464	486.72
288	S604	4446	344.72
289	S603	4428	486.72
290	S602	4410	344.72
291	S601	4392	486.72
292	S600	4374	344.72
293	S599	4356	486.72
294	S598	4338	344.72
295	S597	4320	486.72
296	S596	4302	344.72
297	S595	4284	486.72
298	S594	4266	344.72
299	S593	4248	486.72
300	S592	4230	344.72
301	S591	4212	486.72
302	S590	4194	344.72
303	S589	4176	486.72
304	S588	4158	344.72
305	S587	4140	486.72
306	S586	4122	344.72
307	S585	4104	486.72
308	S584	4086	344.72
309	S583	4068	486.72
310	S582	4050	344.72
311	S581	4032	486.72
312	S580	4014	344.72
313	S579	3996	486.72
314	S578	3978	344.72
315	S577	3960	486.72
316	S576	3942	344.72
317	S575	3924	486.72
318	S574	3906	344.72
319	S573	3888	486.72
320	S572	3870	344.72

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PAD No.	PIN Name	X	Y
321	S571	3852	486.72
322	S570	3834	344.72
323	S569	3816	486.72
324	S568	3798	344.72
325	S567	3780	486.72
326	S566	3762	344.72
327	S565	3744	486.72
328	S564	3726	344.72
329	S563	3708	486.72
330	S562	3690	344.72
331	S561	3672	486.72
332	S560	3654	344.72
333	S559	3636	486.72
334	S558	3618	344.72
335	S557	3600	486.72
336	S556	3582	344.72
337	S555	3564	486.72
338	S554	3546	344.72
339	S553	3528	486.72
340	S552	3510	344.72
341	S551	3492	486.72
342	S550	3474	344.72
343	S549	3456	486.72
344	S548	3438	344.72
345	S547	3420	486.72
346	S546	3402	344.72
347	S545	3384	486.72
348	S544	3366	344.72
349	S543	3348	486.72
350	S542	3330	344.72
351	S541	3312	486.72
352	S540	3294	344.72
353	S539	3276	486.72
354	S538	3258	344.72
355	S537	3240	486.72
356	S536	3222	344.72
357	S535	3204	486.72
358	S534	3186	344.72
359	S533	3168	486.72
360	S532	3150	344.72

PAD No.	PIN Name	X	Y
361	S531	3132	486.72
362	S530	3114	344.72
363	S529	3096	486.72
364	S528	3078	344.72
365	S527	3060	486.72
366	S526	3042	344.72
367	S525	3024	486.72
368	S524	3006	344.72
369	S523	2988	486.72
370	S522	2970	344.72
371	S521	2952	486.72
372	S520	2934	344.72
373	S519	2916	486.72
374	S518	2898	344.72
375	S517	2880	486.72
376	S516	2862	344.72
377	S515	2844	486.72
378	S514	2826	344.72
379	S513	2808	486.72
380	S512	2790	344.72
381	S511	2772	486.72
382	S510	2754	344.72
383	S509	2736	486.72
384	S508	2718	344.72
385	S507	2700	486.72
386	S506	2682	344.72
387	S505	2664	486.72
388	S504	2646	344.72
389	S503	2628	486.72
390	S502	2610	344.72
391	S501	2592	486.72
392	S500	2574	344.72
393	S499	2556	486.72
394	S498	2538	344.72
395	S497	2520	486.72
396	S496	2502	344.72
397	S495	2484	486.72
398	S494	2466	344.72
399	S493	2448	486.72
400	S492	2430	344.72

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PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
401	S491	2412	486.72	441	S451	1692	486.72
402	S490	2394	344.72	442	S450	1674	344.72
403	S489	2376	486.72	443	S449	1656	486.72
404	S488	2358	344.72	444	S448	1638	344.72
405	S487	2340	486.72	445	S447	1620	486.72
406	S486	2322	344.72	446	S446	1602	344.72
407	S485	2304	486.72	447	S445	1584	486.72
408	S484	2286	344.72	448	S444	1566	344.72
409	S483	2268	486.72	449	S443	1548	486.72
410	S482	2250	344.72	450	S442	1530	344.72
411	S481	2232	486.72	451	S441	1512	486.72
412	S480	2214	344.72	452	S440	1494	344.72
413	S479	2196	486.72	453	S439	1476	486.72
414	S478	2178	344.72	454	S438	1458	344.72
415	S477	2160	486.72	455	S437	1440	486.72
416	S476	2142	344.72	456	S436	1422	344.72
417	S475	2124	486.72	457	S435	1404	486.72
418	S474	2106	344.72	458	S434	1386	344.72
419	S473	2088	486.72	459	S433	1368	486.72
420	S472	2070	344.72	460	S432	1350	344.72
421	S471	2052	486.72	461	S431	1332	486.72
422	S470	2034	344.72	462	S430	1314	344.72
423	S469	2016	486.72	463	S429	1296	486.72
424	S468	1998	344.72	464	S428	1278	344.72
425	S467	1980	486.72	465	S427	1260	486.72
426	S466	1962	344.72	466	S426	1242	344.72
427	S465	1944	486.72	467	S425	1224	486.72
428	S464	1926	344.72	468	S424	1206	344.72
429	S463	1908	486.72	469	S423	1188	486.72
430	S462	1890	344.72	470	S422	1170	344.72
431	S461	1872	486.72	471	S421	1152	486.72
432	S460	1854	344.72	472	S420	1134	344.72
433	S459	1836	486.72	473	S419	1116	486.72
434	S458	1818	344.72	474	S418	1098	344.72
435	S457	1800	486.72	475	S417	1080	486.72
436	S456	1782	344.72	476	S416	1062	344.72
437	S455	1764	486.72	477	S415	1044	486.72
438	S454	1746	344.72	478	S414	1026	344.72
439	S453	1728	486.72	479	S413	1008	486.72
440	S452	1710	344.72	480	S412	990	344.72

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PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
481	S411	972	486.72	521	S371	252	486.72
482	S410	954	344.72	522	S370	234	344.72
483	S409	936	486.72	523	S369	216	486.72
484	S408	918	344.72	524	S368	198	344.72
485	S407	900	486.72	525	S367	180	486.72
486	S406	882	344.72	526	S366	162	344.72
487	S405	864	486.72	527	S365	144	486.72
488	S404	846	344.72	528	S364	126	344.72
489	S403	828	486.72	529	S363	108	486.72
490	S402	810	344.72	530	S362	90	344.72
491	S401	792	486.72	531	S361	72	486.72
492	S400	774	344.72	532	DUMMY	54	344.72
493	S399	756	486.72	533	DUMMY	36	486.72
494	S398	738	344.72	534	DUMMY	18	344.72
495	S397	720	486.72	535	DUMMY	0	486.72
496	S396	702	344.72	536	DUMMY	-18	344.72
497	S395	684	486.72	537	DUMMY	-36	486.72
498	S394	666	344.72	538	DUMMY	-54	344.72
499	S393	648	486.72	539	S360	-72	486.72
500	S392	630	344.72	540	S359	-90	344.715
501	S391	612	486.72	541	S358	-108	486.72
502	S390	594	344.72	542	S357	-126	344.715
503	S389	576	486.72	543	S356	-144	486.72
504	S388	558	344.72	544	S355	-162	344.715
505	S387	540	486.72	545	S354	-180	486.72
506	S386	522	344.72	546	S353	-198	344.715
507	S385	504	486.72	547	S352	-216	486.72
508	S384	486	344.72	548	S351	-234	344.715
509	S383	468	486.72	549	S350	-252	486.72
510	S382	450	344.72	550	S349	-270	344.715
511	S381	432	486.72	551	S348	-288	486.72
512	S380	414	344.72	552	S347	-306	344.715
513	S379	396	486.72	553	S346	-324	486.72
514	S378	378	344.72	554	S345	-342	344.715
515	S377	360	486.72	555	S344	-360	486.72
516	S376	342	344.72	556	S343	-378	344.715
517	S375	324	486.72	557	S342	-396	486.72
518	S374	306	344.72	558	S341	-414	344.715
519	S373	288	486.72	559	S340	-432	486.72
520	S372	270	344.72	560	S339	-450	344.715

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PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
561	S338	-468	486.72	601	S298	-1188	486.72
562	S337	-486	344.715	602	S297	-1206	344.715
563	S336	-504	486.72	603	S296	-1224	486.72
564	S335	-522	344.715	604	S295	-1242	344.715
565	S334	-540	486.72	605	S294	-1260	486.72
566	S333	-558	344.715	606	S293	-1278	344.715
567	S332	-576	486.72	607	S292	-1296	486.72
568	S331	-594	344.715	608	S291	-1314	344.715
569	S330	-612	486.72	609	S290	-1332	486.72
570	S329	-630	344.715	610	S289	-1350	344.715
571	S328	-648	486.72	611	S288	-1368	486.72
572	S327	-666	344.715	612	S287	-1386	344.715
573	S326	-684	486.72	613	S286	-1404	486.72
574	S325	-702	344.715	614	S285	-1422	344.715
575	S324	-720	486.72	615	S284	-1440	486.72
576	S323	-738	344.715	616	S283	-1458	344.715
577	S322	-756	486.72	617	S282	-1476	486.72
578	S321	-774	344.715	618	S281	-1494	344.715
579	S320	-792	486.72	619	S280	-1512	486.72
580	S319	-810	344.715	620	S279	-1530	344.715
581	S318	-828	486.72	621	S278	-1548	486.72
582	S317	-846	344.715	622	S277	-1566	344.715
583	S316	-864	486.72	623	S276	-1584	486.72
584	S315	-882	344.715	624	S275	-1602	344.715
585	S314	-900	486.72	625	S274	-1620	486.72
586	S313	-918	344.715	626	S273	-1638	344.715
587	S312	-936	486.72	627	S272	-1656	486.72
588	S311	-954	344.715	628	S271	-1674	344.715
589	S310	-972	486.72	629	S270	-1692	486.72
590	S309	-990	344.715	630	S269	-1710	344.715
591	S308	-1008	486.72	631	S268	-1728	486.72
592	S307	-1026	344.715	632	S267	-1746	344.715
593	S306	-1044	486.72	633	S266	-1764	486.72
594	S305	-1062	344.715	634	S265	-1782	344.715
595	S304	-1080	486.72	635	S264	-1800	486.72
596	S303	-1098	344.715	636	S263	-1818	344.715
597	S302	-1116	486.72	637	S262	-1836	486.72
598	S301	-1134	344.715	638	S261	-1854	344.715
599	S300	-1152	486.72	639	S260	-1872	486.72
600	S299	-1170	344.715	640	S259	-1890	344.715

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PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
641	S258	-1908	486.72	681	S218	-2628	486.72
642	S257	-1926	344.715	682	S217	-2646	344.715
643	S256	-1944	486.72	683	S216	-2664	486.72
644	S255	-1962	344.715	684	S215	-2682	344.715
645	S254	-1980	486.72	685	S214	-2700	486.72
646	S253	-1998	344.715	686	S213	-2718	344.715
647	S252	-2016	486.72	687	S212	-2736	486.72
648	S251	-2034	344.715	688	S211	-2754	344.715
649	S250	-2052	486.72	689	S210	-2772	486.72
650	S249	-2070	344.715	690	S209	-2790	344.715
651	S248	-2088	486.72	691	S208	-2808	486.72
652	S247	-2106	344.715	692	S207	-2826	344.715
653	S246	-2124	486.72	693	S206	-2844	486.72
654	S245	-2142	344.715	694	S205	-2862	344.715
655	S244	-2160	486.72	695	S204	-2880	486.72
656	S243	-2178	344.715	696	S203	-2898	344.715
657	S242	-2196	486.72	697	S202	-2916	486.72
658	S241	-2214	344.715	698	S201	-2934	344.715
659	S240	-2232	486.72	699	S200	-2952	486.72
660	S239	-2250	344.715	700	S199	-2970	344.715
661	S238	-2268	486.72	701	S198	-2988	486.72
662	S237	-2286	344.715	702	S197	-3006	344.715
663	S236	-2304	486.72	703	S196	-3024	486.72
664	S235	-2322	344.715	704	S195	-3042	344.715
665	S234	-2340	486.72	705	S194	-3060	486.72
666	S233	-2358	344.715	706	S193	-3078	344.715
667	S232	-2376	486.72	707	S192	-3096	486.72
668	S231	-2394	344.715	708	S191	-3114	344.715
669	S230	-2412	486.72	709	S190	-3132	486.72
670	S229	-2430	344.715	710	S189	-3150	344.715
671	S228	-2448	486.72	711	S188	-3168	486.72
672	S227	-2466	344.715	712	S187	-3186	344.715
673	S226	-2484	486.72	713	S186	-3204	486.72
674	S225	-2502	344.715	714	S185	-3222	344.715
675	S224	-2520	486.72	715	S184	-3240	486.72
676	S223	-2538	344.715	716	S183	-3258	344.715
677	S222	-2556	486.72	717	S182	-3276	486.72
678	S221	-2574	344.715	718	S181	-3294	344.715
679	S220	-2592	486.72	719	S180	-3312	486.72
680	S219	-2610	344.715	720	S179	-3330	344.715

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PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
721	S178	-3348	486.72	761	S138	-4068	486.72
722	S177	-3366	344.715	762	S137	-4086	344.715
723	S176	-3384	486.72	763	S136	-4104	486.72
724	S175	-3402	344.715	764	S135	-4122	344.715
725	S174	-3420	486.72	765	S134	-4140	486.72
726	S173	-3438	344.715	766	S133	-4158	344.715
727	S172	-3456	486.72	767	S132	-4176	486.72
728	S171	-3474	344.715	768	S131	-4194	344.715
729	S170	-3492	486.72	769	S130	-4212	486.72
730	S169	-3510	344.715	770	S129	-4230	344.715
731	S168	-3528	486.72	771	S128	-4248	486.72
732	S167	-3546	344.715	772	S127	-4266	344.715
733	S166	-3564	486.72	773	S126	-4284	486.72
734	S165	-3582	344.715	774	S125	-4302	344.715
735	S164	-3600	486.72	775	S124	-4320	486.72
736	S163	-3618	344.715	776	S123	-4338	344.715
737	S162	-3636	486.72	777	S122	-4356	486.72
738	S161	-3654	344.715	778	S121	-4374	344.715
739	S160	-3672	486.72	779	S120	-4392	486.72
740	S159	-3690	344.715	780	S119	-4410	344.715
741	S158	-3708	486.72	781	S118	-4428	486.72
742	S157	-3726	344.715	782	S117	-4446	344.715
743	S156	-3744	486.72	783	S116	-4464	486.72
744	S155	-3762	344.715	784	S115	-4482	344.715
745	S154	-3780	486.72	785	S114	-4500	486.72
746	S153	-3798	344.715	786	S113	-4518	344.715
747	S152	-3816	486.72	787	S112	-4536	486.72
748	S151	-3834	344.715	788	S111	-4554	344.715
749	S150	-3852	486.72	789	S110	-4572	486.72
750	S149	-3870	344.715	790	S109	-4590	344.715
751	S148	-3888	486.72	791	S108	-4608	486.72
752	S147	-3906	344.715	792	S107	-4626	344.715
753	S146	-3924	486.72	793	S106	-4644	486.72
754	S145	-3942	344.715	794	S105	-4662	344.715
755	S144	-3960	486.72	795	S104	-4680	486.72
756	S143	-3978	344.715	796	S103	-4698	344.715
757	S142	-3996	486.72	797	S102	-4716	486.72
758	S141	-4014	344.715	798	S101	-4734	344.715
759	S140	-4032	486.72	799	S100	-4752	486.72
760	S139	-4050	344.715	800	S99	-4770	344.715

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PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
801	S98	-4788	486.72	841	S58	-5508	486.72
802	S97	-4806	344.715	842	S57	-5526	344.715
803	S96	-4824	486.72	843	S56	-5544	486.72
804	S95	-4842	344.715	844	S55	-5562	344.715
805	S94	-4860	486.72	845	S54	-5580	486.72
806	S93	-4878	344.715	846	S53	-5598	344.715
807	S92	-4896	486.72	847	S52	-5616	486.72
808	S91	-4914	344.715	848	S51	-5634	344.715
809	S90	-4932	486.72	849	S50	-5652	486.72
810	S89	-4950	344.715	850	S49	-5670	344.715
811	S88	-4968	486.72	851	S48	-5688	486.72
812	S87	-4986	344.715	852	S47	-5706	344.715
813	S86	-5004	486.72	853	S46	-5724	486.72
814	S85	-5022	344.715	854	S45	-5742	344.715
815	S84	-5040	486.72	855	S44	-5760	486.72
816	S83	-5058	344.715	856	S43	-5778	344.715
817	S82	-5076	486.72	857	S42	-5796	486.72
818	S81	-5094	344.715	858	S41	-5814	344.715
819	S80	-5112	486.72	859	S40	-5832	486.72
820	S79	-5130	344.715	860	S39	-5850	344.715
821	S78	-5148	486.72	861	S38	-5868	486.72
822	S77	-5166	344.715	862	S37	-5886	344.715
823	S76	-5184	486.72	863	S36	-5904	486.72
824	S75	-5202	344.715	864	S35	-5922	344.715
825	S74	-5220	486.72	865	S34	-5940	486.72
826	S73	-5238	344.715	866	S33	-5958	344.715
827	S72	-5256	486.72	867	S32	-5976	486.72
828	S71	-5274	344.715	868	S31	-5994	344.715
829	S70	-5292	486.72	869	S30	-6012	486.72
830	S69	-5310	344.715	870	S29	-6030	344.715
831	S68	-5328	486.72	871	S28	-6048	486.72
832	S67	-5346	344.715	872	S27	-6066	344.715
833	S66	-5364	486.72	873	S26	-6084	486.72
834	S65	-5382	344.715	874	S25	-6102	344.715
835	S64	-5400	486.72	875	S24	-6120	486.72
836	S63	-5418	344.715	876	S23	-6138	344.715
837	S62	-5436	486.72	877	S22	-6156	486.72
838	S61	-5454	344.715	878	S21	-6174	344.715
839	S60	-5472	486.72	879	S20	-6192	486.72
840	S59	-5490	344.715	880	S19	-6210	344.715

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PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
881	S18	-6228	486.72	921	G33	-6948	486.72
882	S17	-6246	344.715	922	G35	-6966	344.72
883	S16	-6264	486.72	923	G37	-6984	486.72
884	S15	-6282	344.715	924	G39	-7002	344.72
885	S14	-6300	486.72	925	G41	-7020	486.72
886	S13	-6318	344.715	926	G43	-7038	344.72
887	S12	-6336	486.72	927	G45	-7056	486.72
888	S11	-6354	344.715	928	G47	-7074	344.72
889	S10	-6372	486.72	929	G49	-7092	486.72
890	S9	-6390	344.715	930	G51	-7110	344.72
891	S8	-6408	486.72	931	G53	-7128	486.72
892	S7	-6426	344.715	932	G55	-7146	344.72
893	S6	-6444	486.72	933	G57	-7164	486.72
894	S5	-6462	344.715	934	G59	-7182	344.72
895	S4	-6480	486.72	935	G61	-7200	486.72
896	S3	-6498	344.715	936	G63	-7218	344.72
897	S2	-6516	486.72	937	G65	-7236	486.72
898	S1	-6534	344.715	938	G67	-7254	344.72
899	DUMMY	-6552	486.72	939	G69	-7272	486.72
900	DUMMY	-6570	344.72	940	G71	-7290	344.72
901	DUMMY	-6588	486.72	941	G73	-7308	486.72
902	DUMMY	-6606	344.72	942	G75	-7326	344.72
903	DUMMY	-6624	486.72	943	G77	-7344	486.72
904	DUMMY	-6642	344.72	944	G79	-7362	344.72
905	G1	-6660	486.72	945	G81	-7380	486.72
906	G3	-6678	344.72	946	G83	-7398	344.72
907	G5	-6696	486.72	947	G85	-7416	486.72
908	G7	-6714	344.72	948	G87	-7434	344.72
909	G9	-6732	486.72	949	G89	-7452	486.72
910	G11	-6750	344.72	950	G91	-7470	344.72
911	G13	-6768	486.72	951	G93	-7488	486.72
912	G15	-6786	344.72	952	G95	-7506	344.72
913	G17	-6804	486.72	953	G97	-7524	486.72
914	G19	-6822	344.72	954	G99	-7542	344.72
915	G21	-6840	486.72	955	G101	-7560	486.72
916	G23	-6858	344.72	956	G103	-7578	344.72
917	G25	-6876	486.72	957	G105	-7596	486.72
918	G27	-6894	344.72	958	G107	-7614	344.72
919	G29	-6912	486.72	959	G109	-7632	486.72
920	G31	-6930	344.72	960	G111	-7650	344.72

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PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
961	G113	-7668	486.72	1001	G193	-8388	486.72
962	G115	-7686	344.72	1002	G195	-8406	344.72
963	G117	-7704	486.72	1003	G197	-8424	486.72
964	G119	-7722	344.72	1004	G199	-8442	344.72
965	G121	-7740	486.72	1005	G201	-8460	486.72
966	G123	-7758	344.72	1006	G203	-8478	344.72
967	G125	-7776	486.72	1007	G205	-8496	486.72
968	G127	-7794	344.72	1008	G207	-8514	344.72
969	G129	-7812	486.72	1009	G209	-8532	486.72
970	G131	-7830	344.72	1010	G211	-8550	344.72
971	G133	-7848	486.72	1011	G213	-8568	486.72
972	G135	-7866	344.72	1012	G215	-8586	344.72
973	G137	-7884	486.72	1013	G217	-8604	486.72
974	G139	-7902	344.72	1014	G219	-8622	344.72
975	G141	-7920	486.72	1015	G221	-8640	486.72
976	G143	-7938	344.72	1016	G223	-8658	344.72
977	G145	-7956	486.72	1017	G225	-8676	486.72
978	G147	-7974	344.72	1018	G227	-8694	344.72
979	G149	-7992	486.72	1019	G229	-8712	486.72
980	G151	-8010	344.72	1020	G231	-8730	344.72
981	G153	-8028	486.72	1021	G233	-8748	486.72
982	G155	-8046	344.72	1022	G235	-8766	344.72
983	G157	-8064	486.72	1023	G237	-8784	486.72
984	G159	-8082	344.72	1024	G239	-8802	344.72
985	G161	-8100	486.72	1025	G241	-8820	486.72
986	G163	-8118	344.72	1026	G243	-8838	344.72
987	G165	-8136	486.72	1027	G245	-8856	486.72
988	G167	-8154	344.72	1028	G247	-8874	344.72
989	G169	-8172	486.72	1029	G249	-8892	486.72
990	G171	-8190	344.72	1030	G251	-8910	344.72
991	G173	-8208	486.72	1031	G253	-8928	486.72
992	G175	-8226	344.72	1032	G255	-8946	344.72
993	G177	-8244	486.72	1033	G257	-8964	486.72
994	G179	-8262	344.72	1034	G259	-8982	344.72
995	G181	-8280	486.72	1035	G261	-9000	486.72
996	G183	-8298	344.72	1036	G263	-9018	344.72
997	G185	-8316	486.72	1037	G265	-9036	486.72
998	G187	-8334	344.72	1038	G267	-9054	344.72
999	G189	-8352	486.72	1039	G269	-9072	486.72
1000	G191	-8370	344.72	1040	G271	-9090	344.72

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PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1041	G273	-9108	486.72	1081	DGND0	-8705	-450.28
1042	G275	-9126	344.72	1082	RCM0	-8625	-450.28
1043	G277	-9144	486.72	1083	VDDIO	-8545	-450.28
1044	G279	-9162	344.72	1084	RCM1	-8465	-450.28
1045	G281	-9180	486.72	1085	DGND0	-8385	-450.28
1046	G283	-9198	344.72	1086	SRGB	-8305	-450.28
1047	G285	-9216	486.72	1087	VDDIO	-8225	-450.28
1048	G287	-9234	344.72	1088	SMX	-8145	-450.28
1049	G289	-9252	486.72	1089	DGND0	-8065	-450.28
1050	G291	-9270	344.72	1090	SMY	-7985	-450.28
1051	G293	-9288	486.72	1091	VDDIO	-7905	-450.28
1052	G295	-9306	344.72	1092	IDM	-7825	-450.28
1053	G297	-9324	486.72	1093	DGND0	-7745	-450.28
1054	G299	-9342	344.72	1094	REV	-7665	-450.28
1055	G301	-9360	486.72	1095	VDDIO	-7585	-450.28
1056	G303	-9378	344.72	1096	RL	-7505	-450.28
1057	G305	-9396	486.72	1097	DGND0	-7425	-450.28
1058	G307	-9414	344.72	1098	TB	-7345	-450.28
1059	G309	-9432	486.72	1099	VDDIO	-7265	-450.28
1060	G311	-9450	344.72	1100	SHUT	-7185	-450.28
1061	G313	-9468	486.72	1101	DGND0	-7105	-450.28
1062	G315	-9486	344.72	1102	GS	-7025	-450.28
1063	G317	-9504	486.72	1103	LCM1	-6945	-450.28
1064	G319	-9522	344.72	1104	LCM0	-6865	-450.28
1065	DUMMY	-9540	486.72	1105	VDDIO	-6785	-450.28
1066	DUMMY	-9558	344.72	1106	TP0	-6705	-450.28
1067	DUMMY	-9576	486.72	1107	TP1	-6625	-450.28
1068	DUMMY	-9594	344.72	1108	TP2	-6545	-450.28
1069	DUMMY	-9612	486.72	1109	TP3	-6465	-450.28
1070	DUMMY	-9585	-450.28	1110	D17	-6385	-450.28
1071	DUMMY	-9505	-450.28	1111	D16	-6305	-450.28
1072	EXTC	-9425	-450.28	1112	D15	-6225	-450.28
1073	DGND0	-9345	-450.28	1113	D14	-6145	-450.28
1074	IM0	-9265	-450.28	1114	D13	-6065	-450.28
1075	VDDIO	-9185	-450.28	1115	D12	-5985	-450.28
1076	IM1	-9105	-450.28	1116	D11	-5905	-450.28
1077	DGND0	-9025	-450.28	1117	D10	-5825	-450.28
1078	IM2	-8945	-450.28	1118	D9	-5745	-450.28
1079	VDDIO	-8865	-450.28	1119	D8	-5665	-450.28
1080	P68	-8785	-450.28	1120	DGND0	-5585	-450.28

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PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1121	DUMMY	-5505	-450.28	1161	DGND	-2380	-450.28
1122	TEST_EN	-5425	-450.28	1162	DGND	-2315	-450.28
1123	D7	-5345	-450.28	1163	DGND	-2250	-450.28
1124	D6	-5265	-450.28	1164	VDDI	-2170	-450.28
1125	D5	-5185	-450.28	1165	VDDI	-2105	-450.28
1126	D4	-5105	-450.28	1166	VDDI	-2040	-450.28
1127	D3	-5025	-450.28	1167	VDDI	-1975	-450.28
1128	D2	-4945	-450.28	1168	VREF	-1895	-450.28
1129	D1	-4865	-450.28	1169	VREF	-1830	-450.28
1130	D0	-4785	-450.28	1170	VREF	-1765	-450.28
1131	TPO0	-4705	-450.28	1171	REGP	-1685	-450.28
1132	TPO1	-4625	-450.28	1172	REGPT	-1605	-450.28
1133	TPO2	-4545	-450.28	1173	VCC	-1525	-450.28
1134	TPO3	-4465	-450.28	1174	VCC	-1460	-450.28
1135	TPO4	-4385	-450.28	1175	VCC	-1395	-450.28
1136	TPO5	-4305	-450.28	1176	VCC	-1330	-450.28
1137	TPO6	-4225	-450.28	1177	VCC	-1265	-450.28
1138	TPO7	-4145	-450.28	1178	VCC	-1200	-450.28
1139	OSC	-4065	-450.28	1179	DUMMY	-1120	-450.28
1140	TE	-3985	-450.28	1180	DUMMY	-1040	-450.28
1141	CSX	-3905	-450.28	1181	VCI1	-960	-450.28
1142	RDX	-3825	-450.28	1182	VCI1	-895	-450.28
1143	WRX	-3745	-450.28	1183	VCI1	-830	-450.28
1144	SDA	-3665	-450.28	1184	VCI1	-765	-450.28
1145	DUMMY	-3585	-450.28	1185	AGND	-685	-450.28
1146	AUTO	-3505	-450.28	1186	AGND	-620	-450.28
1147	RESX	-3425	-450.28	1187	AGND	-555	-450.28
1148	DGND	-3345	-450.28	1188	AGND	-490	-450.28
1149	D/CX	-3265	-450.28	1189	AGND	-425	-450.28
1150	DGND	-3185	-450.28	1190	AGND	-360	-450.28
1151	PCLK	-3105	-450.28	1191	AGND	-295	-450.28
1152	DGND	-3025	-450.28	1192	AGND	-230	-450.28
1153	DE	-2945	-450.28	1193	VDD	-150	-450.28
1154	HS	-2865	-450.28	1194	VDD	-85	-450.28
1155	VS	-2785	-450.28	1195	VDD	-20	-450.28
1156	DGND	-2705	-450.28	1196	VDD	45	-450.28
1157	DGND	-2640	-450.28	1197	VDD	110	-450.28
1158	DGND	-2575	-450.28	1198	VDD	175	-450.28
1159	DGND	-2510	-450.28	1199	VDD	240	-450.28
1160	DGND	-2445	-450.28	1200	VDD	305	-450.28

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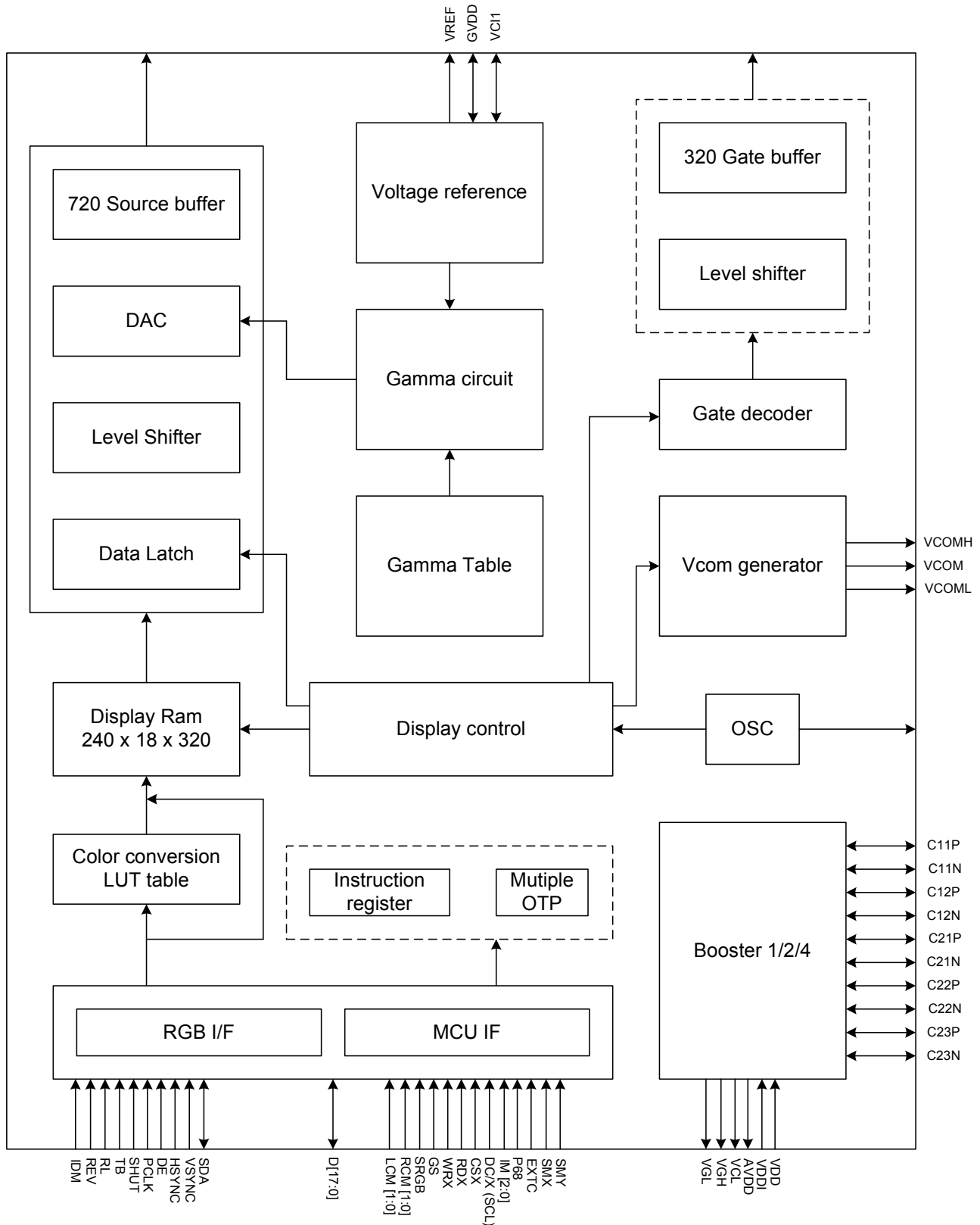
PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1201	VDD	370	-450.28	1241	C12N	3075	-450.28
1202	VDD	435	-450.28	1242	C12N	3140	-450.28
1203	AVDD	515	-450.28	1243	C12N	3205	-450.28
1204	AVDD	580	-450.28	1244	C12N	3270	-450.28
1205	AVDD	645	-450.28	1245	C12N	3335	-450.28
1206	AVDD	710	-450.28	1246	DUMMY	3415	-450.28
1207	AVDD	775	-450.28	1247	DUMMY	3495	-450.28
1208	AVDD	840	-450.28	1248	AGND	3575	-450.28
1209	AVDD	905	-450.28	1249	AGND	3640	-450.28
1210	AVDDO	970	-450.28	1250	AGND	3705	-450.28
1211	AVDDO	1035	-450.28	1251	AGND	3770	-450.28
1212	AVDDS	1100	-450.28	1252	AGND	3835	-450.28
1213	C1SO	1180	-450.28	1253	AGND	3900	-450.28
1214	C1SO	1245	-450.28	1254	AGND	3965	-450.28
1215	VC1S	1310	-450.28	1255	AGND	4030	-450.28
1216	VC1S	1375	-450.28	1256	DUMMY	4110	-450.28
1217	VC1S	1440	-450.28	1257	DUMMY	4190	-450.28
1218	VC1S	1505	-450.28	1258	VCL	4270	-450.28
1219	GVDD	1585	-450.28	1259	VCL	4335	-450.28
1220	GVDD	1650	-450.28	1260	VCL	4400	-450.28
1221	GVDD	1715	-450.28	1261	VCLO	4465	-450.28
1222	C11P	1795	-450.28	1262	VCLO	4530	-450.28
1223	C11P	1860	-450.28	1263	VCLS	4595	-450.28
1224	C11P	1925	-450.28	1264	C21P	4675	-450.28
1225	C11P	1990	-450.28	1265	C21P	4740	-450.28
1226	C11P	2055	-450.28	1266	C21P	4805	-450.28
1227	C11P	2120	-450.28	1267	C21P	4870	-450.28
1228	C11N	2200	-450.28	1268	C21N	4950	-450.28
1229	C11N	2265	-450.28	1269	C21N	5015	-450.28
1230	C11N	2330	-450.28	1270	C21N	5080	-450.28
1231	C11N	2395	-450.28	1271	C21N	5145	-450.28
1232	C11N	2460	-450.28	1272	C22P	5225	-450.28
1233	C11N	2525	-450.28	1273	C22P	5290	-450.28
1234	C12P	2605	-450.28	1274	C22P	5355	-450.28
1235	C12P	2670	-450.28	1275	C22P	5420	-450.28
1236	C12P	2735	-450.28	1276	C22N	5500	-450.28
1237	C12P	2800	-450.28	1277	C22N	5565	-450.28
1238	C12P	2865	-450.28	1278	C22N	5630	-450.28
1239	C12P	2930	-450.28	1279	C22N	5695	-450.28
1240	C12N	3010	-450.28	1280	C23P	5775	-450.28

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PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1281	C23P	5840	-450.28	1321	VCOM	8620	-450.28
1282	C23P	5905	-450.28	1322	VCOM	8685	-450.28
1283	C23P	5970	-450.28	1323	VCOM	8750	-450.28
1284	C23N	6050	-450.28	1324	VCOM	8815	-450.28
1285	C23N	6115	-450.28	1325	VCOM	8880	-450.28
1286	C23N	6180	-450.28	1326	VCOM	8945	-450.28
1287	C23N	6245	-450.28	1327	VCOM	9010	-450.28
1288	DUMMY	6325	-450.28	1328	DUMMY	9090	-450.28
1289	DUMMY	6405	-450.28	1329	DUMMY	9170	-450.28
1290	VGL	6485	-450.28	1330	VPP	9250	-450.28
1291	VGL	6550	-450.28	1331	VPP	9315	-450.28
1292	VGL	6615	-450.28	1332	VPP	9380	-450.28
1293	VGL	6680	-450.28	1333	VPP	9445	-450.28
1294	VGLS	6745	-450.28	1334	DUMMY	9525	-450.28
1295	DUMMY	6825	-450.28	1335	DUMMY	9605	-450.28
1296	DUMMY	6905	-450.28				
1297	VGH	6985	-450.28				
1298	VGH	7050	-450.28				
1299	VGHO	7115	-450.28				
1300	VGHO	7180	-450.28				
1301	VGHS	7245	-450.28				
1302	DUMMY	7325	-450.28				
1303	DUMMY	7405	-450.28				
1304	VCOMH	7485	-450.28				
1305	VCOMH	7550	-450.28				
1306	VCOMH	7615	-450.28				
1307	VCOMH	7680	-450.28				
1308	VCOMH	7745	-450.28				
1309	VCOMH	7810	-450.28				
1310	VCOMH	7875	-450.28				
1311	VCOMH	7940	-450.28				
1312	VCOML	8020	-450.28				
1313	VCOML	8085	-450.28				
1314	VCOML	8150	-450.28				
1315	VCOML	8215	-450.28				
1316	VCOML	8280	-450.28				
1317	VCOML	8345	-450.28				
1318	VCOML	8410	-450.28				
1319	VCOML	8475	-450.28				
1320	VCOM	8555	-450.28				

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5. Block diagram



## 6. Pin description

### 6.1 Power supply pin

Name	I/O	Description	Count	Connect pin
VDD	I	Power supply for analog, digital system and booster circuit	10	VDD
VDDI	I	Power supply for I/O system	4	VDDI
VPP	I	Power supply for OTP circuit	4	VPP
AGND	I	System ground for analog system and booster circuit	16	GND
DGND	I	System ground for I/O system and internal digital system	11	GND

### 6.2 Interface logic pin

Name	I/O	Description	Count	Connect pin						
P68	I	-8080/6800 MCU interface mode select -P68='1', select 6800 MCU parallel interface -P68='0', select 8080 MCU parallel interface -If not used, please fix this pin at VDDI or DGND level	1	GND/VDDI						
IM0-IM2	I	-Selection for MCU parallel interface or serial interface -If not used, please connect this pin to VDDI or DGND <table border="1" style="margin-left: 20px;"> <tr> <td>IM2</td> <td>MCU &amp; SPI interface mode selection</td> </tr> <tr> <td>0</td> <td>SPI interface</td> </tr> <tr> <td>1</td> <td>MCU parallel interface</td> </tr> </table>	IM2	MCU & SPI interface mode selection	0	SPI interface	1	MCU parallel interface	3	GND/VDDI
IM2	MCU & SPI interface mode selection									
0	SPI interface									
1	MCU parallel interface									
RESX	I	-This signal will reset the device and it must be applied to properly initialize the chip -Signal is active low	1	MCU						
CSX	I	-Chip select input pin ("Low" is enable) -This pin can be permanently fixed "Low" in MCU interface mode only	1	MCU						
D/CX (SCL)	I	-Display data/command selection pin in MCU interface -D/CX='1': display data -D/CX='0': command data -In serial interface, this is used as SCL -If not used, please connect this pin to VDDI or DGND	1	MCU						
RDX (E)	I	-Read enable in 8080 MCU parallel interface -Read/write operation enable pin in 6800 MCU parallel interface -If not used, please connect this pin to VDDI or DGND	1	MCU						
WRX	I	-Write enable in MCU parallel interface - Read/write operation enable pin in 8080 MCU parallel interface -If not used, please connect this pin to VDDI or DGND <b>-In RGB interface, WRX are not used and should be connected to VDDI</b>	1	MCU						
SDA	I	-When RCM1, RCM0='1X' (RGB interface), this pin is used as serial input/output pin. -When RCM1, RCM0='0X' (MCU interface), this pin is not used and please connect to VDDI or DGND level. The serial input/output pin in MCU interface mode is D0.	1	MCU DGND/VDDI						
OSC	O	-Monitoring pin of internal oscillator clock and is turned ON/OFF by S/W command -When this pin is inactive (function OFF), this pin is DGND level -If not used, please keep this pin open	1	-						
D[17:0]	I/O	-When RCM="1" (RGB interface), D[17:0] are used as RGB interface data bus -When RCM="0" (MCU interface), D[17:0] are used as MCU parallel interface data bus <b>-D0 is the serial input/output signal in serial interface mode</b> <b>-In serial interface, D[17:1] are not used and should be connected to VDDI or DGND</b>	18	MCU						
TE	I/O	-Tearing effect output pin to synchronies MCU to frame writing, activated by S/W command -External VSYNC signal input pin with MCU interface. -When this pin is not inactive, this pin is low -If not used, please open this pin	1	MCU						
PCLK	I	-Pixel clock signal in RGB interface mode -If not used, please fix this pin at VDDI or DGND	1	RGB interface						
VS	I	-Vertical sync. Signal in RGB interface mode -If not used, please fix this pin at VDDI or DGND	1	RGB interface						
HS	I	-Horizontal sync. Signal in RGB interface mode -If not used, please fix this pin at VDDI or DGND	1	RGB interface						
DE	I	-Data enable signal in RGB interface mode	1	RGB interface						

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		-If not used, please fix this pin at VDDI or DGND		
--	--	---	--	--

*Note1. If CSX is connected to ground in parallel interface mode, there will be no abnormal visible effect on the display module. Also there will be no restriction on using the parallel Read/Write protocols, power On/Off sequences or other functions. Furthermore there will be no influence to the power consumption of the display module.*

*Note2. When in 8-line parallel mode (IM2 , IM1, IM0 ="001") then if some data or signal appears on D[17:8] then it will have no influence to the system. (D[17:8] can be connected to "1" or "0")*

*Note3. When CSX="1", there is no influence to the parallel and serial interface.*

*Note4. "1" = VDDI level, "0" = DGND level.*

6.3 Mode selection pin

Name	I/O	Description	Count	Connect pin			
EXTC	I	-To use extended command set, please connect this pin to VDDI -During normal operation, please open this pin (internal R <sub>pull-down</sub> =2MΩ)	1	VDDI/GND			
		<b>EXTC</b> Enable/disable modification of extend command					
		0 Only use default command set					
		1 Use extended command table (command register can be modify by user)					
GS	I	-Gamma arrangement selection pin when LCM[1]=0,LCM[0]=0	1	VDDI/GND			
		<b>GS</b> GC[7:0] Reg. LCM1 LCM0 LC Type Gamma					
		1			01H	0 0 MVA	Curve 2.2
						0 1 Transflective(TR)	
						1 0 Transmissive(TM)	
						1 1 N/A	
		02H X X Transflective(TR) 1.8					
		04H X X Transflective(TR) 2.5					
		08H X X Transflective(TR) 1.0					
		0			04H	0 0 MVA	Curve 2.2
						0 1 Transflective(TR)	
						1 0 Transmissive(TM)	
						1 1 N/A	
		08H X X Transflective(TR) 1.8					
		IDM			I	-Normal mode and Idle mode selection pin -Please refer RGB interface for detail usage	1
<b>IDM</b> Enable/disable idle mode							
0 Normal display (can be changed to Idle mode by S/W)							
		1 Idle mode enable					
LCM1, LCM0	I	-Liquid crystal (LC) type selection pins	1	VDDI/GND			
		<b>LCM[1:0]</b> Selection of LC type					
		0 0 MVA					
		0 1 Transflective					
		1 0 Transmissive					
1 1 Reserved							
RCM1, RCM0	I	-RGB or MCU interface mode selection pins	2	VDDI/GND			
		<b>RCM[1:0]</b> Selection of MCU or RGB interface					
		00 0 MCU Interface					
		01 1 MCU Interface					
		10 2 RGB Interface (1)					
11 3 RGB Interface (2)							
SRGB	I	-RGB arrangement selection pin for color filter design	1	VDDI/GND			
		<b>SRGB</b> RGB arrangement					
		0 S1, S2, S3 filter order = 'R', 'G', 'B'					
		1 S1, S2, S3 filter order = 'B', 'G', 'R'					
SMX	I	-Please refer chapter 14 for detail using	1	VDDI/GND			
		-Scanning direction of source output selection pin					
		<b>SMX</b> Scanning direction of source output					
		0 S1 -> S720					
		1 S720 -> S1					
SMY	I	-Please refer chapter 14 for detail using	1	VDDI/GND			
		-Scanning direction of gate output selection pin					
		<b>SMY</b> Scanning direction of gate output					
		0 G1 -> G320					

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		1	G320 -> G1				
		-Please refer chapter 14 for detail using					
REV	I	REV		Polarity of source output		1	VDDI/GND
		0	Data not reverse				
		1	Data reverse				
		-Please refer RGB interface for detail using -If not used, please fix this pin at VDDI or DGND					
SHUT	I	SHUT		Display On/Off		1	VDDI/GND
		0	Display On				
		1	Display Off				
		-Please refer RGB interface for detail using -If not used, please fix this pin at VDDI or DGND					
RL	I	RL	SMX	Scanning direction of source output		1	VDDI/GND
		0	0	S1 -> S720			
		0	1	S720 -> S1			
		1	0	S720 -> S1			
		1	1	S1 -> S720			
		-Please refer RGB interface for detail using -If not used, please fix this pin at VDDI or DGND level					
TB	I	TB	SMY	Scanning direction of gate output		1	VDDI/GND
		0	0	G1 -> G320			
		0	1	G320 -> G1			
		1	0	G320 -> G1			
		1	1	G1 -> G320			
		-Please refer RGB interface for detail using -If not used, please fix this pin at VDDI or DGND					
AUTO	I	AUTO		Automatic power-on sequence enable/disable		1	VDDI
		0	Reserved				
		1	Enable (auto mode)				
		-Enable/disable the automatic power-on sequence					
TEST_EN	I	TEST_EN		Test mode enable/disable		1	VDDI/GND
		0	Disable				
		1	Enable				
		-Enable/disable the test mode					

6.4 Driver output pin

Name	I/O	Description	Count	Connect pin
S1 to S720	O	-Source driver output pins	720	-
G1 to G320	O	-Gate driver output pins	320	-
VCI1	I/O	-A reference voltage for step-up circuit 1 -Connect a capacitor for stabilization.	4	Capacitor
AVDD	I	-Power input pin for analog circuit block -In normal usage, connect it to AVDD	7	Capacitor
AVDDO	O	-A power output pin that the voltage is generated from power block -Output of booster 1 circuit -Connect a capacitor for stabilization.	2	AVDD
AVDDS	I	- A reference voltage for step-up circuit 2	1	AVDD
VC1S	I	- A reference voltage for analog circuit including gamma, source and gate	4	Capacitor
C1SO	O	- Output of regulator in 2x boost system	2	C1S
VCL	I	-Power input pin for VCOM circuit -In normal usage, connect it to VCL	3	Capacitor
VCLO	O	-A power output pin of step-up circuit 4 -When VCOML is higher than AGND, VCL=AGND -Connect a capacitor for stabilization	2	VCL
VCLS	I	- A reference voltage for step-up circuit 2	1	VCL
VGH	I	-Power input pin for gate driver circuit -In normal usage, connect it to VGH	2	VGH
VGHO	O	-Positive output pin of the step-up circuit 2	2	Capacitor

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		-Connect a capacitor for stabilization		
VGHS	I	- A reference voltage for step-up circuit 2	1	VGH
VGL	I	-Power input pin for gate driver circuit -In normal usage, connect it to VGL	2	Capacitor
VGLO	O	-Negative output of the step-up circuit 2 -Connect a capacitor for stabilization	2	VGL
VGLS	I	- A reference voltage for step-up circuit 2	1	VGL
VREF	O	-Reference voltage for power circuit block. -Connect a capacitor for stabilization	3	Capacitor
GVDD	O	-A standard level for grayscale voltage generator -Connect a capacitor for stabilization. -When internal GVDD generator is not used, connect an external power supply (AVDD-0.5V)	3	Capacitor
VCOMH	O	-Positive voltage output of VCOM -Connect a capacitor for stabilization	8	Capacitor
VCOML	O	-Negative voltage output of VCOM -Connect a capacitor for stabilization	8	Capacitor
VCOM	O	-A power supply for the TFT-LCD common electrode	8	Common electrode
C11P, C11N C12P, C12N	O	-Capacitor connecting pins for step-up circuit 1 (for AVDD)	24	Step-up Capacitor
C21P, C21N C22P, C22N C23P, C23N	O	-Capacitor connecting pins for step-up circuit 2 (for VGH, VGL, VCL)	24	Step-up Capacitor
VDDIO	O	-VDDI voltage output level for monitoring	8	-
DGND0	O	-DGND voltage output level for monitoring	9	-
VCC	O	-Monitoring pin of internal digital reference voltage -Connect a capacitor fir stabilization	6	Capacitor
REGP REGPT	O	Test pin	2	Open

## 6.5 Test pin

Name	I/O	Description	Count	Connect pin
TPI, TPO	I/O	-Test pins. In regular usage, please open these pins	12	Open
Dummy		-These pins are dummy (have no function inside) -Can allow signal traces pass through under these pads on TFT glass	24	Open

## 7. Driver electrical characteristics

### 7.1 Absolute operation range

Item	Symbol	Rating	Unit
Supply voltage	VDD	- 0.3 ~ +4.6	V
Supply voltage (Logic)	VDDI	- 0.3 ~ +4.6	V
Supply voltage (Digital)	VCC	-0.3 ~ +4.6	V
Driver supply voltage	VGH-VGL	-0.3 ~ +30.0	V
Logic Input voltage range	V <sub>IN</sub>	0.5 ~ VDDI + 0.5	V
Logic Output voltage range	V <sub>O</sub>	0.5 ~ VDDI + 0.5	V
Operating temperature range	T <sub>OPR</sub>	-30 ~ +70	°C
Storage temperature range	T <sub>STG</sub>	-55 ~ +125	°C

Note: If one of the above items is exceeded its maximum limitation momentarily, the quality of the product may be degraded. Absolute maximum limitation, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range.

### 7.2 ESD protection level

Model	Test Condition	Protection Level	Unit
Human Body Model	C = 100 pF, R = 1.5k ohm. 3 times zapping/each pin, 1sec/per zapping	±2500 for each pin ±3000 for connector pin	V
Machine Model	C = 200 pF, R = 0.0 ohm. 3 times zapping/each pin, 1sec/per zapping	±250 for each pin	V

Note: connector pin is DATA BUS, Power, CSX, RDX, WRX, RESX, TE.

### 7.3 Latch-up protection level

The device will not latch up at trigger current level less than ±100 mA.

### 7.4 Light Sensitivity

The operation of the IC will not be materially altered by incident light.

### 7.5 DC characteristic

Parameter	Symbol	Condition	Specification			Unit	Related Pins
			Min	TYP	Max		
<b>Power &amp; operation voltage</b>							
System voltage	VDD	Operating voltage	2.45	2.78	3.3	V	Note 2
Interface operation voltage	VDDI	I/O supply voltage	1.65	1.8/2.78	3.3	V	Note 2
Digital operating voltage	VCC	Digital supply voltage	1.65		2.0	V	Note 2
Gate driver high voltage	VGH		10		16.5	V	Note 3
Gate driver low voltage	VGL		-14		-5	V	Note 3
Gate driver supply voltage		VGH-VGL	19		30	V	Note 3
I/O operating voltage			1.65		3.3	V	
OTP operation voltage	VPP	Operating voltage	7.5	7.8		V	
<b>Input / Output</b>							
Logic-high input voltage	V <sub>IH</sub>		0.7VDDI		VDDI	V	Note 1,2,3
Logic-low input voltage	V <sub>IL</sub>		VSS		0.3VDDI	V	Note 1,2,3
Logic-high output voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1.0mA	0.8VDDI		VDDI	V	Note 1,2,3
Logic-low output voltage	V <sub>OL</sub>	I <sub>OL</sub> = +1.0mA	VSS		0.2VDDI	V	Note 1,2,3
Logic-high input current	I <sub>IH</sub>	V <sub>IN</sub> = VDDI or VSS			1	uA	Note 1,2,3
Logic-low input current	I <sub>IL</sub>		-1			uA	Note 1,2,3
Input leakage current	I <sub>IL</sub>	I <sub>OH</sub> = -1.0mA	-0.1		+0.1	uA	Note 1,2,3
<b>VCOM voltage</b>							
VCOM high voltage	VCOMH	C <sub>com</sub> =12nF	2.5		5.0	V	Note 3
VCOM low voltage	VCOML	C <sub>com</sub> =12nF	-2.5		0.0	V	Note 3
VCOM amplitude	VCOMAC	VCOMH-VCOML	4.0		6.0	V	Note 3
<b>Source driver</b>							
Source output range	V <sub>sout</sub>		0.1		AVDD-0.1	V	Note 4
Gamma reference voltage	GVDD		3.0		5.0	V	Note 3
Source output settling time	T <sub>r</sub>	Below with 99% precision		10	14	us	Note 4,5
Output deviation voltage (Source output channel)	V <sub>dev</sub>	S <sub>out</sub> >=4.2V, S <sub>out</sub> <=0.8V			20	mV	Note 4,5
		4.2V > S <sub>out</sub> > 0.8V			15	mV	

Output offset voltage	$V_{OFSET}$				35	mv	Note 6
<b>Step-up circuit</b>							
Internal reference voltage	$V_{REF}$					%	Note 3
1st step-up (VDDx2) voltage	AVDD		4.95		6.0	V	Note 3
1st step-up (VDDx2) drop voltage	VDDx2,dorp	I AVDD = 2.5mA (include panel loading)			4%	%	Note 3
Linear range	$V_{Linear}$		0.2		AVDD-0.2	V	

Note 1: VDDI=1.65 to 3.3V, VDD=2.45 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 °C

Note 2, 3, 4: When the measurements are performed with LCD module, measured points are like below.

Note 3: P68, CSX, RDX, WRX, D[17:0], D/CX, RESX, TE, PCLK, VS, HS, EXT\_C, GS, IDM, SCL, LCM[1:0], RCM[1:0], IM[2:0], SRGB, SMX, SMY, REV, SHUT, RL, TB and Test pins

Note 5, Source channel loading= 2.2kohm , 10pF/channel, Gate channel loading=0.8kohm , 50pF/channel.

Note 6, The Max. value is between measured point of note 4 and gamma setting value.

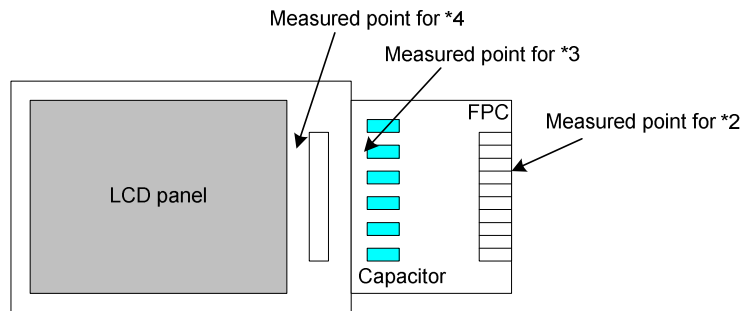


Fig. 7.5.1 Example of measured point on the panel

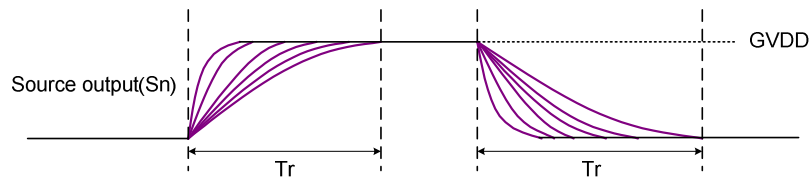


Fig. 7.5.2 Tr: the source output stabling time.

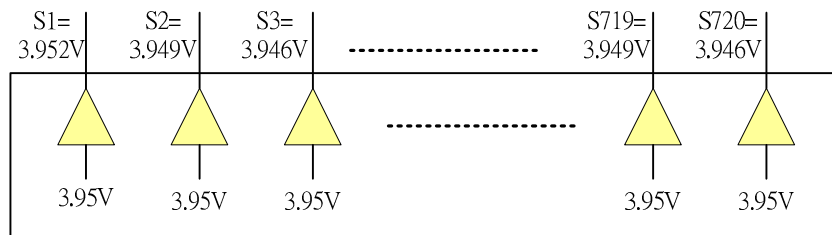


Fig. 7.5.3 Source output deviation (channel to channel).

-When  $S_{out} \geq 4.2V$ ,  $S_{out} \leq 0.8V$

$$\text{Max}(S1, S2, S3, \dots, S720) - \text{Min}(S1, S2, S3, \dots, S720) \leq 20\text{mV}$$

-When  $4.2V > S_{out} > 0.8V$

$$\text{Max}(S1, S2, S3, \dots, S720) - \text{Min}(S1, S2, S3, \dots, S720) \leq 6\text{mV}$$

-Example

When  $S_{out}$  level is 3.95V (Gray scale voltage)

$$\text{Max}(S1, S2, S3, \dots, S720) = 3.96\text{V}$$

$$\text{Min}(S1, S2, S3, \dots, S720) = 3.944\text{V}$$

$$S_{out} \text{ deviation} = \text{Max}(S1, S2, S3, \dots, S720) - \text{Min}(S1, S2, S3, \dots, S720) = 10\text{mV} \leftarrow \text{Out of Spec}$$

## 7.6 Power consumption

Operation mode	Inversion mode	Image	Current consumption			
			Typical		Maximum	
			IDDI (uA)	IDD (mA)	IDDI (uA)	IDD (mA)
-Normal mode	One Line	Note 1	1	2.6	1	3.0
	One Line	Note 2	1	2.5	1	2.8
-Partial + Idle mode (40 lines)	One Line	Note 3,4	1	0.65	1	0.8
-Sleep-in mode	N/A	N/A	1	9uA	1	9uA

**Notes:**

1. All pixels black.
2. Grayscale from top to bottom.
3. Black & white checker board 8 by 8
4. Absolute worst case patterns: all pixels black.

**Typical case:**

TA = 25 °C

VDD = 2.78 V

VDDI = 1.80 V

**Worst Case:**

TA = -30 to 70°C

VDD = 2.45 V to 3.3 V

VDDI = 1.65 V to 3.3 V

Includes process variance.

8. Timing chart

8.1 Parallel interface characteristics: 18, 16, 9 or 8-bits bus (8080-series MCU interface)

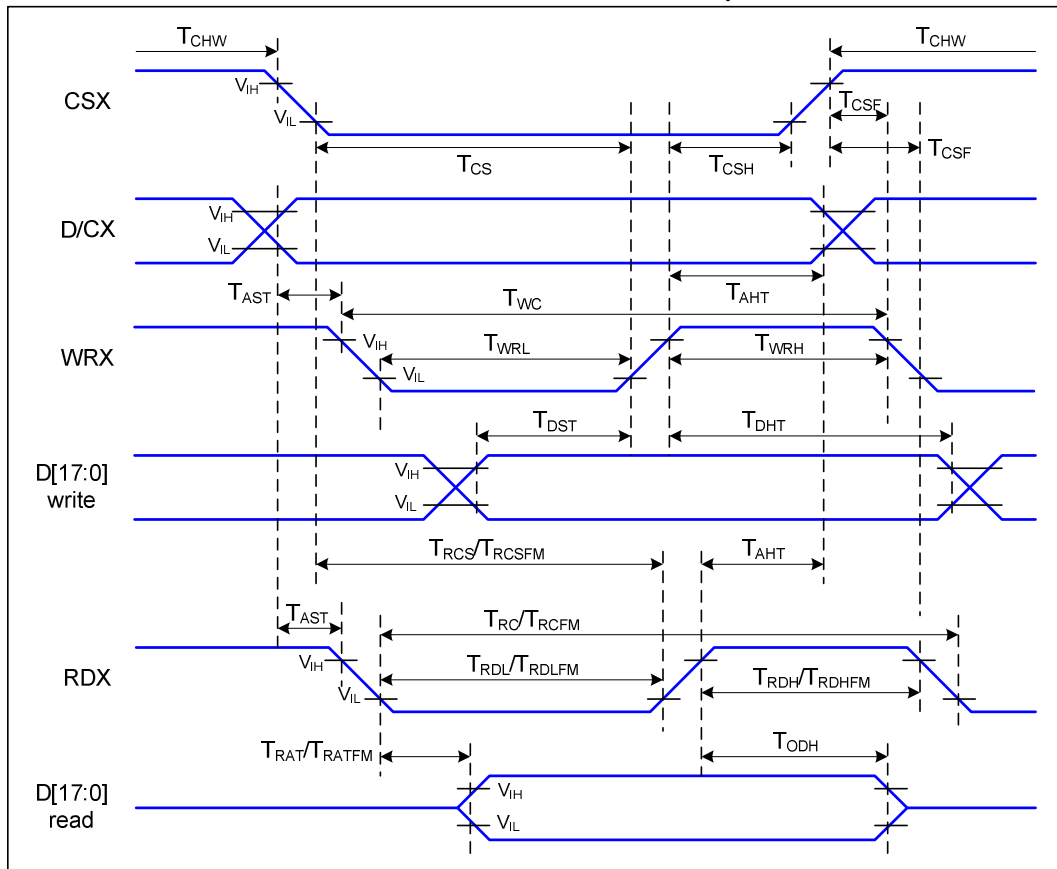


Fig. 8.1.1 Parallel interface timing characteristics (8080-series MCU interface)

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T <sub>AST</sub>	Address setup time	10	-	ns	-
	T <sub>AHT</sub>	Address hold time (Write/Read)	10	-	ns	
CSX	T <sub>CHW</sub>	Chip select "H" pulse width	0	-	ns	-(3-transfer for one pixel)
	T <sub>CS</sub>	Chip select setup time (Write)	15	-	ns	
	T <sub>RCS</sub>	Chip select setup time (Read ID)	45	-	ns	
	T <sub>RCSFM</sub>	Chip select setup time (Read RAM)	355	-	ns	
	T <sub>CSF</sub>	Chip select wait time (Write/Read)	10	-	ns	
	T <sub>CSH</sub>	Chip select hold time	10	-	ns	
WRX	T <sub>WC</sub>	Write cycle	66	-	ns	-(15Mhz)
	T <sub>WRH</sub>	Control pulse "H" duration	20	-	ns	
	T <sub>WRL</sub>	Control pulse "L" duration	20	-	ns	
RDX (ID)	T <sub>RC</sub>	Read cycle (ID)	160	-	ns	When read ID data
	T <sub>RDH</sub>	Control pulse "H" duration (ID)	90	-	ns	
	T <sub>RDL</sub>	Control pulse "L" duration (ID)	45	-	ns	
RDX (FM)	T <sub>RCSFM</sub>	Read cycle (FM)	450	-	ns	When read from frame memory
	T <sub>RDHFM</sub>	Control pulse "H" duration (RAM)	90	-	ns	
	T <sub>RDLFM</sub>	Control pulse "L" duration (RAM)	355	-	ns	
D[17:0]	T <sub>DST</sub>	Data setup time	20	-	ns	For maximum CL=30pF For minimum CL=8pF
	T <sub>DHT</sub>	Data hold time	20	-	ns	
	T <sub>RAT</sub>	Read access time (ID)	-	40	ns	
	T <sub>RATFM</sub>	Read access time (FM)	-	340	ns	
	T <sub>ODH</sub>	Output disable time	20	80	ns	

Note 1: VDDI=1.65 to 3.3V, VDD=2.45 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 °C

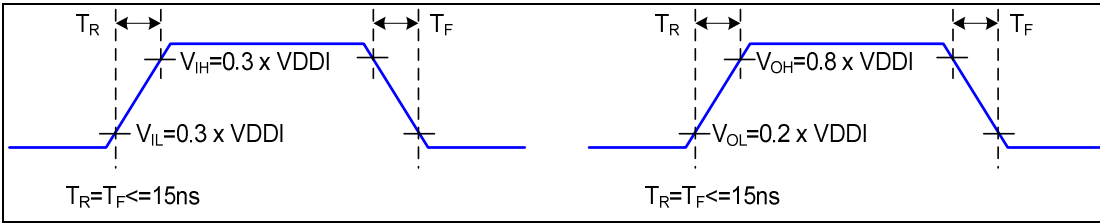


Fig. 8.1.2 Rising and falling timing for input and output signal

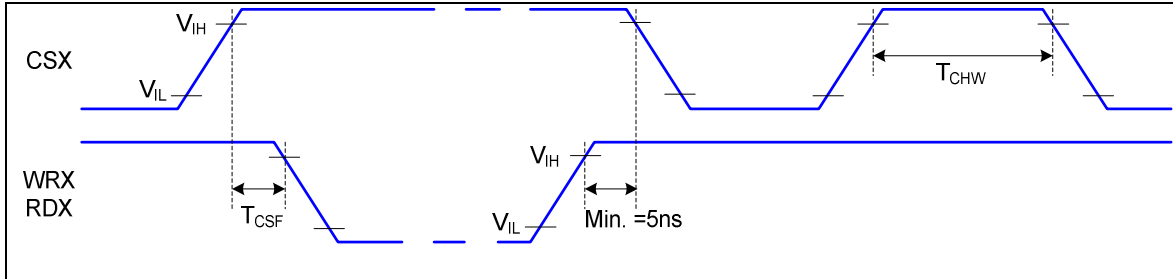


Fig.8.1.3 Chip selection (CSX) timing

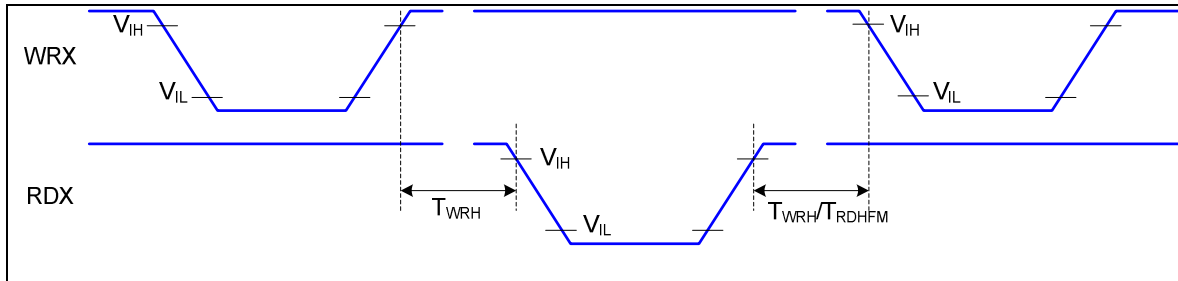


Fig. 8.1.4 Write-to-read and read-to-write timing

NOTE: The rising time and falling time ( $T_r$ ,  $T_f$ ) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

8.2 Parallel interface characteristics: 18, 16, 9 or 8-bits bus (6800-series MCU interface)

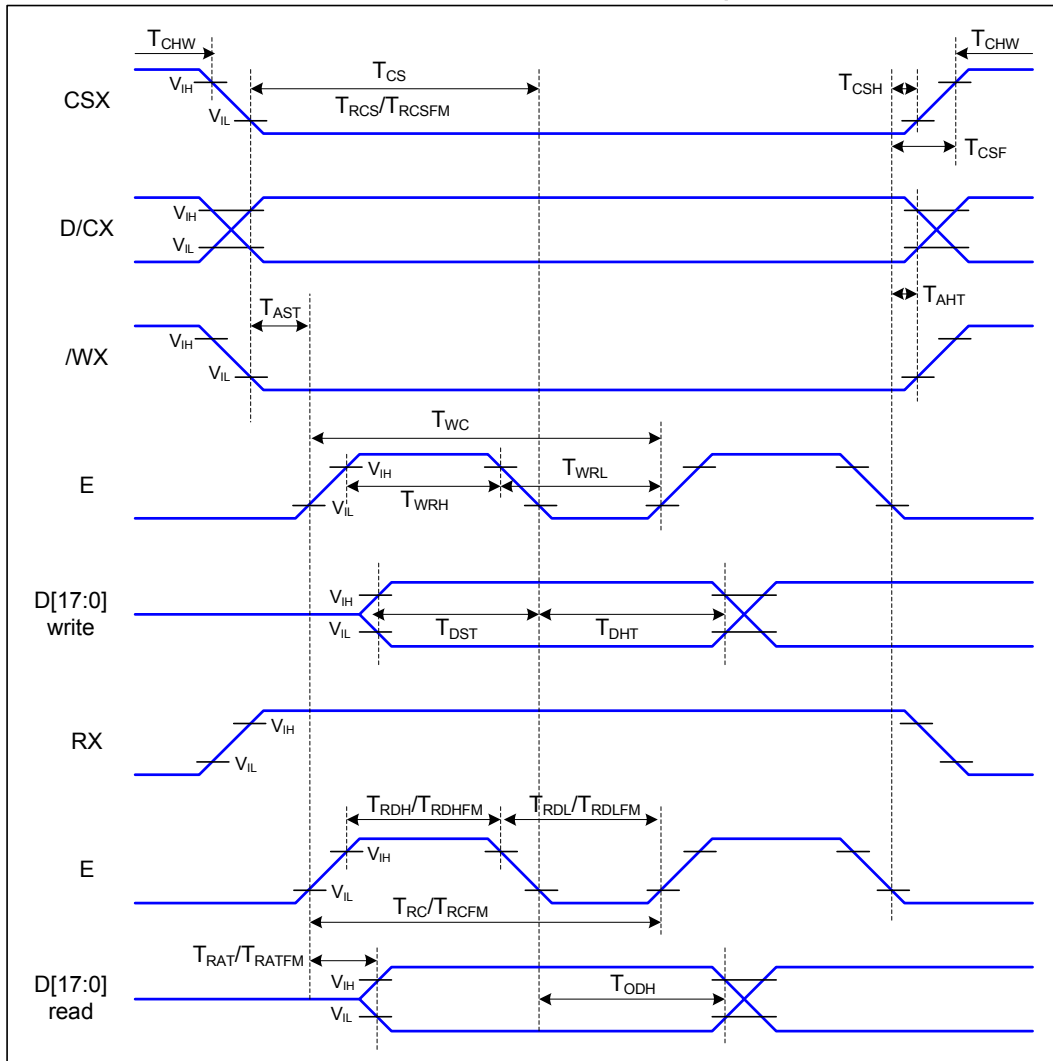


Fig. 8.2.1 Parallel interface timing characteristics (6800-series MCU interface)

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T <sub>AST</sub>	Address setup time	10	-	ns	-
	T <sub>AHT</sub>	Address hold time (Write/Read)	10	-	ns	
CSX	T <sub>CHW</sub>	Chip select "H" pulse width	0	-	ns	-
	T <sub>CS</sub>	Chip select setup time (Write)	15	-	ns	
	T <sub>RCS</sub>	Chip select setup time (Read ID)	45	-	ns	
	T <sub>RCSFM</sub>	Chip select setup time (Read FM)	355	-	ns	
	T <sub>CSF</sub>	Chip select wait time (Write/Read)	10	-	ns	
	T <sub>CSH</sub>	Chip select hold time	10	-	ns	
WRX	T <sub>WC</sub>	Write cycle	66	-	ns	-(15Mhz)
	T <sub>WRH</sub>	Control pulse "H" duration	20	-	ns	
	T <sub>WRL</sub>	Control pulse "L" duration	20	-	ns	
RDX (ID)	T <sub>RC</sub>	Read cycle (ID)	160	-	ns	When read ID data
	T <sub>RDH</sub>	Control pulse "H" duration (ID)	90	-	ns	
	T <sub>RDL</sub>	Control pulse "L" duration (ID)	45	-	ns	
RDX (FM)	T <sub>RCFM</sub>	Read cycle (FM)	450	-	ns	When read from frame memory
	T <sub>RDHF</sub>	Control pulse "H" duration (FM)	90	-	ns	
	T <sub>RDLF</sub>	Control pulse "L" duration (FM)	355	-	ns	
D[17:0]	T <sub>DST</sub>	Data setup time	20	-	ns	For maximum CL=30pF For minimum CL=8pF
	T <sub>DHT</sub>	Data hold time	20	-	ns	
	T <sub>RAT</sub>	Read access time (ID)	-	40	ns	
	T <sub>RATFM</sub>	Read access time (FM)	-	340	ns	
	T <sub>ODH</sub>	Output disable time	20	80	ns	

Note 1: VDDI=1.65 to 3.3V, VDD=2.45 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 °C

Note 2: The rising time and falling time (Tr, Tf) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.



8.3 Serial interface characteristics (3-line serial)

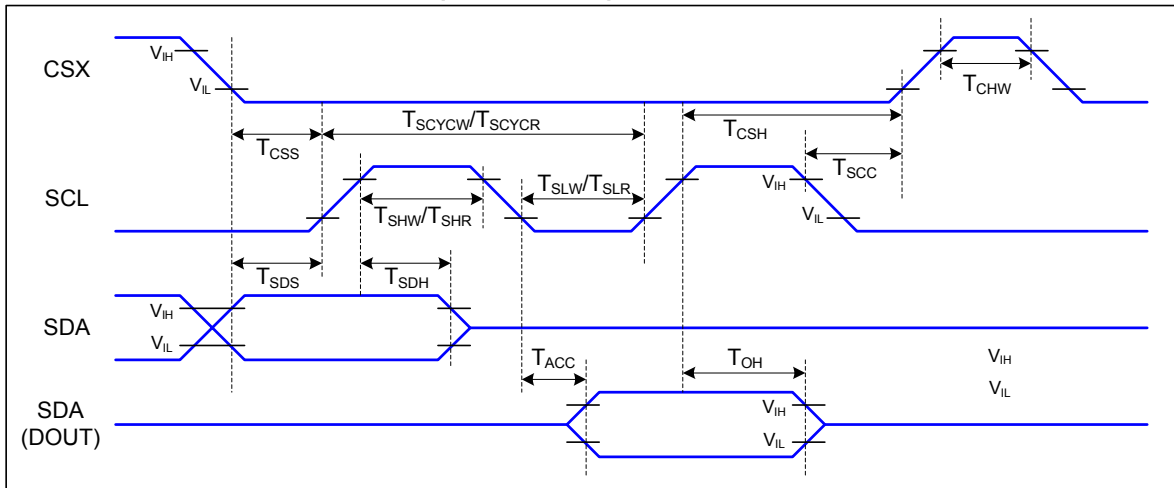


Fig. 8.3.1 3-line serial interface timing

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T <sub>CSS</sub>	Chip select setup time	60		ns	
	T <sub>CSH</sub>	Chip select hold time	60		ns	
	T <sub>SCH</sub>	Chip select setup time	20		ns	
	T <sub>CHW</sub>	Chip select setup time	40		ns	
SCL	T <sub>SCYC</sub> <sub>W</sub>	Serial clock cycle (Write)	66		ns	
	T <sub>SHW</sub>	SCL "H" pulse width (Write)	20		ns	
	T <sub>SLW</sub>	SCL "L" pulse width (Write)	20		ns	
	T <sub>SCYC</sub> <sub>R</sub>	Serial clock cycle (Read)	150		ns	
	T <sub>SHR</sub>	SCL "H" pulse width (Read)	60		ns	
SDA (DIN) (DOUT)	T <sub>SLR</sub>	SCL "L" pulse width (Read)	60		ns	For maximum CL=30pF For minimum CL=8pF
	T <sub>SDS</sub>	Data setup time	10		ns	
	T <sub>SDH</sub>	Data hold time	10		ns	
	T <sub>ACC</sub>	Access time	10		ns	
	T <sub>OH</sub>	Output disable time	15		ns	

Table 8.3: 3-line Serial Interface Characteristics

Note 1: VDDI=1.65 to 3.3V, VDD=2.45 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 °C

Note 2: The rising time and falling time (Tr, Tf) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

8.4 Vertical synchronizing signal timing characteristic

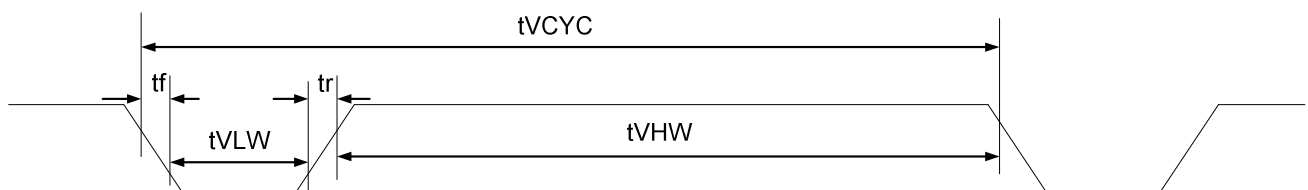


Fig. 8.4 Vertical synchronizing signal timing

Signal	Symbol	Parameter	Min	Max	Unit	Description
VSYNC	t <sub>VCYC</sub>	VSYNC Cycle	1F+2H	-	-	
	t <sub>VLW</sub>	VSYNC Pulse L Width	1H	1F-1H	-	
	t <sub>VHW</sub>	VSYNC Pulse H Width	3H	-	-	

-Standing up standing fall time of the input signal(tr,tf) is provided for by 15ns or less.

-The signal level is provided for based on 30% and 70% of VDDI-DGND

-This is provided for while external VSYNC is synchronizing.

-F indicates the time of one frame in internal synchronization.

-H indicates the time in internal synchronization for one line.

## 9. Function description

### 9.1 Interface type selection

The selection of given interfaces are done by setting P68, IM2, IM1, and IM0 pins as shown in following table.

P68	IM2	IM1	IM0	Interface	Read back selection
-	0	-	-	3-line serial interface	Via the read instruction
0	1	0	0	8080 8-bit parallel	RDX strobe (8-bit read data and 8-bit read parameter)
0	1	0	1	8080 16-bit parallel	RDX strobe (16-bit read data and 8-bit read parameter)
0	1	1	0	8080 9-bit parallel	RDX strobe (9-bit read data and 8-bit read parameter)
0	1	1	1	8080 18-bit parallel	RDX strobe (18-bit read data and 8-bit read parameter)
-	0	-	-	3-line serial interface	Via the read instruction
1	1	0	0	6800 8-bit parallel	E strobe (8-bit read data and 8-bit read parameter)
1	1	0	1	6800 16-bit parallel	E strobe (16-bit read data and 8-bit read parameter)
1	1	1	0	6800 9-bit parallel	E strobe (9-bit read data and 8-bit read parameter)
1	1	1	1	6800 18-bit parallel	E strobe (18-bit read data and 8-bit read parameter)

P68	IM2	IM1	IM0	Interface	RDX	WRX	D/CX	Read back selection
-	0	-	-	3-line serial interface	Note1	Note1	SCL	D[17:1]: unused, D0: SDA
0	1	0	0	8080 8-bit parallel	RDX	WRX	D/CX	D[17:8]: unused, D7-D0: 8-bit data
0	1	0	1	8080 16-bit parallel	RDX	WRX	D/CX	D[17:16]: unused, D15-D0: 16-bit data
0	1	1	0	8080 9-bit parallel	RDX	WRX	D/CX	D[17:9]: unused, D8-D0: 9-bit data
0	1	1	1	8080 18-bit parallel	RDX	WRX	D/CX	D17-D0: 18-bit data
1	1	0	0	6800 8-bit parallel	E	WRX	RS	D[17:8]: unused, D7-D0: 8-bit data
1	1	0	1	6800 16-bit parallel	E	WRX	RS	D[17:16]: unused, D15-D0: 16-bit data
1	1	1	0	6800 9-bit parallel	E	WRX	RS	D[17:9]: unused, D8-D0: 9-bit data
1	1	1	1	6800 18-bit parallel	E	WRX	RS	D17-D0: 18-bit data

Note 1. Unused pins can be open, or connected to DGND or VDDI.

### 9.2 8080-series MCU parallel interface (P68='0')

The MCU can use on of following interfaces: 11-lines with 8-data parallel interface, 12-lines with 9-data parallel interface, 19-lines with 16-data parallel interface or 21-lines with 18-data parallel interface. The chip-select CSX (active low) enables/disables the parallel interface. RESX (active low) is an external reset signal. WRX is the parallel data write, RDX is the parallel data read and D[17:0] is parallel data.

The graphics controller chip reads the data at the rising edge of WRX signal. The D/CX is the data/command flag. When D/CX='1', D[17:0] bits are either display data or command parameters. When D/C='0', D[17:0] bits are commands.

The 6800-series bi-directional interface can be used for communication between the micro controller and LCD driver chip. The selection of this interface is done when P68 pin is in low state (DGND). Interface bus width can be selected with IM2, IM1 and IM0.

The interface functions of 8080-series parallel interface are given in following table.

P68	IM2	IM1	IM0	Interface	RDX	WRX	D/CX	Read back selection
0	1	0	0	8-bit parallel	0	1	↑	Write 8-bit command (D7 to D0)
					1	1	↑	Write 8-bit display data or 8-bit parameter (D7 to D0)
					1	↑	1	Read 8-bit display data (D7 to D0)
					1	↑	1	Read 8-bit parameter or status (D7 to D0)
0	1	0	1	16-bit parallel	0	1	↑	Write 8-bit command (D7 to D0)
					1	1	↑	Write 16-bit display data or 8-bit parameter (D15 to D0)
					1	↑	1	Read 16-bit display data (D15 to D0)
					1	↑	1	Read 8-bit parameter or status (D7 to D0)
0	1	1	0	9-bit parallel	0	1	↑	Write 8-bit command (D7 to D0)
					1	1	↑	Write 9-bit display data or 8-bit parameter (D8 to D0)
					1	↑	1	Read 9-bit display data (D8 to D0)
					1	↑	1	Read 8-bit parameter or status (D7 to D0)
0	1	1	1	18-bit parallel	0	1	↑	Write 8-bit command (D7 to D0)
					1	1	↑	Write 18-bit display data or 8-bit parameter (D17 to D0)
					1	↑	1	Read 18-bit display data (D17 to D0)
					1	↑	1	Read 8-bit parameter or status (D7 to D0)

Note: applied for command code: DAh, DBh, DCh, 04h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh

## 9.2.1 Write cycle sequence

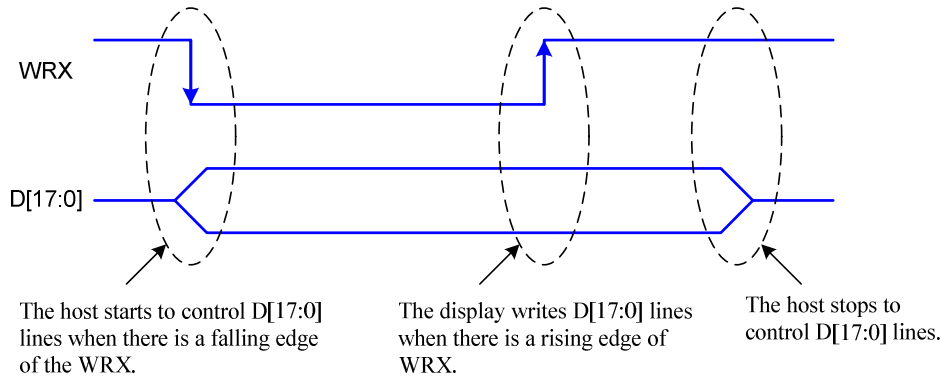


Fig. 9.2.1 8080-series WRX protocol

Note: WRX is an unsynchronized signal (It can be stopped).

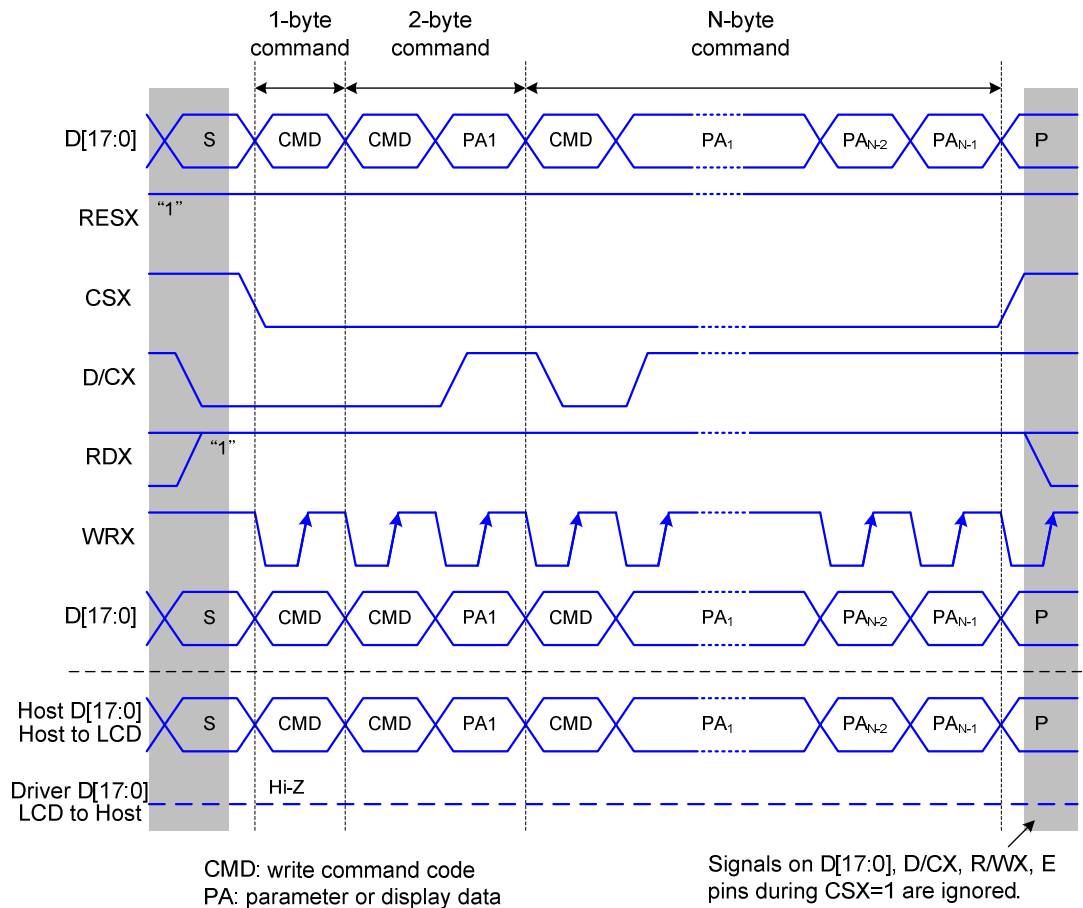


Fig. 9.2.2 8080-series parallel bus protocol, write to register or display RAM

## 9.2.2 Read cycle sequence

The read cycle (RDX high-low-high sequence) means that the host reads information from display via interface. The driver sends data (D[17:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

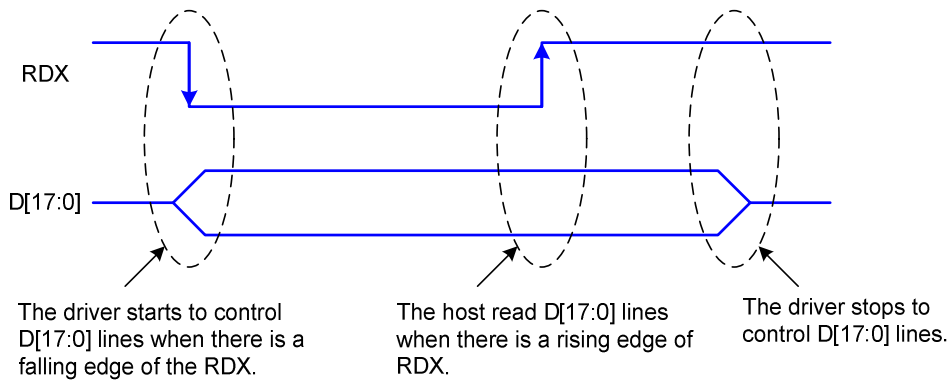


Fig. 9.2.3 8080-series RDX protocol

Note: RDX is an unsynchronized signal (It can be stopped).

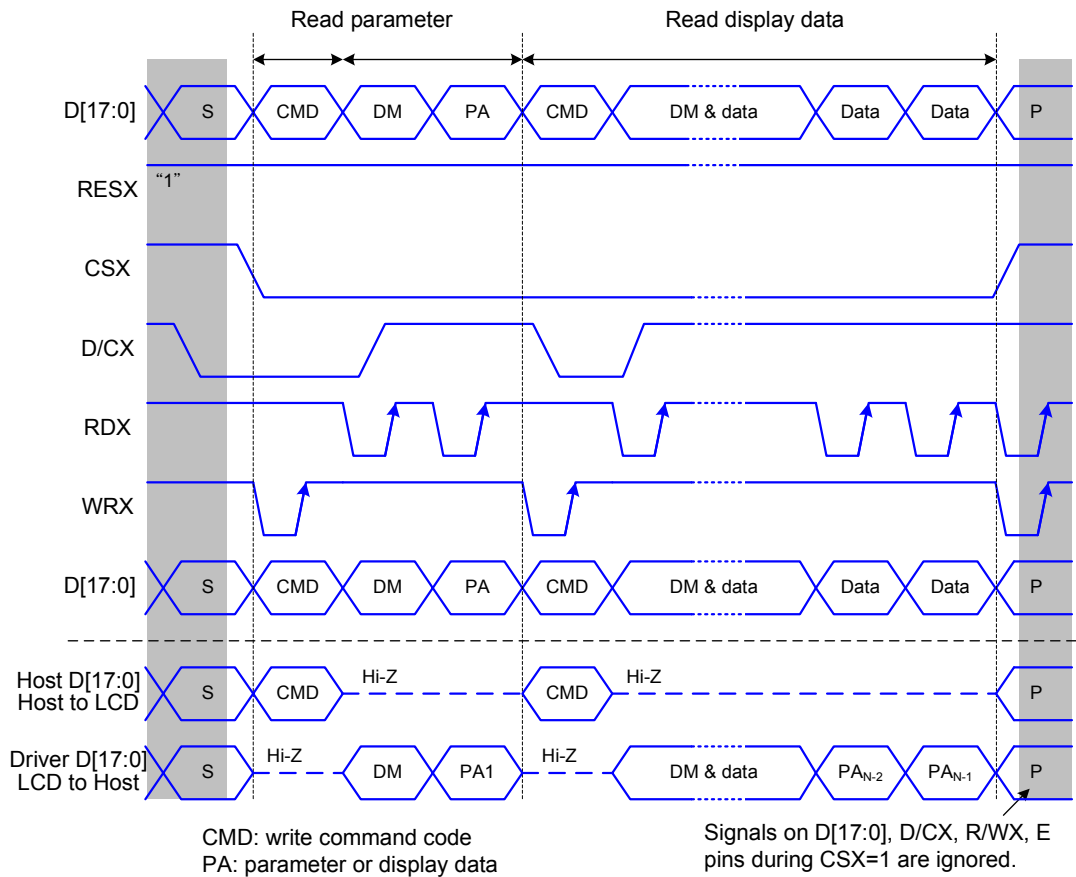


Fig. 9.2.4 8080-series parallel bus protocol, read data from register or display RAM

## 9.3 6800-Series Parallel Interface (P68='1')

The MCU uses a 11-lines 8-data parallel interface or 12-lines 9-data parallel interface or 19-lines 16-data parallel interface or 21-lines 18-data parallel interface. The chip-select CSX(active low) enables and disables the parallel interface. RESX (active low) is an external reset signal. The R/WX is the Read/Write flag and D[17:0] is parallel data.

The Graphics Controller Chip reads the data at the falling edge of E signal when R/WX= '1' and Writes the data at the falling of the E signal when R/WX='0'. The D/CX is the data/command flag. When D/CX='1', D[17:0] bits are display RAM data or command parameters. When D/C= '0', D[17:0] bits are commands.

The 6800-series bi-directional interface can be used for communication between the micro controller and LCD driver chip. The selection of this interface is done when P68 pin is high state (VDDI). Interface bus width can be selected with IM2, IM1 and IM0.

The interface functions of 6800-series parallel interface are given in Table 9.3.1.

Table 9.3.1 The function of 6800-series parallel interface

P68	IM2	IM1	IM0	Interface	D/CX	R/WX	E	Function
1	1	0	0	8-bit Parallel	0	0	↓	Write 8-bit command (D7 to D0)
					1	0	↓	Write 8-bit display data or 8-bit parameter (D7 to D0)
					1	1	↓	Read 8-bit Display data (D7 to D0)
					1	1	↓	Read 8-bit parameter or status (D7 to D0)
1	1	0	1	16-bit Parallel	0	0	↓	Write 8-bit command (D7 to D0)
					1	0	↓	Write 16-bit display data or 8-bit parameter (D15 to D0)
					1	1	↓	Read 16-bit Display data (D15 to D0)
					1	1	↓	Read 8-bit parameter or status (D7 to D0)
1	1	1	0	9-bit Parallel	0	0	↓	Write 8-bit command (D7 to D0)
					1	0	↓	Write 9-bit display data or 8-bit parameter (D8 to D0)
					1	1	↓	Read 9-bit Display data (D8 to D0)
					1	1	↓	Read 8-bit parameter or status (D7 to D0)
1	1	1	1	18-bit Parallel	0	0	↓	Write 8-bit command (D7 to D0)
					1	0	↓	Write 18-bit display data or 8-bit parameter (D17 to D0)
					1	1	↓	Read 18-bit Display data (D17 to D0)
					1	1	↓	Read 8-bit parameter or status (D7 to D0)

Note: applied for command code: DAh, DBh, DCh, 04h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh.

### 9.3.1 Write cycle sequence

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (E low-high-low sequence) consists of 3 control (D/CX, E, R/WX) and data signals (D[17:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (=0') and vice versa it is data (=1').

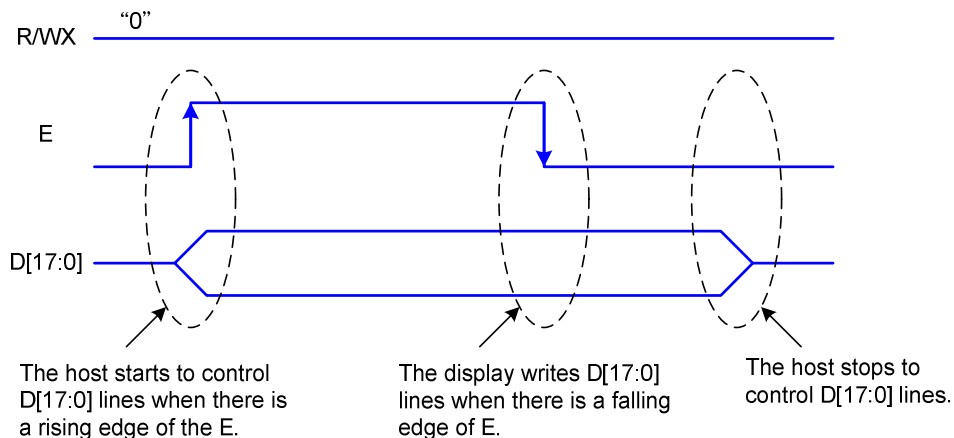


Fig. 9.3.1 6800-Series Write Protocol

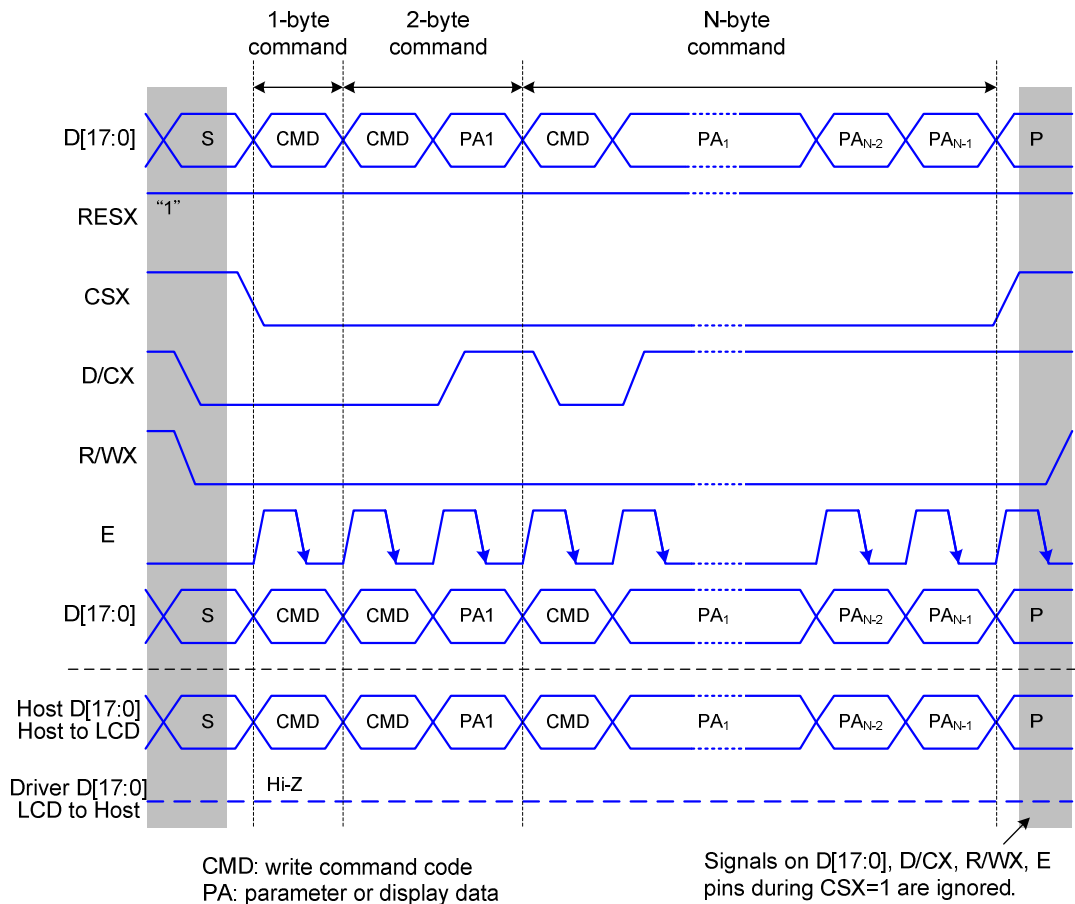


Fig. 9.3.2 6800-series parallel bus protocol, write to register or display RAM

### 9.3.2 Read cycle sequence

The write cycle means that the host reads information (command or/and data) to the display via the interface. Each read cycle (E low-high-low sequence) consists of 3 control (D/CX, E, R/WX) and data signals (D[17:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (=0') and vice versa it is data (=1').

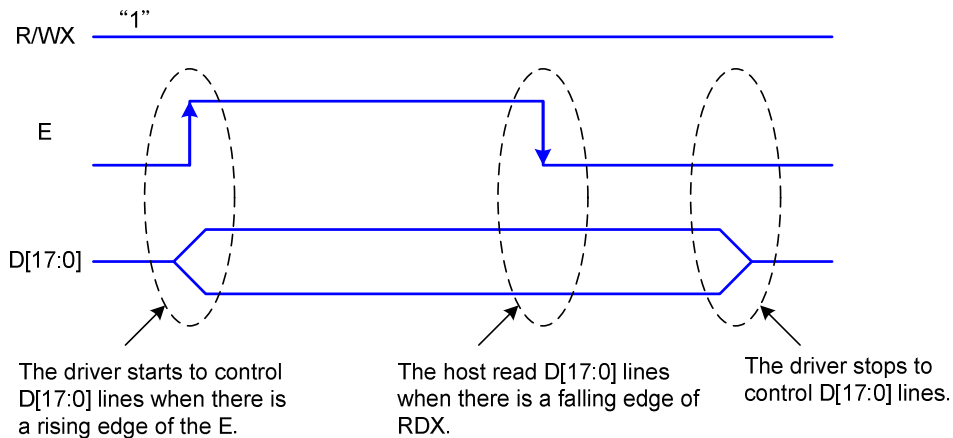


Fig. 9.3.3 6800-series read protocol

www. *Note: E is an unsynchronized signal (It can be stopped)*

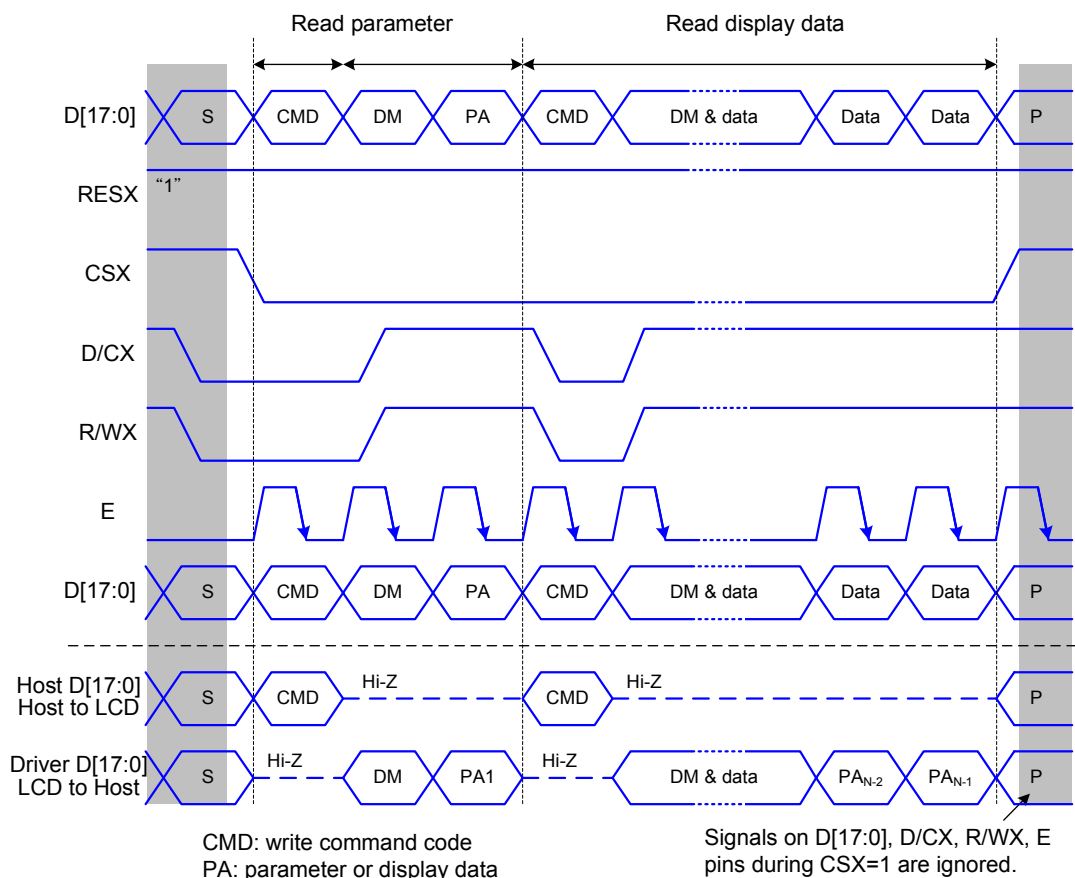


Fig. 9.3.4 6800-series parallel bus protocol, read data form register or display RAM

## 9.4 Serial interface

The selection of this interface is done by IM2. See the Table 9.4.1.

Table 9.4.1 Serial Interface Type Selection

P68	IM2	IM1	IM0	Interface	Read back selection
'0'	0	'0'	'0'	3-line Serial interface	Via the read instruction (8-bit, 24-bit and 32-bit read parameter)

The serial interface is a 3-lines/ 9-bits bi-directional interface for communication between the micro controller and the LCD driver chip. The 3-lines serial use: CSX (chip enable), SCL (serial clock) and SDA (serial data input/output) Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

### 9.4.1 Command Write Mode

The write mode of the interface means the micro controller writes commands and data to the LCD driver. 3-lines serial data packet contains a control bit D/CX and a transmission byte is transferred by the D/CX pin. If D/CX is “low”, the transmission byte is interpreted as a command byte. If D/CX is “high”, the transmission byte is stored in the display data RAM (Memory write command), or command register as parameter.

Any instruction can be sent in any order to the DRIVER. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

#### 3-Line Serial Data Stream Format

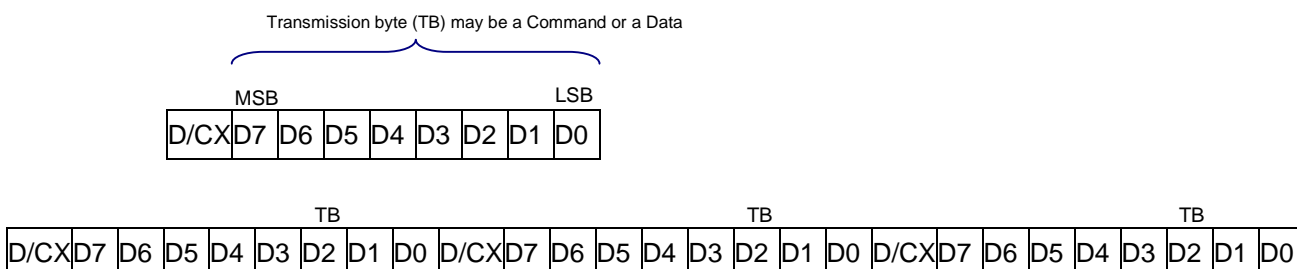


Fig. 9.4.1 Serial interface data Stream format

When CSX is “high”, SCL clock is ignored. During the high time of CSX the serial interface is initialized. At the falling edge of CSX, SCL can be high or low (see Fig 6.1.1.2). SDA is sampled at the rising edge of CSX. D/CX indicates, whether the byte is command code (D/CX='0') or parameter/RAM data (D/CX='1'). It is sampled when first rising edge of SCL (3-lines serial interface). If CSX stays low after the last bit of command/data byte, the serial interface expects the D/CX bit (3-lines serial interface) at the next rising edge of SCL.

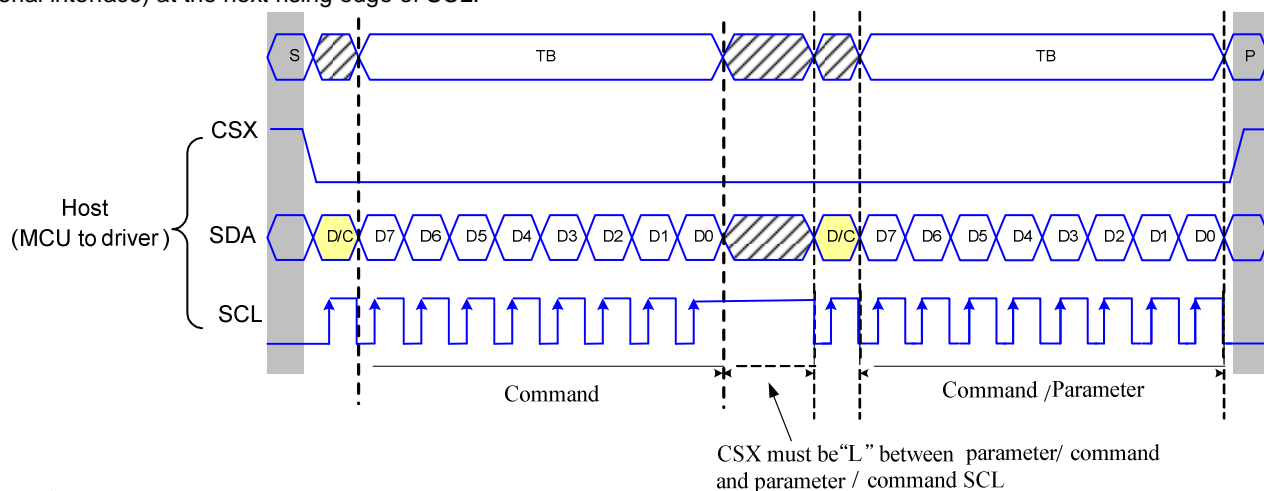


Fig. 9.4.2 3-line serial interface write protocol (write to register with control bit in transmission)

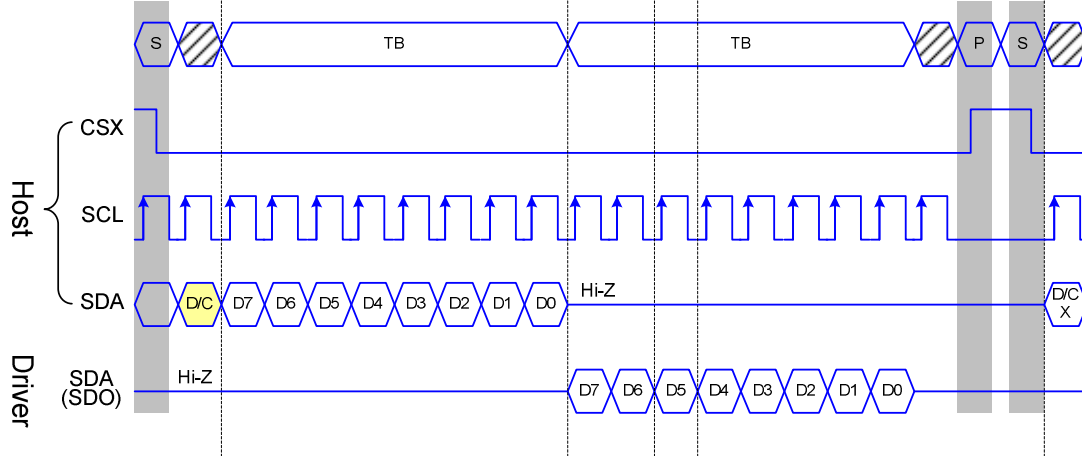


### 9.4.2 Read Functions

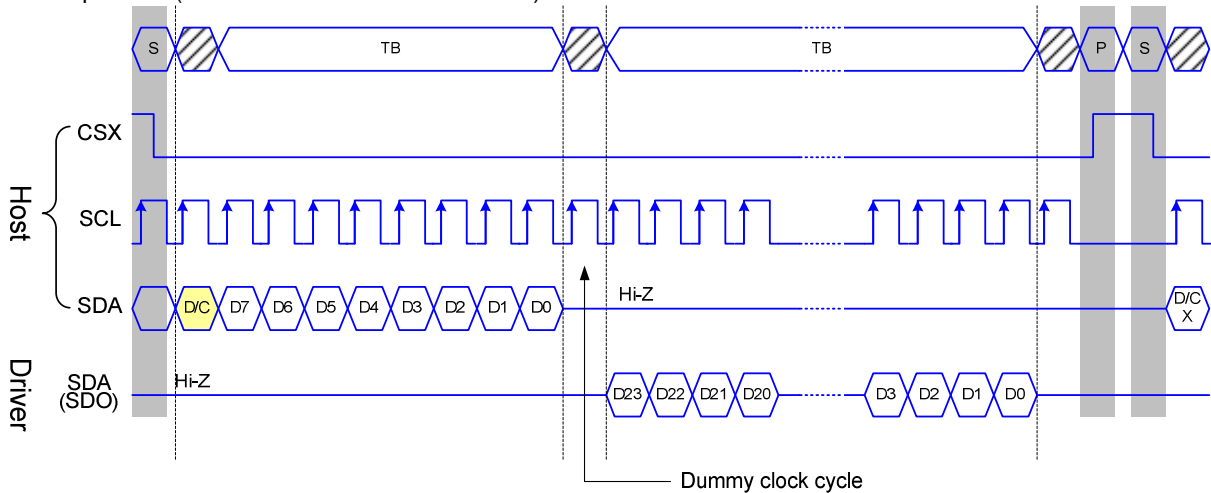
The read mode of the interface means that the micro controller reads register value from the Driver. To do the micro controller first has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. After that CSX is required to go to high before a new command is send (see the below figure). The Driver samples the SDA (input data) at rising edge of SCL, but shifts SDA (output data) at the falling edge of SCL. Thus the micro controller is supported to read at the rising edge of SCL.

After the read status command has been sent, the SDA line must be set to tri-state no later than at the falling edge of SCL of the last bit.

3-line serial protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read):



3-line serial protocol (for RDDID command: 24-bit read)



3-line Serial Protocol (for RDDST command: 32-bit read)

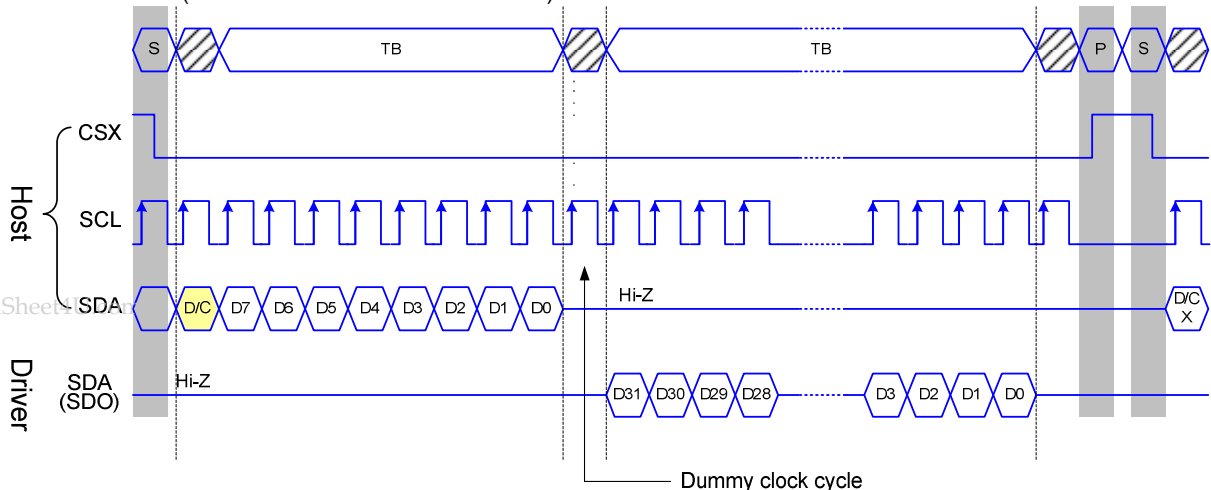


Fig. 9.4.4 3-line serial interface read protocol

9.5 Data Transfer Break and Recovery

If there is a break in data transmission by RESX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then DRIVER will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select line (CSX) is next activated after RESX have been High state. See the following example

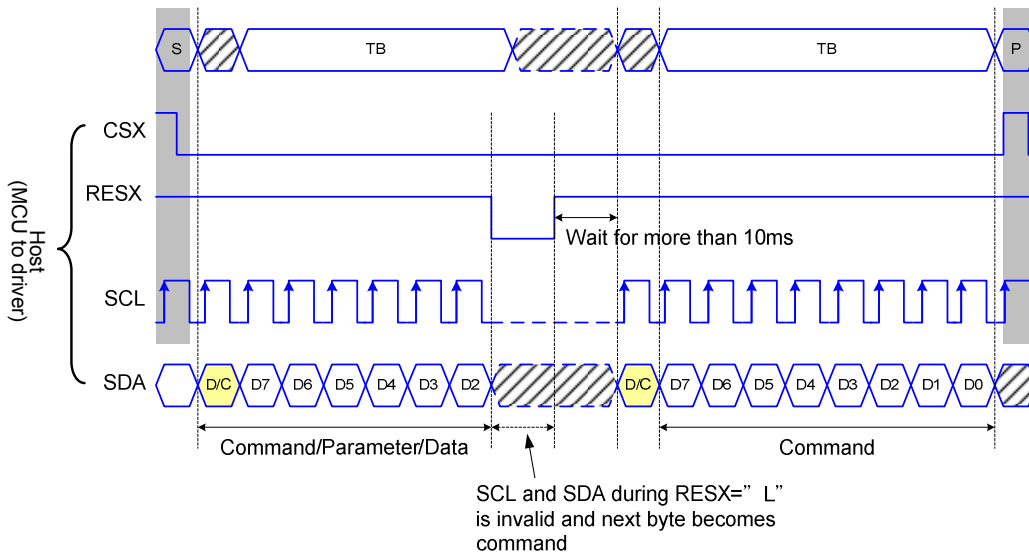


Fig. 9.5.1 Serial bus protocol, write mode - interrupted by RESX

If there is a break in data transmission by CSX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then DRIVER will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated. See the following example

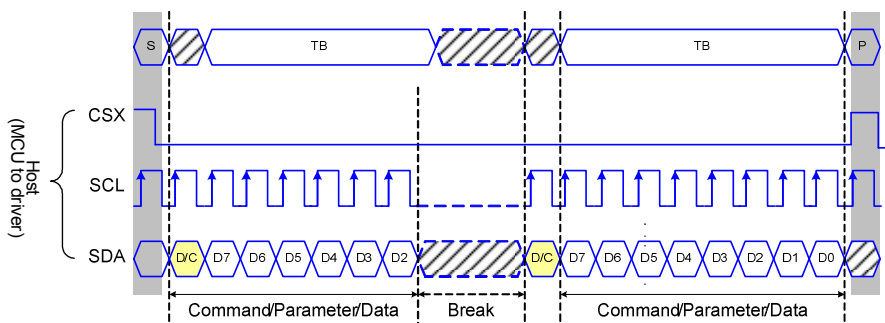


Fig. 9.5.2 Serial bus protocol, write mode - interrupted by CSX

If 1, 2 or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.

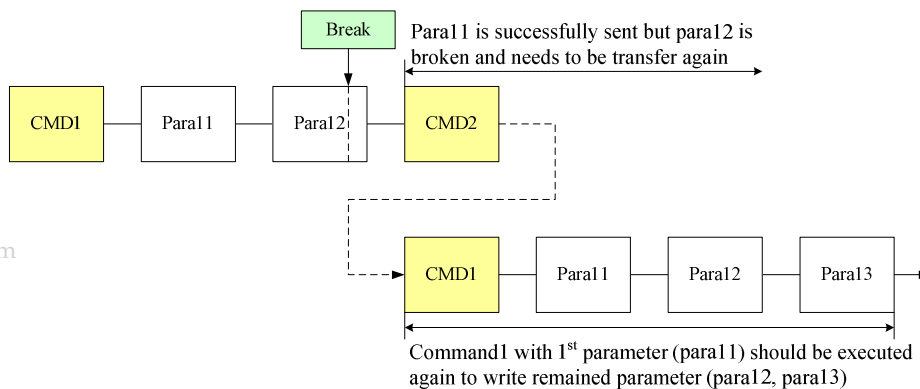


Fig.9.5.3 Write interrupts recovery (serial interface)

If a 2 or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters that were successfully sent are stored and the other parameter of that command remains previous value.

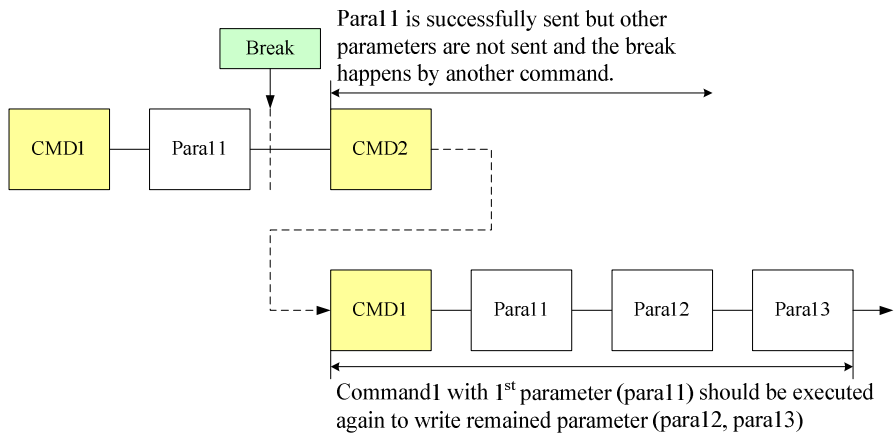


Fig. 9.5.4 Write interrupts recovery (both serial and parallel Interface )

## 9.6 Data transfer pause

It will be possible when transferring a Command, Frame Memory Data or Multiple Parameter Data to invoke a pause in the data transmission. If the Chip Select Line is released after a whole byte of a Frame Memory Data or Multiple Parameter Data has been completed, then DRIVER will wait and continue the Frame Memory Data or Parameter Data Transmission from the point where it was paused. If the Chip Select Line is released after a whole byte of a command has been completed, then the Display Module will receive either the command's parameters (if appropriate) or a new command when the Chip Select Line is next enabled as shown below.

This applies to the following 4 conditions:

- 1) Command-Pause-Command
- 2) Command-Pause-Parameter
- 3) Parameter-Pause-Command
- 4) Parameter-Pause-Parameter

### 9.6.1 Serial interface pause

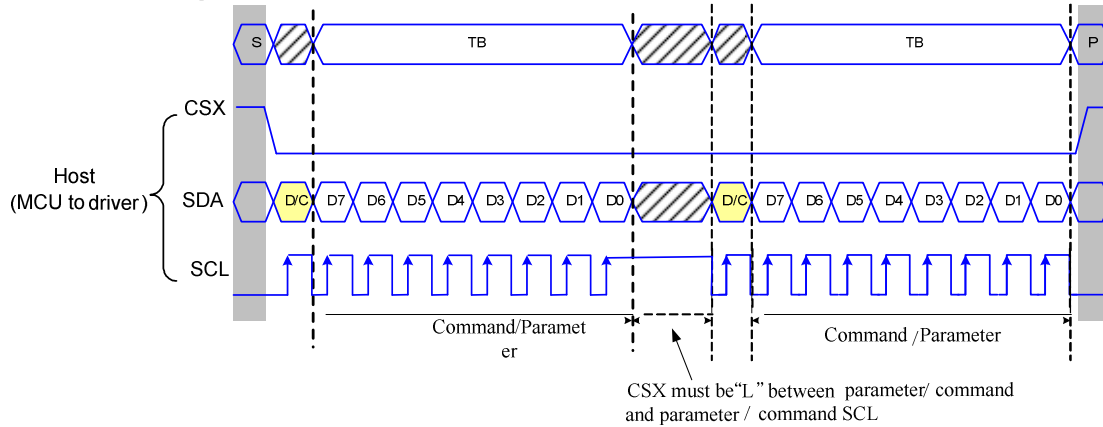


Fig. 9.6.1 Serial interface pause protocol (pause by CSX)

### 9.6.2 Parallel interface pause

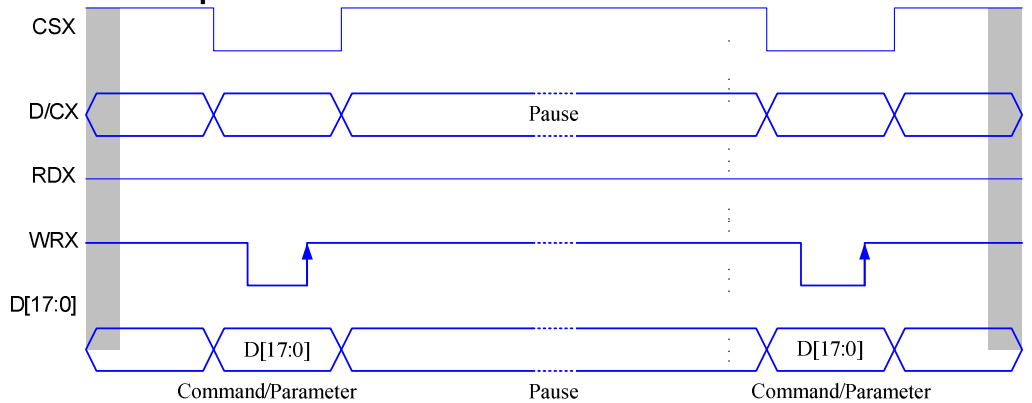


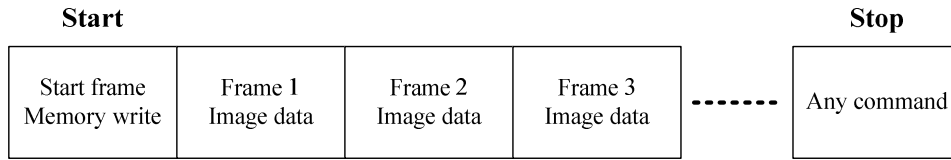
Fig. 9.6.2 Parallel bus pause protocol (paused by CSX)

## 9.7 Data Transfer Modes

The Module has three kinds Color modes for transferring data to the display RAM. These are 12-bit Color per pixel, 16-bit Color per pixel and 18-bit Color per pixel. The data format is described for each interface. Data can be downloaded to the Frame Memory by 2 methods.

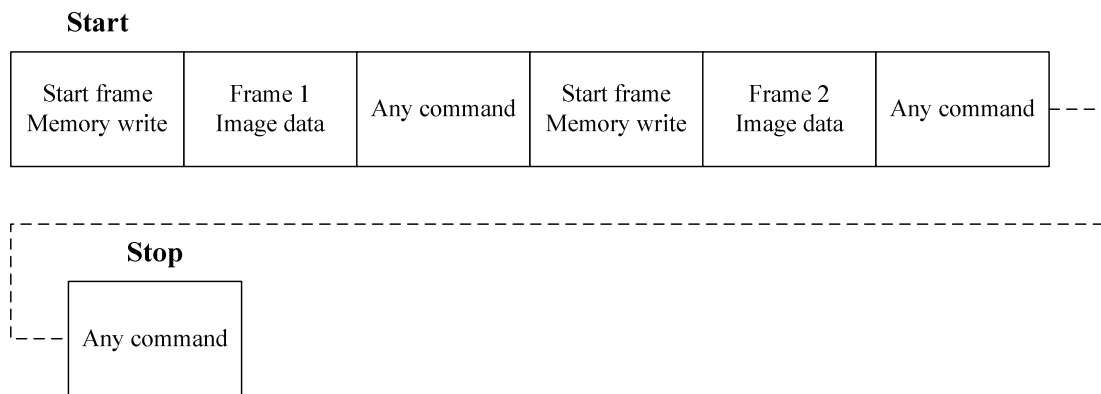
### 9.7.1 Method 1

The Image data is sent to the Frame Memory in successive Frame writes, each time the Frame Memory is filled, the Frame Memory pointer is reset to the start point and the next Frame is written.



### 9.7.2 Method 2

Image Data is sent and at the end of each Frame Memory download, a command is sent to stop Frame Memory Write. Then Start Memory Write command is sent, and a new Frame is downloaded.



Note:

- 1) These apply to all data transfer Color modes on both serial and parallel interfaces.
- 2) The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

## 9.8 Data Color Coding

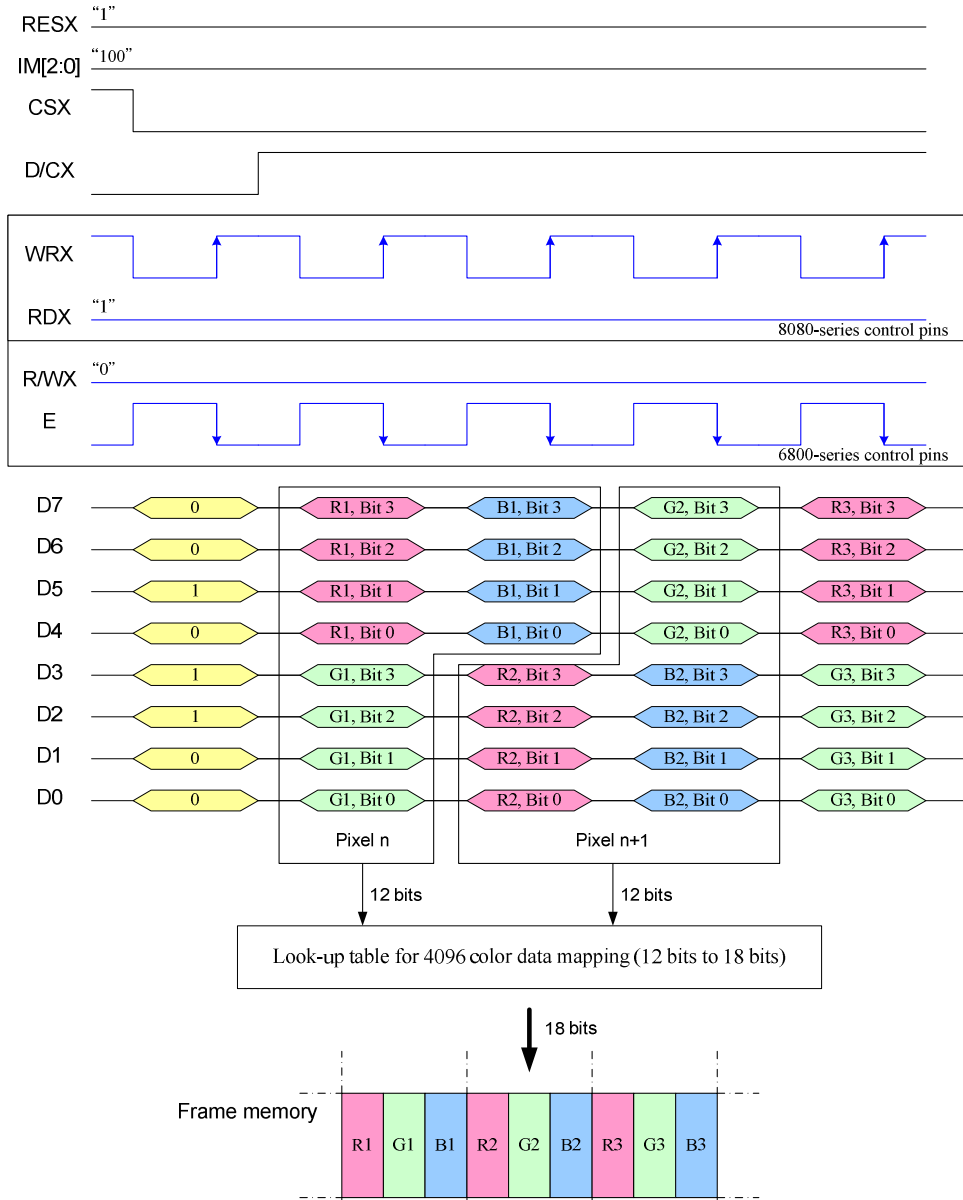
### 9.8.1 8-bit Parallel Interface (IM2, IM1, IM0="100")

Different display data formats are available for three Colors depth supported by listed below.

- 4k Colors, RGB 4,4,4-bit input,
- 65k Colors, RGB 5,6,5-bit input,
- 262k Colors, RGB 6,6,6-bit input,

#### 9.8.1.1 8-bit data bus for 12-bit/pixel (RGB 4-4-4-bit input), 4K-Colors, 3AH="03h"

There are 2 pixels (6 sub-pixels) per 3-bytes.



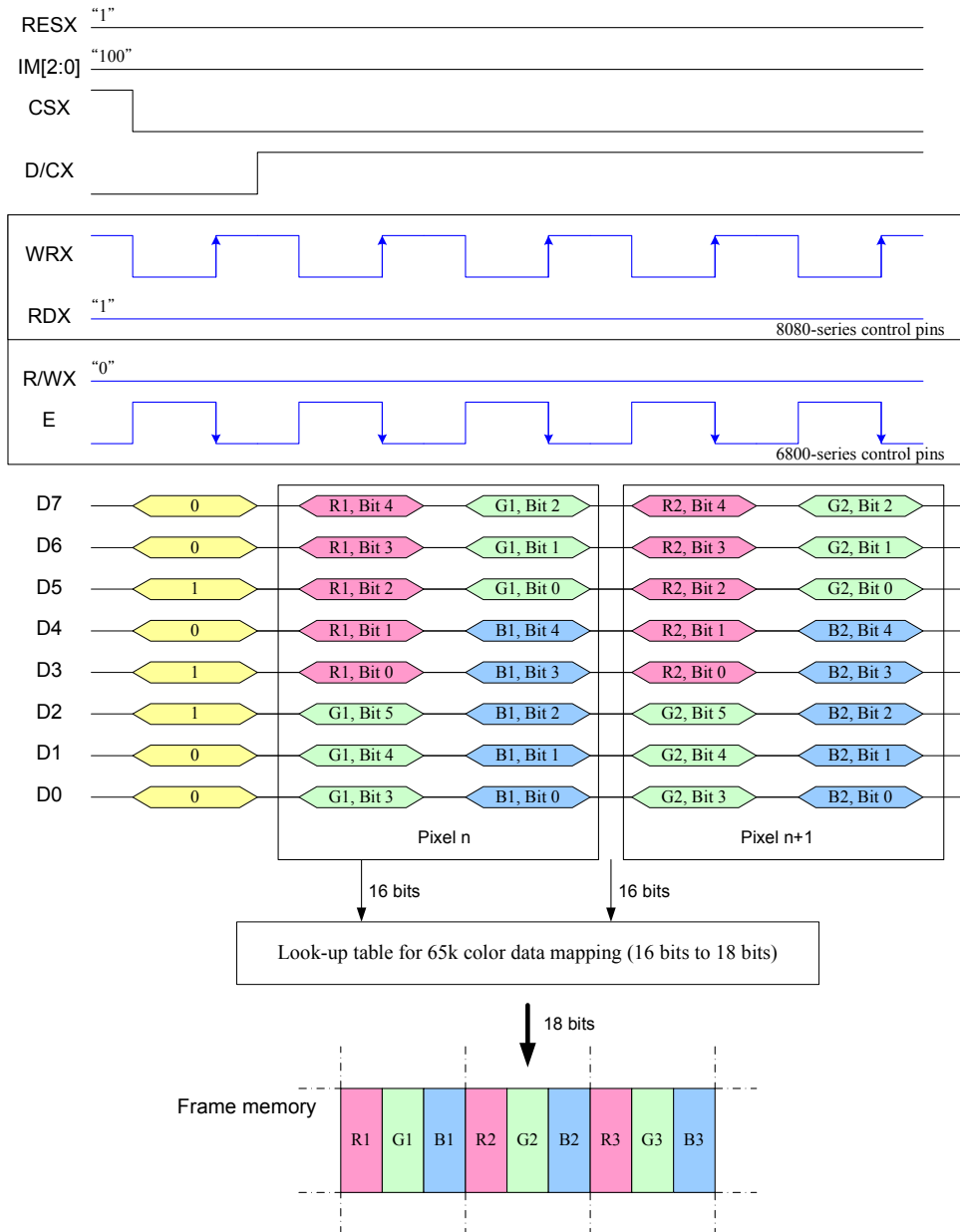
Note 1. The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.

Note 2. 3-times transfer is used to transmit 1 pixel data with the 12-bit color depth information.

Note 3. '-' = Don't care - Can be set to '0' or '1'

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9.8.1.2 8-bit data bus for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3AH="05h"  
 There are 1 pixel (3 sub-pixels) per 2-bytes.



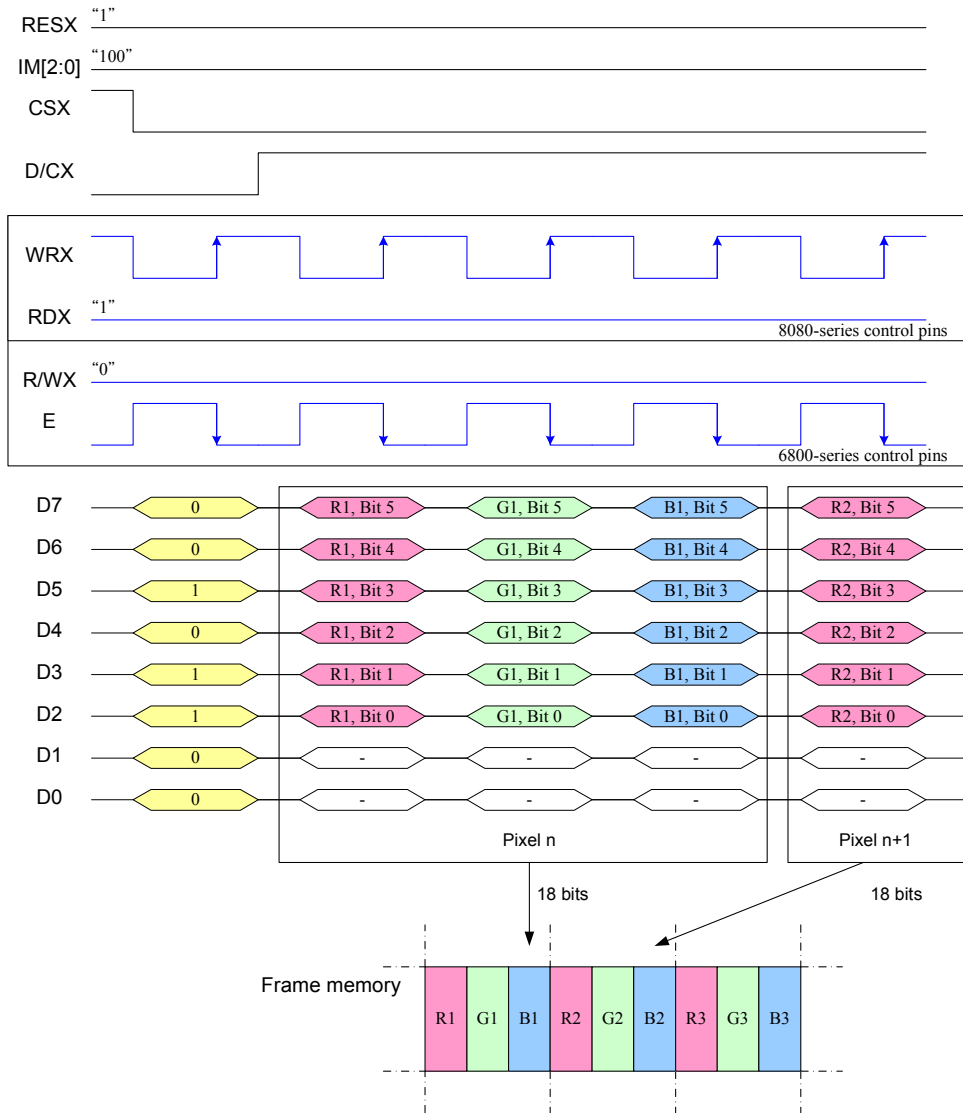
Note 1. The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2. 2-times transfer is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3. '-' = Don't care - Can be set to '0' or '1'

# ST7787

9.8.1.3 8-bit data bus for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3AH="06h"  
 There are 1 pixel (3 sub-pixels) per 3-bytes.



Note 1. The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2. 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3. '-' = Don't care - Can be set to '0' or '1'



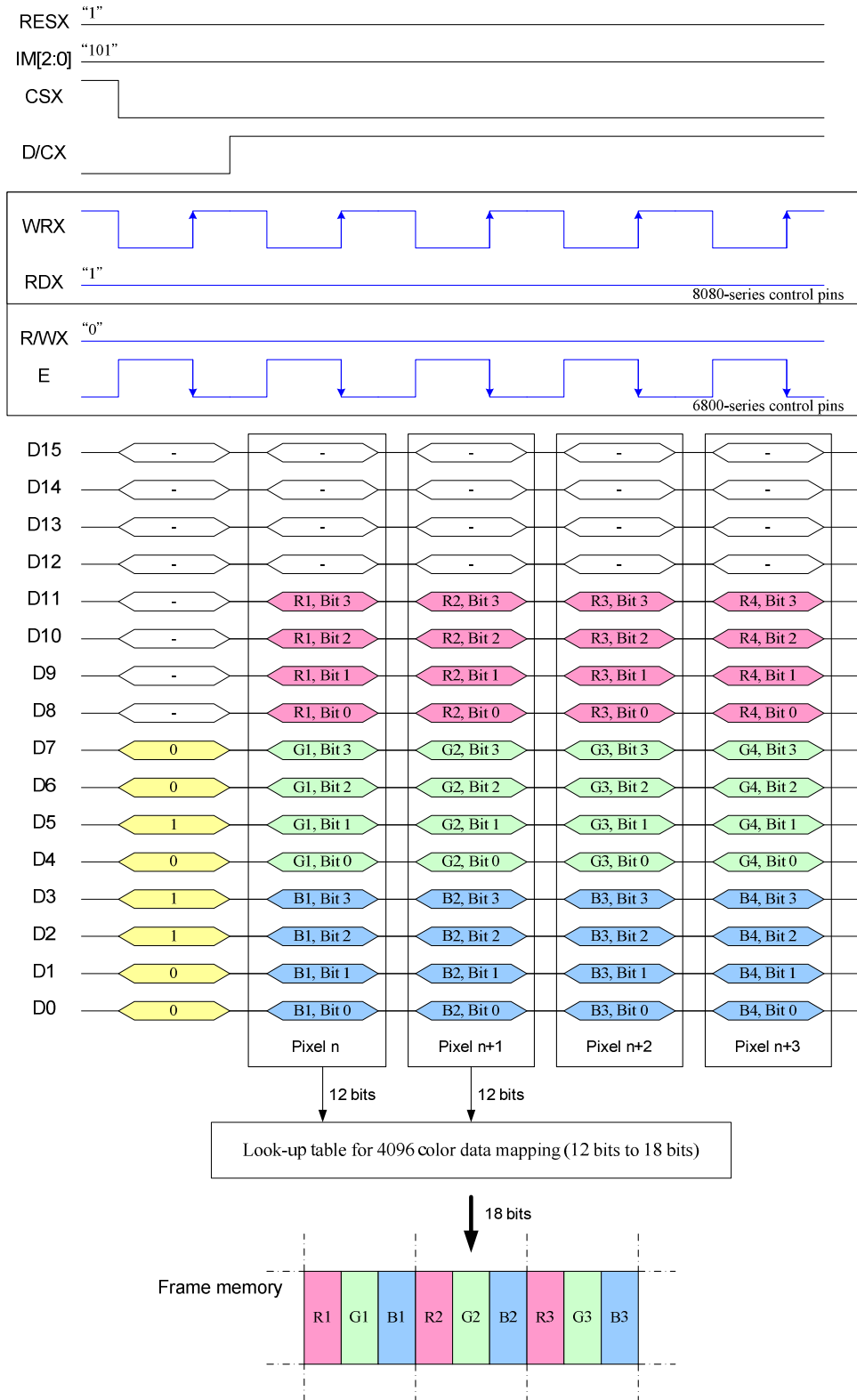
## 9.8.2 16-Bit Parallel Interface (IM2,IM1, IM0="101")

Different display data formats are available for three colors depth supported by listed below.

- 4k colors, RGB 4,4,4-bit input
- 65k colors, RGB 5,6,5-bit input
- 262k colors, RGB 6,6,6-bit input

## 9.8.2.1 16-bit data bus for 12-bit/pixel (RGB 4-4-4-bit input), 4K-Colors, 3AH="03h"

There are 1 pixel (3 sub-pixels) per 1 bytes, 12-bit/pixel.



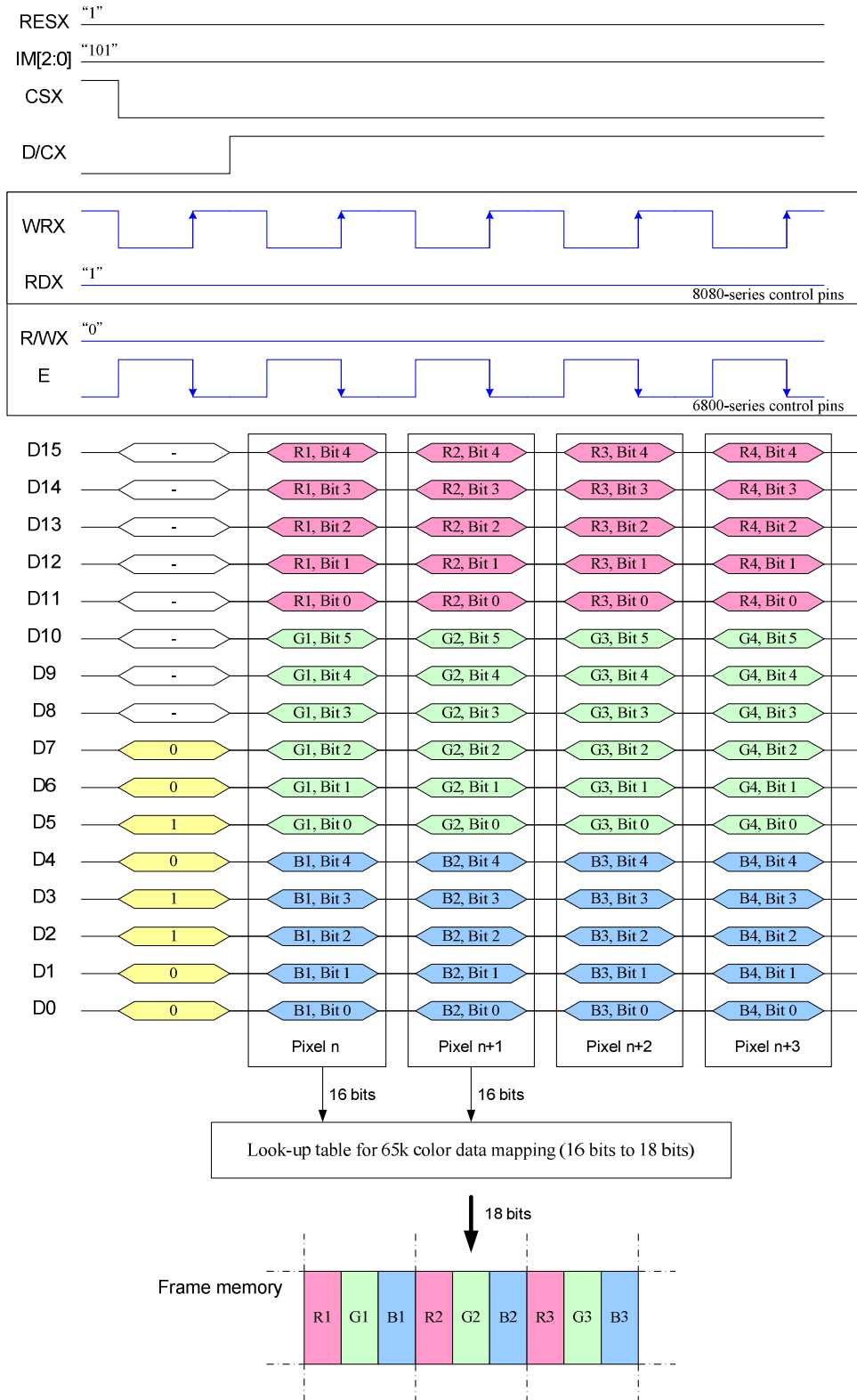
*Note 1. The data order is as follows, MSB=D11, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.*

*Note 2. 1-times transfer (D11 to D0) is used to transmit 1 pixel data with the 12-bit color depth information.*

*Note 3. '-' = Don't care - Can be set to '0' or '1'*

## 9.8.2.2 16-bit data bus for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3AH="05h"

There are 1 pixel (3 sub-pixels) per 1 bytes, 16-bit/pixel.



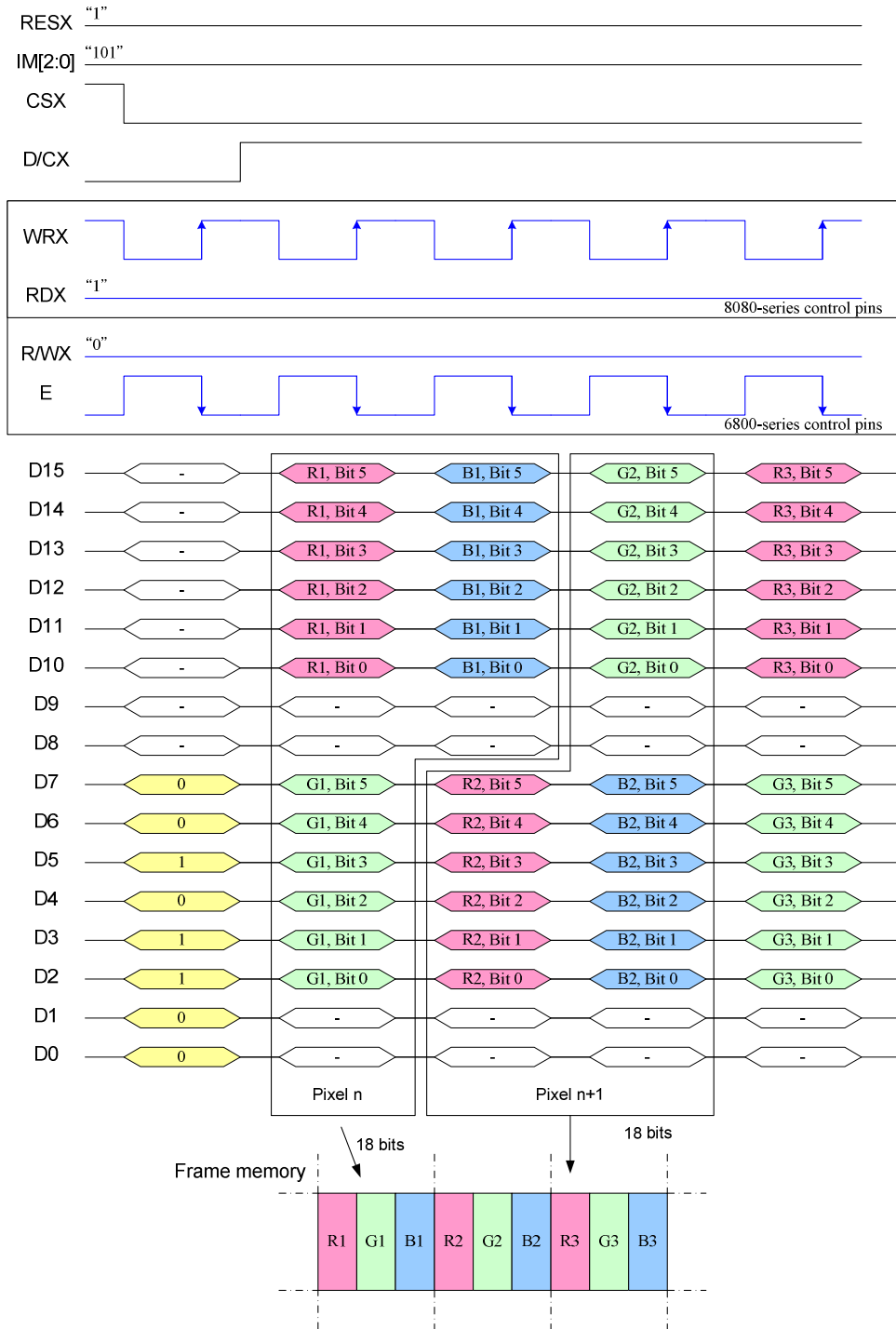
Note 1. The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2. 1-times transfer (D15 to D0) is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3. '-' = Don't care - Can be set to '0' or '1'

# ST7787

9.8.2.3 16-bit data bus for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3AH="06h"  
 There are 2 pixel (6 sub-pixels) per 3 bytes, 18-bit/pixel.



Note 1. The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2. 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

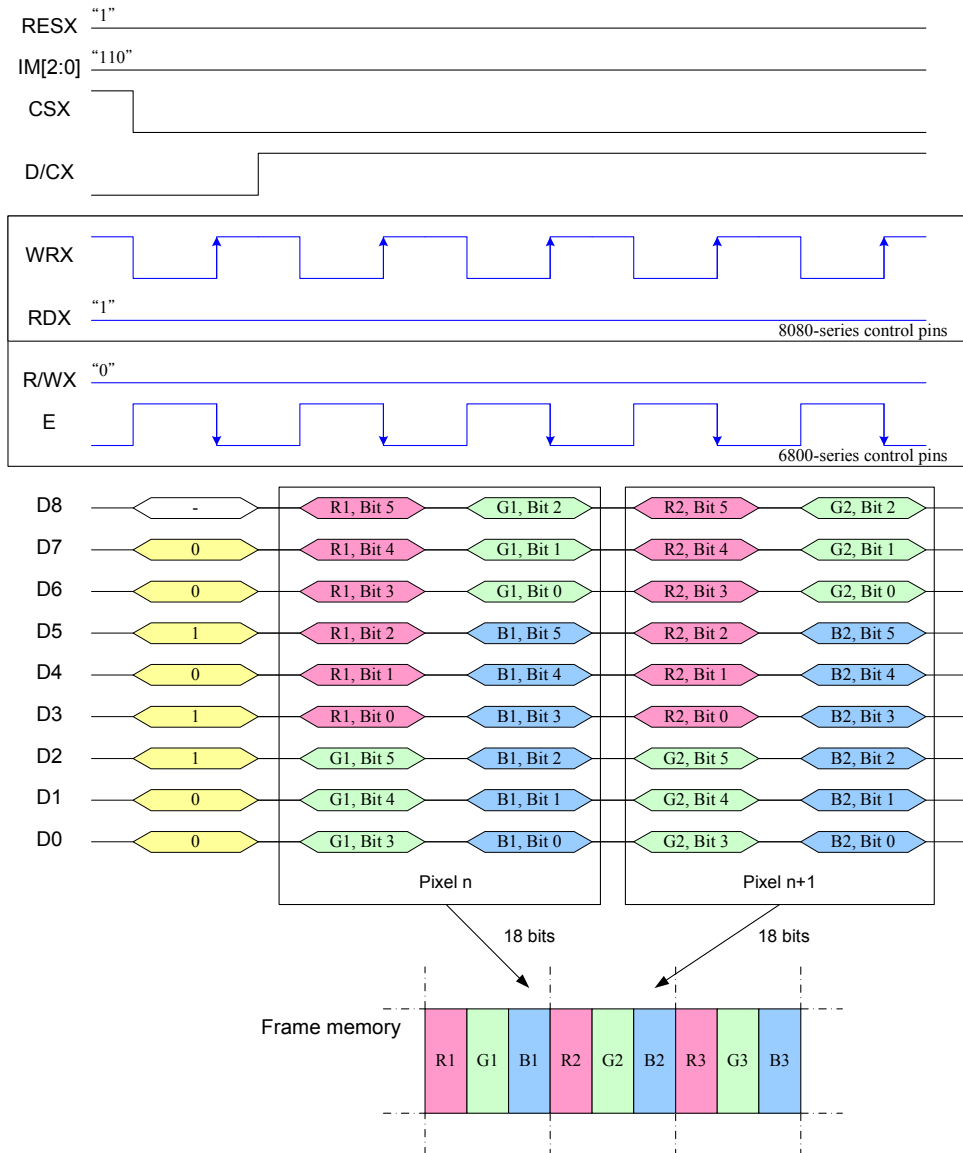
Note 3. '-' = Don't care - Can be set to '0' or '1'

## 9.8.3 9-Bit Parallel Interface (IM2, IM1, IM0="110")

Different display data formats are available for three colors depth supported by listed below.  
 - 262k colors, RGB 6,6,6-bit input

### 9.8.3.1 Write 9-bit data for RGB 6-6-6-bit input (262k-color)

There are 1 pixel (6 sub-pixels) per 3 bytes, 18-bit/pixel.



Note 1. The data order is as follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2. 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3. '-' = Don't care - Can be set to '0' or '1'

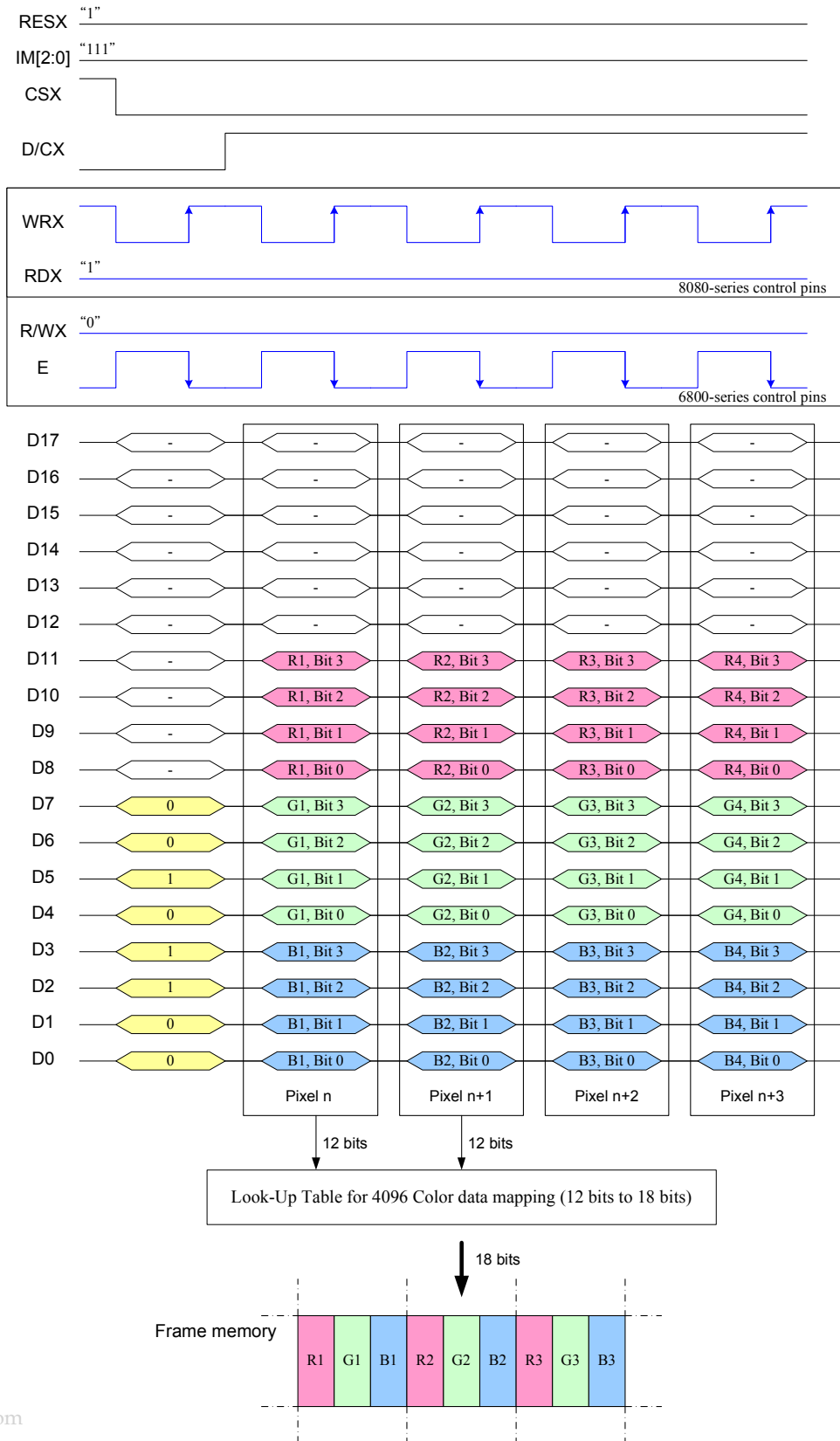
## 9.8.4 18-Bit Parallel Interface (IM2, IM1, IM0="111")

Different display data formats are available for three colors depth supported by listed below.

- 4k colors, RGB 4,4,4-bit input
- 65k colors, RGB 5,6,5-bit input
- 262k colors, RGB 6,6,6-bit input.

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9.8.4.1 18-bit data bus for 12-bit/pixel (RGB 4-4-4-bit input), 4K-Colors, 3AH="03h"  
 There are 1 pixel (3 sub-pixels) per 1 byte, 12-bit/pixel.



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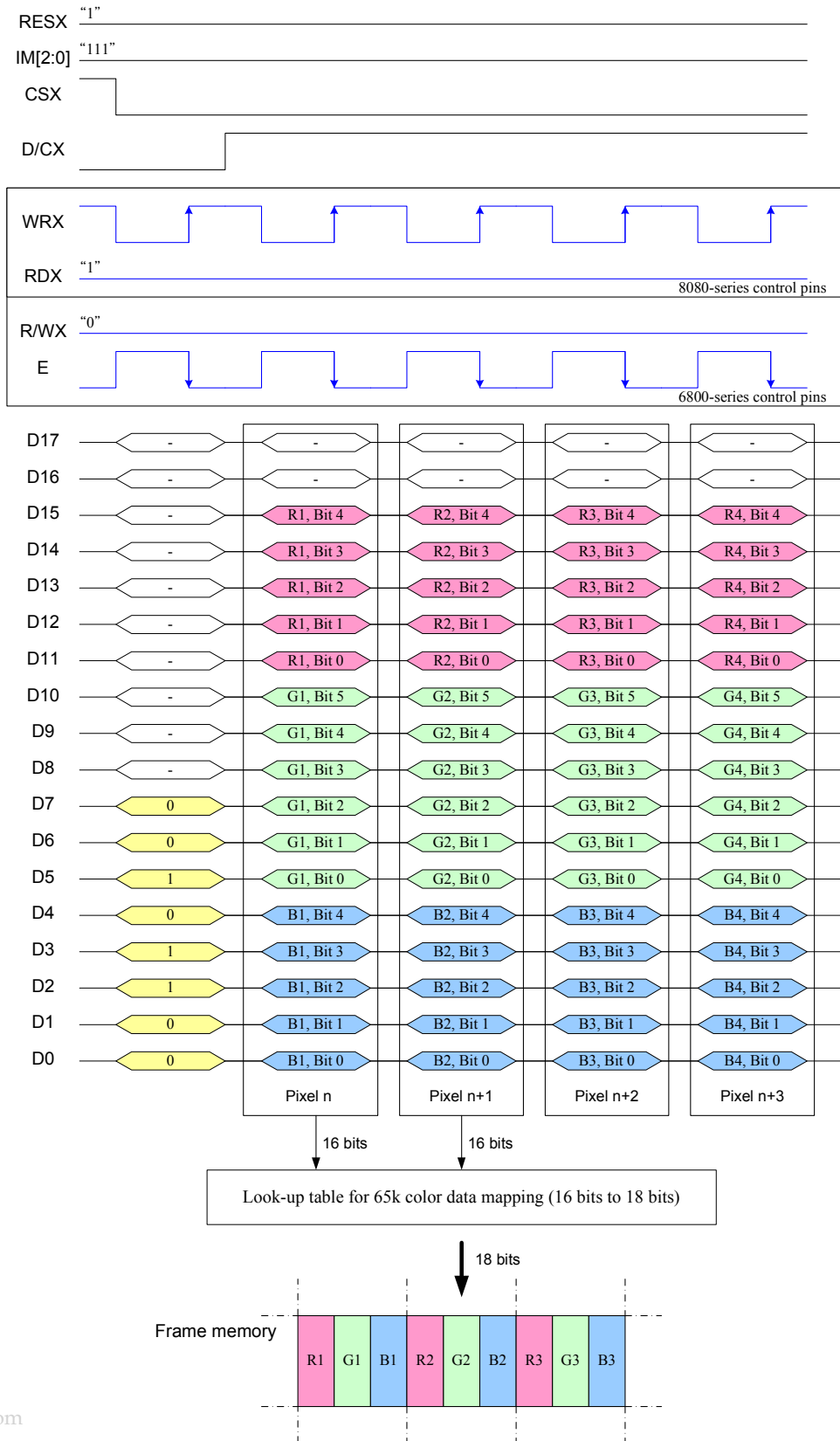
Note 1. The data order is as follows, MSB=D11, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.

Note 2. 1-times transfer is used to transmit 1 pixel data with the 12-bit color depth information.

Note 3. '-' = Don't care - Can be set to '0' or '1'

# ST7787

9.8.4.2 18-bit data bus for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3AH="05h"  
 There are 1 pixel (3 sub-pixels) per 1 byte, 16-bit/pixel.



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Note 1. The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

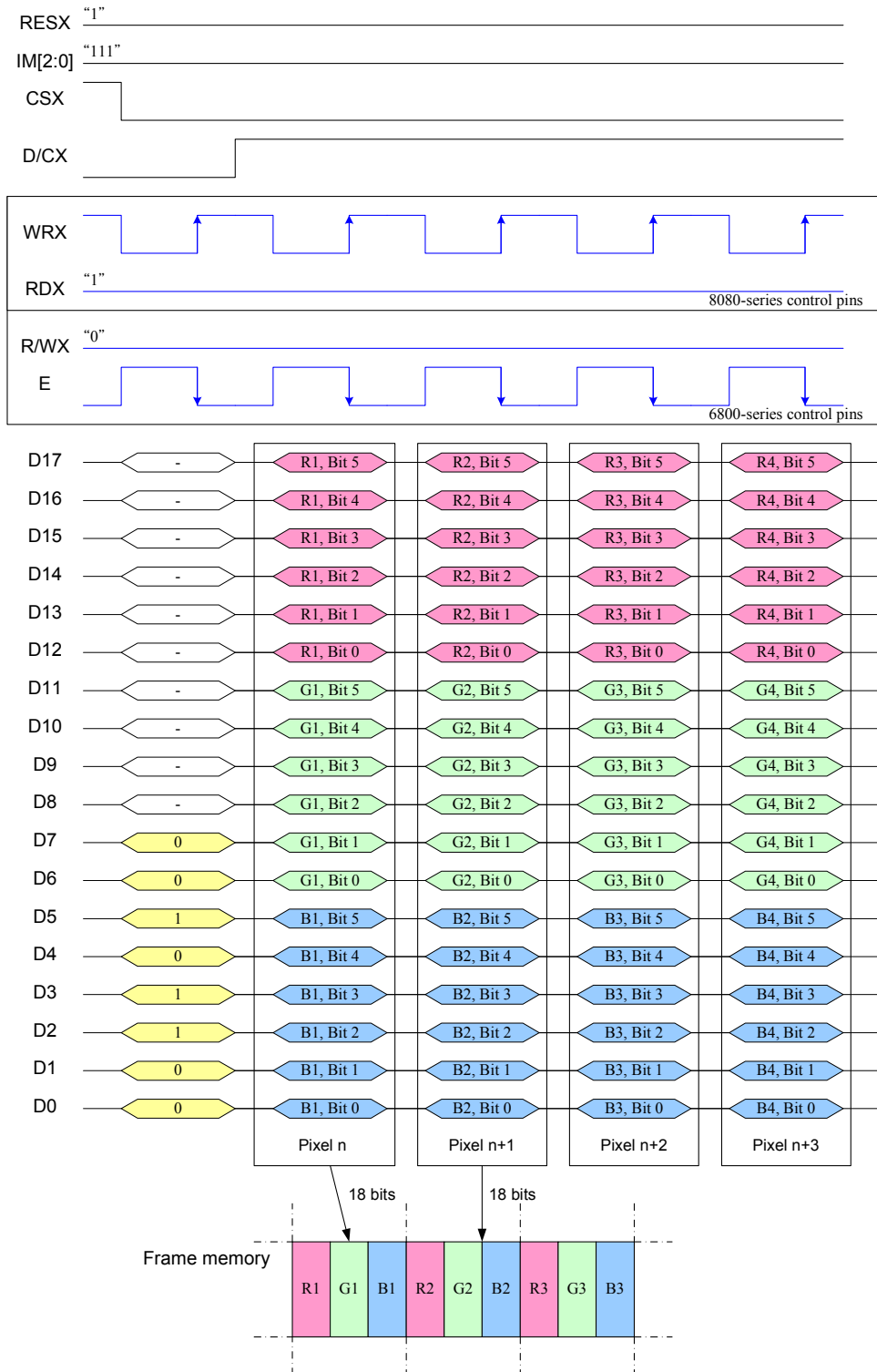
Note 2. 1-times transfer is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3. '-' = Don't care - Can be set to '0' or '1'



# ST7787

9.8.4.3 18-bit data bus for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3AH="06h"  
 There are 1 pixel (3 sub-pixels) per 1 bytes, 18-bit/pixel.



Note 1. The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Read, Green and Blue data.

Note 2. 1-times transfer (D17 to D0) is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3. '-' = Don't care - Can be set to '0' or '1'

## 9.8.5 3-line serial Interface

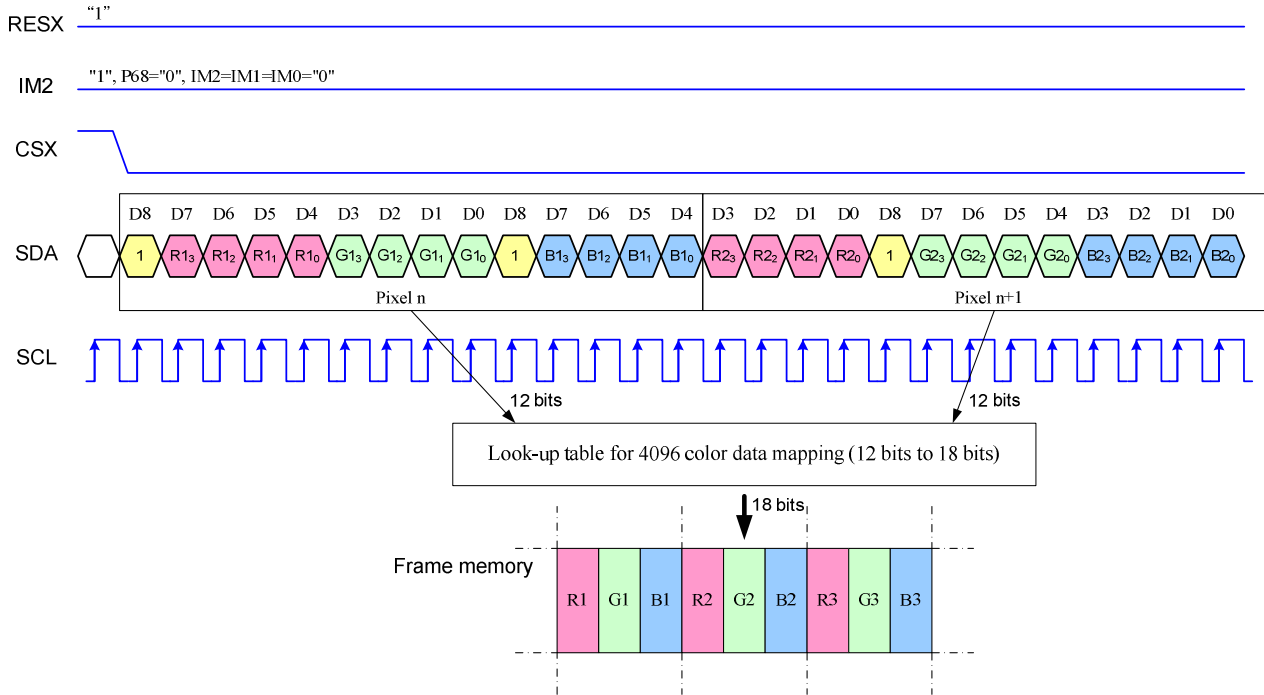
Different display data formats are available for three colors depth supported by the LCM listed below.

4k colors, RGB 4-4-4-bit input

65k colors, RGB 5-6-5-bit input

262k colors, RGB 6-6-6-bit input

### 9.8.5.1 Write data for 12-bit/pixel (RGB 4-4-4-bit input), 4K-Colors, 3AH="03h"



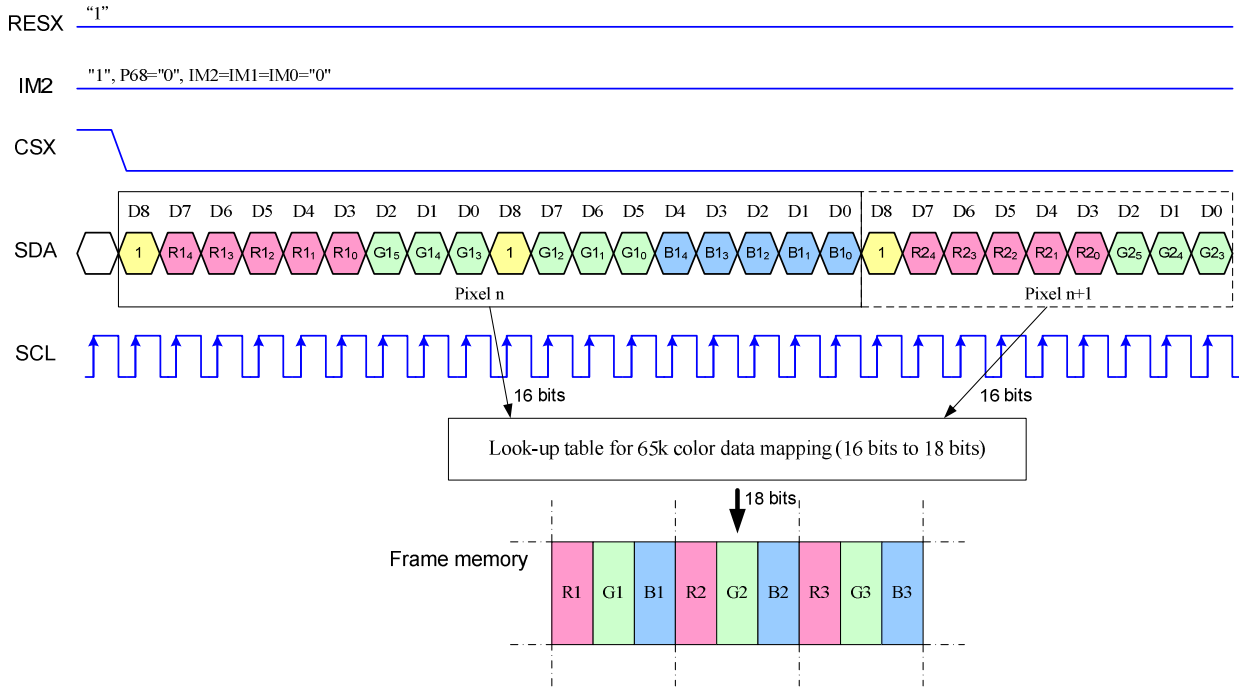
Note 1. pixel data with the 12-bit color depth information

Note 2. The most significant bits are: Rx3, Gx3 and Bx3

Note 3. The least significant bits are: Rx0, Gx0 and Bx0

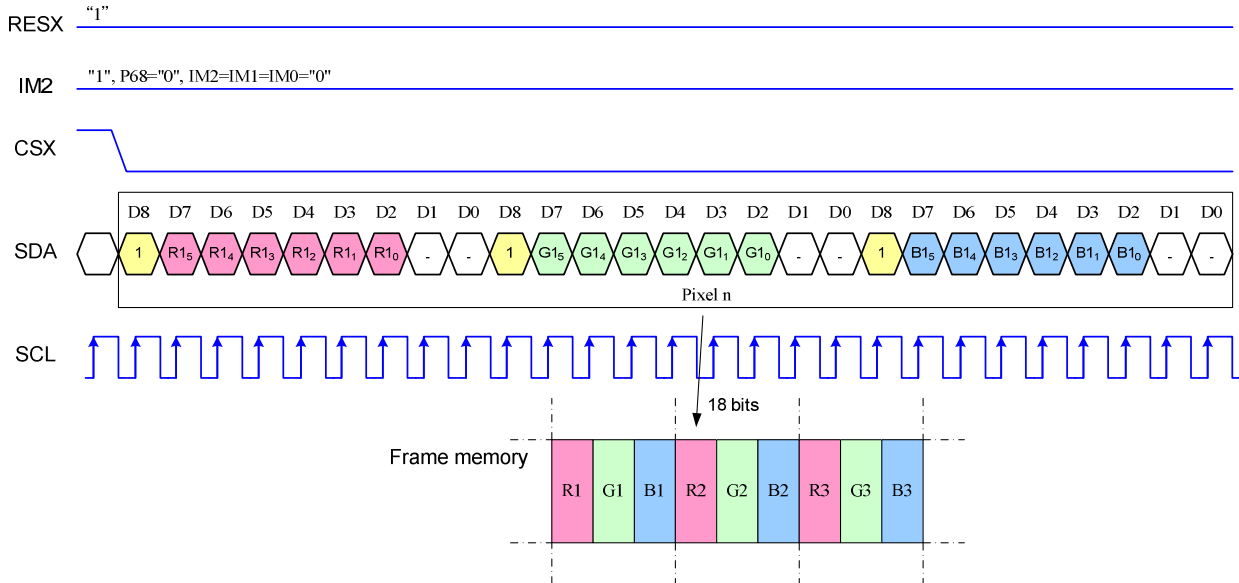
Note 4. X = Don't care - Can be set to '0' or '1'

## 9.8.5.2 Write data for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3AH="05h"



- Note 1. pixel data with the 16-bit color depth information
- Note 2. The most significant bits are: Rx4, Gx5 and Bx4
- Note 3. The least significant bits are: Rx0, Gx0 and Bx0
- Note 4. X = Don't care - Can be set to '0' or '1'

## 9.8.5.3 Write data for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3AH="06h"



- Note 1. pixel data with the 18-bit color depth information
- Note 2. The most significant bits are: Rx5, Gx5 and Bx5
- Note 3. The least significant bits are: Rx0, Gx0 and Bx0
- Note 4. X = Don't care - Can be set to '0' or '1'

## 9.9 RGB interface

### 9.9.1 General Description

The module uses 6, 16 and 18-bit parallel RGB interface which includes: VS, HS, DE, PCLK, D[17:0]. The interface is activated after Power On sequence (See section Power On/Off Sequence)

Pixel clock (PCLK) is running all the time without stopping and it is used to entering VS, HS, DE and D[17:0] states when there is a rising edge of the PCLK. The PCLK cannot be used as continues internal clock for other functions of the display module e.g. Sleep In –mode etc.

Vertical synchronization (VS) is used to tell when there is received a new frame of the display. This is negative ('0', low) active and its state is read to the display module by a rising edge of he PCLK signal.

Horizontal synchronization (HS) is used to tell when there is received a new line of the frame. This is negative ('0', low) active and its state is read to the display module by a rising edge of the PCLK signal.

Data Enable (DE) is used to tell when there is received a RGB information that should be transferred on the display. This is a positive ('1', high) active and its state is read to the display module by a rising edge of the PCLK signal.

D[17:0] (18-bit: R5-R0, G5-G0 and B5-B0; 16-bit: R4-R0, G5-G0 and B4-B0) are used to tell what is the information of the image that is transferred on the display (When DE='1' and there is a rising edge of PCLK). D[17:0] can be '0' (low) or '1' (high). These lines are read by a rising edge of the PCLK signal.

The PCLK cycle is described in the following figure.

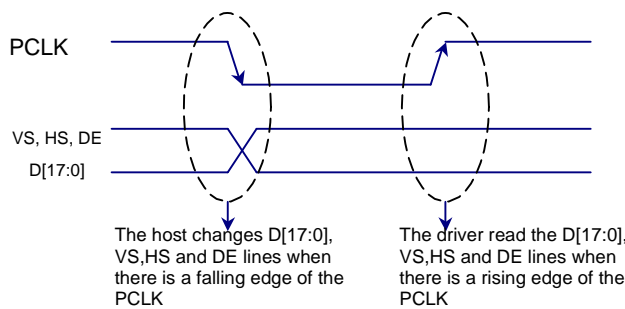


Fig. 9.9.1 PCLK cycle

*Note: PCLK is an unsynchronized signal (It can be stopped).*

## 9.9.2 General Timing Diagram

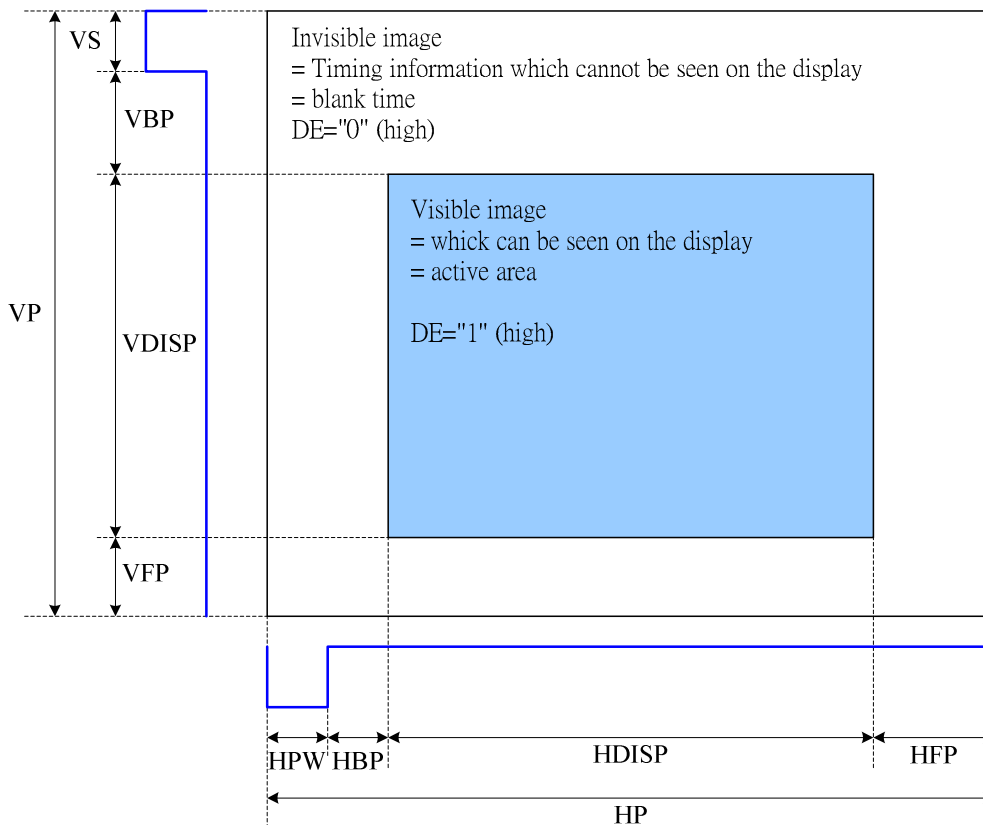


Fig. 9.9.2 RGB general timing diagram

The image information must be correct on the display, when the timings are in range on the interface.

However, the image information can be incorrect on the display, when timings are not out of range on the interface (Out of the range timings cannot on the host side). The correct image information must be displayed automatically (by the display module) on the next frame (vertical sync.) when there is returned from out of the range to in range interface timing.

## 9.9.3 Updating Order on Display Active Area (Normal Display Mode On + Sleep Out)

There is defined different kind of updating orders for display. These updating orders are controlled by H/W (SMX, SMY) and S/W (MX, MY, MV) bits.

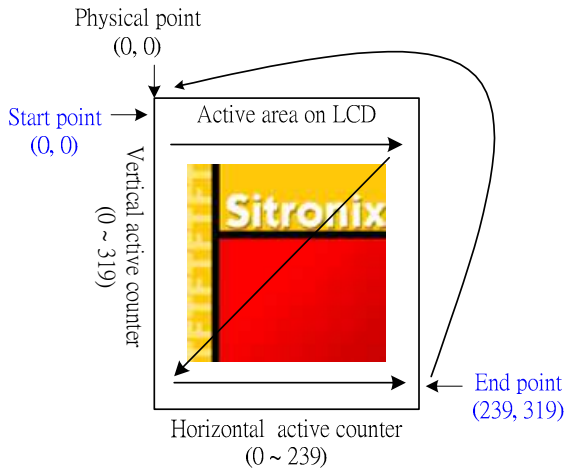


Fig. 9.9.3 Updating order when MADCTL's MX="0" and MY="0"

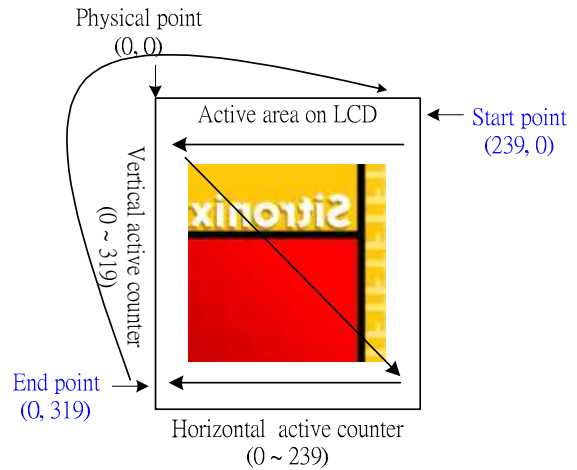


Fig. 9.9.4 Updating order when MADCTL's MX="1" and MY="0"

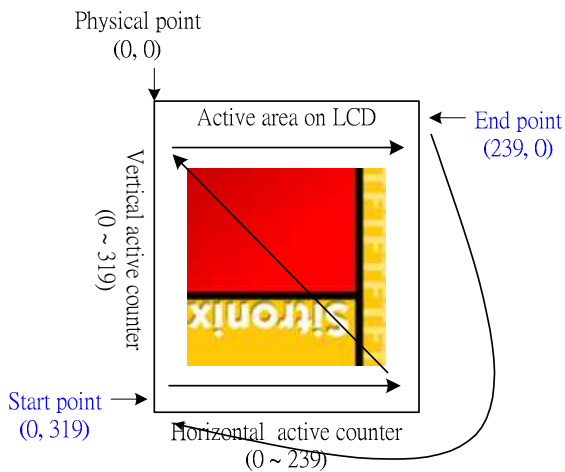


Fig. 9.9.5 Updating order when MADCTL's MX="0" and MY="1"

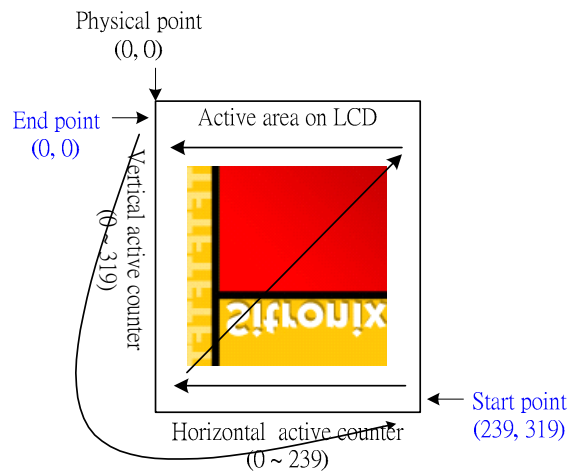


Fig. 9.9.6 Updating order when MADCTL's MX="1" and MY="1"

Table 9.9.1 Rules for Updating Order

Condition	Horizontal Counter	Vertical Counter
An active VS signal is received	Return to 0	Return to 0
Signal Pixel information of the active area is received	Increment by 1	No change
An active HS signal between two active area lines	Return to 0	Increment by 1
The Horizontal counter is larger than 239 and the Vertical counter is larger than 319	Return to 0	Return to 0

Note 1. Pixel order is RGB on the display.

Note 2. Data streaming direction from the host to the display is described in the following figure.

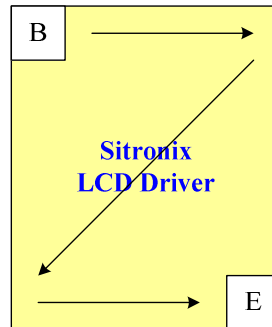


Fig. 9.9.3 Data streaming order for RGB interface

### 9.9.4 RGB Interface Bus Width set

All 4-kinds of bus width can be available during RGB interface mode (selected by COLMOD (3Ah) command for 6-bit, 16-bit and 18-bit data width)

VIPF[3:0]	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bus width
0101	R4	R3	R2	R1	R0	x	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	x	16-bit data
0110	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	18-bit data
VIPF[3:0]	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bus width
1110	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	6-bit data
	x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
	x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	

Note 1: When VIPF[3:0]=”1110”, 6-bit data width of 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 2: Only VIPF[3:0]= ”0101”, ”0110” and ”1110” are valid on RGB I/F, Others are invalid.

Note 3: ‘x’ Don’t care, but need to set VDDI or DGND level.

### 9.9.5 RGB Interface Mode Set

Table 9.9.5.1 RGB Interface Mode Set

RGB I/F Mode	PCLK	DE	VS	HS	Video Data bus D[17:0]	Register for Blanking Porch setting	Reference clock for Display
RGB Mode 1	Used	Used	Used	Used	Used	Not Used	Internal Oscillator
RGB Mode 2	Used	Used	Used	Used	Used	Used	Internal Oscillator

There are 2-kinds of RGB mode which is selected by RCM1 & RCM0 hardware pins.

**In RGB Mode 1** (RCM1, RCM0 = “10”), writing data to frame memory is done by PCLK and Video Data Bus (D[17:0]), when DE is high state. The external synchronization signals (PCLK, VS and HS) are used for internal display signals. So, controller (host) must always transfer PCLK, VS, HS and DE signals to IC.

**In RGB Mode 2** (RCM1, RCM0 = “11”), blanking porch setting of VS and HS signals are defined by RGBBPCTR (B5h) command. DE pin is used for data making. When DE pin is high, valid data is directly stored to frame memory. In the contrast, if DE pin is low the data of frame memory will keep same status.

Table 9.9.5.2 MCU & RGB Interface Comparisons table

Function	RCM1, RCM0		RCM1, RCM0			
	"0x"		"10"		"11"	
Mode selection 1	8080/ 6800 I/F + SPI I/F		RGB I/F + SPI I/Mode selection 1/F			
	MCU Mode		RGB Mode 1		RGB Mode 2	
Mode selection 2	IMx=	IMx="00"	ICM=0'	ICM=1'	ICM=0'	ICM=1'
	8080/ 6800 I/F	SPI I/F	RGB-1 I/F + SPI I/F		RGB-2 I/F + SPI I/F	
Motion /Still selection	Motion or Still picture	Still picture	Motion or Still picture	Still picture	Motion or Still picture	Still picture
Input data	D[17:0]	D0	D[17:0]	SDA H/W pin enable	D[17:0]	SDA H/W pin enable
Input signal	CSX	D/CX = SCL	PCLK	D/CX = SCL	PCLK	D/CX = SCL
	WRX (R/WX), RDX (E)	CSX	VS, HS, DE	CSX	VS, HS, DE	CSX
GRAM Write cycle	Refer the WRX cycle	Refer SCL	Refer PCLK	Refer SCL	Refer PCLK	Refer SCL
GRAM Read Cycle	Refer Internal Oscillator	Refer Internal Oscillator	Refer PCLK	Refer Internal Oscillator	Refer PCLK	Refer Internal Oscillator
Command setting	D[7:0]	D0	SDA	SDA	SDA	SDA
SMX, SMY, SRGB	-If those register not change, those H/W pins are always valid. If those registers be changed, should be follow registers setting. -When Power On or H/W reset, those function follow H/W pins setting first.					
TE Function	-By command setting		-By command setting		-By command setting	
Normal / Partial mode	-By command setting		-By command setting		-By Command setting	
Idle Mode (IDM H/W pin)	-By command setting -Don't care in this mode, but should be set to VDDI or DGND			-By IDM H/W pin -IDM On/OFF (39h/28h) are disable		
Display On/ Off (SHUT H/W pin)				-By SHUT H/W pin -SLPIN(10h), SLPOUT(11h), Display On/OFF (29h/28h) are disable		
Data inverter setting (REV H/W pin)				-By REV H/W pin -INVON/OFF (21h/20h) are disable		
DE H/W pin	-Don't care in this mode, but should be set to VDDI or DGND		-The data latched by rising edge of PCLK when DE='1' -When display data coming the DE signal should be VDDI level		-When DE='0' area, the data of GRAM will keep the same status.	
RL H/W pin			-Don't care in this mode, but should be set to VDDI or DGND		-By H/W pin	
TB H/W pin					-No commands conflict	
Blanking porch	-Don't care in this mode		-Control by DE signal		-Control by RGBBPCTR (B5h)	
Colors format	-Control by IFPF[2:0] of COLMOD(3A)		-Control by VIPF[3:0] of COLMOD(3A)			

Note 1: RCM1 and RCM0 are H/W setting pins.

Note 2: In RGB + SPI I/F (RCM="1x"), VS, HS, DE, PCLK and D[17:0] are Hi-Z by Driver and can be stop for Host, when ICM='1'.

Note 3: In RGB + SPI I/F (RCM="1x"), the data deliver via GRAM

Note 4: When Power on Driver IC should be detect SMX, SMY, SRGB H/W setting

Note 5: When Power on Driver IC should be detect RCM1, RCM0 H/W setting and get into the I/F mode.

Note 6: When Power on Driver IC should be detect LCM1, LCM0 H/W setting and get into the setting mode.



## 9.9.6 RGB Interface Timing Diagram

### 9.9.6.1 General Timings for RGB I/F

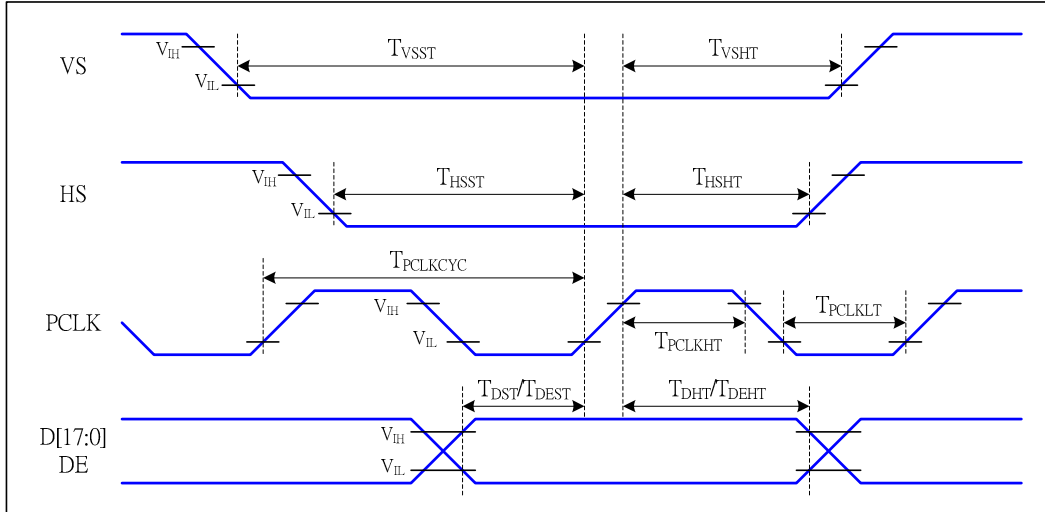


Fig. 9.9.6 General timing of RGB interface

Table 9.9.6.1 General Timing for RGB I/F

Item	Symbol	Condition	Specification			Unit
			Min	Type.	Max	
Pixel low pulse width	$T_{PCLKLT}$		12			ns
Pixel high pulse width	$T_{PCLKHT}$		12			ns
Vertical Sync. set-up time	$T_{VSSST}$		15			ns
Vertical Sync. hold time	$T_{VSSH}$		15			ns
Horizontal Sync. set-up time	$T_{HSST}$		15			ns
Horizontal Sync. hold time	$T_{HSH}$		15			ns
Data Enable set-up time	$T_{DEST}$		15			ns
Data Enable hold time	$T_{DEHT}$		15			ns
Data set-up time	$T_{DST}$		15			ns
Data hold time	$T_{DHT}$		15			ns

Note 1:  $V_{DDI}=1.65$  to  $3.3V$ ,  $V_{DD}=2.45$  to  $3.3V$ ,  $AGND=DGND=0V$ ,  $T_a=-30$  to  $70$  °C (to  $+85$  °C no damage)

Note 2: The input signal rise time and fall time ( $t_r$ ,  $t_f$ ) is specified at 15 ns or less.

Note 3: Data lines can be set to "High" or "Low" during blanking time – Don't care.

Note 4: Logic high and low levels are specified as 30% and 70% of  $V_{DDI}$  for Input signals.

Note 5: HP is multiples of eight PCLK.

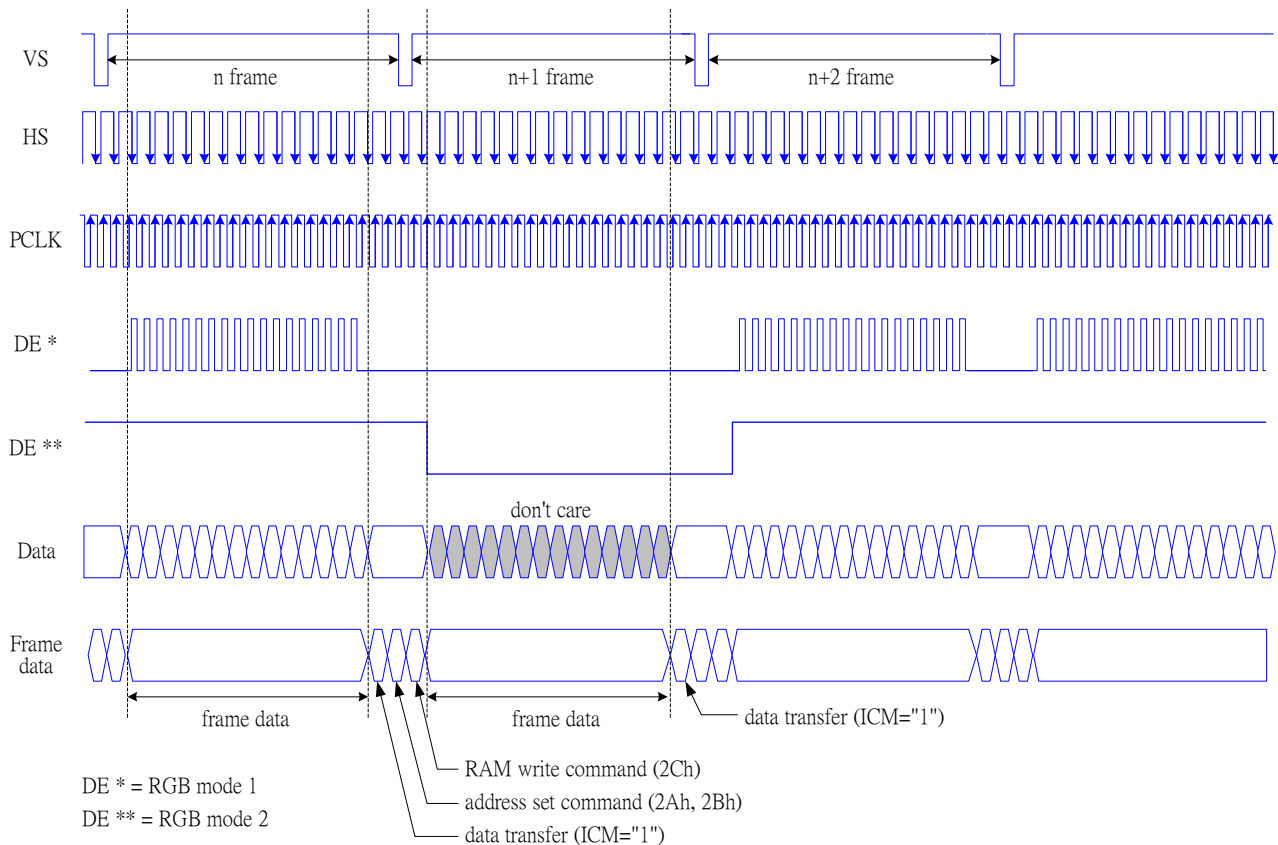


Fig. 9.9.7 RAM access via SPI interface in RGB mode

Note: DP='0', EP='0', HSP='0' and VSP='0' of RGBCTR (B0h) command.

## 9.9.6.2 RGB Interface Mode 1 Timing Diagram

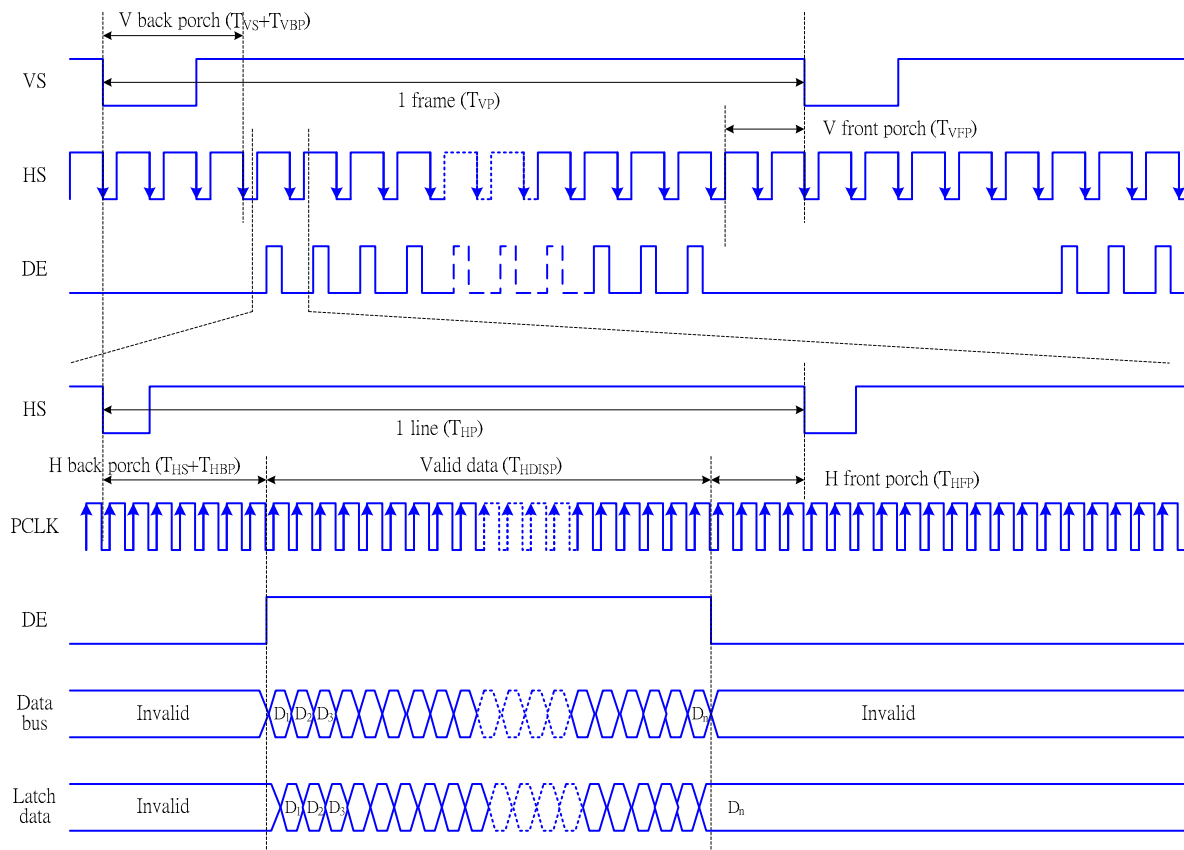
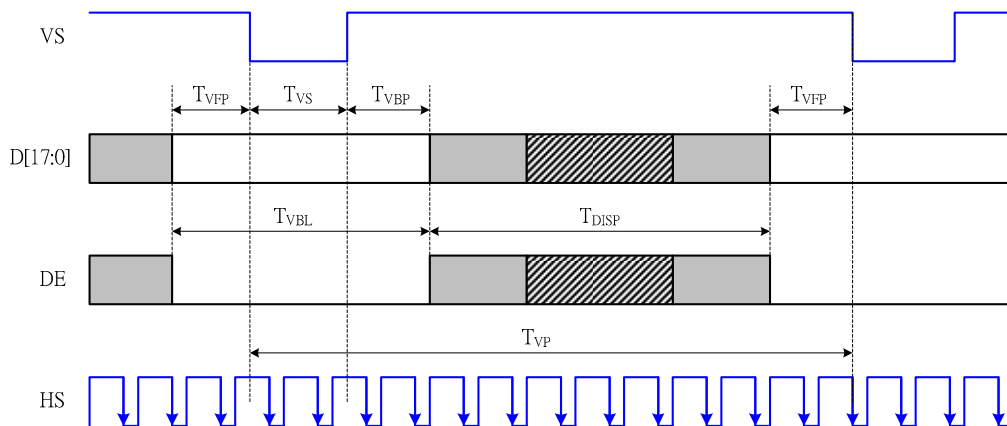


Fig. 9.9.8 RGB mode 1 timing diagram

Note:  $DP=0$ ,  $EP=0$ ,  $HSP=0$  and  $VSP=0$  of RGBCTR (B0h) command.

Vertical timing for RGB I/F



Horizontal timing for RGB I/F

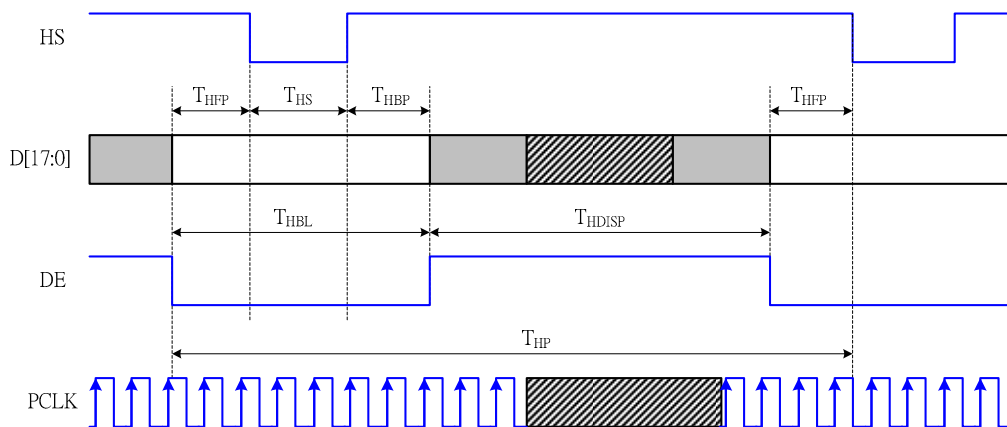


Fig. 9.9.9 Vertical and horizontal timing of RGB interface

Table 9.9.6.2 Vertical and Horizontal Timing for RGB I/F

Item	Symbol	Condition	Specification			Unit
			Min	Typ.	Max	
<b>Vertical Timing</b>						
Vertical cycle period	$T_{VP}$		326		330	HS
Vertical low pulse width	$T_{VS}$		2		4	HS
Vertical front porch	$T_{VFP}$		2		4	HS
Vertical back porch	$T_{VBP}$		2		4	HS
Vertical data start line		$T_{VS} + T_{VBP}$	4		8	HS
Vertical blanking period	$T_{VBL}$	$T_{VS} + T_{VBP} + T_{VFP}$	6		10	HS
Vertical active area	$T_{VDISP}$			320		HS
Vertical refresh rate	$T_{VRR}$	Frame rate	61.75	65	68.25	Hz
<b>Horizontal Timing</b>						
Horizontal cycle period	$T_{HP}$		272		512	PCLK
Horizontal low pulse width	$T_{HS}$		2		256	PCLK
Horizontal front porch	$T_{HFP}$		2		256	PCLK
Horizontal back porch	$T_{HBP}$		2		256	PCLK
Horizontal data start point		$T_{HS} + T_{HBP}$	30		256	PCLK
		$ff_{HS} + f_{HBP}$	1.0			us
Horizontal blanking period	$T_{HBL}$		32		256	PCLK
Horizontal active area	$T_{HDISP}$			240		PCLK
Pixel clock cycle	$T_{PCLKCYC}$	TVRR=65Hz	33.3		174	ns
	$f_{PCLKCYC}$		5.8		30.0	MHz

Note 1. VDDI=1.65 to 3.3V, VDD=2.45 to 3.3V, AGND=DGND=0V, Ta=-30 to 70°C (to +85°C no damage)

Note 2. Data lines can be set to "High" or "Low" during blanking time – Don't care.

Note 3. HP is multiples of eight PCLK.

9.9.6.3 RGB Interface Mode 2 Timing Diagram

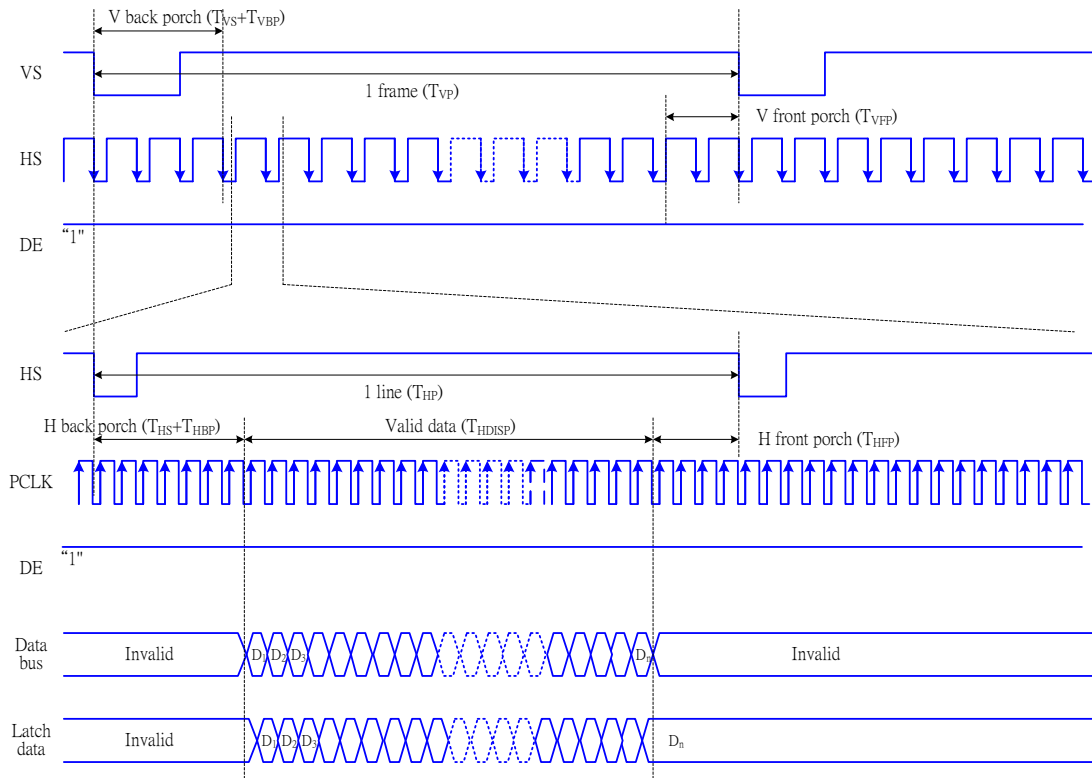


Fig. 9.9.10 RGB mode 2 timing diagram

Vertical timing for RGB I/F

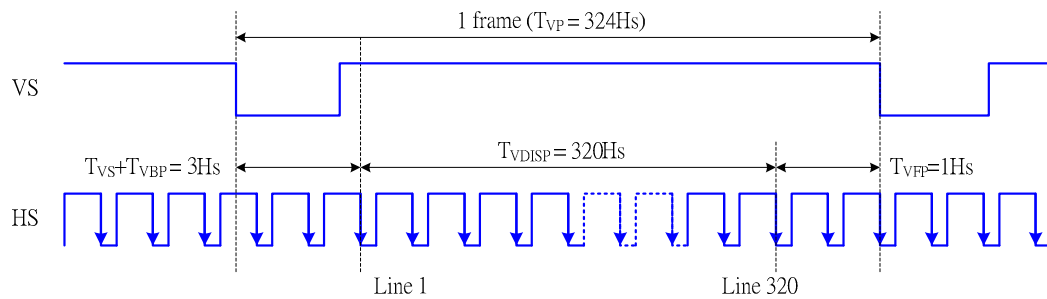


Fig. 9.9.11 RGB mode 2 vertical timing diagram

Note:  $DP=0'$ ,  $EP=0'$ ,  $HSP=0'$  and  $VSP=0'$  of RGBCTR (B0h) command.

Horizontal timing for RGB I/F

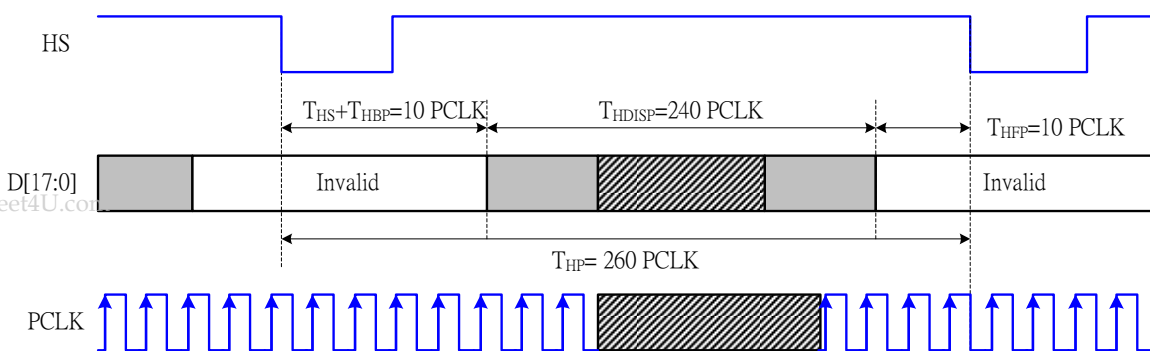


Fig. 9.9.12 RGB mode 2

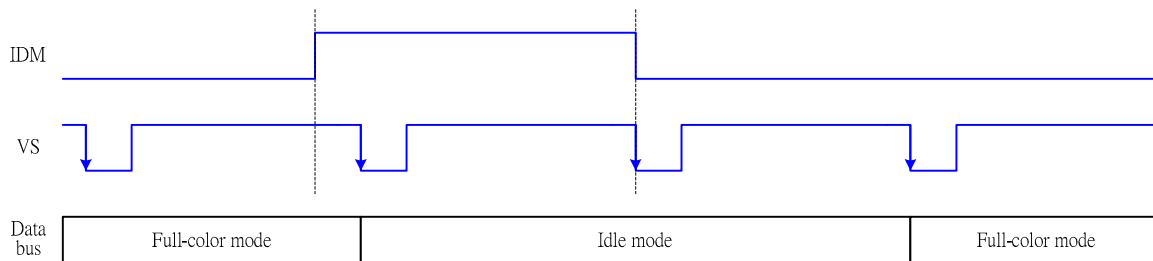
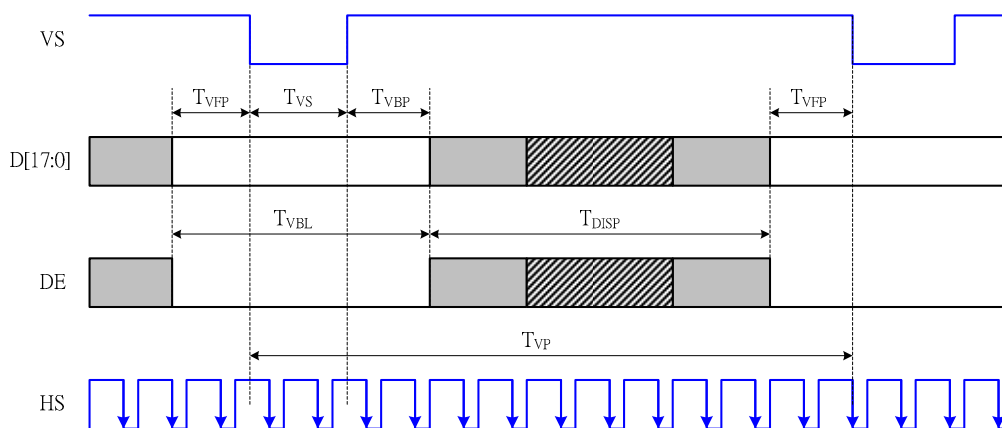


Fig. 9.9.13 RGB mode 2 idle mode timing diadram

Note:  $DP=0'$ ,  $EP=0'$ ,  $HSP=0'$  and  $VSP=0'$  of RGBCTR (B0h) command.

### Vertical timing for RGB I/F



### Horizontal timing for RGB I/F

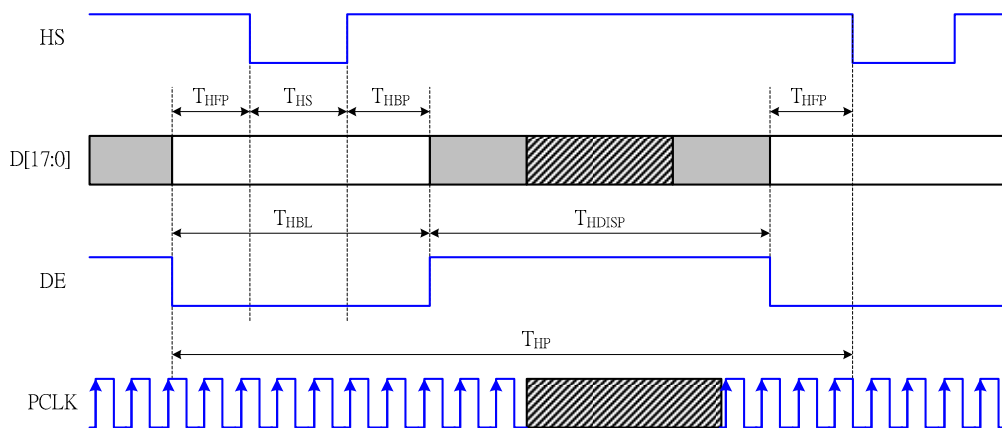


Fig. 9.9.14 Vertical and Horizontal in RGB interface

Table 9.9.6.3 Vertical and Horizontal Timing for RGB I/F

Item	Symbol	Condition	Specification			Unit
			Min	Type.	Max	
<b>Vertical Timing</b>						
Vertical cycle period	$T_{VP}$		323	324		HS
Vertical low pulse width	$T_{VS}$		1		4	HS
Vertical front porch	$T_{VFP}$		1	1	1023	HS
Vertical back porch	$T_{VBP}$		1		1023	HS
Vertical data start line		TVS + TVBP	2	3	1023	HS
Vertical blanking period	$T_{VBL}$	TVS + TVBP + TVFP	3	4	1023	HS
Vertical active area	$T_{VDISP}$			320		HS
Vertical refresh rate	TVRR	Frame rate	61.75	65	68.25	Hz
<b>Horizontal Timing</b>						
Horizontal cycle period	$T_{HP}$		243	260	511	PCLK
Horizontal low pulse width	$T_{HS}$		1		63	PCLK
Horizontal front porch	$T_{HFP}$		1		63	PCLK
Horizontal back porch	$T_{HBP}$		1		63	PCLK
Horizontal data start point		THS + THBP	1	10	63	PCLK
		ff HS + fHBP	0.196			us
Horizontal blanking period	$T_{HBL}$		3	20	256	PCLK
Horizontal active area	$T_{HDISP}$			240		PCLK
Pixel clock cycle	$T_{PCLKCYC}$	TVRR=65Hz	33.3	182	196	ns
	$f_{PCLKCYC}$		5.1	5.48	30	MHz

Note 1. VDDI=1.65 to 3.3V, VDD=2.45 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 °C (to +85 °C no damage)

Note 2. Data lines can be set to "High" or "Low" during blanking time – Don't care.

Note 3. HP is multiples of eight PCLK.



## 9.9.6.4 Power On Sequence on RGB Mode 2

The Driver operates power up and display ON by VDD, VDDI, SHUT, VS, HS, DE, PCLK on RGB mode 2 as show as following figure.

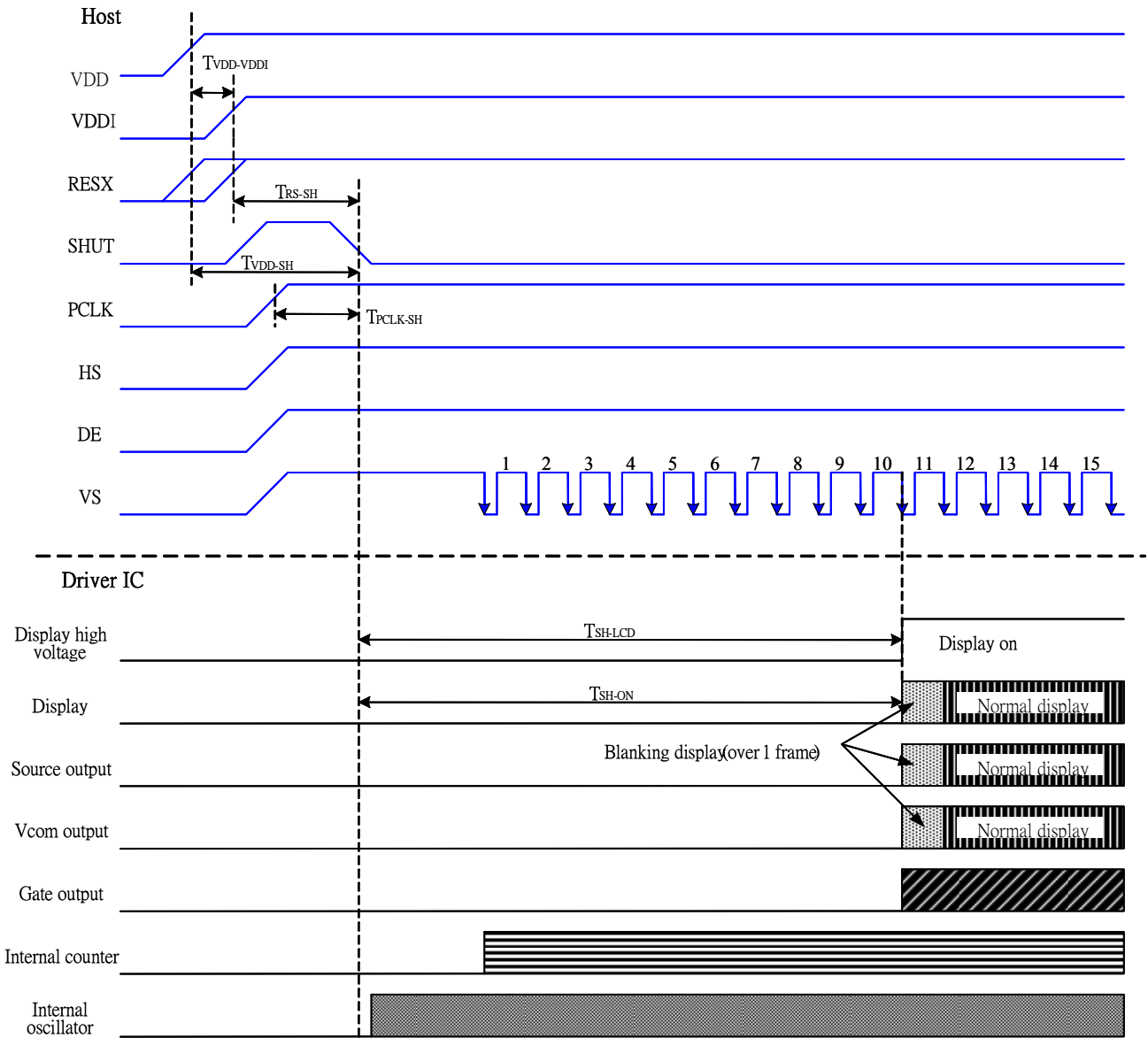


Fig. 9.9.15 Power-ON sequence in RGB mode 2

Table 9.9.6.4 Power ON AC Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit	Remark
VDD On to VDDI On	TVDD-VDDI	0			ns	
VDDI/VDD on to falling edge of SHUT	TVDD-SH	1			ms	
RESX to falling of SHUT	TRS-SH	10			us	
Signals input to falling edge of SHUT *	TCLK-SH	1			PCLK	Note1
Falling edge of SHUT to LCD power ON	TSH-LCD			120	ms	
Falling edge of SHUT to Display start	TSH-ON		10		VS	

Note 1: Signals mean VS, HS, DE and PCLK signal.

Note 2: DP='0', EP='0', HSP='0' and VSP='0' of RGBCTR (B0h) command.

## 9.9.6.5 Power OFF Sequence on RGB Mode 2

The Driver operates power off and display OFF by VDD, VDDI, SHUT, VS, HS and DE on RGB mode 2 as show as following figure.

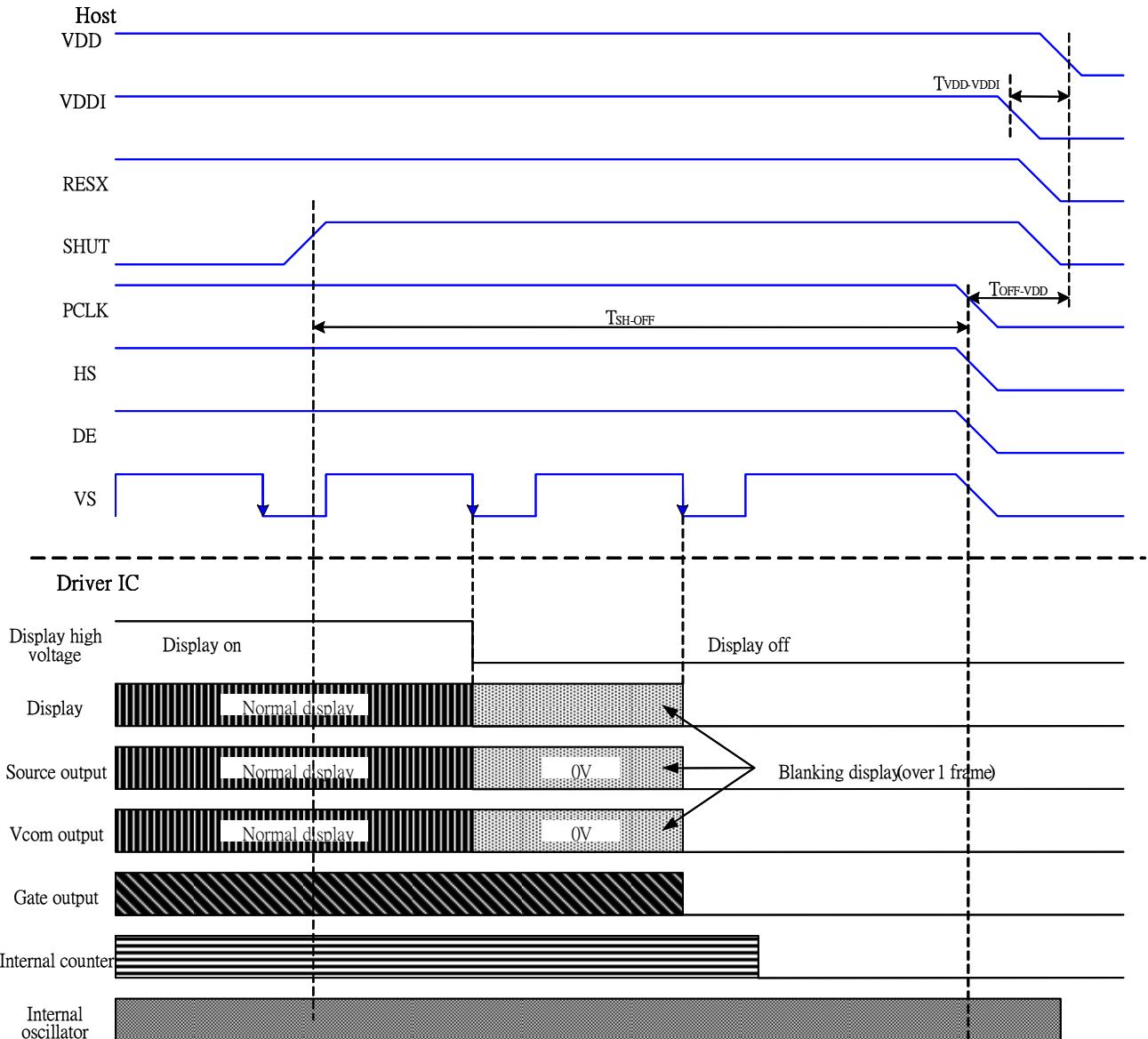


Fig. 9.9.16 Power-OFF sequence in RGB mode 2

Table 9.9.6.5 Power OFF AC Characteristics

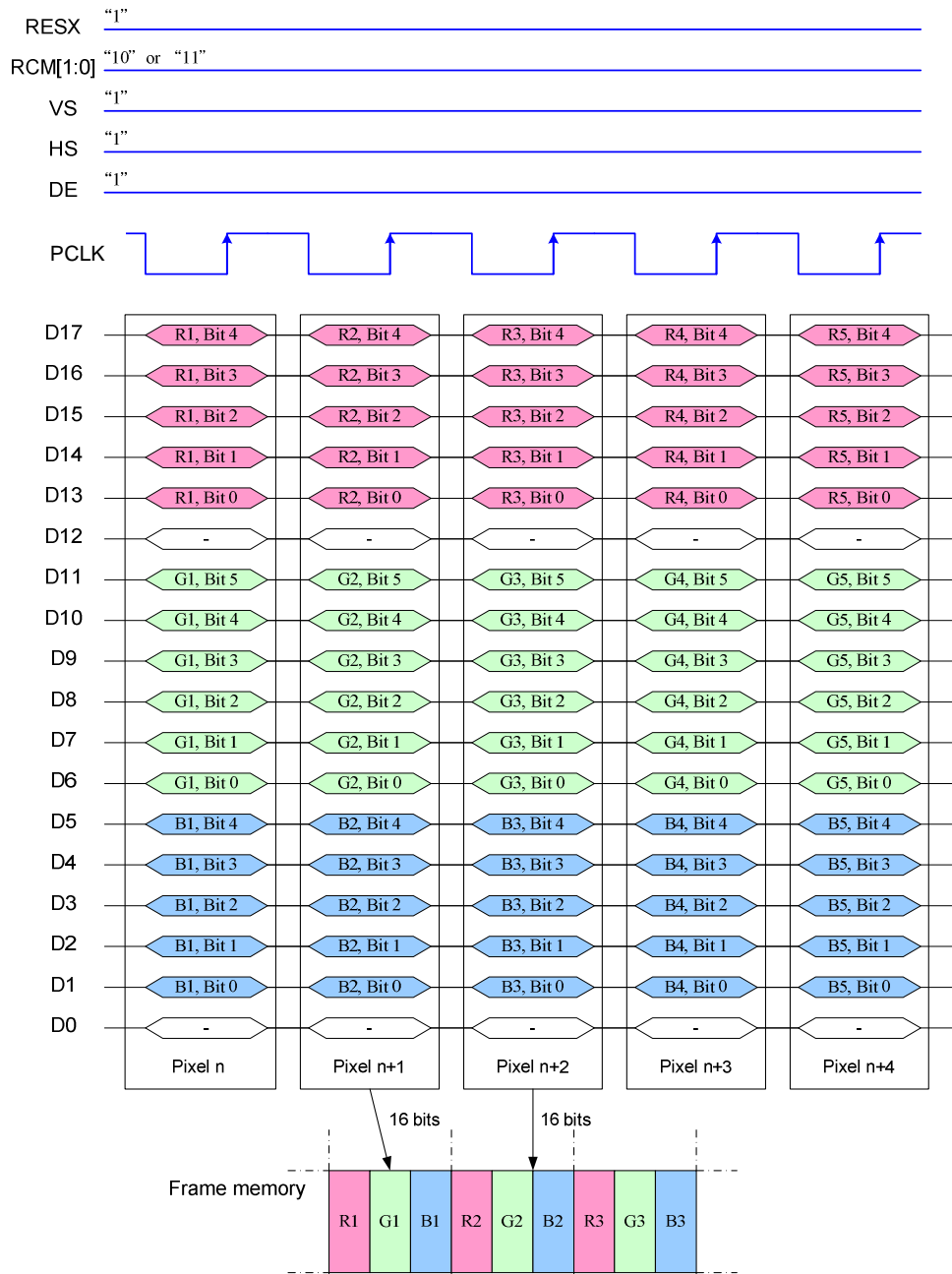
Characteristics	Symbol	Min	Typ	Max	Unit	Remark
VDDI On to VDD On	TVDD-VDDI	0			ns	
Signals input to VDDI/VDD off	TSH-OFF	1			us	Note1
Rising edge of SHUT to Display off	TSH-OFF	2			VS	

Note 1: Signals mean VS, HS, DE and PCLK signal.

Note 2: DP='0', EP='0', HSP='0' and VSP='0' of RGBCTR (B0h) command.

## 9.9.7 RGB Data Color Coding

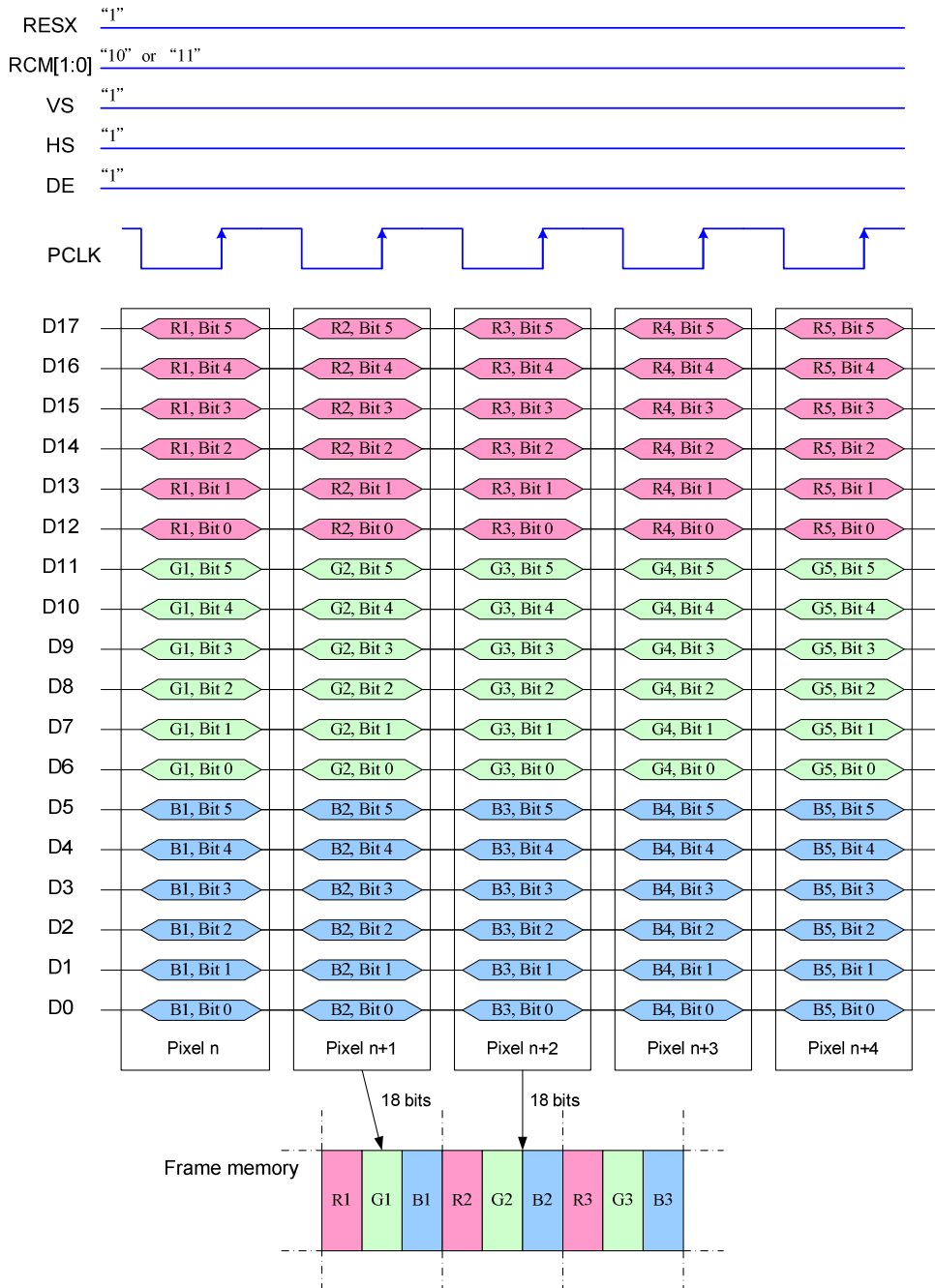
### 9.9.7.1 16-bit/pixel Color Order on the RGB Interface



Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit5, LSB=Bit0 for Green data and MSB=Bit4, LSB=Bit0 for Red and Blue data.

Note 2: '-' Don't care, but need set to VDDI or DGND level.

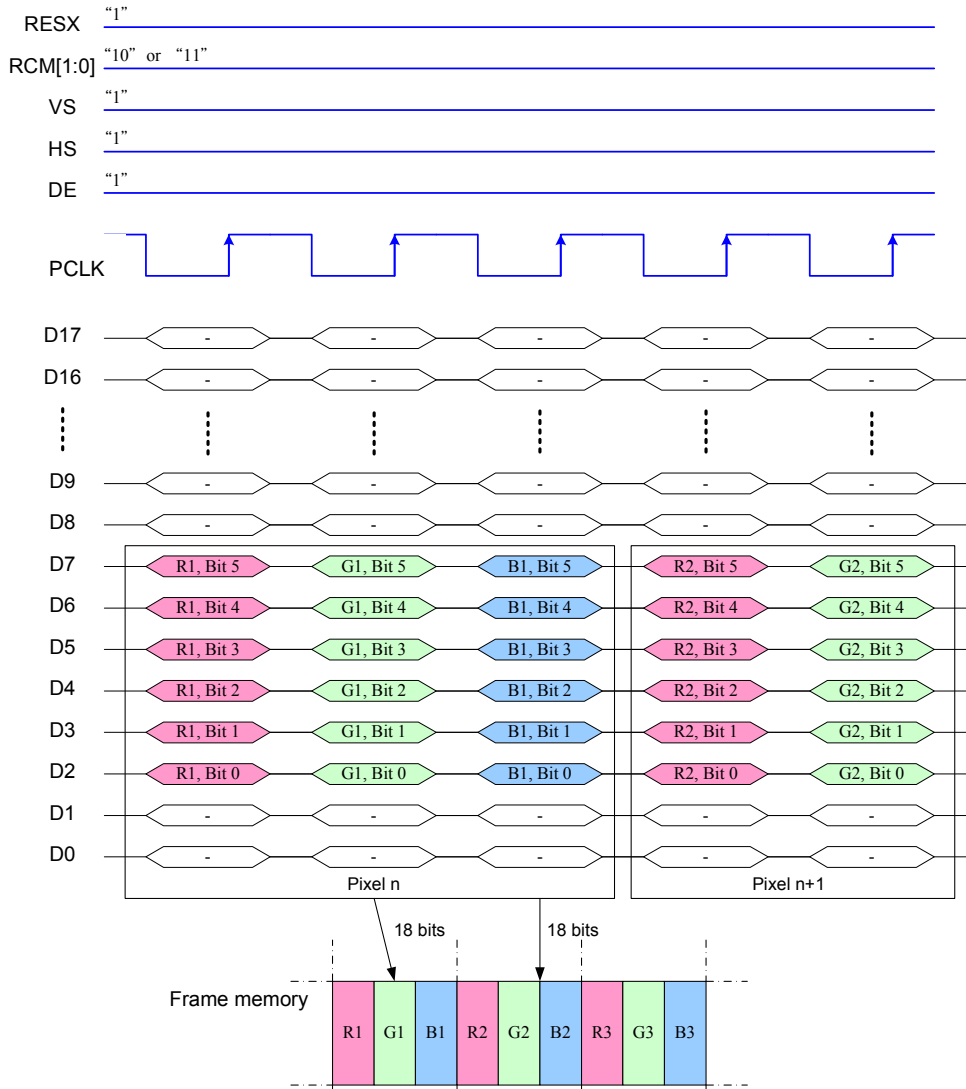
## 9.9.7.2 18-bit/pixel Color Order on the RGB Interface



Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit5, LSB=Bit0 for Red, Green and Blue data.

Note 2: '-' Don't care, but need set to VDDI or DGND level.

## 9.9.7.3 6-bit/pixel Color Order on the RGB Interface



Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit5, LSB=Bit0 for Red, Green and Blue data.

Note 2: '-' Don't care, but need set to VDDI or DGND level.

## 9.10 Display Data RAM

### 9.10.1 Configuration

The display module has an integrated 240x320x18-bit graphic type static RAM. This 1382,400-bit memory allows to store on-chip a 240xRGBx320 image with an 18-bpp resolution (262K-color).

There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

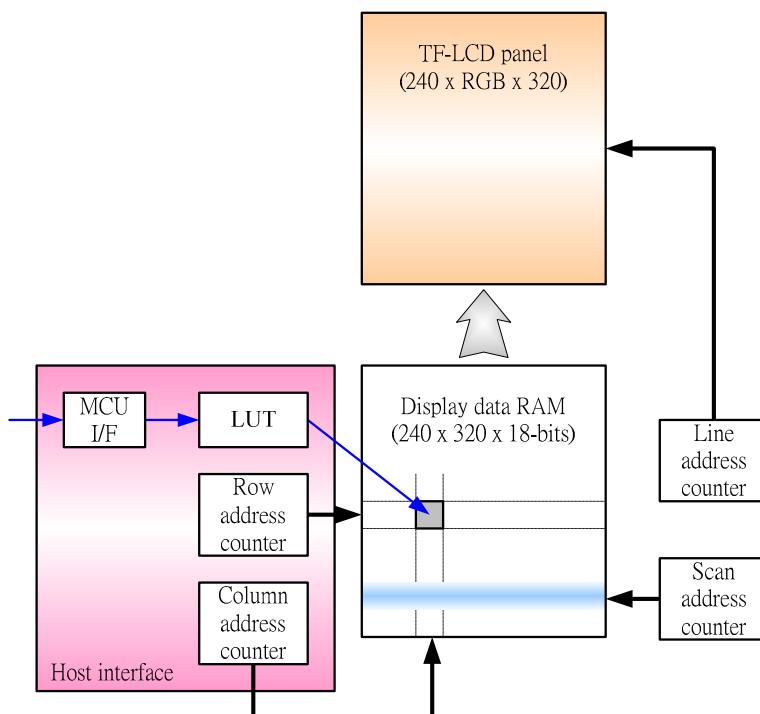
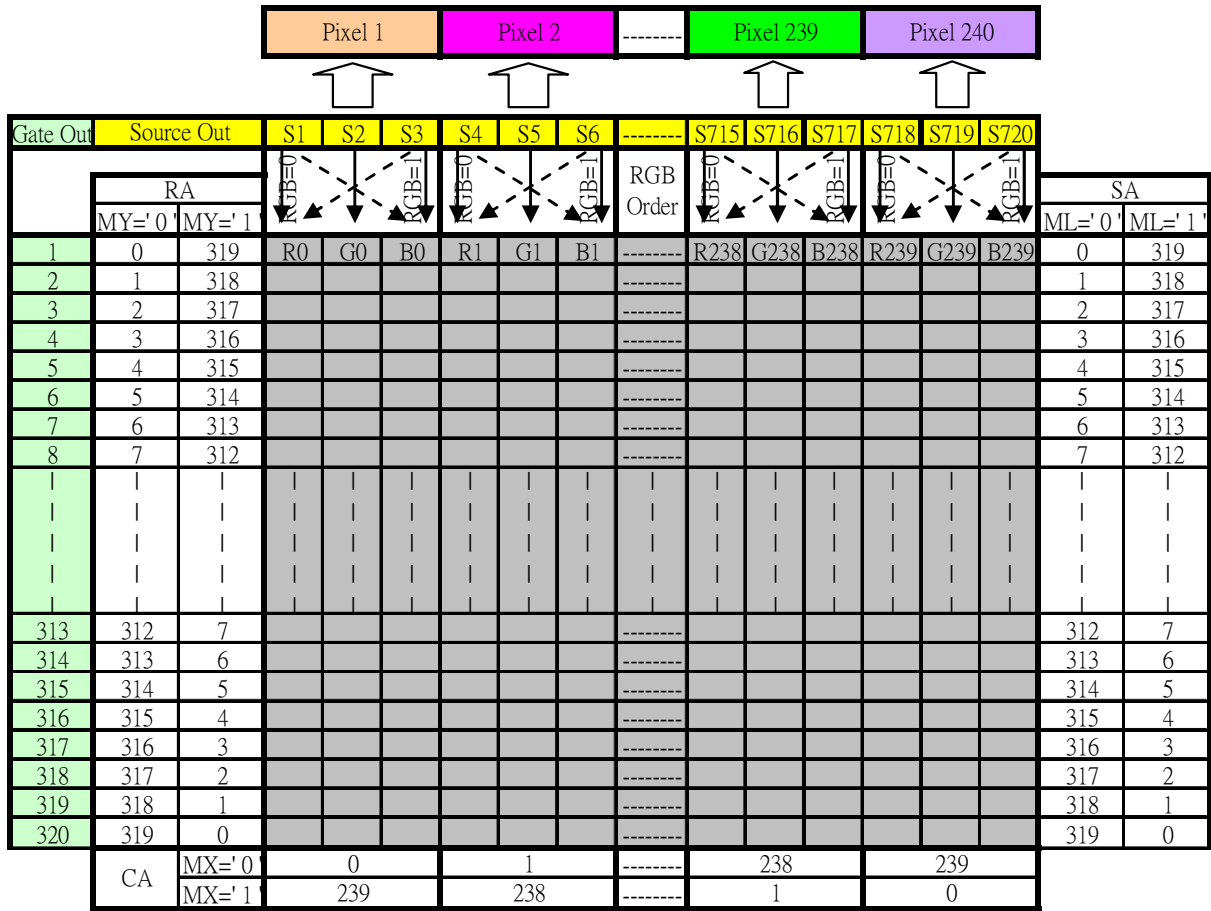


Fig. 9.10.1 Display data RAM organization

## 9.10.2 Memory to Display Address Mapping

### 9.10.2.1 When using 240RGB x 320 resolution (SMX=SMY=SRGB='0')



Note  
 RA = Row Address,  
 CA = Column Address  
 SA = Scan Address  
 MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command  
 MY = Mirror Y-axis (Row address direction parameter), D7 parameter of MADCTL command  
 MV = Scan direction parameter, D4 parameter of MADCTL command  
 RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

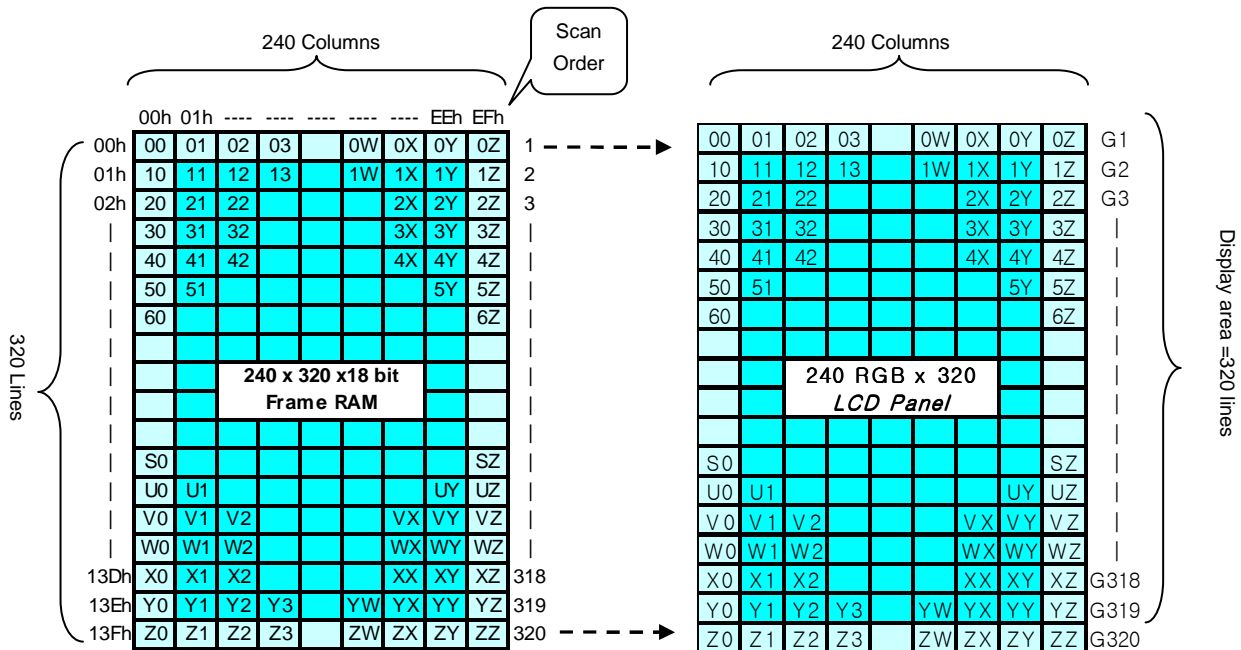
## 9.10.3 Normal Display On or Partial Mode On, Vertical Scroll Off

### 9.10.3.4 When using 240RGB x 320 resolution

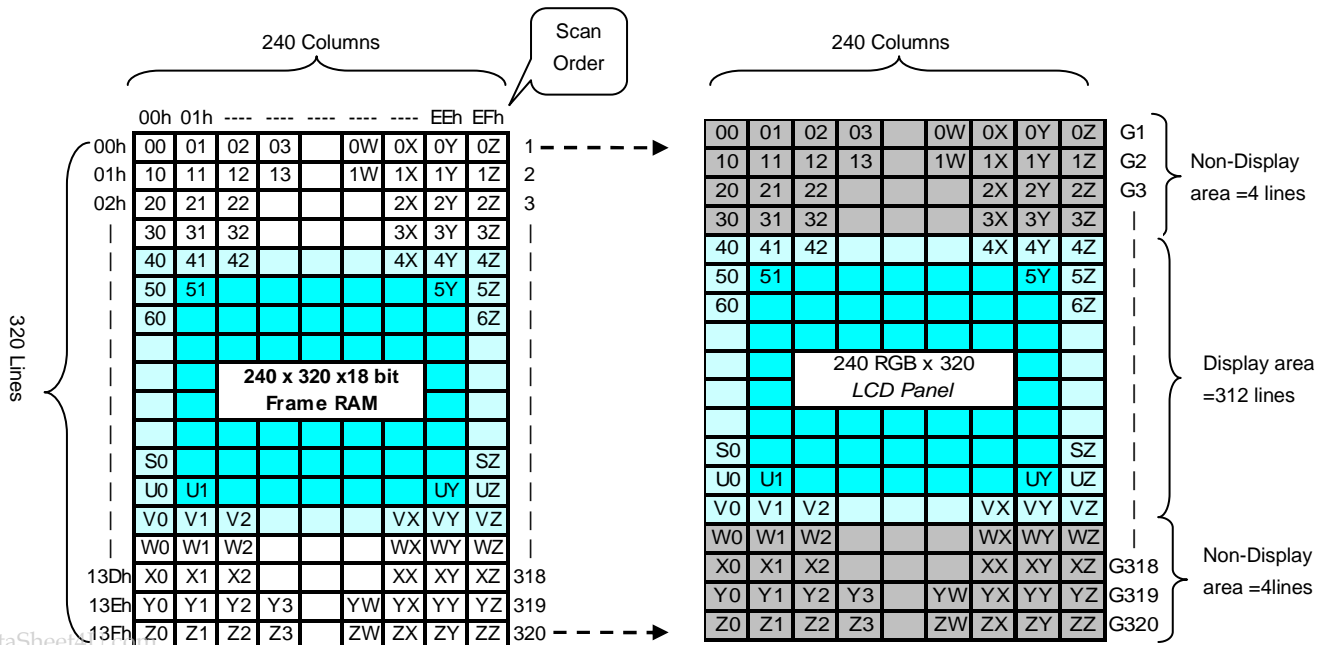
In this mode, contents of the frame memory within an area where column pointer is 00h to EFh and page pointer is 00h to 13Fh is displayed.

To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

#### 1). Example for Normal Display On (MX=MY=ML='0', SMX=SMY='0')



#### 2). Example for Partial Display On (PSL[7:0]=04h, PEL[7:0]=13Bh, MX=MV=ML='0', SMX=SMY='0')





## 9.10.4 Vertical Scroll Mode

There is vertical scrolling, which are determined by the commands "Vertical Scrolling Definition" (33h) and Vertical Scrolling Start Address" (37h).

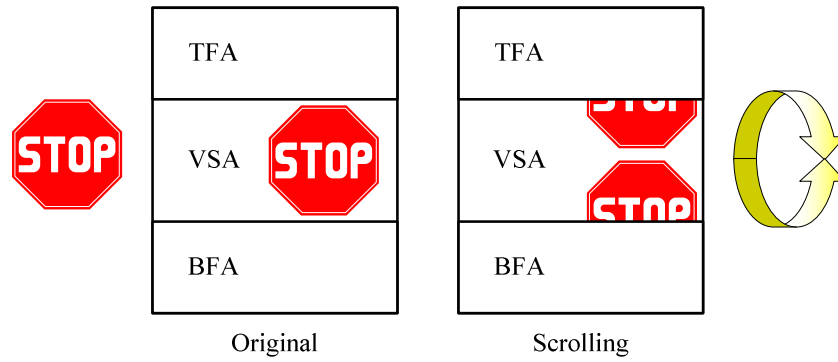
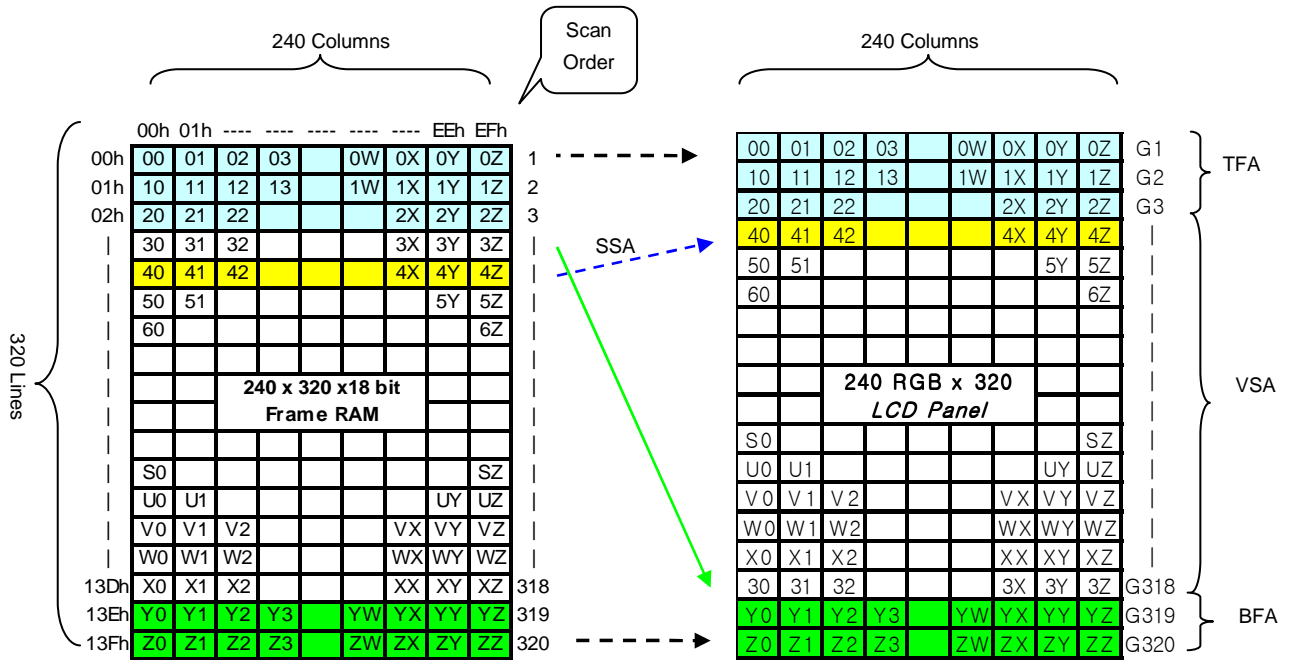


Fig. 9.10.2 Difference between Scrolling and original

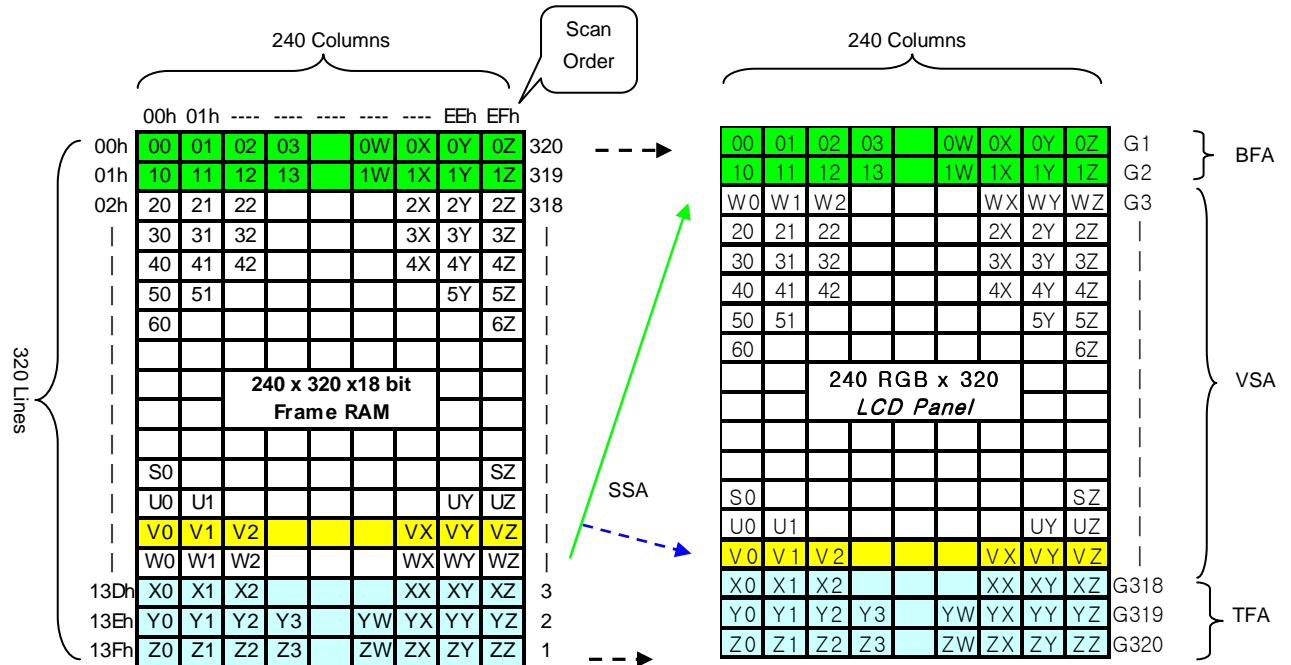
## 9.10.4.1 When using 240RGB x 320 resolution

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA)=320. In this case, scrolling is applied as shown below.

### 1). Example for TFA =3, VSA=315, BFA=2, SSA=4, ML=0: Scrolling



### 2). Example for TFA =3, VSA=315, BFA=2, SSA=4, ML=1: Scrolling: TFA and BFT are exchanged



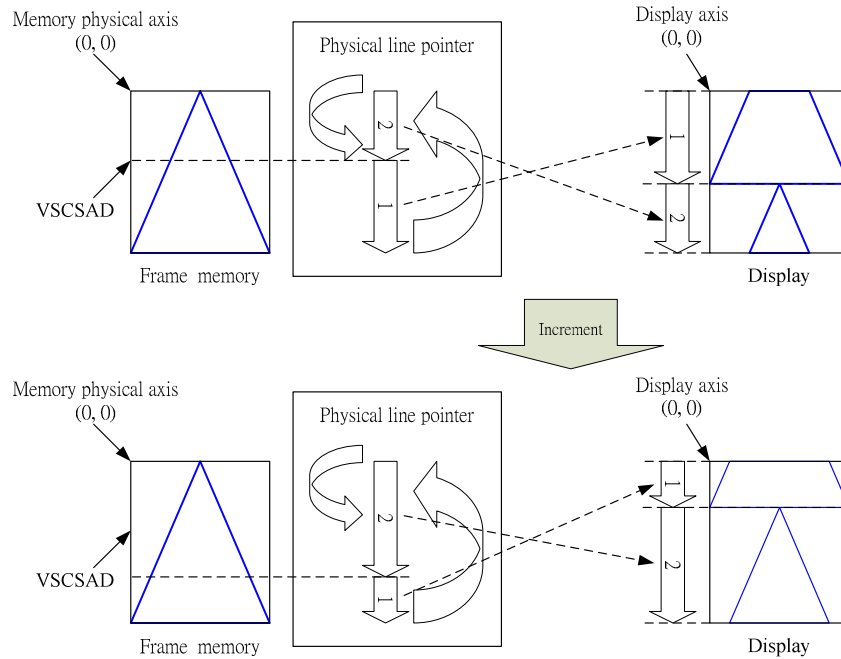
9.10.5 Vertical Scroll Example

Case 1: TFA + VSA + BFA ≠ 320

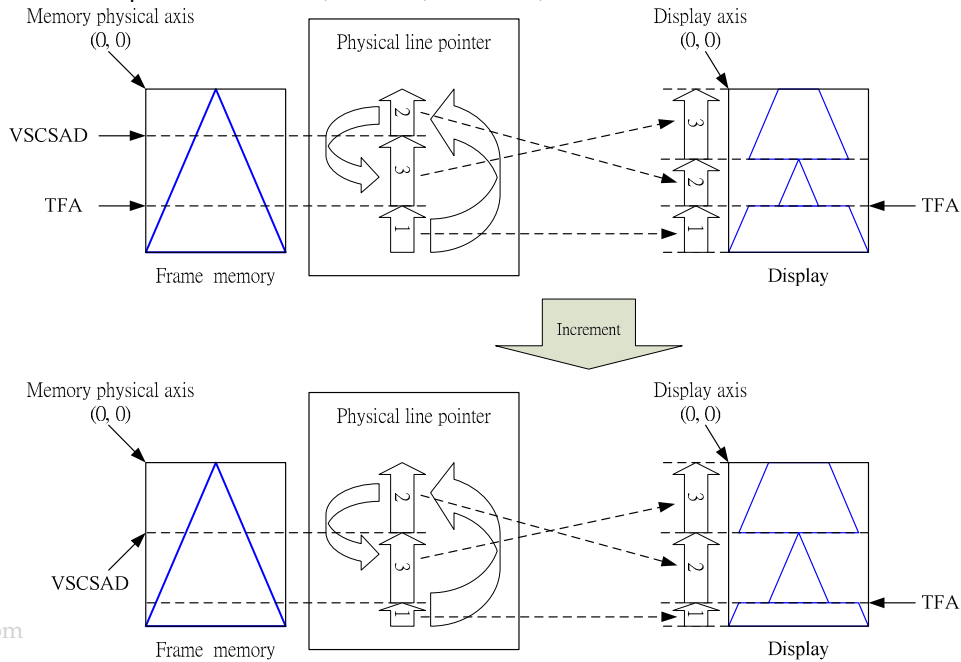
N/A. Do not set TFA + VSA + BFA ≠ 320. In that case, unexpected picture will be shown.

Case 2: TFA + VSA + BFA=320 (Scrolling)

Example1) When MADCTL parameter ML="0", TFA=0, VSA=320, BFA=0 and VSCSAD=80.



Example2) When MADCTL parameter ML="1", TFA=30, VSA=290, BFA=0 and VSCSAD=80.



## 9.11 Address Counter

The address counter sets the addresses of the display data RAM for writing and reading.

Data is written pixel-wise into the RAM matrix of DRIVER. The data for one pixel or two pixels is collected (RGB 6-6-6-bit), according to the data formats. As soon as this pixel-data information is complete the "Write access" is activated on the RAM. The locations of RAM are addressed by the address pointers. The address ranges are X=0 to X=239 (EFh) and Y=0 to Y=319 (13Fh). Addresses outside these ranges are not allowed. Before writing to the RAM a window must be defined into which will be written. The window is programmable via the command registers XS, YS designating the start address and XE, YE designating the end address.

For example the whole display contents will be written, the window is defined by the following values: XS=0 (0h) YS=0 (0h) and XE=239 (EFh), YE=319 (13Fh).

In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (V=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to XS and Y increments to address the next row. After the every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS).

For flexibility in handling a wide variety of display architectures, the commands "CASET, RASET" and "MADCTL" (see section 10 command list), define flags MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Section 9.12 show the available combinations of writing to the display RAM. When MX, MY and MV will be changed the data must be rewritten to the display RAM.

For each image condition, the controls for the column and row counters apply as section. 9.12 below:

Condition	Column Counter	Row Counter
When RAMWR/RAMRD command is accepted	Return to "Start Column (XS)"	Return to "Start Row (YS)"
Complete Pixel Read / Write action	Increment by 1	No change
The Column counter value is larger than "End Column (XE)"	Return to "Start Column (XS)"	Increment by 1
The Column counter value is larger than "End Column (XE)" and the Row counter value is larger than "End Row (YE)"	Return to "Start Column (XS)"	Return to "Start Row (YS)"

## 9.12. Memory Data Write/ Read Direction

The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by "Memory Data Access Control" Command, bits B5 (MV), B6 (MX), B7 (MY) as described below.

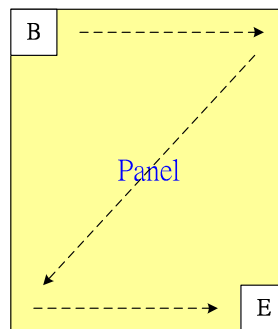
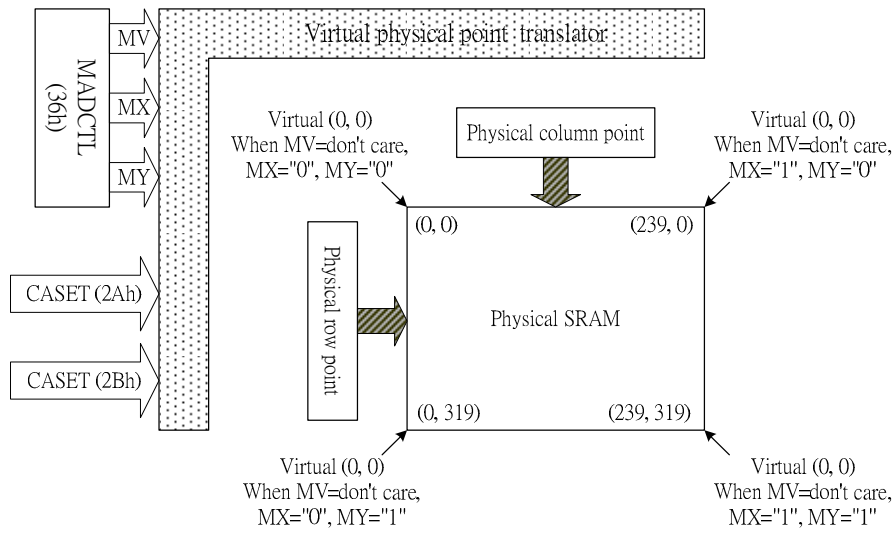


Fig. 9.12.1 Data streaming order

## 9.12.1 When 240RGBx320



MV	MX	MY	CASET	RASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Row Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (319-Physical Row Pointer)
0	1	0	Direct to (239-Physical Column Pointer)	Direct to Physical Row Pointer
0	1	1	Direct to (239-Physical Column Pointer)	Direct to (319-Physical Row Pointer)
1	0	0	Direct to Physical Row Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (319-Physical Row Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Row Pointer	Direct to (239-Physical Column Pointer)
1	1	1	Direct to (319-Physical Row Pointer)	Direct to (239-Physical Column Pointer)

Note: Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MADCTL bits B7 (MY), B6 (MX), B5 (MV). The write order for each pixel unit is

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

One pixel unit represents 1 column and 1page counter value on the Frame Memory.

9.12.2 Frame Data Write Direction According to the MADCTL parameters (MV, MX and MY)

Display Data Direction	MADCTL Parameter			Image in the Host (MPU)	Image in the Driver (DDRAM)
	MV	MX	MY		
Normal	0	0	0		<p>H/W position (0,0) → </p> <p>X-Y address (0,0) X: CASET Y: RASET</p>
Y-Mirror	0	0	1		<p>H/W position (0,0) → </p> <p>X-Y address (0,0) X: CASET Y: RASET</p>
X-Mirror	0	1	0		<p>H/W position (0,0) → </p> <p>X-Y address (0,0) X: CASET Y: RASET</p>
X-Mirror Y-Mirror	0	1	1		<p>H/W position (0,0) → </p> <p>X-Y address (0,0) X: CASET Y: RASET</p>
X-Y Exchange	1	0	0		<p>H/W position (0,0) → </p> <p>X-Y address (0,0) X: RASET Y: CASET</p>
X-Y Exchange Y-Mirror	1	0	1		<p>H/W position (0,0) → </p> <p>X-Y address (0,0) X: RASET Y: CASET</p>
X-Y Exchange X-Mirror	1	1	0		<p>H/W position (0,0) → </p> <p>X-Y address (0,0) X: RASET Y: CASET</p>
X-Y Exchange X-Mirror Y-Mirror	1	1	1		<p>H/W position (0,0) → </p> <p>X-Y address (0,0) X: RASET Y: CASET</p>

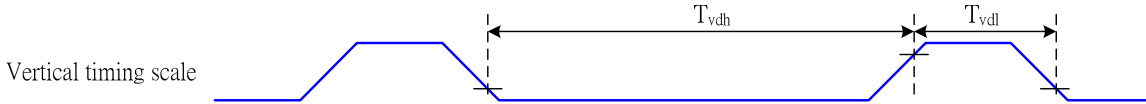
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## 9.13 Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

### 9.13.1 Tearing Effect Line Modes

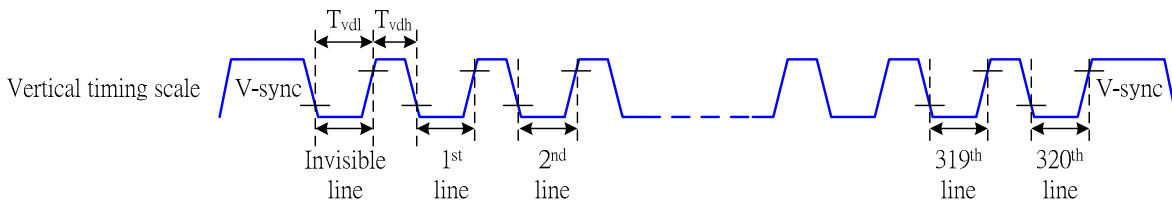
**Mode 1**, the Tearing Effect Output signal consists of V-Blanking Information only:



$tvdh$ = The LCD display is not updated from the Frame Memory

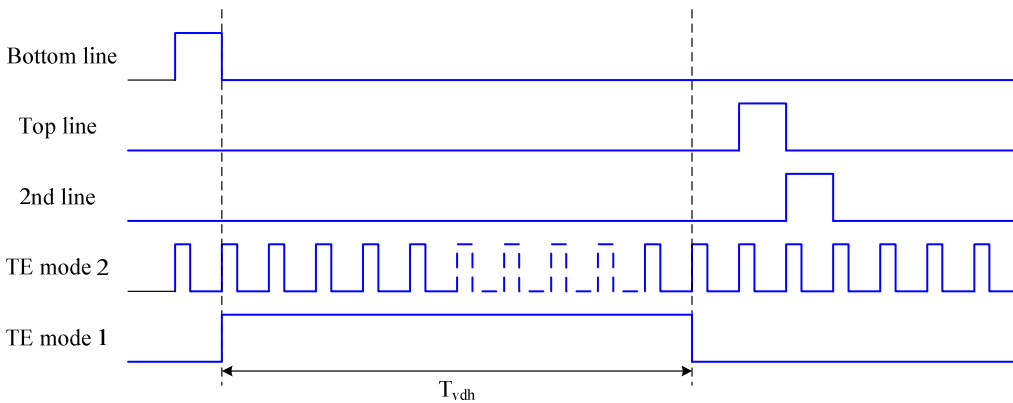
$tvdI$ = The LCD display is updated from the Frame Memory (except Invisible Line – see below)

**Mode 2**, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 320 H-sync pulses per field.



$thdh$ = The LCD display is not updated from the Frame Memory

$thdl$ = The LCD display is updated from the Frame Memory (except Invisible Line – see above)



Note: During Sleep In Mode, the Tearing Output Pin is active Low.

## 9.13.2 Tearing Effect Line Timings

The Tearing Effect signal is described below:

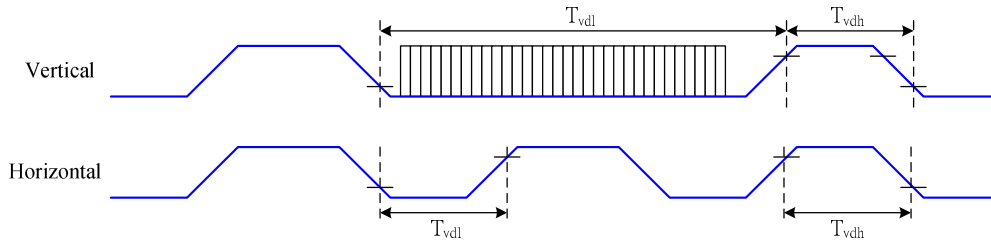
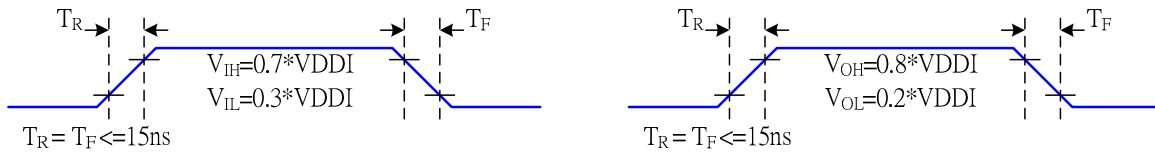


Table 9.13.1 AC characteristics of Tearing Effect Signal Idle Mode Off (Frame Rate = 58.9 Hz)

Symbol	Parameter	min	max	unit	description
$t_{vdl}$	Vertical Timing Low Duration	13	-	ms	
$t_{vdh}$	Vertical Timing High Duration	1000	-	$\mu$ s	
$t_{hdl}$	Horizontal Timing Low Duration	33	-	$\mu$ s	
$t_{hdh}$	Horizontal Timing High Duration	25	500	$\mu$ s	

NOTE: The timings in Table 9.3.1 apply when MADCTL ML=0 and ML=1

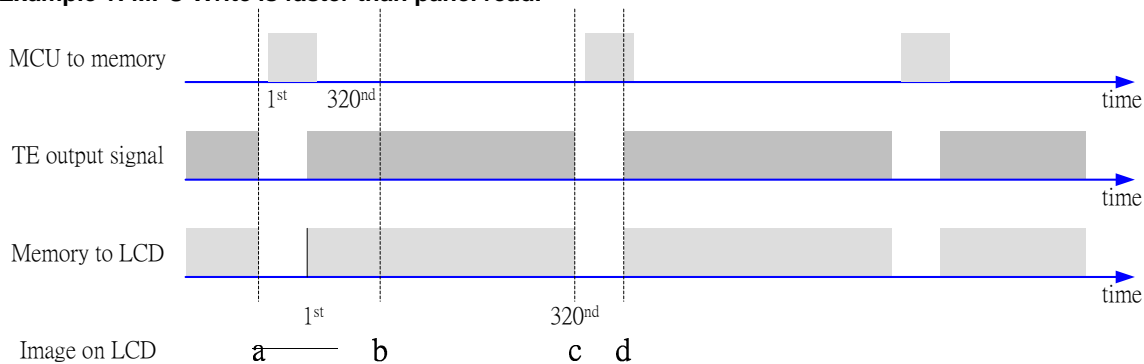
The signal's rise and fall times ( $t_f$ ,  $t_r$ ) are stipulated to be equal to or less than 15ns.



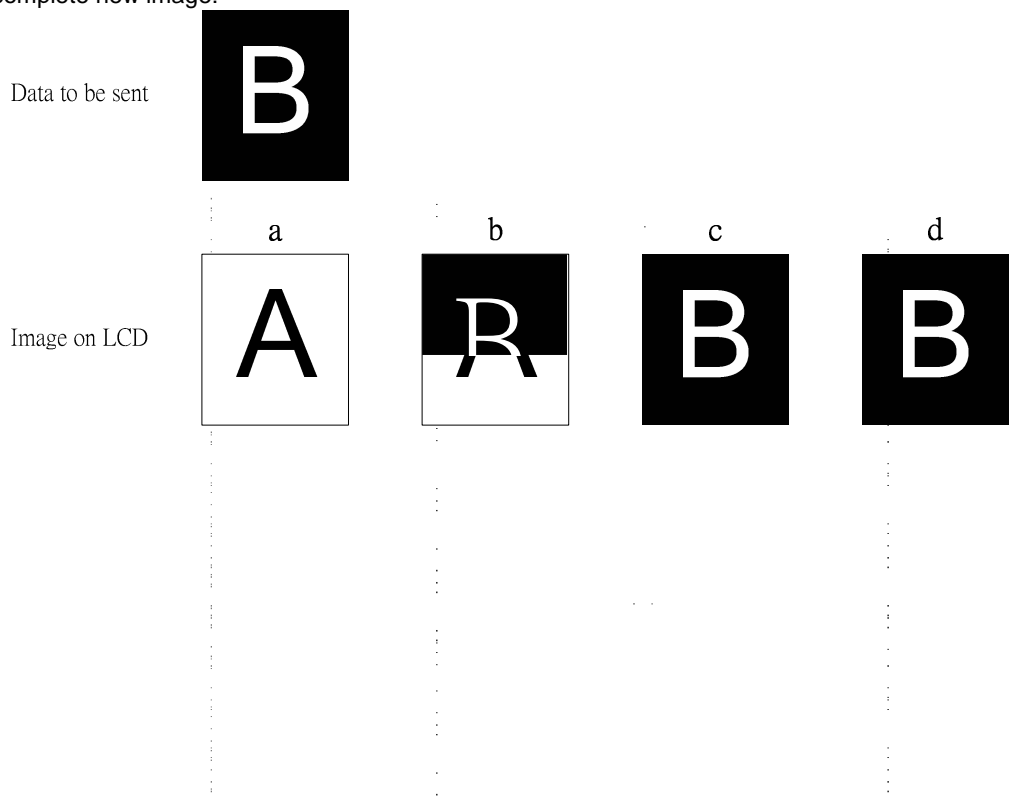
The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:



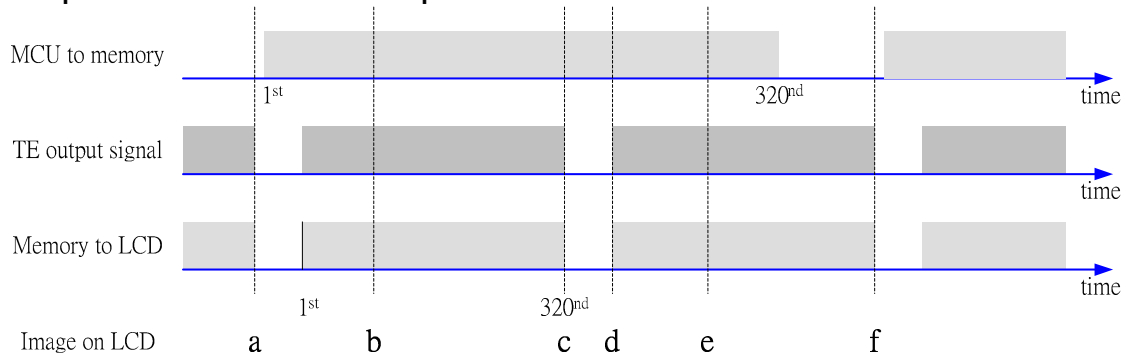
### 9.13.3 Example 1: MPU Write is faster than panel read.



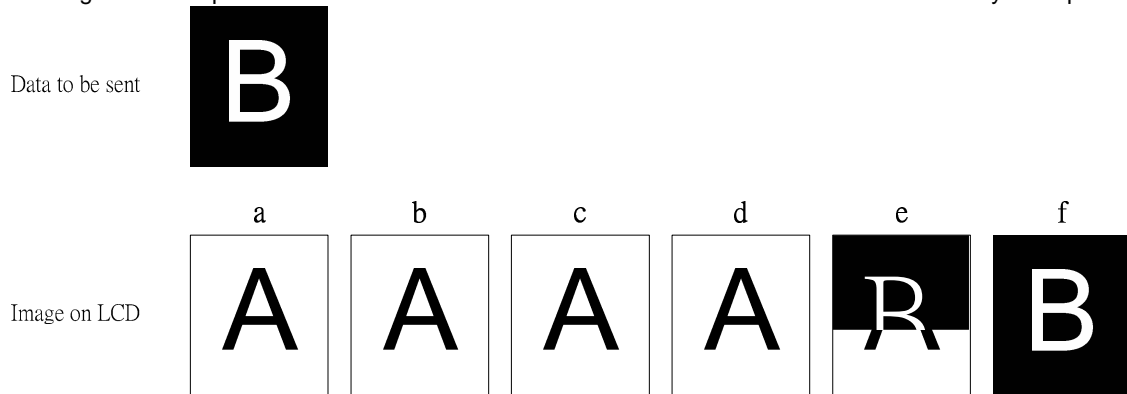
Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:



## 9.13.4 Example 2: MPU write is slower than panel read.



The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MPU to Frame memory write position.

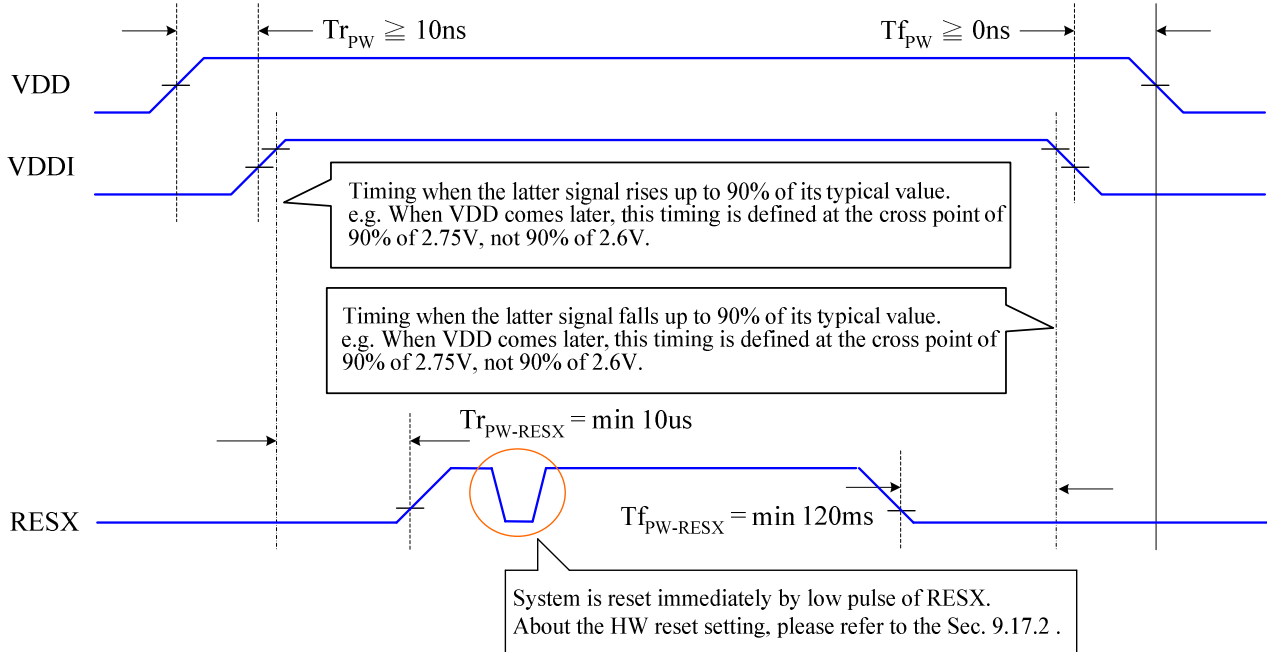


## 9.14 Preset Values

ST7787 will set preset values on our production line for each display module. Any of these preset values do not need customer's SW support.

## 9.15 Power ON/OFF Sequence

The power on/off sequence is illustrated below:



### 9.15.1 Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface.

2. At an uncontrolled power off the display will go blank and there will not be any visible effects within (TBD) second on the display (blank display) and remains blank until "Power On Sequence" powers it up.

## 9.16 Power Level Definition

### 9.16.1 Power Level

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

**1. Normal Mode On (full display), Idle Mode Off, Sleep Out.**

In this mode, the display is able to show maximum 262,144 colors.

**2. Partial Mode On, Idle Mode Off, Sleep Out.**

In this mode part of the display is used with maximum 262,144 colors.

**3. Normal Mode On (full display), Idle Mode On, Sleep Out.**

In this mode, the full display area is used but with 8 colors.

**4. Partial Mode On, Idle Mode On, Sleep Out.**

In this mode, part of the display is used but with 8 colors.

**5. Sleep In Mode**

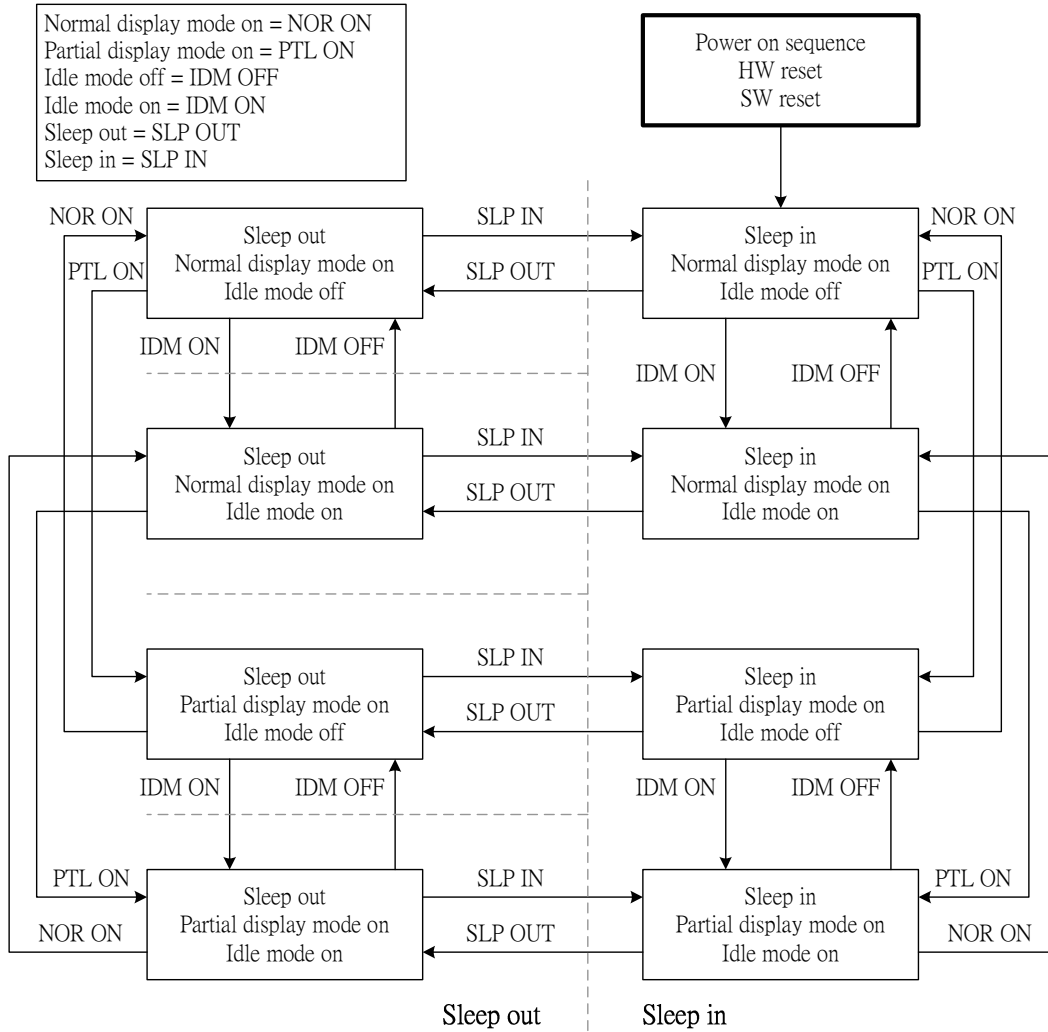
In this mode, the DC: DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDDI power supply. Contents of the memory are safe.

**6. Power Off Mode**

In this mode, both VDD and VDDI are removed.

*Note: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.*

9.16.2 Power Flow Chart



Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.  
 Note 2: There is not any limitation, which is not specified by this spec, when there is changing from one power mode to another power mode.

## 9.17 Reset

### 9.17.1 Reset Table (240RGB x320)

Item	After Power On	After Hardware Reset	After Software Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display On/Off	Off	Off	Off
Display mode (normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
VSYNCIN	On	On	On
VSYNCOUT	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column: Start Address (XS)	0000h	0000h	0000h
Column: End Address (XE)	00Efh	00EFh	00EFh (239d) (when MV=0) 013Fh (319d) (when MV=1)
Row: Start Address (YS)	0000h	0000h	0000h
Row: End Address (YE)	013Fh	013Fh	013Fh (319d) (when MV=0) 00EFh (239d) (when MV=1)
Gamma setting	GC0	GC0	GC0
RGB for 4k and 65k Color Mode	See Section 9.19	See Section 9.19	No Change
Partial: Start Address (PSL)	0000h	0000h	0000h
Partial: End Address (PEL)	013Fh	013Fh	013Fh
Scroll: Vertical scrolling	Off	Off	Off
Scroll: Top Fixed Area (TFA)	0000h	0000h	0000h
Scroll: Scroll Area (VSA)	0140h	0140h	0140h
Scroll: Bottom Fixed Area (BFA)	0000h	0000h	0000h
Scroll Start Address (SSA)	0000h	0000h	0000h
Tearing: On/Off	Off	Off	Off
Tearing Effect Mode *3)	0 (Mode1)	0 (Mode1)	0 (Mode1)
Memory Data Access Control (MY/MX/MV/ML/RGB)	0/0/0/0/0	0/0/0/0/0	No Change
Interface Pixel Color Format	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDPM	08h	08h	08h
RDDMADCTL	00h	00h	No Change
RDDCOLMOD	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
RDDSDR	00h	00h	00h
ID1	38h	38h	38h
ID2	NV value	NV value	NV value
ID3	NV value	NV value	NV value

Notes 1. There will be no abnormal visible effects on the display when S/W or H/W Reset is applied.

Notes:2. Powered-On Reset finishes within 10μs after both VDD & VDDI are applied.

Notes:3. TE Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

## 9.17.2 Module Input/Output Pins

### 9.17.2.1 Output or Bi-directional (I/O) Pins

Output or Bi-directional pins	After Power On	After Hardware Reset	After Software Reset
TE	Low	Low	Low
D7 to D0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)

*Note: There will be no output from D7-D0 during Power On/Off sequence, Hardware Reset and Software Reset.*

### 9.17.2.2 Input Pins

Input pins	During Power On Process	After Power On	After Hardware Reset	After Software Reset	During Power Off Process
RESX	See 9.15	Input valid	Input valid	Input valid	See 9.15
CSX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D/CX	Input invalid	Input valid	Input valid	Input valid	Input invalid
WRX	Input invalid	Input valid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D7 to D0	Input invalid	Input valid	Input valid	Input valid	Input invalid
P/SX	Input invalid	Input valid	Input valid	Input valid	Input invalid

## 9.17.3 Reset Timing

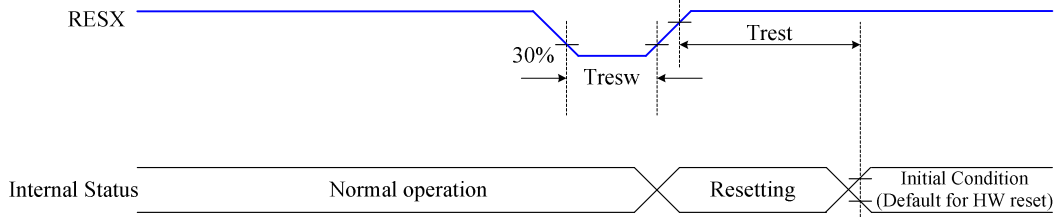


Table 9.18.3.1 Reset input timing

VSS=0V, VDDI=1.65V to 1.95V, VDD=2.45V to 2.9V, Ta = -30 to 70°C)

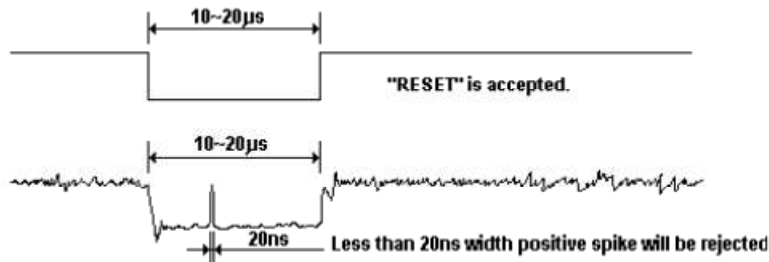
Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t <sub>RESW</sub>	*1) Reset low pulse width	RESX	30	-	-	-	us
t <sub>REST</sub>	*2) Reset complete time	-	120	-	-	-	ms

Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

Note 3. During Reset Complete Time, ID2 and VCOMOF value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (t<sub>REST</sub>) within 120ms after a rising edge of RESX.

Note 4. Spike Rejection also applies during a valid reset pulse as shown below:





## 9.18 Color Depth Conversion Look Up Tables

### 9.18.1 4096 and 65536 Color to 262,144 Color

Color	Look Up Table Outputs Frame Memory Data (6-bit)	Default value after H/W Reset	RGBSET Parameter	Look Up Table Input Data	
				4k Color	65k Color
RED	R005 R004 R003 R002 R001 R000	000000	1	0000	00000
	R015 R014 R013 R012 R011 R010	000011	2	0001	00001
	R025 R024 R023 R022 R021 R020	000101	3	0010	00010
	R035 R034 R033 R032 R031 R030	000111	4	0011	00011
	R045 R044 R043 R042 R041 R040	001001	5	0100	00100
	R055 R054 R053 R052 R051 R050	001011	6	0101	00101
	R065 R064 R063 R062 R061 R060	001101	7	0110	00110
	R075 R074 R073 R072 R071 R070	001111	8	0111	00111
	R085 R084 R083 R082 R081 R080	010001	9	1000	01000
	R095 R094 R093 R092 R091 R090	010011	10	1001	01001
	R105 R104 R103 R102 R101 R100	010101	11	1010	01010
	R115 R114 R113 R112 R111 R110	010111	12	1011	01011
	R125 R124 R123 R122 R121 R120	011001	13	1100	01100
	R135 R134 R133 R132 R131 R130	011011	14	1101	01101
	R145 R144 R143 R142 R141 R140	011101	15	1110	01110
	R155 R154 R153 R152 R151 R150	011111	16	1111	01111
	R165 R164 R163 R162 R161 R160	100001	17	Not Used	10000
	R175 R174 R173 R172 R171 R170	100011	18		10001
	R185 R184 R183 R182 R181 R180	100101	19		10010
	R195 R194 R193 R192 R191 R190	100111	20		10011
	R205 R204 R203 R202 R201 R200	101001	21		10100
	R215 R214 R213 R212 R211 R210	101011	22		10101
	R225 R224 R223 R222 R221 R220	101101	23		10110
	R235 R234 R233 R232 R231 R230	101111	24		10111
	R245 R244 R243 R242 R241 R240	110001	25		11000
	R255 R254 R253 R252 R251 R250	110011	26		11001
	R265 R264 R263 R262 R261 R260	110101	27		11010
	R275 R274 R273 R272 R271 R270	110111	28		11011
	R285 R284 R283 R282 R281 R280	111001	29		11100
	R295 R294 R293 R292 R291 R290	111011	30		11101
	R305 R304 R303 R302 R301 R300	111101	31		11110
	R315 R314 R313 R312 R311 R310	111111	32		11111

Color	Look Up Table Outputs Frame Memory Data (6-bit)	Default value after H/W Reset	RGBSET Parameter	Look Up Table Input Data	
				4k Color	65k Color
GREEN	G <sub>005</sub> G <sub>004</sub> G <sub>003</sub> G <sub>002</sub> G <sub>001</sub> G <sub>000</sub>	000000	33	0000	000000
	G <sub>015</sub> G <sub>014</sub> G <sub>013</sub> G <sub>012</sub> G <sub>011</sub> G <sub>010</sub>	000001	34	0001	000001
	G <sub>025</sub> G <sub>024</sub> G <sub>023</sub> G <sub>022</sub> G <sub>021</sub> G <sub>020</sub>	000010	35	0010	000010
	G <sub>035</sub> G <sub>034</sub> G <sub>033</sub> G <sub>032</sub> G <sub>031</sub> G <sub>030</sub>	000011	36	0011	000011
	G <sub>045</sub> G <sub>044</sub> G <sub>043</sub> G <sub>042</sub> G <sub>041</sub> G <sub>040</sub>	000100	37	0100	000100
	G <sub>055</sub> G <sub>054</sub> G <sub>053</sub> G <sub>052</sub> G <sub>051</sub> G <sub>050</sub>	000101	38	0101	000101
	G <sub>065</sub> G <sub>064</sub> G <sub>063</sub> G <sub>062</sub> G <sub>061</sub> G <sub>060</sub>	000110	39	0110	000110
	G <sub>075</sub> G <sub>074</sub> G <sub>073</sub> G <sub>072</sub> G <sub>071</sub> G <sub>070</sub>	000111	40	0111	000111
	G <sub>085</sub> G <sub>084</sub> G <sub>083</sub> G <sub>082</sub> G <sub>081</sub> G <sub>080</sub>	001000	41	1000	001000
	G <sub>095</sub> G <sub>094</sub> G <sub>093</sub> G <sub>092</sub> G <sub>091</sub> G <sub>090</sub>	001001	42	1001	001001
	G <sub>105</sub> G <sub>104</sub> G <sub>103</sub> G <sub>102</sub> G <sub>101</sub> G <sub>100</sub>	001010	43	1010	001010
	G <sub>115</sub> G <sub>114</sub> G <sub>113</sub> G <sub>112</sub> G <sub>111</sub> G <sub>110</sub>	001011	44	1011	001011
	G <sub>125</sub> G <sub>124</sub> G <sub>123</sub> G <sub>122</sub> G <sub>121</sub> G <sub>120</sub>	001100	45	1100	001100
	G <sub>135</sub> G <sub>134</sub> G <sub>133</sub> G <sub>132</sub> G <sub>131</sub> G <sub>130</sub>	001101	46	1101	001101
	G <sub>145</sub> G <sub>144</sub> G <sub>143</sub> G <sub>142</sub> G <sub>141</sub> G <sub>140</sub>	001110	47	1110	001110
	G <sub>155</sub> G <sub>154</sub> G <sub>153</sub> G <sub>152</sub> G <sub>151</sub> G <sub>150</sub>	001111	48	1111	001111
	G <sub>165</sub> G <sub>164</sub> G <sub>163</sub> G <sub>162</sub> G <sub>161</sub> G <sub>160</sub>	010000	49	Not Used	010000
	G <sub>175</sub> G <sub>174</sub> G <sub>173</sub> G <sub>172</sub> G <sub>171</sub> G <sub>170</sub>	010001	50		010001
	G <sub>185</sub> G <sub>184</sub> G <sub>183</sub> G <sub>182</sub> G <sub>181</sub> G <sub>180</sub>	010010	51		010010
	G <sub>195</sub> G <sub>194</sub> G <sub>193</sub> G <sub>192</sub> G <sub>191</sub> G <sub>190</sub>	010011	52		010011
	G <sub>205</sub> G <sub>204</sub> G <sub>203</sub> G <sub>202</sub> G <sub>201</sub> G <sub>200</sub>	010100	53		010100
	G <sub>215</sub> G <sub>214</sub> G <sub>213</sub> G <sub>212</sub> G <sub>211</sub> G <sub>210</sub>	010101	54		010101
	G <sub>225</sub> G <sub>224</sub> G <sub>223</sub> G <sub>222</sub> G <sub>221</sub> G <sub>220</sub>	010110	55		010110
	G <sub>235</sub> G <sub>234</sub> G <sub>233</sub> G <sub>232</sub> G <sub>231</sub> G <sub>230</sub>	010111	56		010111
	G <sub>245</sub> G <sub>244</sub> G <sub>243</sub> G <sub>242</sub> G <sub>241</sub> G <sub>240</sub>	011000	57		011000
	G <sub>255</sub> G <sub>254</sub> G <sub>253</sub> G <sub>252</sub> G <sub>251</sub> G <sub>250</sub>	011001	58		011001
	G <sub>265</sub> G <sub>264</sub> G <sub>263</sub> G <sub>262</sub> G <sub>261</sub> G <sub>260</sub>	011010	59		011010
	G <sub>275</sub> G <sub>274</sub> G <sub>273</sub> G <sub>272</sub> G <sub>271</sub> G <sub>270</sub>	011011	60		011011
	G <sub>285</sub> G <sub>284</sub> G <sub>283</sub> G <sub>282</sub> G <sub>281</sub> G <sub>280</sub>	011100	61		011100
	G <sub>295</sub> G <sub>294</sub> G <sub>293</sub> G <sub>292</sub> G <sub>291</sub> G <sub>290</sub>	011101	62		011101
	G <sub>305</sub> G <sub>304</sub> G <sub>303</sub> G <sub>302</sub> G <sub>301</sub> G <sub>300</sub>	011110	63		011110
	G <sub>315</sub> G <sub>314</sub> G <sub>313</sub> G <sub>312</sub> G <sub>311</sub> G <sub>310</sub>	011111	64		011111

Color	Look Up Table Outputs Frame Memory Data (6-bit)	Default value after H/W Reset	RGBSET parameter	Look Up Table Input Data	
				4k Color	65k Color
GREEN	G <sub>325</sub> G <sub>324</sub> G <sub>323</sub> G <sub>322</sub> G <sub>321</sub> G <sub>320</sub>	100000	65	Not Used	100000
	G <sub>335</sub> G <sub>334</sub> G <sub>333</sub> G <sub>332</sub> G <sub>331</sub> G <sub>330</sub>	100001	66		100001
	G <sub>345</sub> G <sub>344</sub> G <sub>343</sub> G <sub>342</sub> G <sub>341</sub> G <sub>340</sub>	100010	67		100010
	G <sub>355</sub> G <sub>354</sub> G <sub>353</sub> G <sub>352</sub> G <sub>351</sub> G <sub>350</sub>	100011	68		100011
	G <sub>365</sub> G <sub>364</sub> G <sub>363</sub> G <sub>362</sub> G <sub>361</sub> G <sub>360</sub>	100100	69		100100
	G <sub>375</sub> G <sub>374</sub> G <sub>373</sub> G <sub>372</sub> G <sub>371</sub> G <sub>370</sub>	100101	70		100101
	G <sub>385</sub> G <sub>384</sub> G <sub>383</sub> G <sub>382</sub> G <sub>381</sub> G <sub>380</sub>	100110	71		100110
	G <sub>395</sub> G <sub>394</sub> G <sub>393</sub> G <sub>392</sub> G <sub>391</sub> G <sub>390</sub>	100111	72		100111
	G <sub>405</sub> G <sub>404</sub> G <sub>403</sub> G <sub>402</sub> G <sub>401</sub> G <sub>400</sub>	101000	73		101000
	G <sub>415</sub> G <sub>414</sub> G <sub>413</sub> G <sub>412</sub> G <sub>411</sub> G <sub>410</sub>	101001	74		101001
	G <sub>425</sub> G <sub>424</sub> G <sub>423</sub> G <sub>422</sub> G <sub>421</sub> G <sub>420</sub>	101010	75		101010
	G <sub>435</sub> G <sub>434</sub> G <sub>433</sub> G <sub>432</sub> G <sub>431</sub> G <sub>430</sub>	101011	76		101011
	G <sub>445</sub> G <sub>444</sub> G <sub>443</sub> G <sub>442</sub> G <sub>441</sub> G <sub>440</sub>	101100	77		101100
	G <sub>455</sub> G <sub>454</sub> G <sub>453</sub> G <sub>452</sub> G <sub>451</sub> G <sub>450</sub>	101101	78		101101
	G <sub>465</sub> G <sub>464</sub> G <sub>463</sub> G <sub>462</sub> G <sub>461</sub> G <sub>460</sub>	101110	79		101110
	G <sub>475</sub> G <sub>474</sub> G <sub>473</sub> G <sub>472</sub> G <sub>471</sub> G <sub>470</sub>	101111	80		101111
	G <sub>485</sub> G <sub>484</sub> G <sub>483</sub> G <sub>482</sub> G <sub>481</sub> G <sub>480</sub>	110000	81		110000
	G <sub>495</sub> G <sub>494</sub> G <sub>493</sub> G <sub>492</sub> G <sub>491</sub> G <sub>490</sub>	110001	82		110001
	G <sub>505</sub> G <sub>504</sub> G <sub>503</sub> G <sub>502</sub> G <sub>501</sub> G <sub>500</sub>	110010	83		110010
	G <sub>515</sub> G <sub>514</sub> G <sub>513</sub> G <sub>512</sub> G <sub>511</sub> G <sub>510</sub>	110011	84		110011
	G <sub>525</sub> G <sub>524</sub> G <sub>523</sub> G <sub>522</sub> G <sub>521</sub> G <sub>520</sub>	110100	85		110100
	G <sub>535</sub> G <sub>534</sub> G <sub>533</sub> G <sub>532</sub> G <sub>531</sub> G <sub>530</sub>	110101	86		110101
	G <sub>545</sub> G <sub>544</sub> G <sub>543</sub> G <sub>542</sub> G <sub>541</sub> G <sub>540</sub>	110110	87		110110
	G <sub>555</sub> G <sub>554</sub> G <sub>553</sub> G <sub>552</sub> G <sub>551</sub> G <sub>550</sub>	110111	88		110111
	G <sub>565</sub> G <sub>564</sub> G <sub>563</sub> G <sub>562</sub> G <sub>561</sub> G <sub>560</sub>	111000	89		111000
	G <sub>575</sub> G <sub>574</sub> G <sub>573</sub> G <sub>572</sub> G <sub>571</sub> G <sub>570</sub>	111001	90		111001
	G <sub>585</sub> G <sub>584</sub> G <sub>583</sub> G <sub>582</sub> G <sub>581</sub> G <sub>580</sub>	111010	91		111010
	G <sub>595</sub> G <sub>594</sub> G <sub>593</sub> G <sub>592</sub> G <sub>591</sub> G <sub>590</sub>	111011	92		111011
	G <sub>605</sub> G <sub>604</sub> G <sub>603</sub> G <sub>602</sub> G <sub>601</sub> G <sub>600</sub>	111100	93		111100
	G <sub>615</sub> G <sub>614</sub> G <sub>613</sub> G <sub>612</sub> G <sub>611</sub> G <sub>610</sub>	111101	94		111101
	G <sub>625</sub> G <sub>624</sub> G <sub>623</sub> G <sub>622</sub> G <sub>621</sub> G <sub>620</sub>	111110	95		111110
	G <sub>635</sub> G <sub>634</sub> G <sub>633</sub> G <sub>632</sub> G <sub>631</sub> G <sub>630</sub>	111111	96		111111

Color	Look Up Table Outputs Frame Memory Data (6-bit)	Default value after H/W Reset	RGBSET parameter	Look Up Table Input Data	
				4k Color	65k Color
BLUE	B <sub>005</sub> B <sub>004</sub> B <sub>003</sub> B <sub>002</sub> B <sub>001</sub> B <sub>000</sub>	000000	97	0000	00000
	B <sub>015</sub> B <sub>014</sub> B <sub>013</sub> B <sub>012</sub> B <sub>011</sub> B <sub>010</sub>	000011	98	0001	00001
	B <sub>025</sub> B <sub>024</sub> B <sub>023</sub> B <sub>022</sub> B <sub>021</sub> B <sub>020</sub>	000101	99	0010	00010
	B <sub>035</sub> B <sub>034</sub> B <sub>033</sub> B <sub>032</sub> B <sub>031</sub> B <sub>030</sub>	000111	100	0011	00011
	B <sub>045</sub> B <sub>044</sub> B <sub>043</sub> B <sub>042</sub> B <sub>041</sub> B <sub>040</sub>	001001	101	0100	00100
	B <sub>055</sub> B <sub>054</sub> B <sub>053</sub> B <sub>052</sub> B <sub>051</sub> B <sub>050</sub>	001011	102	0101	00101
	B <sub>065</sub> B <sub>064</sub> B <sub>063</sub> B <sub>062</sub> B <sub>061</sub> B <sub>060</sub>	001101	103	0110	00110
	B <sub>075</sub> B <sub>074</sub> B <sub>073</sub> B <sub>072</sub> B <sub>071</sub> B <sub>070</sub>	001111	104	0111	00111
	B <sub>085</sub> B <sub>084</sub> B <sub>083</sub> B <sub>082</sub> B <sub>081</sub> B <sub>080</sub>	010001	105	1000	01000
	B <sub>095</sub> B <sub>094</sub> B <sub>093</sub> B <sub>092</sub> B <sub>091</sub> B <sub>090</sub>	010011	106	1001	01001
	B <sub>105</sub> B <sub>104</sub> B <sub>103</sub> B <sub>102</sub> B <sub>101</sub> B <sub>100</sub>	010101	107	1010	01010
	B <sub>115</sub> B <sub>114</sub> B <sub>113</sub> B <sub>112</sub> B <sub>111</sub> B <sub>110</sub>	010111	108	1011	01011
	B <sub>125</sub> B <sub>124</sub> B <sub>123</sub> B <sub>122</sub> B <sub>121</sub> B <sub>120</sub>	011001	109	1100	01100
	B <sub>135</sub> B <sub>134</sub> B <sub>133</sub> B <sub>132</sub> B <sub>131</sub> B <sub>130</sub>	011011	110	1101	01101
	B <sub>145</sub> B <sub>144</sub> B <sub>143</sub> B <sub>142</sub> B <sub>141</sub> B <sub>140</sub>	011101	111	1110	01110
	B <sub>155</sub> B <sub>154</sub> B <sub>153</sub> B <sub>152</sub> B <sub>151</sub> B <sub>150</sub>	011111	112	1111	01111
	B <sub>165</sub> B <sub>164</sub> B <sub>163</sub> B <sub>162</sub> B <sub>161</sub> B <sub>160</sub>	100001	113	Not Used	10000
	B <sub>175</sub> B <sub>174</sub> B <sub>173</sub> B <sub>172</sub> B <sub>171</sub> B <sub>170</sub>	100011	114		10001
	B <sub>185</sub> B <sub>184</sub> B <sub>183</sub> B <sub>182</sub> B <sub>181</sub> B <sub>180</sub>	100101	115		10010
	B <sub>195</sub> B <sub>194</sub> B <sub>193</sub> B <sub>192</sub> B <sub>191</sub> B <sub>190</sub>	100111	116		10011
	B <sub>205</sub> B <sub>204</sub> B <sub>203</sub> B <sub>202</sub> B <sub>201</sub> B <sub>200</sub>	101001	117		10100
	B <sub>215</sub> B <sub>214</sub> B <sub>213</sub> B <sub>212</sub> B <sub>211</sub> B <sub>210</sub>	101011	118		10101
	B <sub>225</sub> B <sub>224</sub> B <sub>223</sub> B <sub>222</sub> B <sub>221</sub> B <sub>220</sub>	101101	119		10110
	B <sub>235</sub> B <sub>234</sub> B <sub>233</sub> B <sub>232</sub> B <sub>231</sub> B <sub>230</sub>	101111	120		10111
	B <sub>245</sub> B <sub>244</sub> B <sub>243</sub> B <sub>242</sub> B <sub>241</sub> B <sub>240</sub>	110001	121		11000
	B <sub>255</sub> B <sub>254</sub> B <sub>253</sub> B <sub>252</sub> B <sub>251</sub> B <sub>250</sub>	110011	122		11001
	B <sub>265</sub> B <sub>264</sub> B <sub>263</sub> B <sub>262</sub> B <sub>261</sub> B <sub>260</sub>	110101	123		11010
	B <sub>275</sub> B <sub>274</sub> B <sub>273</sub> B <sub>272</sub> B <sub>271</sub> B <sub>270</sub>	110111	124		11011
	B <sub>285</sub> B <sub>284</sub> B <sub>283</sub> B <sub>282</sub> B <sub>281</sub> B <sub>280</sub>	111001	125		11100
	B <sub>295</sub> B <sub>294</sub> B <sub>293</sub> B <sub>292</sub> B <sub>291</sub> B <sub>290</sub>	111011	126		11101
	B <sub>305</sub> B <sub>304</sub> B <sub>303</sub> B <sub>302</sub> B <sub>301</sub> B <sub>300</sub>	111101	127		11110
	B <sub>315</sub> B <sub>314</sub> B <sub>313</sub> B <sub>312</sub> B <sub>311</sub> B <sub>310</sub>	111111	128		11111

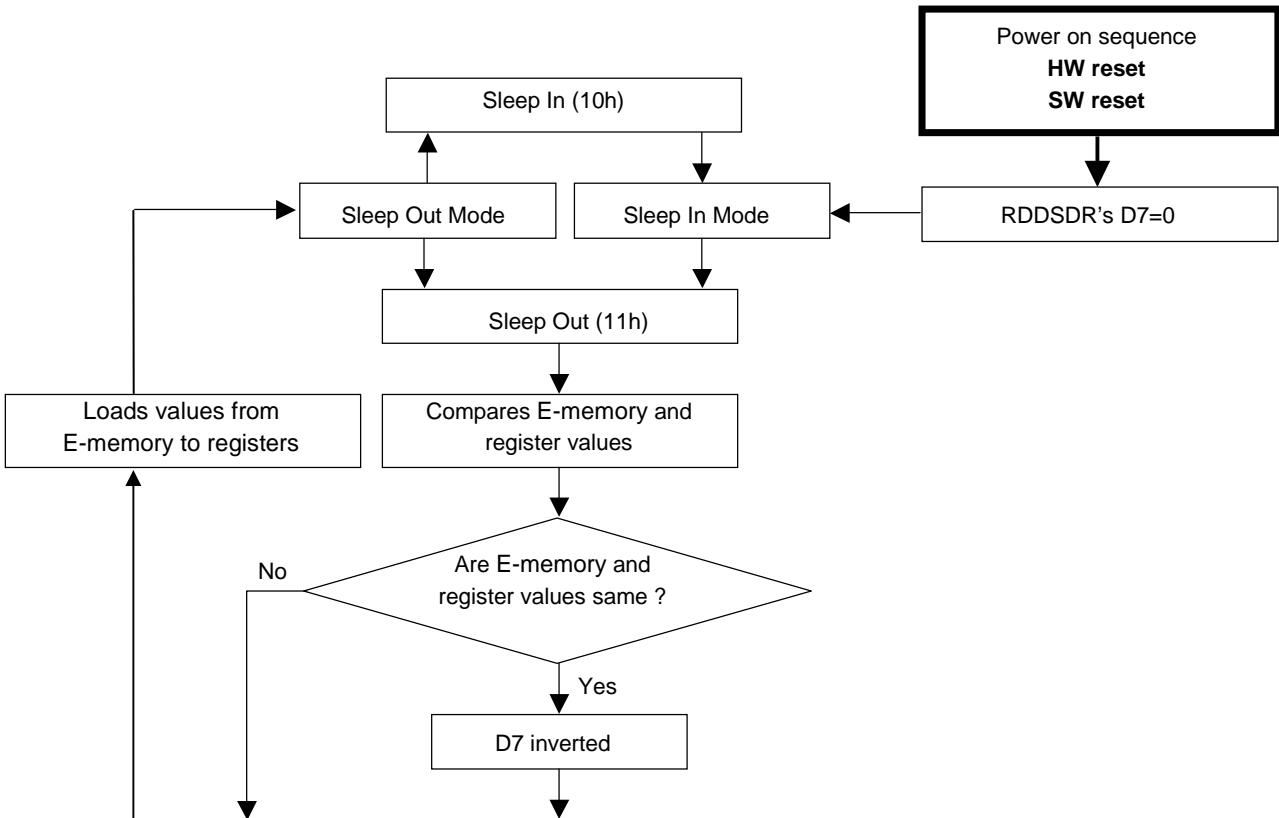
## 9.19 Sleep Out-Command and Self-Diagnostic Functions of the Display Module

### 9.19.1 Register Loading Detection

Sleep Out-command (See section 10.1.12 "Sleep Out (11h)") is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from E-memory (similar device) to registers of the display controller is working properly.

There are compared factory values of the E-memory and register values of the display controller by the display controller. If those both values (E-memory and register values) are same, there is inverted (=increased by 1) a bit, which is defined in command 10.1.10 "Read Display Self-Diagnostic Result (0Fh)" (=RDDSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (= increased by 1).

The flow chart for this internal function is following:



*Note: There is not compared and loaded register values, which can be changed by user (00h to AFh and DAh to DDh), by the display module.*

## 9.20 External Light Source

The operation of the module can meet customer's Environmental reliability requirements.

## 9.21 Oscillator

The chip has on-chip oscillator that does not require external components. This oscillator output signal is used for system clock generation for internal display operation.

## 9.22 System Clock Generator

The timing generator produces the various signals to driver the internal circuitry. Internal chip operation is not affected by operations on the data bus.

## 9.23 Instruction Decoder and Register

The instruction decoder identifies command words arriving at the interface and routes the following data bytes to their destination. The command set can be found in "Command" section.

## 9.24 Source Driver

The source driver block includes 240x3 source outputs (S1 to S720), which should be connected directly to the TFT-LCD. The source output signals are generated in the data processing block after the data is read out of the RAM and latched, which represent the simulatance selected rows.

## 9.25 Gate Driver

The gate driver block include 320 channel gate output (G1 to G320) which should be connected directly to the TFT-LCD.

### 9.25.1 Gate Driver

#### 9.25.1.1 Normal mode

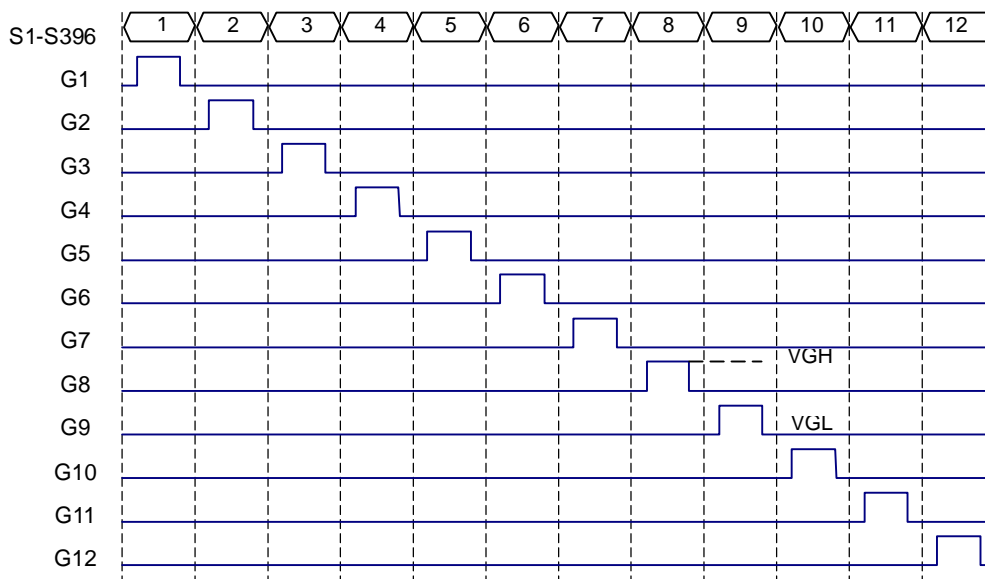


Fig. 9.25.1 Gate Driver Output Option 1

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## 10. Command

### 10.1 System function Command List and Description

Table 10.1.1 System Function command List (1)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
NOP	10.1.1	0	-↑	1	-	0	0	0	0	0	0	0	0	(00h)	No Operation
SWRESET	10.1.2	0	↑	1	-	0	0	0	0	0	0	0	1	(01h)	Software reset
RDDID	10.1.3	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)	Read Display ID
		1	1	↑	-	---	---	---	---	---	---	---	---		Dummy read
		1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		ID1 read
		1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		ID2 read
		1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		ID3 read
RDDST	10.1.4	0	-↑	1	-	0	0	0	0	1	0	0	1	(09h)	Read Display Status
		1	1	↑	-	---	---	---	---	---	---	---	---		Dummy read
		1	1	↑	-	BSTON	MY	MX	MV	ML	RGB	MH	ST24		-
		1	1	↑	-	ST23	IFPF2	IFPF1	IFPF0	IDMON	PTLON	SLOUT	NORON		-
		1	1	↑	-	VSSON	ST14	INVON	ST12	ST11	DISON	TEON	GCS2		-
1	1	-↑	-	GCS1	GCS0	TELOM	HSON	VSON	PCKON	DEON	ST0		-		
RDDPM	10.1.5	0	-↑	1	-	0	0	0	0	1	0	1	0	(0Ah)	Read Display Power Mode
		1	1	-↑	-	---	---	---	---	---	---	---	---		Dummy read
		1	1	-↑	-	BSTON	IDMON	PTLON	SLPOUT	NORON	DISON	D1	D0		-
RDD MADCTL	10.1.6	0	-↑	1	-	0	0	0	0	1	0	1	1	(0Bh)	Read Display MADCTL
		1	1	-↑	-	---	---	---	---	---	---	---	---		Dummy read
		1	1	-↑	-	MX	MY	MV	ML	RGB	MH	D1	D0	00h	-
RDD COLMOD	10.1.7	0	-↑	1	-	0	0	0	0	1	1	0	0	(0Ch)	Read Display Pixel Format
		1	1	-↑	-	---	---	---	---	---	---	---	---		Dummy read
		1	1	-↑	-	VIPF3	VIPF2	VIPF1	VIPF0	D3	IFPF2	IFPF1	IFPF0		-
RDDIM	10.1.8	0	-↑	1	-	0	0	0	0	1	1	0	1	(0Dh)	Read Display Image Mode
		1	1	-↑	-	---	---	---	---	---	---	---	---		Dummy read
		1	1	-↑	-	VSSON	D6	INVON	D4	D3	GCS2	GCS1	GCS0		-
RDDSM	10.1.9	0	-↑	1	-	0	0	0	0	1	1	1	0	(0Eh)	Read Display Signal Mode
		1	1	-↑	-	---	---	---	---	---	---	---	---		Dummy read
		1	1	-↑	-	TEON	TELOM	HSON	VSON	PCKON	DEON	D1	D0	00h	-
RDDSDR	10.1.10	0	-↑	1	-	0	0	0	0	1	1	1	1	(0Fh)	Read Display Self-diagnostic result
		1	1	-↑	-	---	---	---	---	---	---	---	---		Dummy read
		1	1	-↑	-	RELD	FUND	ATTD	BRD	D3	D2	D1	D0		-

"-": Don't care

# ST7787

Table 10.1.2 System Function command List (2)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
SLPIN	10.1.11	0	↑	1	-	0	0	0	1	0	0	0	0	(10h)	Sleep in & booster off
SLPOUT	10.1.12	0	↑	1	-	0	0	0	1	0	0	0	1	(11h)	Sleep out & booster on
PTLON	10.1.13	0	↑	1	-	0	0	0	1	0	0	1	0	(12h)	Partial mode on
NORON	10.1.14	0	↑	1	-	0	0	0	1	0	0	1	1	(13h)	Partial mode off Normal mode
INVOFF	10.1.15	0	↑	1	-	0	0	1	0	0	0	0	0	(20h)	Display inversion off Normal
INVON	10.1.16	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)	Display inversion on
GAMSET	10.1.17	0	↑	1	-	0	0	1	0	0	1	1	0	(26h)	Gamma curve select
		1	↑	1	-	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0		-
DISPOFF	10.1.18	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)	Display off
DISPON	10.1.19	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)	Display on
CASET	10.1.20	0	↑	1	-	0	0	1	0	1	0	1	0	(2Ah)	Column address set
		1	↑	1	-	---	---	---	---	---	---	---	XS8		Xaddress start: $0 \leq XS \leq EF$
		1	↑	1	-	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	00h	MV=0
		1	↑	1	-	---	---	---	---	---	---	---	---	XE8	
RASET	10.1.21	0	↑	1	-	0	0	1	0	1	0	1	1	(2Bh)	Row address set
		1	↑	1	-	---	---	---	---	---	---	---	YS8		Xaddress start: $0 \leq YS \leq 13F$
		1	↑	1	-	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	00h	MV=0
		1	↑	1	-	---	---	---	---	---	---	---	---	YE8	
RAMWR	10.1.22	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)	Memory write
		1	↑	1	-	Write data * Bit assignment varies with the selected interface									Write data
RAMRD	10.1.23	0	↑	1	-	0	0	1	0	1	1	1	0	(2Eh)	Memory read
		1	1	-↑	-	---	---	---	---	---	---	---	---	---	
		1	1	-↑	-	Read data * Bit assignment varies with the selected interface									Read data

"-": Don't care



# ST7787

Table 10.1.3 System Function command List (3)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function	
PTLAR	10.1.25	0	↑	1	-	0	0	1	1	0	0	0	0	(30h)	Partial start/end address set	
		1	↑	1	-	---	---	---	---	---	---	---	---	PSL8	00h	Partial start address 0,1,2,.....,219
		1	↑	1	-	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	PSL0	00h	Partial start address 0,1,2,.....,219
		1	↑	1	-	---	---	---	---	---	---	---	---	PEL8	00h	Partial end address 0,1,2,.....,219
		1	↑	1	-	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0	PEL0	F0h	Partial end address 0,1,2,.....,219
SCRLAR	10.1.26	0	↑	1	-	0	0	1	1	0	0	1	1	(33h)	Scroll area set	
		1	↑	1	-	---	---	---	---	---	---	---	---	TFA8		Top fixed area 0,1,2,.....,219
		1	↑	1	-	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	TFA0		Top fixed area 0,1,2,.....,219
		1	↑	1	-	---	---	---	---	---	---	---	---	VSA8		Vertical scroll area 0,1,2,.....,219
		1	↑	1	-	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	VSA0		Vertical scroll area 0,1,2,.....,219
		1	↑	1	-	---	---	---	---	---	---	---	---	BFA8		Bottom fixed area 0,1,2,.....,219
		1	↑	1	-	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	BFA0		Bottom fixed area 0,1,2,.....,219
TEOFF	10.1.27	0	↑	1	-	0	0	1	1	0	1	0	0	(34h)	Tearing effect line off	
TEON	10.1.28	0	↑	1	-	0	0	1	1	0	1	0	1	(35h)	Tearing effect mode set & on	
		1	↑	1	-	---	---	---	---	---	---	---	M		M="0": Mode 1, M="1": Mode 2	
MADCTL	10.1.29	0	↑	1	-	0	0	1	1	0	1	1	0	(36h)	Memory data access control	
		1	↑	1	-	MY	MX	MV	ML	RGB	MH	---	---		soft rst	
VSCSAD	10.1.30	0	↑	1	-	0	0	1	1	0	1	1	1	(37h)	Scroll start address of RAM	
		1	↑	1	-	---	---	---	---	---	---	---	SSA8		SSA=0,1,2,.....,319	
		1	↑	1	-	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	SSA0	00h	
IDMOFF	10.1.31	0	↑	1	-	0	0	1	1	1	0	0	0	(38h)	Idle mode off	
IDMON	10.1.32	0	↑	1	-	0	0	1	1	1	0	0	1	(39h)	Idle mode on	
COLMOD	10.1.33	0	↑	1	-	0	0	1	1	1	0	1	0	(3Ah)	Interface pixel format	
		1	↑	1	-	VIPF3	VIPF2	VIPF1	VIPF0	---	IFPF2	IFPF1	IFPF0		soft rst	
OTP_process	10.1.34	0	↑	1	-	0	0	1	1	1	1	1	1	(3Fh)	OTP-Process	
		1	↑	1	-	1	1	0	0	1	0	1	0	CAh		
		1	↑	1	-	0	0	0	0	0	0	INI	0			
RDID1	10.1.35	0	↑	1	-	1	1	0	1	1	0	1	0	(DAh)	Read ID1	
		1	1	↑	-	---	---	---	---	---	---	---	---		Dummy read	
		1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		Read parameter	
RDID2	10.1.36	0	↑	1	-	1	1	0	1	1	0	1	1	(DBh)	Read ID2	
		1	1	↑	-	---	---	---	---	---	---	---	---		Dummy read	
		1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		Read parameter	
RDID3	10.1.37	0	↑	1	-	1	1	0	1	1	1	0	0	(DCh)	Read ID3	
		1	1	↑	-	---	---	---	---	---	---	---	---		Dummy read	
		1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		Read parameter	

"-": Don't care

Note 1. After the H/W reset by RESX pin or S/W reset by SWRESET command, each internal register becomes default state (Refer "RESET TABLE" section)

Note 2. Undefined commands are treated as NOP (00 h) command.

Note 3. B0 to D9 and DE to FF are for factory use of driver supplier. Note 4. Commands 10h, 12h, 13h, 20h, 21h, 26h, 28h, 29h, 30h, 33h, 36h (ML parameter only), 37h, 38h and 39h are updated during V-sync when Module is in Sleep Out Mode to avoid abnormal visual effects. During Sleep In mode, these commands are updated immediately. Read status (09h), Read Display Power Mode (0Ah), Read Display MADCTL (0Bh), Read Display Pixel Format (0Ch), Read Display Image Mode (0Dh), Read Display Signal Mode (0Eh) and Read Display Self Diagnostic Result (0Fh) of these commands are updated immediately both in Sleep In mode and Sleep Out mode.

## 10.2 Panel Function Command List and Description

Table 10.2.1 Panel Function Command List (2)

Instruction	Refer	D/CX	WRX	RDX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
RGBCTR	10.2.1	0	↑	1	-	1	0	1	1	0	0	0	0	(B0h)	Set Display I/F mode
		1	↑	1	-	---	---	---	ICM	DP	EP	HSP	VSP		Polarity set
FRMCTR1	10.2.2	0	↑	1	-	1	0	1	1	0	0	0	1	(B1h)	In normal mode full colors
		1	↑	1	-	---	RTNA[6]	RTNA[5]	RTNA[4]	RTNA[3]	RTNA[2]	RTNA[1]	RTNA[0]		Blanking porch setting
		1	↑	1	-	---	---	---	FPA[4]	FPA[3]	FPA[2]	FPA[1]	FPA[0]		
		1	↑	1	-	---	---	---	BPA[4]	BPA[3]	BPA[2]	BPA[1]	BPA[0]		
FRMCTR2	10.2.3	0	↑	1	-	1	0	1	1	0	0	1	0	(B2h)	In idle mode 8-colors
		1	↑	1	-	---	RTNB[6]	RTNB[5]	RTNB[4]	RTNB[3]	RTNB[2]	RTNB[1]	RTNB[0]		Blanking porch setting
		1	↑	1	-	---	---	---	FPB[4]	FPB[3]	FPB[2]	FPB[1]	FPB[0]		
		1	↑	1	-	---	---	---	BPB[4]	BPB[3]	BPB[2]	BPB[1]	BPB[0]		
FRMCTR3	10.2.4	0	↑	1	-	1	0	1	1	0	0	1	1	(B3h)	In partial mode + full colors
		1	↑	1	-	---	RTNC[6]	RTNC[5]	RTNC[4]	RTNC[3]	RTNC[2]	RTNC[1]	RTNC[0]		Blanking porch setting line inversion
		1	↑	1	-	---	---	---	FPC[4]	FPC[3]	FPC[2]	FPC[1]	FPC[0]		
		1	↑	1	-	---	---	---	BPC[4]	BPC[3]	BPC[2]	BPC[1]	BPC[0]		
		1	↑	1	-	---	RTND[6]	RTND[5]	RTND[4]	RTND[3]	RTND[2]	RTND[1]	RTND[0]		Blanking porch setting frame inversion
		1	↑	1	-	---	---	---	FPD[4]	FPD[3]	FPD[2]	FPD[1]	FPD[0]		
		1	↑	1	-	---	---	---	BPD[4]	BPD[3]	BPD[2]	BPD[1]	BPD[0]		
INVCTR	10.2.5	0	↑	1	-	1	0	1	1	0	1	0	0	(B4h)	Display inversion control
		1	↑	1	-	---	---	---	---	---	NLA	NLB	NLC		
RGB PRCTR	10.2.6	0	↑	1	-	1	0	1	1	0	1	0	1	(B5h)	RGB I/F Blanking porch setting
		1	↑	1	-	---	---	---	---	VFP[3]	VFP[2]	VFP[1]	VFP[0]		
		1	↑	1	-	---	---	---	---	VBP[3]	VBP[2]	VBP[1]	VBP[0]		
		1	↑	1	-	---	---	---	---	HFP[3]	HFP[2]	HFP[1]	HFP[0]		
		1	↑	1	-	---	---	---	---	HBP[3]	HBP[2]	HBP[1]	HBP[0]		
DISSET5	10.2.7	0	↑	1	-	1	0	1	1	0	1	1	0	(B6h)	Display function setting
		1	↑	1	-	---	---	NO1	NO0	SDT1	SDT0	EQ1	EQ0		
		1	↑	1	-	---	---	---	---	PTG1	PTG0	PT1	PT0		
VSYNCOUT	10.2.8	0	↑	1	-	1	0	1	1	1	1	0	0	(BCh)	External VSYNC disable
VSYNCIN	10.2.9	0	↑	1	-	1	0	1	1	1	1	0	1	(BDh)	External VSYNC enable

Table 10.2.2 Panel Function Command List (2)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function	
PWCTR1	10.2.10	0	↑	1	--	1	1	0	0	0	0	0	0	(C0h)	Power control setting	
		1	↑	1	--	--	--	--	VRH4	VRH3	VRH2	VRH1	VRH0			
PWCTR2	10.2.11	0	↑	1	--	1	1	0	0	0	0	0	1	(C1h)	Power control setting	
		1	↑	1	--	VGH3	VGH2	VGH1	VGH0	VGL3	VGL2	VGL1	VGL0	BBh		
		1	↑	1	--	--	--	--	--	GOT2	GOT1	GOT0				
PWCTR3	10.2.12	0	↑	1	--	1	1	0	0	0	0	1	0	(C2h)	In normal mode full color	
		1	↑	1	--	--	--	--	--	--	APA2	APA1	APA0			
		1	↑	1	--	STEP1A_SEL3	STEP1A_SEL2	STEP1A_SEL1	STEP1A_SEL0	---	STEP2A_SEL2	STEP2A_SEL1	STEP2A_SEL0			
		1	↑	1	--	1	0	1	1	0	0	0	0	1		
		1	↑	1	--	1	LDO5_SEL2	LDO5_SEL1	LDO5_SEL0	---	STEP4A_SEL2	STEP4A_SEL1	STEP4A_SEL0			
		1	↑	1	--	0	0	0	1	0	0	1	1			
PWCTR4	10.2.13	0	↑	1	--	1	1	0	0	0	0	1	1	(C3h)	In Idle mode (8-colors)	
		1	↑	1	--	--	--	--	--	--	APB2	APB1	APB0			
		1	↑	1	--	STEP1B_SEL3	STEP1B_SEL2	STEP1B_SEL1	STEP1B_SEL0	---	STEP2A_SEL2	STEP2A_SEL1	STEP2B_SEL0			
		1	↑	1	--	0	0	0	0	0	0	0	0			
		1	↑	1	--	--	--	--	--	--	STEP4B_SEL2	STEP4B_SEL1	STEP4B_SEL0			
		1	↑	1	--	--	--	--	--	--	0	0	0			
PWCTR5	10.2.14	0	↑	1	--	1	1	0	0	0	1	0	0	(C4h)	In partial mode + Full colors	
		1	↑	1	--	--	--	--	--	--	APC2	APC1	APC0			
		1	↑	1	--	STEP1C_SEL3	STEP1C_SEL2	STEP1C_SEL1	STEP1C_SEL0	---	STEP2C_SEL2	STEP2C_SEL1	STEP2C_SEL0			
		1	↑	1	--	1	0	1	1	0	0	1	1			
		1	↑	1	--	--	--	--	--	--	STEP4C_SEL2	STEP4C_SEL1	STEP4C_SEL0			
		1	↑	1	--	--	--	--	--	--	0	1	1			
VMCTR1	10.2.15	0	↑	1	--	1	0	1	1	0	1	0	1	(C5h)	VCOM control 1	
		1	↑	1	--	--	VMH6	VMH5	VMH4	VMH3	VMH2	VMH1	VMH0			
		1	↑	1	--	--	0	1	0	1	0	0	0			
		1	↑	1	--	--	VMH_COLOR8M6	VMH_COLOR8M5	VMH_COLOR8M4	VMH_COLOR8M3	VMH_COLOR8M2	VMH_COLOR8M1	VMH_COLOR8M0			
		1	↑	1	--	--	0	1	0	1	0	0	0			
VMCTR2	10.2.16	0	↑	1	--	1	0	1	1	0	1	1	0	(C6h)	VCOM control 2	
		1	↑	1	--	0	0	VMA5	VMA4	VMA3	VMA2	VMA1	VMA0			
		1	↑	1	--	0	0	0	1	0	1	1	0			

“-”: Don't care

Note 1: C0h to CFh are fixed for about power controller.

Note 2: The C9h to CFh are reserved for further using.

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Table 10.2.3 Panel Function Command List (3)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
WRID1	10.2.17	0	↑	1	-	1	1	0	1	0	0	0	0	(D0h)	Reserved for future using
		1	↑	1	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		
WRID2	10.2.18	0	↑	1	-	1	1	0	1	0	0	0	1	(D1h)	LCM version code
		1	↑	1	-	0	ID26	ID25	ID24	ID23	ID22	ID21	ID20		OTP ID2 set the LCM version code.
WRID3	10.2.19	0	↑	1	-	1	1	0	1	0	0	1	0	(D2h)	Customer Project code
		1	↑	1	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		OTP ID3 set the project code.
OTP-Load	10.2.20	0	↑	1	-	1	1	0	1	1	1	1	0	DEh	OTP-Read command
		1	↑	1	-	0	1	1	1	0	1	0	1	75h	
OTP-Prog	10.2.21	0	↑	1	-	1	1	0	1	1	1	1	0	DFh	OTP prog. Command Protection sequence:CA 00AA A5 A5 5A
		1	↑	1	-	1	1	0	0	1	0	1	0	CAh	
		1	↑	1	-	0	0	0	0	0	0	0	0	00h	
		1	↑	1	-	1	0	1	0	1	0	1	0	AAh	
		1	↑	1	-	1	0	1	0	0	1	0	1	5Ah	

"-": Don't care

Note 1: The D1h to D8h registers are fixed for about ID code setting.

Note 2: The D9h, DEh and DFh registers are used for NV Memory function controller. (Ex: write, clear, etc.)

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Table 10.2.4 Panel Function Command List (4)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function		
GAMCTRP1	10.2.22	0	↑	1	-	1	1	1	0	0	0	0	0	(E0h)	Set Gamma		
		1	↑	1	-	MVA_EN	---	---	---	RFP0[3]	RFP0[2]	RFP0[1]	RFP0[0]		Positive Polarity		
		1	↑	1	---	0	0	0	0	0	0	0	0	1			
		1	↑	1	---	0	0	0	0	0	1	1	0	0		0	
		1	↑	1	---	0	0	0	0	1	1	0	0	0		1	
		1	↑	1	---	0	0	0	0	1	1	0	0	0		1	
		1	↑	1	---	0	0	0	0	1	1	0	0	0		1	
		1	↑	1	---	0	0	0	0	1	1	0	0	0		1	
		1	↑	1	---	0	0	0	0	1	1	0	0	0		1	
		1	↑	1	---	0	0	0	0	1	1	0	0	0		1	
		1	↑	1	---	0	0	0	0	1	1	0	0	0		1	
		1	↑	1	---	0	0	0	0	1	1	0	0	0		1	
		1	↑	1	---	0	0	0	0	1	1	0	0	0		1	
		1	↑	1	---	0	0	0	0	1	1	0	0	0		1	
GAMCTRN1	10.2.23	0	↑	1	-	1	1	1	0	0	0	0	1	(E1h)		Set Gamma correction	
		1	↑	1	-	0	0	0	0	0	RFN0[3]	RFN0[2]	RFN0[1]	RFN0[0]		Negative Polarity	
		1	↑	1	---	0	0	0	0	0	1	1	0	0	0		
		1	↑	1	---	0	0	0	0	0	1	1	0	0	0		
		1	↑	1	---	0	0	0	0	1	1	0	0	0	1		
		1	↑	1	---	0	0	0	0	1	1	0	0	0	1		
		1	↑	1	---	0	0	0	0	1	1	0	0	0	1		
		1	↑	1	---	0	0	0	0	1	1	0	0	0	1		
		1	↑	1	---	0	0	0	0	1	1	0	0	0	1		
		1	↑	1	---	0	0	0	0	1	1	0	0	0	1		
		1	↑	1	---	0	0	0	0	1	1	0	0	0	1		
		1	↑	1	---	0	0	0	0	1	1	0	0	0	1		
		1	↑	1	---	0	0	0	0	1	1	0	0	0	1		
		1	↑	1	---	0	0	0	0	1	1	0	0	0	1		
Vcom_multi_mode	10.2.24	0	↑	1	-	1	1	1	1	0	1	0	0	(FBh)	Vcom multi mode		
		1	↑	1	---	1	Vcom Mu_mode	1	1	1	1	1	1				

"-": Don't care

Note 1: E0-E7 registers are fixed for about Gamma adjusting.

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## 10.1.1 NOP (00h)

00H	NOP (No Operation)												(Code)
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
NOP	0	↑	1	-	0	0	0	0	0	0	0	0	(00h)
Parameter	No Parameter												-

NOTE: "-" Don't care

Description	<p>-This command is empty command. It does not have effect on the display module.                      -However it can be used to terminate RAM data write or read as described in RAMWR (Memory Write), RAMRD (Memory Read) and parameter write commands.</p>													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability												
	Normal Mode On, Idle Mode Off, Sleep Out	Yes												
	Normal Mode On, Idle Mode On, Sleep Out	Yes												
	Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>N/A</td> </tr> <tr> <td>S/W Reset</td> <td>N/A</td> </tr> <tr> <td>H/W Reset</td> <td>N/A</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	N/A	S/W Reset	N/A	H/W Reset	N/A				
	Status	Default Value												
	Power On Sequence	N/A												
S/W Reset	N/A													
H/W Reset	N/A													
Flow Chart	-													

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## 10.1.2 SWRESET (01h): Software Reset

01H	SWRESET (Software Reset)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SWRESET	0	↑	1	-	0	0	0	0	0	0	0	1	(01h)
Parameter	No Parameter												-

NOTE: “-“ Don't care

Description	-When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values and all source & gate outputs are set to VSS (display off). (See default tables in each command description) <i>Note: The Frame Memory contents are not affected by this command.</i>													
Restriction	-It will be necessary to wait 120msec before sending new command following software reset. -The display module loads all display supplier 's factory default values to the registers during 120msec. -If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep Out command. -Software Reset command cannot be sent during Sleep Out sequence.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>N/A</td> </tr> <tr> <td>S/W Reset</td> <td>N/A</td> </tr> <tr> <td>H/W Reset</td> <td>N/A</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	N/A	S/W Reset	N/A	H/W Reset	N/A					
Status	Default Value													
Power On Sequence	N/A													
S/W Reset	N/A													
H/W Reset	N/A													
Flow Chart	<pre> graph TD     A[SWRESET (01h)] --&gt; B{{Display whole blank screen}}     B --&gt; C{{Set Commands to S/W Default Value}}     C --&gt; D([Sleep In Mode])     </pre>													

## 10.1.3 RDDID (04h): Read Display ID

04H	RDDID (Read Display ID)												(Code)
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDID	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	Dummy
2nd Parameter	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	
3rd Parameter	1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	
4th Parameter	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	

NOTE: “-“ Don't care

Description	<p>-This read byte returns 24-bit display identification information.</p> <p>-The 1st parameter is dummy data</p> <p>-The 2nd parameter (ID17 to ID10): LCD module's manufacturer ID.</p> <p>-The 3rd parameter (ID27 to ID20): LCD module/driver version ID</p> <p>-The 4th parameter (ID37 to UD30): LCD module/driver ID.</p> <p>NOTE: Commands RDID1/2/3(DAh, DBh, DCh) read data correspond to the parameters 2,3,4 of the command 04h, respectively.</p>				
	Restriction	-			
Register Availability	Status		Availability		
	Normal Mode On, Idle Mode Off, Sleep Out		Yes		
	Normal Mode On, Idle Mode On, Sleep Out		Yes		
	Partial Mode On, Idle Mode Off, Sleep Out		Yes		
	Partial Mode On, Idle Mode On, Sleep Out		Yes		
Sleep In		Yes			
Default	Status		Default Value		
	Power On Sequence		ID1	ID2	ID3
	S/W Reset		N/A	N/A	N/A
	H/W Reset		N/A	N/A	N/A
Flow Chart					



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## 10.1.4 RDDST (09h): Read Display Status

09H	RDDST (Read Display Status)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDST	0	↑	1	-	0	0	0	0	1	0	0	1	(09h)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	BSTON	MY	MX	MV	ML	RGB	MH	ST24	
3rd Parameter	1	1	↑	-	ST23	IFPF2	IFPF1	IFPF0	IDMON	PTLON	SLOUT	NORON	
4th Parameter	1	1	↑	-	VSSON	ST14	INVON	ST12	ST11	DISON	TEON	GCS2	
5th Parameter	1	1	↑	-	GCS1	GCS0	TELOM	HSOON	VSON	PCKON	DEON	ST0	

NOTE: “-“ Don't care

Description	This command indicates the current status of the display as described in the table below:																													
	Bit	Description	Value																											
	BSTON	Booster Voltage Status	'1' =Booster on, '0' =Booster off																											
	MY	Row Address Order (MY)	'1' =Decrement, (Bottom to Top, when MADCTL (36h) D7='1') '0' =Increment, (Top to Bottom, when MADCTL (36h) D7='0')																											
	MX	Column Address Order (MX)	'1' =Decrement, (Right to Left, when MADCTL (36h) D6='1') '0' =Increment, (Left to Right, when MADCTL (36h) D6='1')																											
	MV	Row/Column Exchange (MV)	'1' = Row/column exchange, (when MADCTL (36h) D5='1') '0' = Normal, (when MADCTL (36h) D5='0')																											
	ML	Scan Address Order (ML)	'1' =Decrement, (LCD refresh Top to Bottom, when MADCTL (36h) D4='1') '0' =Increment, (LCD refresh Bottom to Top, when MADCTL (36h) D4='0')																											
	RGB	RGB/ BGR Order (RGB)	'1' =BGR, (When MADCTL (36h) D3='1') '0' =RGB, (When MADCTL (36h) D3='0')																											
	MH	Horizontal Order	'1' =Decrement, (LCD refresh Left to Right, when MADCTL (36h) D2='1') '0' =Increment, (LCD refresh Right to Left, when MADCTL (36h) D2='0')																											
	ST24	For Future Use	'0'																											
	ST23	For Future Use	'0'																											
	IFPF2	Interface Color Pixel Format Definition	"011" = 12-bit / pixel,																											
	IFPF1		"101" = 16-bit / pixel,																											
	IFCPF0		"110" = 18-bit / pixel, others are no define																											
	IDMON	Idle Mode On/Off	'1' = On, "0" = Off																											
	PTLON	Partial Mode On/Off	'1' = On, "0" = Off																											
	SLPOUT	Sleep In/Out	'1' = Out, "0" = In																											
	NORON	Display Normal Mode On/Off	'1' = Normal Display, '0' = Partial Display																											
	VSSON	Vertical Scrolling Status	'1' = Scroll on, "0" = Scroll off																											
	ST14	Horizontal Scroll Status	'0'																											
	INVON	Inversion Status	'1' = On, "0" = Off																											
	ST12	All Pixels On (Not Used)	'0'																											
	ST11	All Pixels Off (Not Used)	'0'																											
	DISON	Display On/Off	'1' = On, "0" = Off																											
	TEON	Tearing effect line on/off	'1' = On, "0" = Off																											
	TELOM	Tearing effect line mode	'0' = mode1, '1' = mode2																											
	HSOON	Horizontal Sync. (HS, RGB I/F)	'1' = On, '0' = Off																											
	VSON	Vertical Sync. (VS, RGB I/F)	'1' = On, '0' = Off																											
PCLKON	Pixel Clock (PCLK, RGB I/F)	'1' = On, '0' = Off																												
DEON	Data Enable (DE, RGB I/F)	'1' = On, '0' = Off																												
ST0	For Future Use	'0'																												
<table border="1"> <thead> <tr> <th>GS</th> <th>GC[7:0]</th> <th>GCS[2:0]</th> <th>TR LCtype</th> </tr> </thead> <tbody> <tr> <td rowspan="4">0</td> <td>01h</td> <td>000</td> <td><math>\gamma = 1.0</math></td> </tr> <tr> <td>02h</td> <td>001</td> <td><math>\gamma = 2.5</math></td> </tr> <tr> <td>04h</td> <td>010 (LCM=[01])</td> <td><math>\gamma = 2.2</math></td> </tr> <tr> <td>08h</td> <td>011</td> <td><math>\gamma = 1.8</math></td> </tr> <tr> <td rowspan="3">1</td> <td>01h</td> <td>000 (LCM=[01])</td> <td><math>\gamma = 2.2</math></td> </tr> <tr> <td>02h</td> <td>001</td> <td><math>\gamma = 1.8</math></td> </tr> <tr> <td>04h</td> <td>010</td> <td><math>\gamma = 2.5</math></td> </tr> </tbody> </table>				GS	GC[7:0]	GCS[2:0]	TR LCtype	0	01h	000	$\gamma = 1.0$	02h	001	$\gamma = 2.5$	04h	010 (LCM=[01])	$\gamma = 2.2$	08h	011	$\gamma = 1.8$	1	01h	000 (LCM=[01])	$\gamma = 2.2$	02h	001	$\gamma = 1.8$	04h	010	$\gamma = 2.5$
GS	GC[7:0]	GCS[2:0]	TR LCtype																											
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	02h	001	$\gamma = 1.8$																											
	04h	010	$\gamma = 2.5$																											

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	Note: ST0, ST5, ST9, ST11-ST15, ST19, ST23, ST24 are set to '0', when RGB I/F.				
Restriction	-				
Register Availability	Status		Availability		
	Normal Mode On, Idle Mode Off, Sleep Out		Yes		
	Normal Mode On, Idle Mode On, Sleep Out		Yes		
	Partial Mode On, Idle Mode Off, Sleep Out		Yes		
	Partial Mode On, Idle Mode On, Sleep Out		Yes		
	Sleep In		Yes		
Default	Status		Default Value (ST31 to ST0)		
		ST[31:24]	ST[23:16]	ST[15:8]	ST[7:0]
	Power On Sequence	0000-0000	0110-0001	0000-0000	0000-0000
	S/W Reset	0xxx0xx00	0xxx-0001	0000-0000	0000-0000
	H/W Reset	0000-0000	0110-0001	0000-0000	0000-0000
Flow Chart	Serial I/F Mode		Parallel I/F Mode		
			Host Driver		
	<div style="border: 1px dashed black; padding: 5px;"> <p style="text-align: center;">Legend</p> <div style="display: flex; flex-direction: column; gap: 10px;"> <div style="border: 1px solid black; width: 50px; height: 15px; margin: 0 auto;"></div> <div style="border: 1px solid black; width: 50px; height: 15px; transform: rotate(-45deg); margin: 0 auto;"></div> <div style="border: 1px solid black; width: 50px; height: 15px; border-radius: 5px; margin: 0 auto;"></div> <div style="border: 1px solid black; width: 50px; height: 15px; border-radius: 5px; margin: 0 auto;"></div> <div style="border: 1px solid black; width: 50px; height: 15px; border-radius: 5px; margin: 0 auto;"></div> <div style="border: 1px solid black; width: 50px; height: 15px; border-radius: 5px; margin: 0 auto;"></div> </div> </div>				

## 10.1.5 RDDPM (0Ah): Read Display Power Mode

0Ah	RDDPM (Read Display Power Mode)												(Code)
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	
RDDPM	0	↑	1	-	0	0	0	0	1	0	1	0	0Ah
1 <sup>st</sup> Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2 <sup>nd</sup> Parameter	1	1	↑		BSTON	IDMON	PTLON	SLPOUT	NORON	DISON	D1	D0	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	This command indicates the current status of the display as described in the table below:		
	Bit	Description	Value
	BSTON	Booster Voltage Status	1' =Booster on, 0' =Booster off
	IDMON	Idle Mode On/Off	"1" = Idle Mode On, "0" = Idle Mode Off
	PTLON	Partial Mode On/Off	"1" = Partial Mode On, "0" = Partial Mode Off
	SLPON	Sleep In/Out	"1" = Sleep Out, "0" = Sleep In
	NORON	Display Normal Mode On/Off	"1" = Normal Display, "0" = Partial Display
	DISON	Display On/Off	"1" = Display On, "0" = Display Off
D1	Not Used	"0"	
D0	Not Used	"0"	
Restriction	-		
Register Availability	Status	Availability	
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	
Default	Status	Default Value (D7 to D0)	
	Power On Sequence	08h	
	S/W Reset	08h	
	H/W Reset	08h	
Flow Chart	<div style="display: flex; justify-content: space-around;"> <div style="text-align: center;"> <p>Serial I/F Mode</p> </div> <div style="text-align: center;"> <p>Parallel I/F Mode</p> </div> </div> <p style="text-align: center;">Host Driver</p>		
	<div style="border: 1px dashed black; padding: 5px;"> <p>Legend</p> <ul style="list-style-type: none"> <li><span style="border: 1px solid black; padding: 2px;">Command</span></li> <li><span style="border: 1px solid black; padding: 2px;">Parameter</span></li> <li><span style="border: 1px solid black; padding: 2px;">Display</span></li> <li><span style="border: 1px solid black; padding: 2px;">Action</span></li> <li><span style="border: 1px solid black; padding: 2px;">Mode</span></li> <li><span style="border: 1px solid black; padding: 2px;">Sequential transfer</span></li> </ul> </div>		

## 10.1.6 RDDMADCTL (0Bh): Read Display MADCTL

0BH	RDDMADCTL (Read Display MADCTL)												(Code)
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	
RDDMADCTL	0	↑	1	-	0	0	0	0	1	0	1	1	(0Bh)
1 <sup>st</sup> Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2 <sup>nd</sup> Parameter	1	1	↑		MY	MX	MV	ML	RGB	MH	D1	D0	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	This command indicates the current status of the display as described in the table below:	
	<b>Bit</b>	<b>Description</b>
	MX	Row Address Order '1' = Bottom to Top (When MADCTL B7='1') '0' = Top to Bottom (When MADCTL B7='0')
	MY	Column Address Order '1' = Right to Left (When MADCTL B6='1') '0' = Left to Right (When MADCTL B6='0')
	MV	Row/Column Order (MV) '1' = Row/column exchange (MV=1) '0' = Normal (MV=0)
	ML	Vertical Refresh Order '1' =LCD Refresh Bottom to Top '0' =LCD Refresh Top to Bottom
	RGB	RGB/BGR Order '1' =BGR, "0"=RGB
	MH	Horizontal order '1' =LCD Refresh Right to Left '0' =LCD Refresh Left to Right
	D1	Not Used "0"
	D0	Not Used "0"
Restriction	-	
Register Availability	<b>Status</b>	
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	<b>Status</b>	
	Power On Sequence	00h
	S/W Reset	No change
	H/W Reset	00h
Flow Chart	<p>Serial I/F Mode</p>	<p>Parallel I/F Mode</p>
	<p>Host Driver</p>	

## 10.1.7 RDDCOLMOD (0Ch): Read Display Pixel Format

0Ch	RDDCOLMOD (Read Display Pixel Format)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDCOLMOD	0	↑	1	-	0	0	0	0	1	1	0	0	(0Ch)
1 <sup>st</sup> Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2 <sup>nd</sup> Parameter	1	1	↑	-	VIPF3	VIPF2	VIPF1	VIPF0	D3	IFPF2	IFPF1	IFPF0	

NOTE: "-" Don't care, can be set to VDDI or DGND level

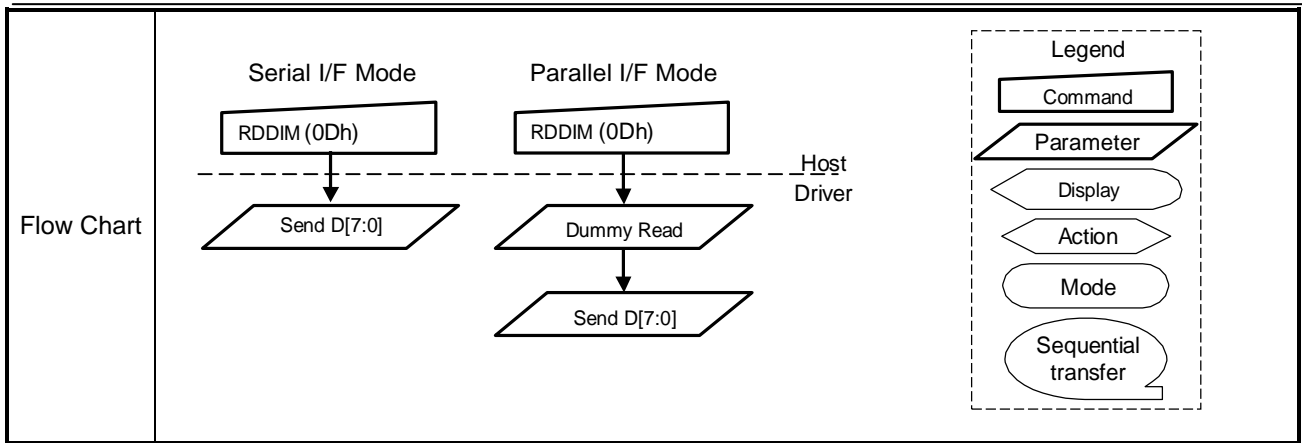
Description	This command indicates the current status of the display as described in the table below:															
	IFPF[2:0]															
	011	3														
	101	5														
Restriction	Others are no define and invalid															
	VIFPF[2:0]															
	0101	5														
	0110	6														
Register Availability	Others are no define and invalid															
	0111	7														
	1110	14														
	Others are no define and invalid															
Default	-															
	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes		
	Status	Availability														
	Normal Mode On, Idle Mode Off, Sleep Out	Yes														
	Normal Mode On, Idle Mode On, Sleep Out	Yes														
Partial Mode On, Idle Mode Off, Sleep Out	Yes															
Partial Mode On, Idle Mode On, Sleep Out	Yes															
Sleep In	Yes															
<table border="1"> <thead> <tr> <th>Status</th> <th colspan="2">Default Value</th> </tr> <tr> <td></td> <th>IFPF[2:0]</th> <th>VIPF[3:0]</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>0110 (18 bits/pixel)</td> <td>0110 (18 bits/pixel)</td> </tr> <tr> <td>S/W Reset</td> <td>No Change</td> <td>No Change</td> </tr> <tr> <td>H/W Reset</td> <td>0110 (18 bits/pixel)</td> <td>0110 (18 bits/pixel)</td> </tr> </tbody> </table>		Status	Default Value			IFPF[2:0]	VIPF[3:0]	Power On Sequence	0110 (18 bits/pixel)	0110 (18 bits/pixel)	S/W Reset	No Change	No Change	H/W Reset	0110 (18 bits/pixel)	0110 (18 bits/pixel)
Status	Default Value															
	IFPF[2:0]	VIPF[3:0]														
Power On Sequence	0110 (18 bits/pixel)	0110 (18 bits/pixel)														
S/W Reset	No Change	No Change														
H/W Reset	0110 (18 bits/pixel)	0110 (18 bits/pixel)														
Flow Chart	<div style="display: flex; justify-content: space-around;"> <div style="text-align: center;"> <p>Serial I/F Mode</p> </div> <div style="text-align: center;"> <p>Parallel I/F Mode</p> </div> </div>															
	<div style="border: 1px dashed black; padding: 5px;"> <p>Legend</p> <ul style="list-style-type: none"> <li><span style="border: 1px solid black; padding: 2px;">Command</span></li> <li><span style="border: 1px solid black; padding: 2px;">Parameter</span></li> <li><span style="border: 1px solid black; padding: 2px;">Display</span></li> <li><span style="border: 1px solid black; padding: 2px;">Action</span></li> <li><span style="border: 1px solid black; padding: 2px;">Mode</span></li> <li><span style="border: 1px solid black; padding: 2px;">Sequential transfer</span></li> </ul> </div>															

## 10.1.8 RDDIM (0Dh): Read Display Image Mode

0DH	RDDIM (0Dh): Read Display Image Mode												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDIM	0	↑	1	-	0	0	0	0	1	1	0	1	(0Dh)
1 <sup>st</sup> Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2 <sup>nd</sup> Parameter	1	1	↑	-	VSSON	D6	INVON	D4	D3	GCS2	GCS1	GCS0	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	This command indicates the current status of the display as described in the table below:																																																																	
	Bit	Description			Value																																																													
	VSSON	Vertical Scrolling On/Off			"1" = Vertical scrolling is On, "0" = Vertical scrolling is Off																																																													
	D6	Horizontal Scrolling On/Off			"0" (Not used)																																																													
	INVON	Inversion On/Off			"1" = Inversion is On, "0" = Inversion is Off																																																													
	D4	All Pixels On			"0" (Not used)																																																													
	D3	All Pixels Off			"0" (Not used)																																																													
	<table border="1"> <thead> <tr> <th>GS</th> <th>GC[7:0] Reg.</th> <th>LCM1</th> <th>LCM0</th> <th>LC Type</th> <th>Gamma</th> </tr> </thead> <tbody> <tr> <td rowspan="7">1</td> <td rowspan="4">01H</td> <td>0</td> <td>0</td> <td>MVA</td> <td rowspan="4">Curve 2.2</td> </tr> <tr> <td>0</td> <td>1</td> <td>Transflective(TR)</td> </tr> <tr> <td>1</td> <td>0</td> <td>Transmissive(TM)</td> </tr> <tr> <td>1</td> <td>1</td> <td>N/A</td> </tr> <tr> <td>02H</td> <td>X</td> <td>X</td> <td>Transflective(TR) 1.8</td> </tr> <tr> <td>04H</td> <td>X</td> <td>X</td> <td>Transflective(TR) 2.5</td> </tr> <tr> <td>08H</td> <td>X</td> <td>X</td> <td>Transflective(TR) 1.0</td> </tr> <tr> <td rowspan="7">0</td> <td>01H</td> <td>X</td> <td>X</td> <td>Transflective(TR) 1.0</td> <td rowspan="7">Curve 2.2</td> </tr> <tr> <td>02H</td> <td>X</td> <td>X</td> <td>Transflective(TR) 2.5</td> </tr> <tr> <td rowspan="4">04H</td> <td>0</td> <td>0</td> <td>MVA</td> </tr> <tr> <td>0</td> <td>1</td> <td>Transflective(TR)</td> </tr> <tr> <td>1</td> <td>0</td> <td>Transmissive(TM)</td> </tr> <tr> <td>1</td> <td>1</td> <td>N/A</td> </tr> <tr> <td>08H</td> <td>X</td> <td>X</td> <td>Transflective(TR) 1.8</td> </tr> </tbody> </table>						GS	GC[7:0] Reg.	LCM1	LCM0	LC Type	Gamma	1	01H	0	0	MVA	Curve 2.2	0	1	Transflective(TR)	1	0	Transmissive(TM)	1	1	N/A	02H	X	X	Transflective(TR) 1.8	04H	X	X	Transflective(TR) 2.5	08H	X	X	Transflective(TR) 1.0	0	01H	X	X	Transflective(TR) 1.0	Curve 2.2	02H	X	X	Transflective(TR) 2.5	04H	0	0	MVA	0	1	Transflective(TR)	1	0	Transmissive(TM)	1	1	N/A	08H	X	X	Transflective(TR) 1.8
	GS	GC[7:0] Reg.	LCM1	LCM0	LC Type	Gamma																																																												
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		1	1	N/A																																																														
	08H	X	X	Transflective(TR) 1.8																																																														
Note 1: While LCM[1:0]="00"																																																																		
Note 2: Even GCS[2:0] value is be changeable from read status, the gamma curve of Transmissive and MVA only $\gamma = 2.2$ .																																																																		
Restriction	-																																																																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>					Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																																																	
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Sleep In	Yes																																																																	
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S/W Reset	0000_0001 (01h)																																																																	
H/W Reset	0000_0001 (01h)																																																																	



## 10.1.9 RDDSM (0Eh): Read Display Signal Mode

0EH	RDDSM (0Eh): Read Display Signal Mode												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDSM	0	↑	1	-	0	0	0	0	1	1	1	0	(0Eh)
1 <sup>st</sup> Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2 <sup>nd</sup> Parameter	1	1	↑	-	TEON	TELOM	HSON	VSON	PCKON	DEON	D1	D0	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	This command indicates the current status of the display as described in the table below:	
	<b>Bit</b>	<b>Description</b>
	TEON	Tearing Effect Line On/Off
	TELOM	Tearing effect line mode
	HSON	Horizontal Sync. (RGB I/F) On/Off
	VSON	Vertical Sync. (RGB I/F) On/Off
	PCKON	Pixel Clock (PCLK, RGB I/F) On/Off
	DEON	Data Enable (DE, RGB I/F) On/Off
	D1	Not Used
D0	Not Used	
Restriction	-	
Register Availability	<b>Status</b>	<b>Availability</b>
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	<b>Status</b>	<b>Default Value(D7~D0)</b>
	Power On Sequence	00h
	S/W Reset	00h
	H/W Reset	00h
Flow Chart	<div style="display: flex; justify-content: space-around;"> <div style="text-align: center;"> <p>Serial I/F Mode</p> </div> <div style="text-align: center;"> <p>Parallel I/F Mode</p> </div> </div> <p style="text-align: center;">Host Driver</p>	
	<div style="border: 1px dashed black; padding: 5px;"> <p>Legend</p> <ul style="list-style-type: none"> <li><span style="border: 1px solid black; display: inline-block; width: 20px; height: 10px; margin-right: 5px;"></span> Command</li> <li><span style="border: 1px solid black; display: inline-block; width: 20px; height: 10px; transform: rotate(-45deg); margin-right: 5px;"></span> Parameter</li> <li><span style="border: 1px solid black; display: inline-block; width: 20px; height: 10px; border-radius: 5px; margin-right: 5px;"></span> Display</li> <li><span style="border: 1px solid black; display: inline-block; width: 20px; height: 10px; border-radius: 5px; margin-right: 5px;"></span> Action</li> <li><span style="border: 1px solid black; display: inline-block; width: 20px; height: 10px; border-radius: 5px; margin-right: 5px;"></span> Mode</li> <li><span style="border: 1px solid black; display: inline-block; width: 20px; height: 10px; border-radius: 5px; margin-right: 5px;"></span> Sequential transfer</li> </ul> </div>	



## 10.1.10 RDDSDR (0Fh): Read Display Self-Diagnostic Result

0FH	RDDSDR (0Fh): Read Display Self-Diagnostic Result												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDSDR	0	↑	1	-	0	0	0	0	1	1	1	1	(0Fh)
1 <sup>st</sup> Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2 <sup>nd</sup> Parameter	1	1	↑	-	RELD	FUND	ATTD	BRD	D3	D2	D1	D0	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	This command indicates the current status of the display as described in the table below:	
	<b>Bit</b>	<b>Description</b>
	RELD	Register Loading Detection
	FUND	Functionality Detection
	ATTD	Chip Attachment Detection
	BRD	Display Glass Break Detection
	D3	Not Used
	D2	Not Used
D1	Not Used	
D0	Not Used	
Restriction	-	
Register Availability	<b>Status</b>	<b>Availability</b>
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes	
Default	<b>Status</b>	<b>Default Value(D7~D0)</b>
	Power On Sequence	
	S/W Reset	
	H/W Reset	
Flow Chart	<div style="display: flex; justify-content: space-around;"> <div style="text-align: center;"> <p>Serial I/F Mode</p> <p>RDDSDR (0Fh)</p> <p>↓</p> <p>Send D[7:0]</p> </div> <div style="text-align: center;"> <p>Parallel I/F Mode</p> <p>RDDSDR (0Fh)</p> <p>↓</p> <p>Dummy Read</p> <p>↓</p> <p>Send D[7:0]</p> </div> </div> <p style="text-align: center; margin-top: 10px;">Host Driver</p>	
	<div style="border: 1px dashed black; padding: 5px;"> <p>Legend</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul> </div>	

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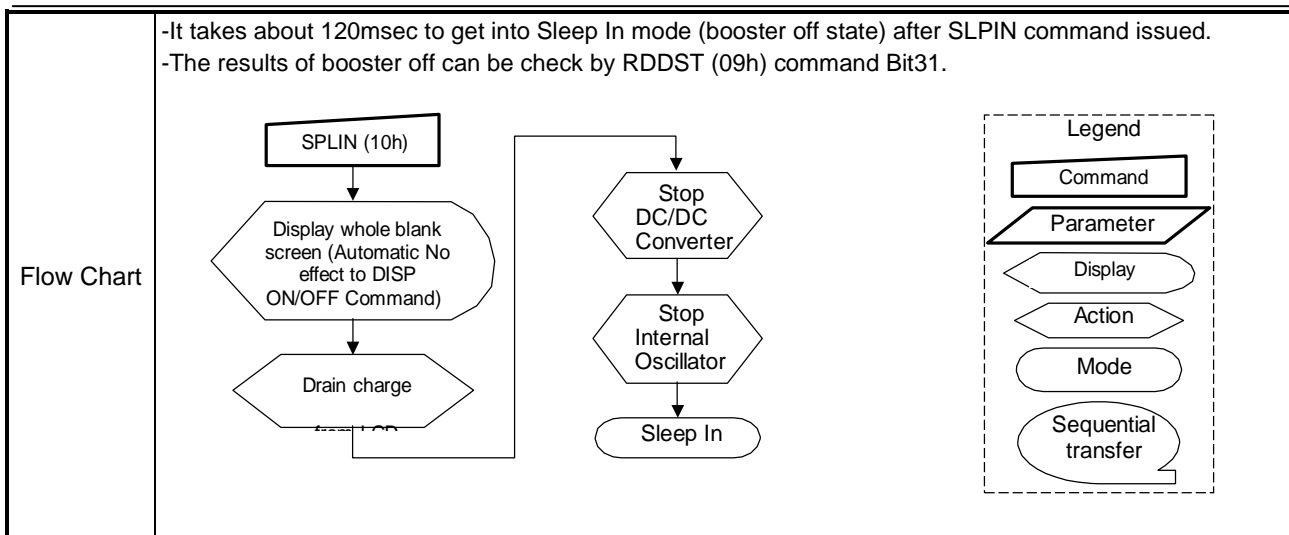
## 10.1.11 SLPIN (10h): Sleep In

10H	SLPIN (Sleep In)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SLPIN	0	↑	1	-	0	0	0	1	0	0	0	0	(10h)
1 <sup>st</sup> Parameter	No parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	<p>-This command causes the LCD module to enter the minimum power consumption mode. -In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped.</p> <p>* Note: complete 1 frame display (ex: continue 2-falling edges of VS)</p>												
	<p>-MCU interface and memory are still working and the memory keeps its contents</p>												
Restriction	<p>-This command has no effect when module is already in sleep in mode. Sleep In Mode can only be exit by the Sleep Out Command (11h). -It will be necessary to wait <u>120msec</u> before sending next command , this is to allow time for the supply voltages and clock circuits to stabilize. -It will be necessary to wait <u>120msec</u> after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.</p>												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Sleep in mode</td> </tr> <tr> <td>S/W Reset</td> <td>Sleep in mode</td> </tr> <tr> <td>H/W Reset</td> <td>Sleep in mode</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Sleep in mode	S/W Reset	Sleep in mode	H/W Reset	Sleep in mode				
Status	Default Value												
Power On Sequence	Sleep in mode												
S/W Reset	Sleep in mode												
H/W Reset	Sleep in mode												

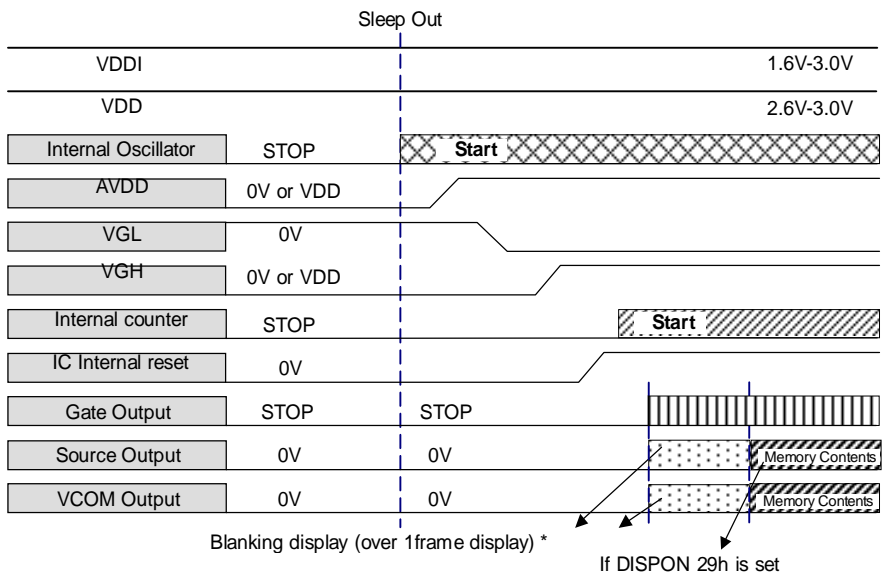
# ST7787



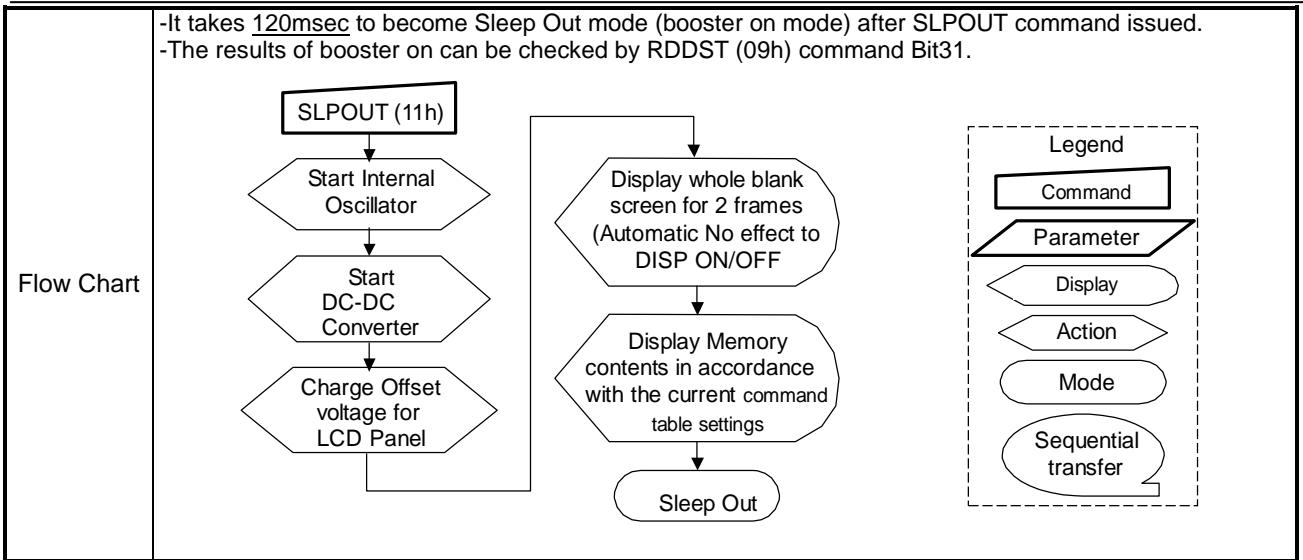
## 10.1.12 SLPOUT (11h): Sleep Out

11H	SLPOUT (Sleep Out)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SLPOUT	0	↑	1	-	0	0	0	1	0	0	0	1	(11h)
1st Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	<p>-This command turns off sleep mode. -In this mode the DC/DC converter is enabled, Internal display oscillator is started, and panel scanning is started.</p>  <p>* Note: complete 1 frame display (ex: continue 2-falling edges of VS)</p>												
Restriction	<p>-This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be exit by the Sleep In Command (10h). -It will be necessary to wait <b>120msec</b> before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. -DRIVER loads all default values of extended and test command to the registers during this 120msec and there cannot be any abnormal visual effect on the display image if those default and register values are same when this load is done and when the DRIVER is already Sleep Out mode. -DRIVER is doing self-diagnostic functions during this <b>120msec</b>. See also section 9.20. -It will be necessary to wait <b>120msec</b> after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent</p>												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Sleep in mode</td> </tr> <tr> <td>S/W Reset</td> <td>Sleep in mode</td> </tr> <tr> <td>H/W Reset</td> <td>Sleep in mode</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Sleep in mode	S/W Reset	Sleep in mode	H/W Reset	Sleep in mode				
Status	Default Value												
Power On Sequence	Sleep in mode												
S/W Reset	Sleep in mode												
H/W Reset	Sleep in mode												

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## 10.1.13 PTLON (12h): Partial Display Mode On

12H	PTLON (12h): Partial Display Mode On												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PTLON	0	↑	1	-	0	0	0	1	0	0	1	0	(12h)
1 <sup>st</sup> Parameter	No Parameter												

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	<p>-This command turns on Partial mode. The partial mode window is described by the Partial Area command (30h)</p> <p>-To leave Partial mode, the Normal Display Mode On command (13H) should be written.</p> <p>-There is no abnormal visual effect during mode change between Normal mode On &lt;-&gt; Partial mode On.</p>													
Restriction	This command has no effect when Partial mode is active.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
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Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
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Status	Default Value													
Power On Sequence	Normal Mode On													
S/W Reset	Normal Mode On													
H/W Reset	Normal Mode On													
Flow Chart	See Partial Area (30h)													

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## 10.1.14 NORON (13h): Normal Display Mode On

13H	NORON (Normal Display Mode On)												(Code)
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	
NORON	0	↑	1	-	0	0	0	1	0	0	1	1	(13h)
1 <sup>st</sup> Parameter	No Parameter												-

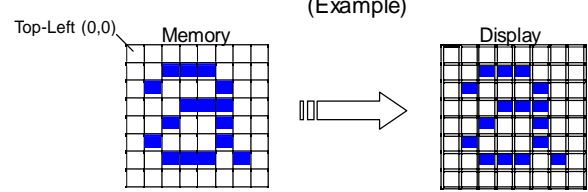

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	<ul style="list-style-type: none"> <li>-This command returns the display to normal mode.</li> <li>-Normal display mode on means <u>Partial mode off</u>, <u>Scroll mode Off</u>.</li> <li>-Exit from NORON by the Partial mode On command (12h)</li> <li>-There is no abnormal visual effect during mode change from Normal mode On to Partial mode On.</li> </ul>													
Restriction	-This command has no effect when Normal Display mode is active.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability												
	Normal Mode On, Idle Mode Off, Sleep Out	Yes												
	Normal Mode On, Idle Mode On, Sleep Out	Yes												
	Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
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	Status	Default Value												
	Power On Sequence	Normal Mode On												
S/W Reset	Normal Mode On													
H/W Reset	Normal Mode On													
Flow Chart	-See Partial Area and Vertical Scrolling Definition Descriptions for details of when to use this command													

## 9.1.15 INVOFF (20h): Display Inversion Off

20H	IVNOFF (Normal Display Mode Off)												(Code)
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	
INVOFF	0	↑	1	-	0	0	1	0	0	0	0	0	(20h)
1 <sup>st</sup> Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	<p>-This command is used to recover from display inversion mode.                      -This command makes no change of <u>contents</u> of frame memory.                      -This command does not change any other status.</p> <p>(Example)</p> 													
	Restriction	-This command has no effect when module is already inversion off mode.												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability												
	Normal Mode On, Idle Mode Off, Sleep Out	Yes												
	Normal Mode On, Idle Mode On, Sleep Out	Yes												
	Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display Inversion off</td> </tr> <tr> <td>S/W Reset</td> <td>Display Inversion off</td> </tr> <tr> <td>H/W Reset</td> <td>Display Inversion off</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	Display Inversion off	S/W Reset	Display Inversion off	H/W Reset	Display Inversion off				
	Status	Default Value												
	Power On Sequence	Display Inversion off												
S/W Reset	Display Inversion off													
H/W Reset	Display Inversion off													
Flow Chart														



## 10.1.16 INVON (21h): Display Inversion On

21H	IVNOFF (Display Inversion On)												(Code)
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	
INVON	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)
1 <sup>st</sup> Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	<p>-This command is used to enter into display inversion mode                  -This command makes no change of <u>contents of frame memory</u>.                  -This command does not change any other status.                  -To exit from Display Inversion On, the Display Inversion Off command (20h) should be written.</p>													
	<p>(Example)</p>													
Restriction	-This command has no effect when module is already Inversion On mode.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display Inversion off</td> </tr> <tr> <td>S/W Reset</td> <td>Display Inversion off</td> </tr> <tr> <td>H/W Reset</td> <td>Display Inversion off</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	Display Inversion off	S/W Reset	Display Inversion off	H/W Reset	Display Inversion off				
Status	Default Value													
Power On Sequence	Display Inversion off													
S/W Reset	Display Inversion off													
H/W Reset	Display Inversion off													
Flow Chart														

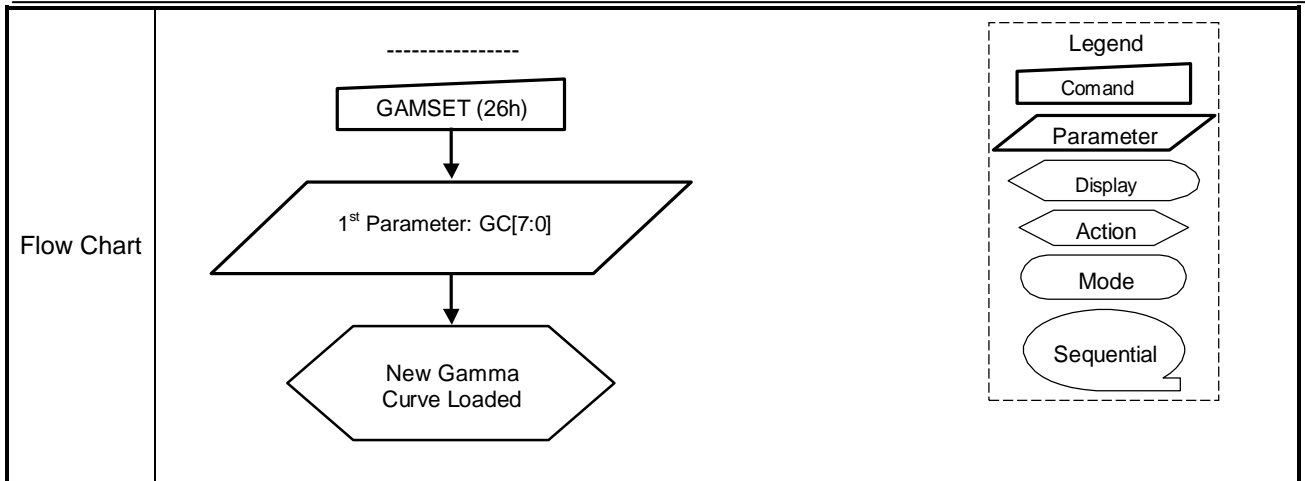
## 10.1.17 GAMSET (26h): Gamma Set

26H	GAMSET (Gamma Set)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GAMSET	0	↑	1	-	0	0	1	0	0	1	1	0	(26h)
1 <sup>st</sup> Parameter	1	↑	1	-	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	-This command is used to select the desired Gamma curve for the current display. A maximum of 4 curves can be selected. The curves are defined in section 9.17 The curve is selected by setting the appropriate bit in the parameter as described in the Table.																	
	GS	GC[7:0] Reg.	LCM1	LCM0	LC Type	Gamma												
1	01H		0	0	MVA	Curve 2.2												
			0	1	Transflective(TR)													
			1	0	Transmissive(TM)													
			1	1	N/A													
	02H		X	X	Transflective(TR) 1.8													
	04H		X	X	Transflective(TR) 2.5													
	08H		X	X	Transflective(TR) 1.0													
	0	01H		X	X	Transflective(TR) 1.0												
		02H		X	X	Transflective(TR) 2.5												
		04H		0	0	MVA	Curve 2.2											
0				1	Transflective(TR)													
1				0	Transmissive(TM)													
1	1	N/A																
08H		X	X	Transflective(TR) 1.8														
Restriction	-Values of GC [7:0] not shown in table above are invalid and will not change the current selected Gamma curve until valid is received.																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>					Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	
Status	Availability																	
Normal Mode On, Idle Mode Off, Sleep Out	Yes																	
Normal Mode On, Idle Mode On, Sleep Out	Yes																	
Partial Mode On, Idle Mode Off, Sleep Out	Yes																	
Partial Mode On, Idle Mode On, Sleep Out	Yes																	
Sleep In	Yes																	
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>01h</td> </tr> <tr> <td>S/W Reset</td> <td>01h</td> </tr> <tr> <td>H/W Reset</td> <td>01h</td> </tr> </tbody> </table>					Status	Default Value	Power On Sequence	01h	S/W Reset	01h	H/W Reset	01h					
Status	Default Value																	
Power On Sequence	01h																	
S/W Reset	01h																	
H/W Reset	01h																	

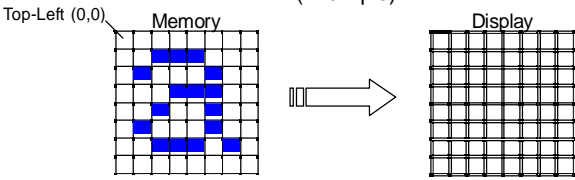
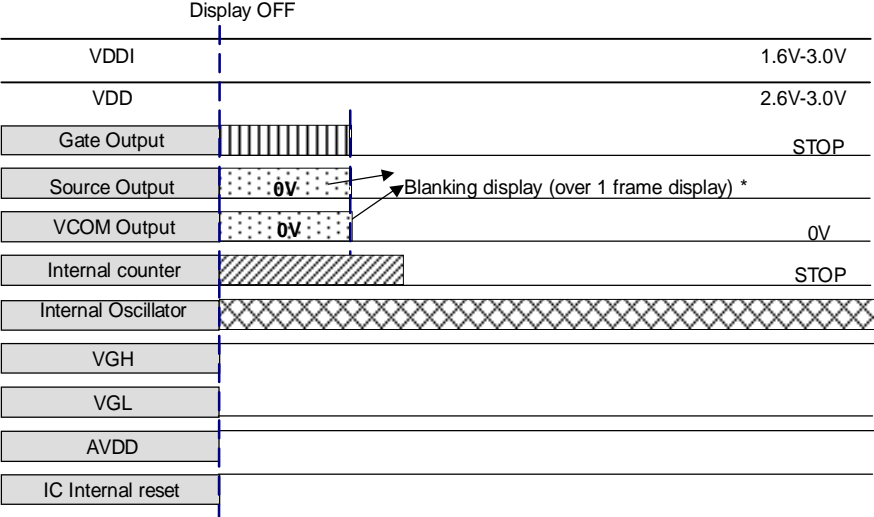
# ST7787



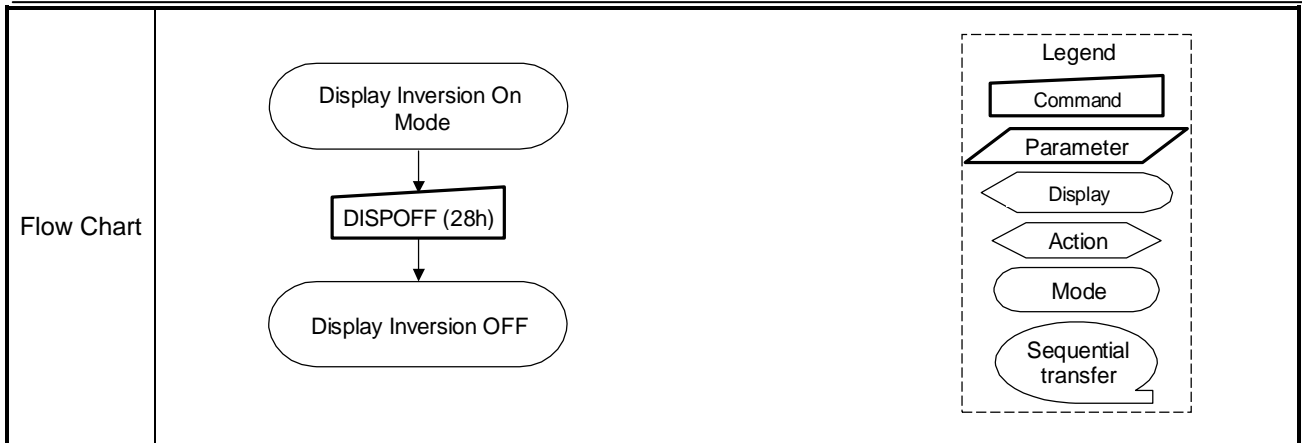
## 10.1.18 DISPOFF (28h): Display Off

28H	DISPOFF (Display Off)												(Code)
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DISPOFF	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)
1 <sup>st</sup> Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	<p>-This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted.</p> <p>-This command makes no change of contents of frame memory.</p> <p>-This command does not change any other status.</p> <p>-There will be no abnormal visible effect on the display.</p> <p>-Exit from this command by Display On (29h)</p>													
	<p>(Example)</p>  <p>Display OFF</p>  <p>* Note: complete 1 frame display (ex: continue 2-falling edges of VS)</p>													
Restriction	-This command has no effect when module is already in Display Off mode.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
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Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display off</td> </tr> <tr> <td>S/W Reset</td> <td>Display off</td> </tr> <tr> <td>H/W Reset</td> <td>Display off</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	Display off	S/W Reset	Display off	H/W Reset	Display off				
Status	Default Value													
Power On Sequence	Display off													
S/W Reset	Display off													
H/W Reset	Display off													

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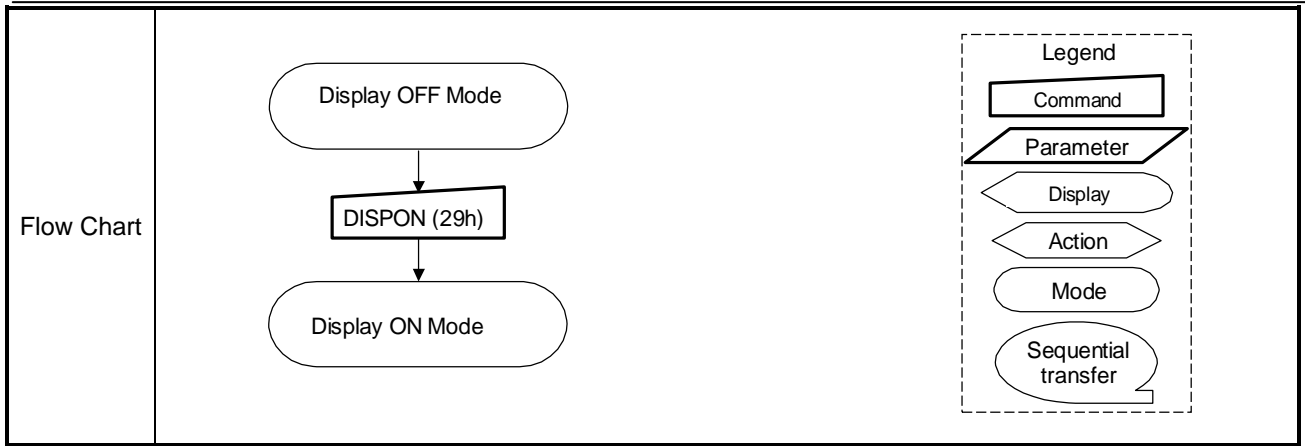
## 10.1.19 DISPON (29h): Display On

29H	DISPON (Display On)												(Code)
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DISPON	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)
1 <sup>st</sup> Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	<p>-This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled.                  -This command makes no change of contents of frame memory.                  -This command does not change any other status.</p>													
	<div style="text-align: center;"> </div>													
Restriction	-This command has no effect when module is already in Display On mode.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
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Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
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Status	Default Value													
Power On Sequence	Display off													
S/W Reset	Display off													
H/W Reset	Display off													

# ST7787



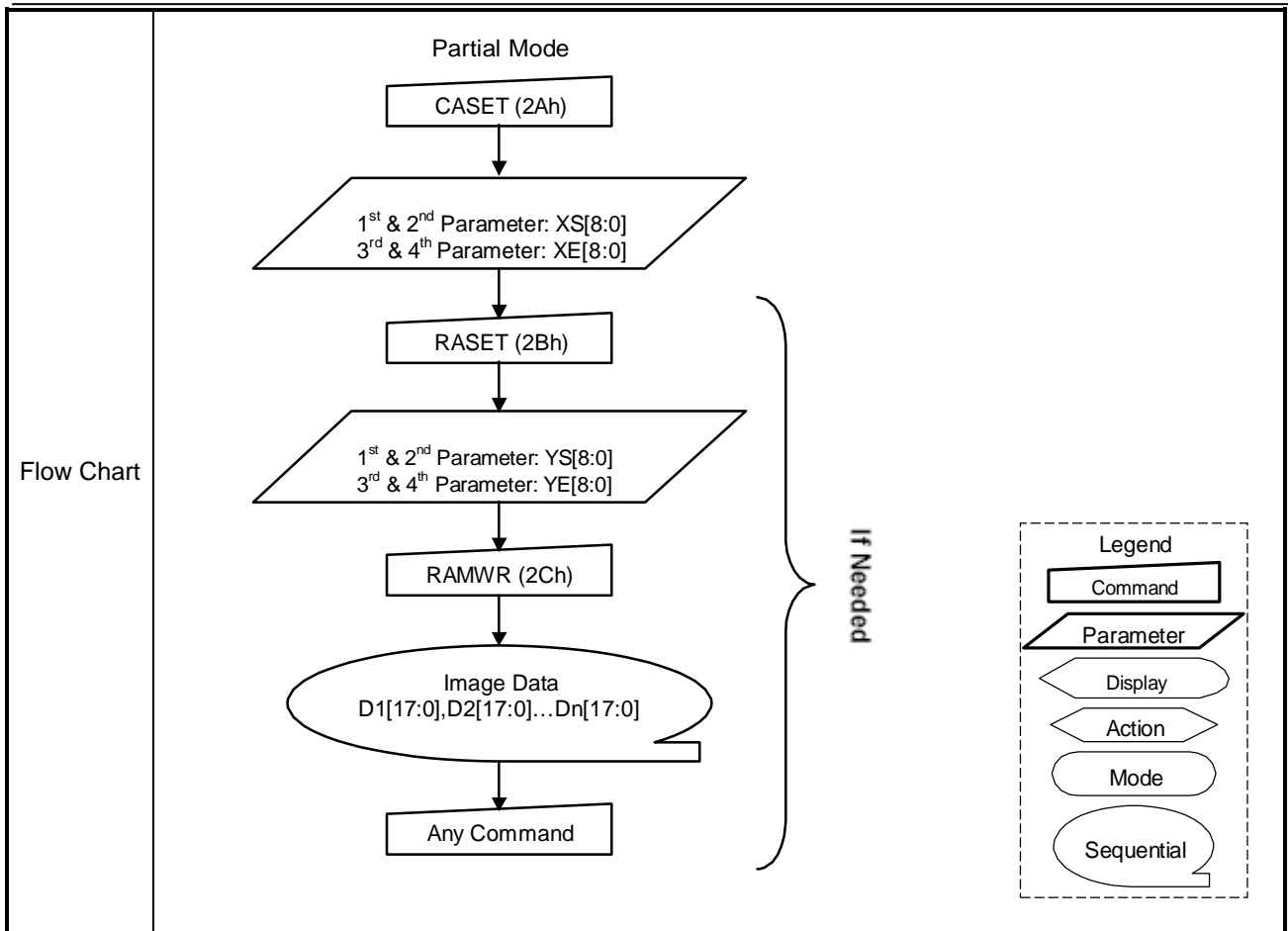
## 10.1.20 CASET (2Ah): Column Address Set

2AH	CASET(Colume Address Set)_												(Code)
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GAMSET	0	↑	1	-	0	0	1	0	0	1	1	0	(2Ah)
1 <sup>st</sup> Parameter	1	↑	1	-	-	-	-	-	-	-	-	XS8	
2 <sup>nd</sup> Parameter	1	↑	1		XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	
3 <sup>rd</sup> Parameter	1	↑	1		-	-	-	-	-	-	-	XE8	
4 <sup>th</sup> Parameter	1	↑	1		XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	<ul style="list-style-type: none"> <li>-This command is used to define area of frame memory where MCU can access.</li> <li>-This command makes no change on the other driver status.</li> <li>-The value of XS [8:0] and XE [8:0] are referred when RAMWR command comes.</li> <li>-Each value represents one column line in the Frame Memory.</li> </ul>															
	<p>(Example)</p>															
Restriction	<p>Xaddress start: <math>0 \leq XS \leq EF</math>            MV=0            Xaddress end: <math>XS \leq XE \leq EF</math>            MV=0</p>															
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes		
Status	Availability															
Normal Mode On, Idle Mode Off, Sleep Out	Yes															
Normal Mode On, Idle Mode On, Sleep Out	Yes															
Partial Mode On, Idle Mode Off, Sleep Out	Yes															
Partial Mode On, Idle Mode On, Sleep Out	Yes															
Sleep In	Yes															
Default	<p>1. 240x320 memory base</p> <table border="1"> <thead> <tr> <th rowspan="2">2Status</th> <th colspan="2">Default Value</th> </tr> <tr> <th>XS[8:0]</th> <th>XE[8:0]</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>0000h</td> <td>00EFh</td> </tr> <tr> <td>S/W Reset</td> <td>0000h</td> <td>00EFh</td> </tr> <tr> <td>H/W Reset</td> <td>0000h</td> <td>00EFh</td> </tr> </tbody> </table>		2Status	Default Value		XS[8:0]	XE[8:0]	Power On Sequence	0000h	00EFh	S/W Reset	0000h	00EFh	H/W Reset	0000h	00EFh
2Status	Default Value															
	XS[8:0]	XE[8:0]														
Power On Sequence	0000h	00EFh														
S/W Reset	0000h	00EFh														
H/W Reset	0000h	00EFh														



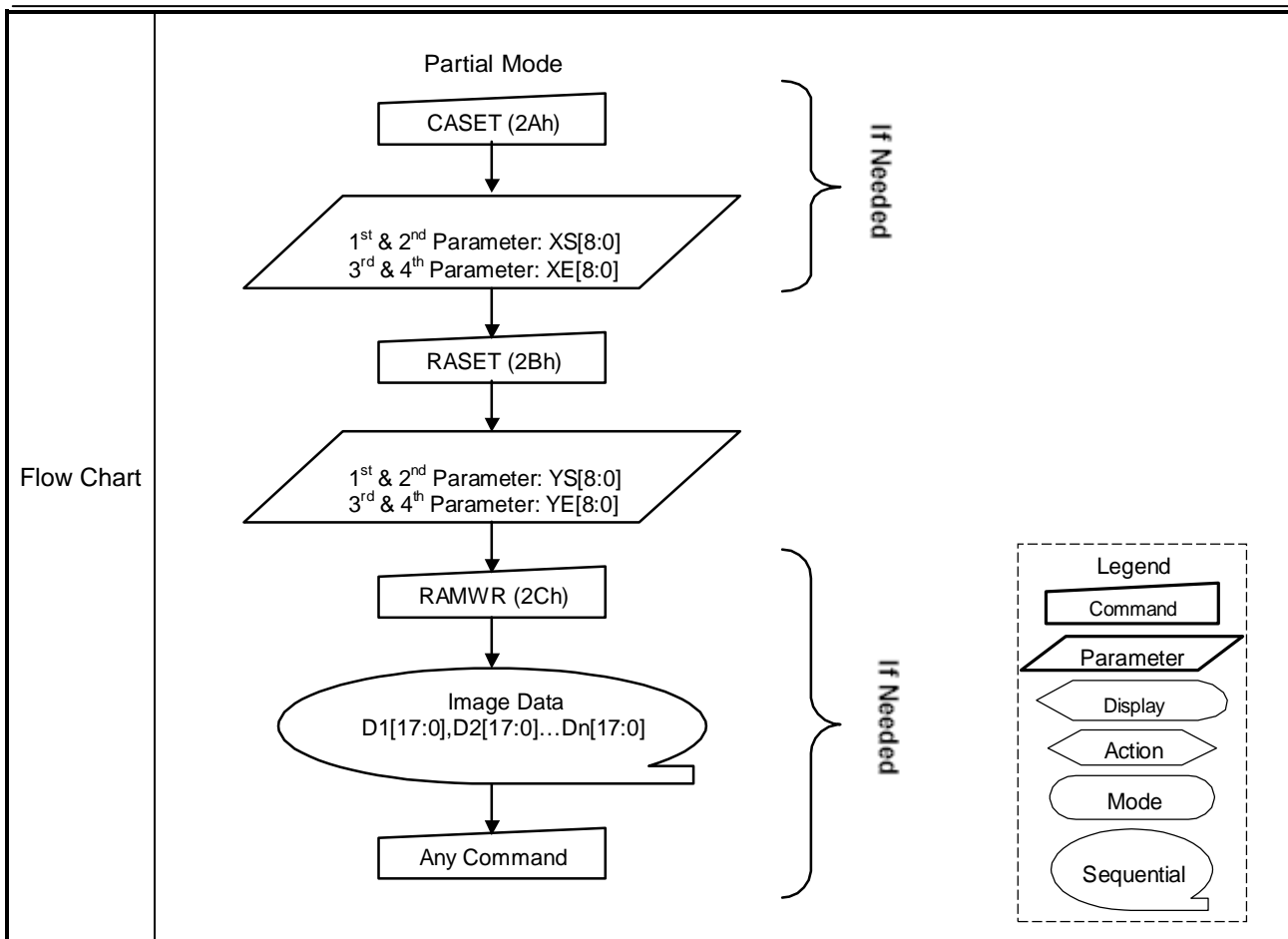


## 10.1.21 RASET (2Bh): Row Address Set

2BH	RASET (Row Address Set)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RASET (2Bh)	0	↑	1	-	0	0	1	0	1	0	1	1	(2Bh)
1st Parameter	1	↑	1	-	-	-	-	-	-	-	-	YS8	
2nd Parameter	1	↑	1	-	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
3rd Parameter	1	↑	1	-	-	-	-	-	-	-	-	YE8	
4th Parameter	1	↑	1	-	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	<p>This command is used to define area of frame memory where MCU can access.                  This command makes no change on the other driver status.                  The value of YS [8:0] and YE [8:0] are referred when RAMWR command comes.                  Each value represents one column line in the Frame Memory.</p> <p style="text-align: center;">Example</p>															
	Restriction	<p>Xaddress start: <math>0 \leq YS \leq 13F</math>                  MV=0                  Xaddress end: <math>YS \leq YE \leq 13F</math>                  MV=0</p>														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes		
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Normal Mode On, Idle Mode On, Sleep Out	Yes															
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Partial Mode On, Idle Mode On, Sleep Out	Yes															
Sleep In	Yes															
Default	<p>1. 240x320 memory base</p> <table border="1"> <thead> <tr> <th rowspan="2">2Status</th> <th colspan="2">Default Value</th> </tr> <tr> <th>YS[8:0]</th> <th>YE[8:0]</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>0000h</td> <td>013Fh</td> </tr> <tr> <td>S/W Reset</td> <td>0000h</td> <td>013Fh</td> </tr> <tr> <td>H/W Reset</td> <td>0000h</td> <td>013Fh</td> </tr> </tbody> </table>		2Status	Default Value		YS[8:0]	YE[8:0]	Power On Sequence	0000h	013Fh	S/W Reset	0000h	013Fh	H/W Reset	0000h	013Fh
2Status	Default Value															
	YS[8:0]	YE[8:0]														
Power On Sequence	0000h	013Fh														
S/W Reset	0000h	013Fh														
H/W Reset	0000h	013Fh														



## 10.1.22 RAMWR (2Ch): Memory Write

2CH	RAMWR (Memory Write)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RAMWR	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)
1st Parameter	1	↑	1	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	-
Nth Parameter	1	↑	1	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	<p>-This command is used to transfer data from MCU to frame memory.</p> <p>-This command makes no change to the other driver status.</p> <p>-When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions.</p> <p>-The Start Column/Start Row positions are different in accordance with MADCTL setting. (See section 9.12)</p> <p>-Then D[23:0] is stored in frame memory and the column register and the row register incremented as section 9.10.2.</p> <p>-Sending any other command can stop Frame Write.</p>													
Restriction														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	
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Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Contents of memory is set randomly</td> </tr> <tr> <td>S/W Reset</td> <td>Contents of memory is not cleared</td> </tr> <tr> <td>H/W Reset</td> <td>Contents of memory is not cleared</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Contents of memory is set randomly	S/W Reset	Contents of memory is not cleared	H/W Reset	Contents of memory is not cleared					
Status	Default Value													
Power On Sequence	Contents of memory is set randomly													
S/W Reset	Contents of memory is not cleared													
H/W Reset	Contents of memory is not cleared													
Flow Chart														

## 10.1.23 RAMRD (2Eh): Memory Read

2Eh	RAMRD (Memory Read)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RAMRD	0	↑	1	-	0	0	1	0	1	1	1	0	(2Eh)
1 <sup>st</sup> Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2 <sup>nd</sup> Parameter	1	1	↑	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	-
(N+1) <sup>th</sup> Parameter	1	1	↑	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	-

NOTE: "-" Don't care, can be set to VDDI or DGND level

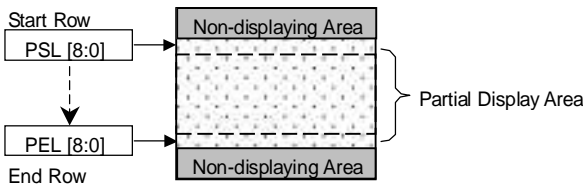
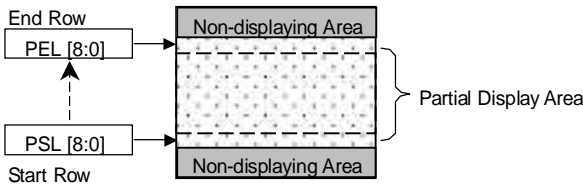
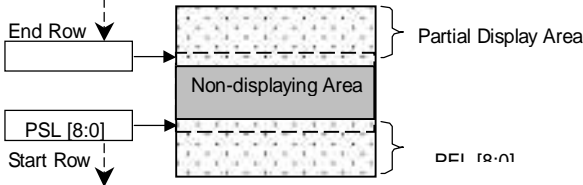
Description	<ul style="list-style-type: none"> <li>-This command is used to transfer data from frame memory to MCU.</li> <li>-This command makes no change to the other driver status.</li> <li>-When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions.</li> <li>-The Start Column/Start Row positions are different in accordance with MADCTL setting. (See section 9.12)</li> <li>-Then D[23:0] is read back from the frame memory and the column register and the row register incremented as section 9.10.2.</li> <li>-Frame Read can be canceled by sending any other command.</li> <li>-See section 9.8 "Data color coding" for color coding (18-bit cases), when there is used 8, 9, 16 and 18-bit data lines for image data.</li> </ul>												
Restriction	<ul style="list-style-type: none"> <li>-In all color modes, the Frame Read is always 18- bits and there is no restriction on length of parameters.</li> <li>-Memory read is only possible via the SPI and parallel interface</li> </ul>												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
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Partial Mode On, Idle Mode Off, Sleep Out	Yes												
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Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Contents of memory is set randomly</td> </tr> <tr> <td>S/W Reset</td> <td>Contents of memory is not cleared</td> </tr> <tr> <td>H/W Reset</td> <td>Contents of memory is not cleared</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Contents of memory is set randomly	S/W Reset	Contents of memory is not cleared	H/W Reset	Contents of memory is not cleared				
Status	Default Value												
Power On Sequence	Contents of memory is set randomly												
S/W Reset	Contents of memory is not cleared												
H/W Reset	Contents of memory is not cleared												
Flow Chart	<pre> graph TD     A[RAMRD (2Eh)] --&gt; B[/Dummy Read/]     B --&gt; C([Image Data D1[17:0], D2[17:0]...Dn[17:0]])     C --&gt; D[Any Command]     </pre>												

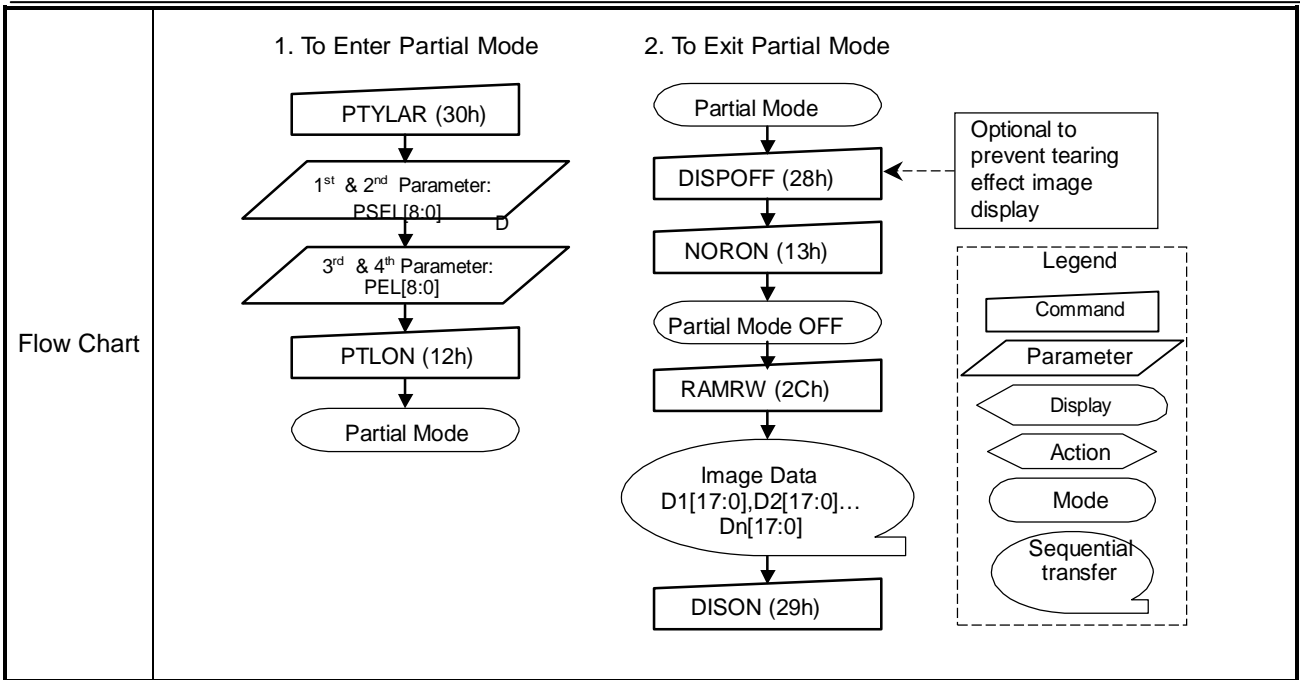
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## 10.1.24 PTLAR (30h): Partial Area

30H	PTLAR (Partial Area)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PTLAR	0	↑	1	-	0	0	1	1	0	0	0	0	(30h)
1 <sup>st</sup> Parameter	1	↑	1	-	--	--	--	--	--	--	--	PSL8	
2 <sup>nd</sup> Parameter	1	↑	1	-	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	
3 <sup>rd</sup> Parameter	1	↑	1	-	--	--	--	--	--	--	--	PEL8	
4 <sup>th</sup> Parameter	1	↑	1	-	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0	

NOTE: "--" Don't care, can be set to VDDI or DGND level

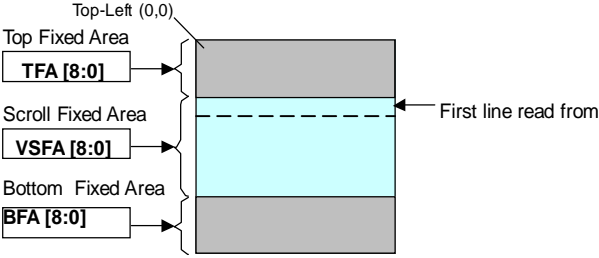
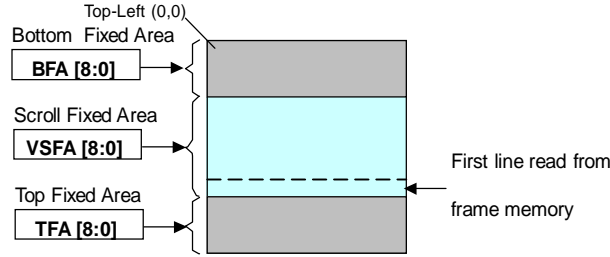
Description	<p>-This command defines the partial mode's display area.                  -There are 4 parameters associated with this command, the first defines the Start Row (PSL) and the second the End Row (PEL), as illustrated in the figures below. PSL and PEL refer to the Frame Memory row address counter.</p> <p>-If End Row &gt; Start Row, when MADCTL ML='0'</p>  <p>-If End Row &gt; Start Row, when MADCTL ML='1'</p>  <p>-If End Row &lt; Start Row, when MADCTL ML='0'</p>  <p>-If End Row = Start Row then the Partial Area will be one row deep.</p>																											
	Restriction	-																										
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes														
	Status	Availability																										
	Normal Mode On, Idle Mode Off, Sleep Out	Yes																										
	Normal Mode On, Idle Mode On, Sleep Out	Yes																										
	Partial Mode On, Idle Mode Off, Sleep Out	Yes																										
Partial Mode On, Idle Mode On, Sleep Out	Yes																											
Sleep In	Yes																											
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="4">Default Value</th> </tr> <tr> <th>PSL[8]</th> <th>PSL[7:0]</th> <th>PE[8]</th> <th>PEL[7:0]</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>0h</td> <td>0000h</td> <td>0h</td> <td>0000h</td> </tr> <tr> <td>S/W Reset</td> <td>0h</td> <td>0000h</td> <td>0h</td> <td>0000h</td> </tr> <tr> <td>H/W Reset</td> <td>0h</td> <td>0000h</td> <td>0h</td> <td>0000h</td> </tr> </tbody> </table>				Status	Default Value				PSL[8]	PSL[7:0]	PE[8]	PEL[7:0]	Power On Sequence	0h	0000h	0h	0000h	S/W Reset	0h	0000h	0h	0000h	H/W Reset	0h	0000h	0h	0000h
	Status	Default Value																										
		PSL[8]	PSL[7:0]	PE[8]	PEL[7:0]																							
	Power On Sequence	0h	0000h	0h	0000h																							
S/W Reset	0h	0000h	0h	0000h																								
H/W Reset	0h	0000h	0h	0000h																								
www.DataSheet4U.com																												



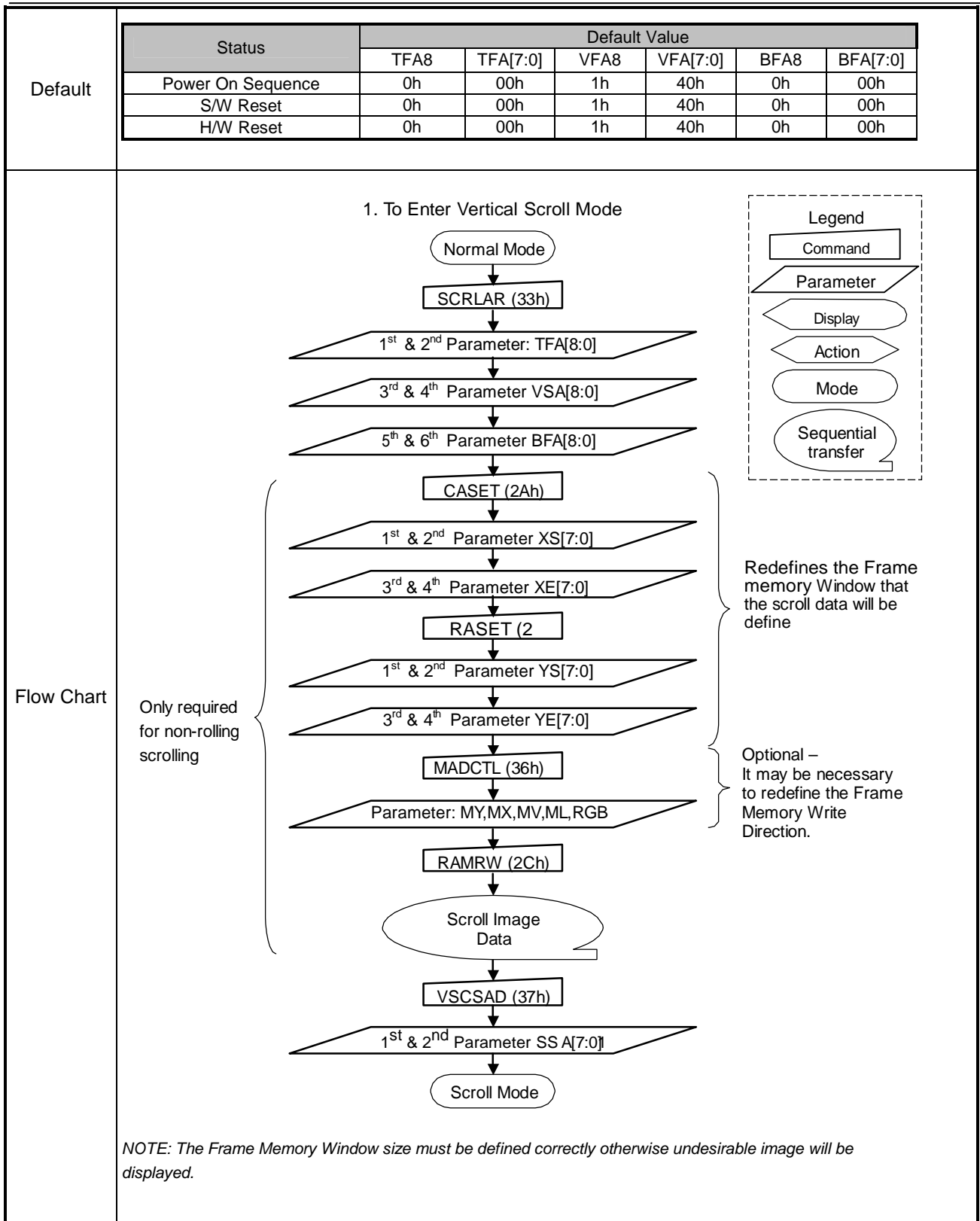
## 10.1.25 SCRLAR (33h): Scroll Area

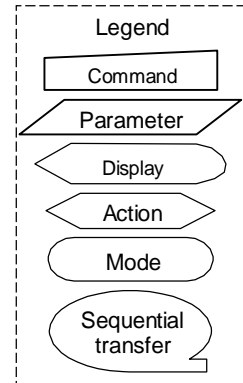
33H	SCRLAR (Scroll Area)												(Code)
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PTLAR	0	↑	1	-	0	0	1	1	0	0	1	1	(33h)
1 <sup>st</sup> Parameter	1	↑	1	-	---	---	---	---	---	---	---	TFA8	
2 <sup>nd</sup> Parameter	1	↑	1	-	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	
3 <sup>rd</sup> Parameter	1	↑	1	-	---	---	---	---	---	---	---	VSA8	
4 <sup>th</sup> Parameter	1	↑	1	-	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	
5 <sup>th</sup> Parameter	1	↑	1	-	---	---	---	---	---	---	---	BFA8	
6 <sup>th</sup> Parameter	1	↑	1	-	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	

NOTE: "-" Don't care, can be set to VDDI or DGND level

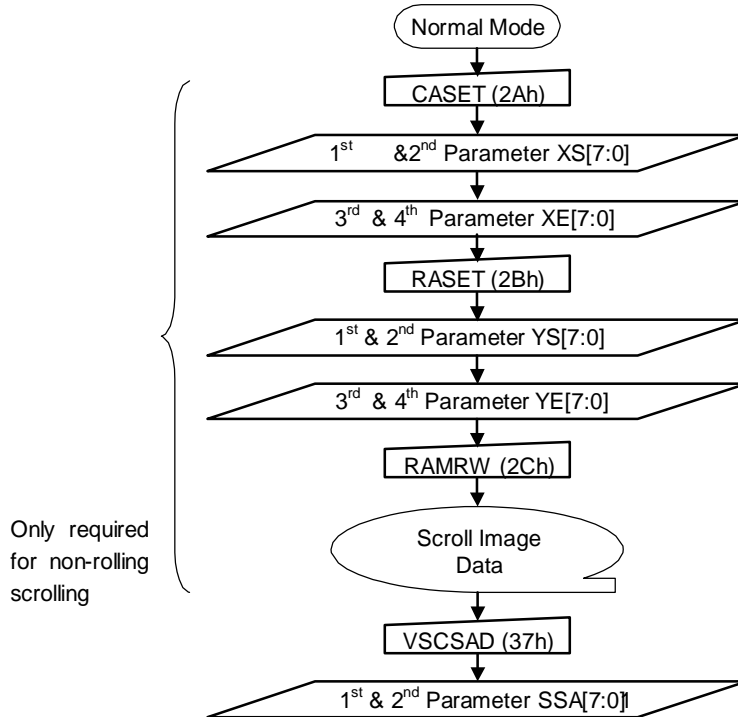
Description	<p>-This command defines the Vertical Scrolling Area of the display.</p> <p>When MADCTL ML=0</p> <ul style="list-style-type: none"> <li>- The 1<sup>st</sup> &amp; 2<sup>nd</sup> parameter TFA [8:0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).</li> <li>- The 3<sup>rd</sup> &amp; 4<sup>th</sup> parameter VSA [8:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address)</li> <li>- The first line appears immediately after the bottom most line of the Top Fixed Area.</li> <li>- The 5<sup>th</sup> &amp; 6<sup>th</sup> parameter BFA [8:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).</li> <li>- TFA, VSA and BFA refer to the Frame Memory row address.</li> </ul> 												
	<p>When MADCTL ML=1</p> <ul style="list-style-type: none"> <li>- The 1<sup>st</sup> &amp; 2<sup>nd</sup> parameter TFA [8:0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).</li> <li>- The 3<sup>rd</sup> &amp; 4<sup>th</sup> parameter VSA [8:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address)</li> <li>- The first line appears immediately after the top most line of the Top Fixed Area.</li> <li>- The 5<sup>th</sup> &amp; 6<sup>th</sup> parameter BFA [8:0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).</li> </ul>  <p>See Section 9.10.4 for details of the Memory to Display Mapping.</p>												
Restriction	-In Vertical Scroll Mode, MADCTL parameter MV should be set to '0'-this only affects the Frame Memory Write. TFA[8:0]+VSA[8:0]+BFA[8:0] must equal to 320 or abnoemal display will be observed.												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												



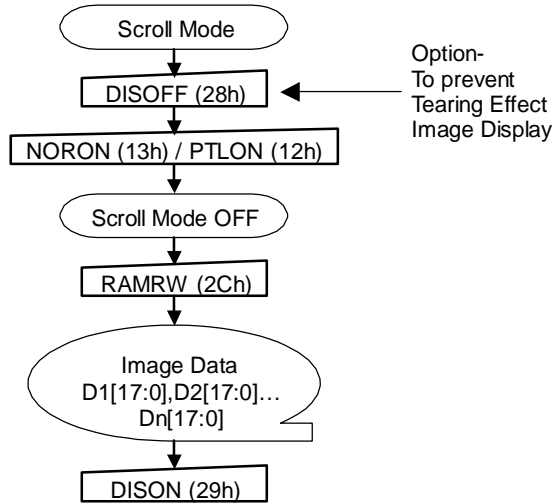




2. Continuous Scroll



3. To Exit Vertical Scroll Mode



NOTE: Scroll Mode can be exit by both the Normal Display Mode On (13h) and Partial Mode On (12h) commands.

# ST7787

## 10.1.26 TEOFF (34h): Tearing Effect Line OFF

34H	TEOFF (Tearing Effect Line OFF)												(Code)
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	
TEOFF	0	↑	1	-	0	0	1	1	0	1	0	0	(34h)
1st Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	-This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.	
Restriction	-This command has no effect when Tearing Effect output is already OFF.	
Register Availability	<b>Status</b>	
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	
Default	<b>Status</b>	
	Power On Sequence	OFF
	S/W Reset	OFF
	H/W Reset	OFF
Flow Chart	<pre> graph TD     A([TE Line Output ON]) --&gt; B[TE]     B --&gt; C([TE Line Output OFF])     </pre>	
	<p>Legend</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mo</li> <li>Sequential transfer</li> </ul>	

## 10.1.27 TEON (35h): Tearing Effect Line ON

35H	TEON (Tearing Effect Line ON)												(Code)
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	
TEON	0	↑	1	-	0	0	1	1	0	1	0	1	(35h)
1st Parameter	1	↑	1	-	0	0	0	0	0	0	0	TELOM	

NOTE: "-" Don't care, can be set to VDDI or DGND level

**Description**

- This command is used to turn ON the Tearing Effect output signal from the TE signal line.
- This output is not affected by changing MADCTL bit ML.
- The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line. ("-="Don't Care).
- When TELOM(M)='0':

The Tearing Effect Output line consists of V-Blanking information only.

- When TELOM M='1':

The Tearing Effect Output line consists of both V-Blanking and H-Blanking information.

*Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.*

**Restriction**

- This command has no effect when Tearing Effect output is already OFF.

**Register Availability**

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

**Default**

Status	Default Value
Power On Sequence	Tearing effect off & TELOM=0
S/W Reset	Tearing effect off & TELOM=0
H/W Reset	Tearing effect off & TELOM=0

**Flow Chart**

```

graph TD
    A([TE Line Output OFF]) --> B[TEON (35h)]
    B --> C[/1st Parameter: (M)/]
    C --> D([TE Line Output ON])
            
```

Legend

- ▭ Command
- ▱ Parameter
- ◊ Display
- ◄ Action
- Mode
- ⊕ Sequential

## 10.1.28 MADCTL (36h): Memory Data Access Control

36H	MADCTL (Memory Data Access Control)												(Code)
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
MADCTL	0	↑	1	-	0	0	1	1	0	1	1	0	(36h)
1st Parameter	1	↑	1	-	MY	MX	MV	ML	RGB	MH	0	0	

NOTE: "-" Don't care, can be set to VDDI or DGND level

-This command defines read/ write scanning direction of frame memory.  
 -This command makes no change on the other driver status.  
 -Bit Assignment

Bit	NAME	DESCRIPTION
MY	Row Address Order	These 3bits controls MCU to memory write/read direction. (See Section 9.12)
MX	Column Address Order	
MV	Row/Column Exchange	
ML	Vertical Refresh Order	LCD vertical refresh direction control '0' = LCD vertical refresh Top to Bottom '1' = LCD vertical refresh Bottom to Top
RGB	RGB-BGR ORDER	Color selector switch control '0' = RGB color filter panel, '1' = BGR color filter panel
MH	Horizontal Refresh Order	LCD horizontal refresh direction control '0' = LCD horizontal refresh Left to right '1' = LCD horizontal refresh right to left

**ML: Vertical Refresh Order**

**RGB: RGB-BGR Order**

Description

<p>Description</p>	<p>The diagram illustrates the horizontal refresh order for the MH mode. It shows two scenarios based on the ML bit: ML='0' and ML='1'. Each scenario includes a 'Memory' grid and a 'Display' grid, both with a top-left corner at (0,0). The Memory grids show a sequence of blue squares representing data being sent from memory to the display. For ML='0', the refresh order is row-major, with arrows labeled 'Sent First', 'Sent 2nd', 'Sent 3rd', and 'Sent Last' pointing to the first four columns. For ML='1', the refresh order is column-major, with arrows labeled 'Sent Last', 'Sent 3rd', 'Sent 2nd', and 'Sent First' pointing to the last four rows.</p>												
<p>Restriction</p>	<p>D1 and D0 of the 1<sup>st</sup> parameter are set to "00" internally.</p>												
<p>Register Availability</p>	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
<p>Default</p>	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>MY=0, MX=0, MV=0, ML=0, RGB=0, MH=0</td> </tr> <tr> <td>S/W Reset</td> <td>No Change</td> </tr> <tr> <td>H/W Reset</td> <td>MY=0, MX=0, MV=0, ML=0, RGB=0, MH=0</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	MY=0, MX=0, MV=0, ML=0, RGB=0, MH=0	S/W Reset	No Change	H/W Reset	MY=0, MX=0, MV=0, ML=0, RGB=0, MH=0				
Status	Default Value												
Power On Sequence	MY=0, MX=0, MV=0, ML=0, RGB=0, MH=0												
S/W Reset	No Change												
H/W Reset	MY=0, MX=0, MV=0, ML=0, RGB=0, MH=0												
<p>Flow Chart</p>	<p>The flow chart shows a box labeled 'MADCTL (36h)' with an arrow pointing to a parallelogram labeled '1<sup>st</sup> Parameter: MY, MX, ML, RGB, MH'. To the right is a legend box containing symbols for Command (rectangle), Parameter (parallelogram), Display (pointed oval), Action (trapezoid), Mode (rounded rectangle), and Sequential (circle with tail).</p>												

## 10.1.29 VSCSAD (37h): Vertical Scroll Start Address of RAM

37H	VSCSAD (Vertical Scroll Start Address of RAM)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VSCSAD	0	↑	1	-	0	0	1	1	0	1	1	1	(37h)
1 <sup>st</sup> Parameter	1	↑	1	-	-	-	-	-	-	-	-	SSA8	
2 <sup>nd</sup> Parameter	1	↑	1	-	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	

NOTE: “-” Don’t care, can be set to VDDI or DGND level

Description	<p>-This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode.</p> <p>-The Vertical Scrolling Start Address command has one parameter which describes which line in the Frame Memory will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:</p> <p>-This command Start the scrolling.</p> <p>-Exit from V-scrolling mode by commands Partial mode On (12h) or Normal mode On (13h).</p> <p><b>When MADCTL ML= '0'</b></p> <p>Example:</p> <ul style="list-style-type: none"> <li>When Top Fixed Area=Bottom Fixed Area=00, Vertical Scrolling Area=320 and Vertical Scrolling Pointer SSA='3'.</li> </ul> <p>(Example)</p> <p>Top-Left (0,0) Memory</p> <p>SSA[7:0] Scroll start address</p> <p>Scan address</p> <p>0 1 2 3 ... 318 319</p> <p>Display</p> <p>G1 G2 G3 G4 ... G319 G320</p> <p><b>When MADCTL ML = '1'</b></p> <p>Example:</p> <ul style="list-style-type: none"> <li>When Top Fixed Area= Bottom Fixed Area=00, Vertical Scrolling Area=320 and SSA= '3'</li> </ul> <p>(Example)</p> <p>Top-Left (0,0) Memory</p> <p>SSA[7:0] Scroll start address</p> <p>Scan address</p> <p>319 318 ... 3 2 1 0</p> <p>Display</p> <p>G1 G2 G3 G4 ... G319 G320</p> <p>NOTE: -When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. -SSA refers to the Frame Memory scan address.</p>												
	Restriction	<p>-Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h)- otherwise undesirable image will be displayed on the Panel.</p> <p>SSA[7:0] is based on 1-line unit.</p> <p>-SSA[7:0] = 0000h, 0001h, 0002h, 0003h, ... , 00A1h</p>											
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>No</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>No</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	No	Partial Mode On, Idle Mode On, Sleep Out	No	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	No												
Partial Mode On, Idle Mode On, Sleep Out	No												
Sleep In	Yes												

# ST7787

Default	<b>Status</b>	<b>Default Value</b>
	Power On Sequence	0000h
	S/W Reset	0000h
	H/W Reset	0000h
Flow Chart	See Vertical Scrolling Definition (33h) description.	



## 10.1.30 IDMOFF (38h): Idle Mode Off

38H	IDMOFF (Idle Mode Off)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
IDMOFF	0	↑	1	-	0	0	1	1	1	0	0	0	(38h)
1st Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	<p>-This command is used to recover from Idle mode on.</p> <p>-There will be no abnormal visible effect on the display mode change transition.</p> <p>-In the idle off mode,</p> <ol style="list-style-type: none"> <li>1. LCD can display 4096, 65k or 262k colors.</li> <li>2. Normal frame frequency is applied.</li> </ol>													
Restriction	-This command has no effect when module is already in idle off mode.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Idle Mode Off</td> </tr> <tr> <td>S/W Reset</td> <td>Idle Mode Off</td> </tr> <tr> <td>H/W Reset</td> <td>Idle Mode Off</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	Idle Mode Off	S/W Reset	Idle Mode Off	H/W Reset	Idle Mode Off				
Status	Default Value													
Power On Sequence	Idle Mode Off													
S/W Reset	Idle Mode Off													
H/W Reset	Idle Mode Off													
Flow Chart	<pre> graph TD     A([Idle mode on]) --&gt; B[IDMOFF (38h)]     B --&gt; C([Idle mode off])     </pre> <p>Legend:</p> <ul style="list-style-type: none"> <li>Command: Rectangle</li> <li>Parameter: Parallelogram</li> <li>Display: Trapezoid</li> <li>Action: Arrow</li> <li>Mode: Oval</li> <li>Sequential transfer: Oval with tail</li> </ul>													

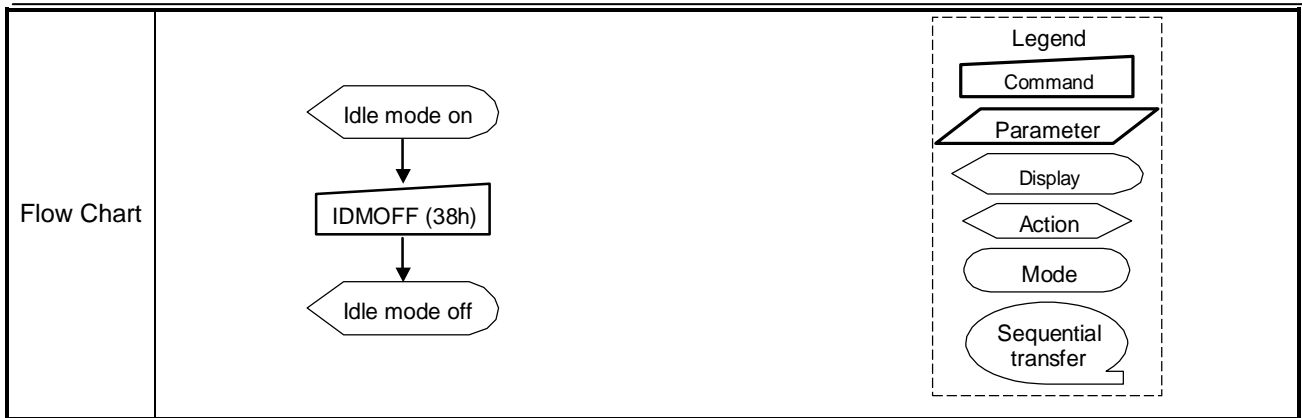
## 10.1.31 IDMON (39h): Idle Mode On

39H	IDMON (Idle Mode On)												(Code)
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
IDMOFF	0	↑	1	-	0	0	1	1	1	0	0	1	(39h)
1st Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	<p>-This command is used to enter into Idle mode on.</p> <p>-There will be no abnormal visible effect on the display mode change transition.</p> <p>-In the idle on mode,</p> <ol style="list-style-type: none"> <li>1. Color expression is reduced. The primary and the secondary colors using MSB of each R,G and B in the Frame Memory, 8 color depth data is displayed.</li> <li>2. 8-Color mode frame frequency is applied.</li> <li>3. Exit from IDMON by Idle Mode Off (38h) command</li> </ol>																																			
	<div style="text-align: center;"> <p>(Example)</p> </div> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Color</th> <th>R<sub>5</sub> R<sub>4</sub> R<sub>3</sub> R<sub>2</sub> R<sub>1</sub> R<sub>0</sub></th> <th>G<sub>5</sub> G<sub>4</sub> G<sub>3</sub> G<sub>2</sub> G<sub>1</sub> G<sub>0</sub></th> <th>B<sub>5</sub> B<sub>4</sub> B<sub>3</sub> B<sub>2</sub> B<sub>1</sub> B<sub>0</sub></th> </tr> </thead> <tbody> <tr> <td>Black</td> <td>0xxxxx</td> <td>0xxxxx</td> <td>0xxxxx</td> </tr> <tr> <td>Blue</td> <td>0xxxxx</td> <td>0xxxxx</td> <td>1xxxxx</td> </tr> <tr> <td>Red</td> <td>1xxxxx</td> <td>0xxxxx</td> <td>0xxxxx</td> </tr> <tr> <td>Magenta</td> <td>1xxxxx</td> <td>0xxxxx</td> <td>1xxxxx</td> </tr> <tr> <td>Green</td> <td>0xxxxx</td> <td>1xxxxx</td> <td>0xxxxx</td> </tr> <tr> <td>Cyan</td> <td>0xxxxx</td> <td>1xxxxx</td> <td>1xxxxx</td> </tr> <tr> <td>Yellow</td> <td>1xxxxx</td> <td>1xxxxx</td> <td>0xxxxx</td> </tr> <tr> <td>White</td> <td>1xxxxx</td> <td>1xxxxx</td> <td>1xxxxx</td> </tr> </tbody> </table>	Color	R <sub>5</sub> R <sub>4</sub> R <sub>3</sub> R <sub>2</sub> R <sub>1</sub> R <sub>0</sub>	G <sub>5</sub> G <sub>4</sub> G <sub>3</sub> G <sub>2</sub> G <sub>1</sub> G <sub>0</sub>	B <sub>5</sub> B <sub>4</sub> B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub>	Black	0xxxxx	0xxxxx	0xxxxx	Blue	0xxxxx	0xxxxx	1xxxxx	Red	1xxxxx	0xxxxx	0xxxxx	Magenta	1xxxxx	0xxxxx	1xxxxx	Green	0xxxxx	1xxxxx	0xxxxx	Cyan	0xxxxx	1xxxxx	1xxxxx	Yellow	1xxxxx	1xxxxx	0xxxxx	White	1xxxxx	1xxxxx
Color	R <sub>5</sub> R <sub>4</sub> R <sub>3</sub> R <sub>2</sub> R <sub>1</sub> R <sub>0</sub>	G <sub>5</sub> G <sub>4</sub> G <sub>3</sub> G <sub>2</sub> G <sub>1</sub> G <sub>0</sub>	B <sub>5</sub> B <sub>4</sub> B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub>																																	
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Magenta	1xxxxx	0xxxxx	1xxxxx																																	
Green	0xxxxx	1xxxxx	0xxxxx																																	
Cyan	0xxxxx	1xxxxx	1xxxxx																																	
Yellow	1xxxxx	1xxxxx	0xxxxx																																	
White	1xxxxx	1xxxxx	1xxxxx																																	
Restriction	This command has no effect when module is already in idle on mode.																																			
Register Availability	<table border="1" style="width: 100%;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>No</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>No</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	No	Partial Mode On, Idle Mode On, Sleep Out	No	Sleep In	Yes																							
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Sleep In	Yes																																			
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Status	Default Value																																			
Power On Sequence	Idle Mode Off																																			
S/W Reset	Idle Mode Off																																			
H/W Reset	Idle Mode Off																																			

# ST7787



## 10.1.32 COLMOD (3Ah): Interface Pixel Format

3AH	COLMOD (3Ah): Interface Pixel Format												(Code)
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	
COLMOD	0	↑	1	-	0	0	1	1	1	0	1	0	(3Ah)
1st Parameter	1	↑	1	-	VIPF3	VIPF2	VIPF1	VIPF0	D3	IFPF2	IFPF1	IFPF0	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	This command is used to define the format of RGB picture data, which is to be transferred via the MCU interface (IFPF) and RGB interface (VIPF). The formats are shown in the table: Others are no define and invalid																
	<table border="1"> <thead> <tr> <th colspan="2">IFPF[2:0]</th> <th></th> </tr> </thead> <tbody> <tr> <td>011</td> <td>3</td> <td>12-bit/pixel</td> </tr> <tr> <td>101</td> <td>5</td> <td>16-bit/pixel</td> </tr> <tr> <td>110</td> <td>6</td> <td>18-bit/pixel</td> </tr> </tbody> </table>	IFPF[2:0]			011	3	12-bit/pixel	101	5	16-bit/pixel	110	6	18-bit/pixel				
IFPF[2:0]																	
011	3	12-bit/pixel															
101	5	16-bit/pixel															
110	6	18-bit/pixel															
Restriction	There is no visible effect until the Frame Memory is written to.																
	Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>No</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>No</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	No	Partial Mode On, Idle Mode On, Sleep Out	No	Sleep In	Yes			
Status	Availability																
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Sleep In	Yes																
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	Status	Default Value															
	IFPF[2:0]	VIPF[3:0]															
Power On Sequence	0110(18-bit/Pixel)	0110(18-bit/Pixel)															
S/W Reset	No Change	No Change															
H/W Reset	0110(18-bit/Pixel)	0110(18-bit/Pixel)															
Flow Chart	<pre> graph TD     A([18-bit/Pixel Mode]) --&gt; B[COLMOD (3Ah)]     B --&gt; C[/1st Parameter: P[2:0]='111'/]     C --&gt; D([16-bit/Pixel Mode])     </pre>																

3FH	OTP-Process												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GMCTRP1	0	-↑	1	-	0	0	1	1	1	1	1	1	(3Fh)
1 <sup>st</sup> Parameter	1	-↑	1	-	1	1	0	0	1	0	1	0	CAh
2 <sup>nd</sup> Parameter	1	-↑	1	-	0	0	0	0	0	0	INI	0	

Description	<p>-While EXTC is fixed to L. Please set INI to "1" for enable OTP programming</p> <p>-While EXTC is fixed to "L" Please set INI to "0" for disable OTP programming</p>													
Restriction	<p>-If this register not using the register need be reserved.</p> <p>-After adjust the C5H command(VcomH voltage) and C6H command(VcomAC voltage), VPP connect <math>\geq 7.5V</math>.</p>													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Sleep In	Yes													
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Status	Default Value													
Power On Sequence	Not Fixed													
S/W Reset	00h													
H/W Reset	00h													
Flow Chart	<pre> graph TD     A[OTP-process (FAh)] --&gt; B[/1st Parameter:/]     </pre> <p>Legend</p> <ul style="list-style-type: none"> <li>Command: Rectangle</li> <li>Parameter: Parallelogram</li> <li>Display: Oval</li> <li>Action: Arrow</li> <li>Mode: Rounded rectangle</li> <li>Sequential transfer: Oval with tail</li> </ul>													

## 10.1.34 RDID1 (Dah): Read ID1 Value

DAH	RDID1 (Read ID1 Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDID1	0	↑	1	-	1	1	0	1	1	0	1	0	(Dah)
1 <sup>st</sup> Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2 <sup>nd</sup> Parameter	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	<p>-This read byte returns 8-bit LCD module's manufacturer ID                      -The 1<sup>st</sup> parameter is dummy data                      -The 2<sup>nd</sup> parameter (ID17 to ID10): LCD module's manufacturer ID.                      NOTE: See command RDDID (04h), 2<sup>nd</sup> parameter.</p>													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>No</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>No</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	No	Partial Mode On, Idle Mode On, Sleep Out	No	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
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Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>FF</td> </tr> <tr> <td>S/W Reset</td> <td>FF</td> </tr> <tr> <td>H/W Reset</td> <td>FF</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	FF	S/W Reset	FF	H/W Reset	FF				
Status	Default Value													
Power On Sequence	FF													
S/W Reset	FF													
H/W Reset	FF													
Flow Chart														

## 10.1.35 RDID2 (DBh): Read ID2 Value

DBH	RDID2 (Read ID2 Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDID2	0	↑	1	-	1	1	0	1	1	0	1	1	(DBh)
1 <sup>st</sup> Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2 <sup>nd</sup> Parameter	1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	<p>-This read byte returns 8-bit LCD module/driver version ID                  -The 1<sup>st</sup> parameter is dummy data                  -The 2<sup>nd</sup> parameter (ID26 to ID20): LCD module/driver version ID                  -Parameter Range: ID=80h to FFh</p> <p>NOTE: See command RDDID (04h), 3<sup>rd</sup> parameter.</p>													
	Restriction	-												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>No</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>No</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	No	Partial Mode On, Idle Mode On, Sleep Out	No	Sleep In	Yes
	Status	Availability												
	Normal Mode On, Idle Mode Off, Sleep Out	Yes												
	Normal Mode On, Idle Mode On, Sleep Out	Yes												
	Partial Mode On, Idle Mode Off, Sleep Out	No												
Partial Mode On, Idle Mode On, Sleep Out	No													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>FF</td> </tr> <tr> <td>S/W Reset</td> <td>FF</td> </tr> <tr> <td>H/W Reset</td> <td>FF</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	FF	S/W Reset	FF	H/W Reset	FF				
	Status	Default Value												
	Power On Sequence	FF												
	S/W Reset	FF												
H/W Reset	FF													
Flow Chart	<pre>                 graph TD                     subgraph Serial_I/F_Mode [Serial I/F Mode]                         C1[RDID2 (DBh)] --&gt; P1[/Send 2nd parameter ID2[7:0]/]                     end                     subgraph Partial_I/F_Mode [Partial I/F Mode]                         C2[RDID2 (DBh)] --&gt; A1[/Dummy Read/]                         A1 --&gt; P2[/Send 2nd parameter: ID2[7:0]/]                     end                     C1 --- Host[Host Driver]                     C2 --- Host                     P1 --- Host                     P2 --- Host                     </pre> <p>Legend:</p> <ul style="list-style-type: none"> <li>Command: Rectangle</li> <li>Parameter: Parallelogram</li> <li>Display: Oval</li> <li>Action: Arrowhead</li> <li>Mode: Oval</li> <li>Sequential transfer: Oval with tail</li> </ul>													

## 10.1.36 RDID3 (DCh): Read ID3 Value

DCH	RDID3 (Read ID2 Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDID3	0	↑	1	-	1	1	0	1	1	1	0	0	(DCh)
1 <sup>st</sup> Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2 <sup>nd</sup> Parameter	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	<p>-This read byte returns 8-bit LCD module/driver ID.                      -The 1<sup>st</sup> parameter is dummy data                      -The 2<sup>nd</sup> parameter (ID37 to ID30): LCD module/driver ID.                      NOTE: See command RDDID (04h), 4<sup>th</sup> parameter.</p>													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>No</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>No</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	No	Partial Mode On, Idle Mode On, Sleep Out	No	Sleep In	Yes	
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	No													
Partial Mode On, Idle Mode On, Sleep Out	No													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>FF</td> </tr> <tr> <td>S/W Reset</td> <td>FF</td> </tr> <tr> <td>H/W Reset</td> <td>FF</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	FF	S/W Reset	FF	H/W Reset	FF					
Status	Default Value													
Power On Sequence	FF													
S/W Reset	FF													
H/W Reset	FF													
Flow Chart														



# ST7787

## 10.2.1 RGBCTR (B0h): RGB signal control

B0H	RGBCTR (RGB signal control)												(Code)
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RGBCTR	0	↑	1	-	1	0	1	1	0	0	0	0	(B0h)
1 <sup>st</sup> Parameter	1	↑	1	-	0	0	0	ICM	DP	EP	HSP	VSP	

NOTE: "-" Don't care

Description	-Set the operation status on the RGB interface. The setting becomes effective as soon as the command is received.	
	-ICM: GRAM Write/Read frequency and data input select on the RGB interface	
	ICM	
		Write cycle
		Read cycle
		Data input
	0	PCLK
	1	SCL
		Internal oscillator
		SDA
Description	Symbol	
	DP	PCLK polarity set
	EP	Enable polarity set
	HSP	Hsync polarity set
	VSP	Vsync polarity set
	'1' = data fetched at the falling edge	
	'0' = data fetched at the rising edge	
	'1' = Low enable for RGB interface	
	'0' = High enable for RGB interface	
	'1' = High level sync clock	
	'0' = Low level sync clock	
	'1' = High level sync clock	
	'0' = Low level sync clock	
Restriction	-If this register not using the register need be reserved.	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
		ICM
		DP/EP/HSP/VSP
	Power On Sequence	
	S/W Reset	
	H/W Reset	
Flow Chart	<pre> graph TD     A[RGBCTR (B0h)] --&gt; B[/1st Parameter: ICM, DW, DP, EP, HSP, VSP/]         </pre>	
	<div style="border: 1px dashed black; padding: 5px;"> <p>Legend</p> <ul style="list-style-type: none"> <li>Command: [Rectangle]</li> <li>Parameter: [Parallelogram]</li> <li>Display: [Oval]</li> <li>Action: [Arrow]</li> <li>Mode: [Oval]</li> <li>Sequential transfer: [Oval with tail]</li> </ul> </div>	

## 10.2.2 FRMCTR1 (B1h): Frame Rate Control (In normal mode/ Full colors)

B1H	FRMCTR1 (Frame Rate Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
FRMCTR1	0	↑	1	-	1	0	1	1	0	0	0	1	(B1h)
1 <sup>st</sup> Parameter	1	↑	1	-	---	RTNA[6]	RTNA[5]	RTNA[4]	RTNA[3]	RTNA[2]	RTNA[1]	RTNA[0]	-
2 <sup>nd</sup> Parameter	1	↑	1	-	---	---	---	FPA[4]	FPA[3]	FPA[2]	FPA[1]	FPA[0]	-
3 <sup>th</sup> Parameter				-	---	---	---	BPA[4]	BPA[3]	BPA[2]	BPA[1]	BPA[0]	

NOTE: "-" Don't care

-Set the frame frequency of the full colors normal mode.  
 -The frame frequency need to meet 60Hz ±5% in this mode.

OSC

Frame rate(Hz) =  $\frac{\text{OSC}}{(\text{RTNA}+2) * (320+\text{FPA}+\text{BPA})}$

RTNA[6:0]		Frame Rate	RTNA[6:0]		Frame Rate
0101000	40	90	1010100	84	43
0101001	41	88	1010101	85	43
0101010	42	86	1010110	86	42
0101011	43	84	1010111	87	42
0101100	44	82	1011000	88	41
0101101	45	80	1011001	89	41
0101110	46	78	1011010	90	40
0101111	47	77	1011011	91	40
0110000	48	75	1011100	92	40
0110001	49	74	1011101	93	39
0110010	50	72	1011110	94	39
0110011	51	71	1011111	95	38
0110100	52	70	1100000	96	38
0110101	53	68	1100001	97	37
0110110	54	67	1100010	98	37
0110111	55	66	1100011	99	37
0111000	56	65	1100100	100	36
0111001	57	63	1100101	101	36
0111010	58	62	1100110	102	36
0111011	59	61	1100111	103	35
0111100	60	60	1101000	104	35
0111101	61	59	1101001	105	35
0111110	62	59	1101010	106	34
0111111	63	57	1101011	107	34
1000000	64	57	1101100	108	34
1000001	65	56	1101101	109	33
1000010	66	55	1101110	110	33
1000011	67	54	1101111	111	33
1000100	68	53	1110000	112	32
1000101	69	53	1110001	113	32
1000110	70	52	1110010	114	32
1000111	71	51	1110011	115	32
1001000	72	51	1110100	116	31
1001001	73	50	1110101	117	31
1001010	74	49	1110110	118	31
1001011	75	48	1110111	119	31
1001100	76	48	1111000	120	30
1001101	77	47	1111001	121	30
1001110	78	47	1111010	122	30
1001111	79	46	1111011	123	30
1010000	80	45	1111100	124	29
1010001	81	45	1111101	125	29
1010010	82	44	1111110	126	29
1010011	83	44	1111111	127	29

**Note: OSC output fre. Is 1.2MHz, FPA=02H and BPA=02H**

FPA[4:0]		Timing	BPA[4:0]		Timing
00000	0	0 line	00000	0	0 line
00001	1	1 line	00001	1	1 line
00010	2	2 lines	00010	2	2 lines
00011	3	3 lines	00011	3	3 lines
00100	4	4 lines	00100	4	4 lines
00101	5	5 lines	00101	5	5 lines
00110	6	6 lines	00110	6	6 lines
00111	7	7 lines	00111	7	7 lines
01000	8	8 lines	01000	8	8 lines
01001	9	9 lines	01001	9	9 lines
01010	10	10 lines	01010	10	10 lines
01011	11	11 lines	01011	11	11 lines
01100	12	12 lines	01100	12	12 lines
01101	13	13 lines	01101	13	13 lines
01110	14	14 lines	01110	14	14 lines
01111	15	15 lines	01111	15	15 lines
10000	16	16 lines	10000	16	16 lines
10001	17	17 lines	10001	17	17 lines
10010	18	18 lines	10010	18	18 lines
10011	19	19 lines	10011	19	19 lines
10100	20	20 lines	10100	20	20 lines
10101	21	21 lines	10101	21	21 lines
10110	22	22 lines	10110	22	22 lines
10111	23	23 lines	10111	23	23 lines
11000	24	24 lines	11000	24	24 lines
11001	25	25 lines	11001	25	25 lines
11010	26	26 lines	11010	26	26 lines
11011	27	27 lines	11011	27	27 lines
11100	28	28 lines	11100	28	28 lines
11101	29	29 lines	11101	29	29 lines
11110	30	30 lines	11110	30	30 lines
11111	31	31 lines	11111	31	31 lines

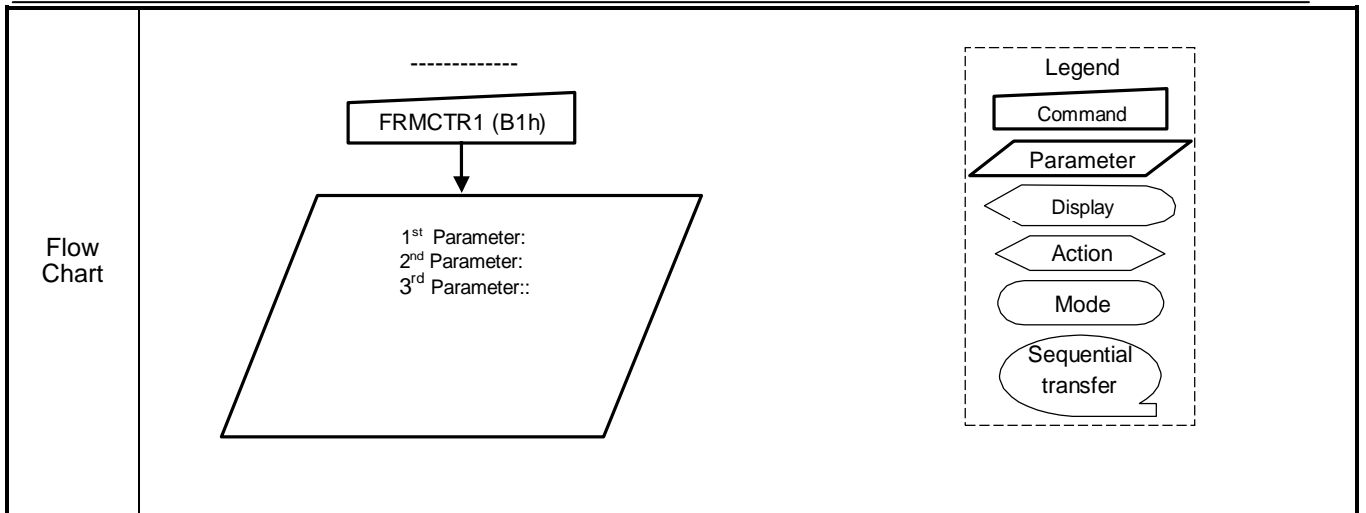
Restriction	-If this register not using the register need be reserved.
-------------	--

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes

Default	Status	Default Value		
		RTNA	FPA	BPA
	Power On Sequence	36h	02h	02h
	S/W Reset	36h	02h	02h
	H/W Reset	36h	02h	02h



## 10.2.3 FRMCTR2 (B2h): Frame Rate Control (In Idle mode/ 8-colors)

B2H	FRMCTR2 (Frame Rate Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
FRMCTR2	0	↑	1	-	1	0	1	1	0	0	1	0	(B2h)
1 <sup>st</sup> Parameter	1	↑	1	-	---	RTNB[6]	RTNB[5]	RTNB[4]	RTNB[3]	RTNB[2]	RTNB[1]	RTNB[0]	-
2 <sup>nd</sup> Parameter	1	↑	1	-	---	---	---	FPB[4]	FPB[3]	FPB[2]	FPB[1]	FPB[0]	-
3th Parameter	1	↑	1	-	---	---	---	BPB[4]	BPB[3]	BPB[2]	BPB[1]	BPB[0]	-

NOTE: "-- Don't care

Description	-Set the frame frequency of the Idle mode.																																																																																																																																																																																					
	-The frame frequency need to meet 60Hz ±5% in this mode.																																																																																																																																																																																					
	$\text{Frame rate(Hz)} = \frac{\text{OSC}}{(\text{RTNA}+2) * (320+\text{FPA}+\text{BPA})}$																																																																																																																																																																																					
	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>RTNB[6:0]</th> <th>Frame Rate</th> <th>RTNB[6:0]</th> <th>Frame Rate</th> </tr> </thead> <tbody> <tr><td>0101000</td><td>40</td><td>1010100</td><td>84</td></tr> <tr><td>0101001</td><td>41</td><td>1010101</td><td>85</td></tr> <tr><td>0101010</td><td>42</td><td>1010110</td><td>86</td></tr> <tr><td>0101011</td><td>43</td><td>1010111</td><td>87</td></tr> <tr><td>0101100</td><td>44</td><td>1011000</td><td>88</td></tr> <tr><td>0101101</td><td>45</td><td>1011001</td><td>89</td></tr> <tr><td>0101110</td><td>46</td><td>1011010</td><td>90</td></tr> <tr><td>0101111</td><td>47</td><td>1011011</td><td>91</td></tr> <tr><td>0110000</td><td>48</td><td>1011100</td><td>92</td></tr> <tr><td>0110001</td><td>49</td><td>1011101</td><td>93</td></tr> <tr><td>0110010</td><td>50</td><td>1011110</td><td>94</td></tr> <tr><td>0110011</td><td>51</td><td>1011111</td><td>95</td></tr> <tr><td>0110100</td><td>52</td><td>1100000</td><td>96</td></tr> <tr><td>0110101</td><td>53</td><td>1100001</td><td>97</td></tr> <tr><td>0110110</td><td>54</td><td>1100010</td><td>98</td></tr> <tr><td>0110111</td><td>55</td><td>1100011</td><td>99</td></tr> <tr><td>0111000</td><td>56</td><td>1100100</td><td>100</td></tr> <tr><td>0111001</td><td>57</td><td>1100101</td><td>101</td></tr> <tr><td>0111010</td><td>58</td><td>1100110</td><td>102</td></tr> <tr><td>0111011</td><td>59</td><td>1100111</td><td>103</td></tr> <tr><td>0111100</td><td>60</td><td>1101000</td><td>104</td></tr> <tr><td>0111101</td><td>61</td><td>1101001</td><td>105</td></tr> <tr><td>0111110</td><td>62</td><td>1101010</td><td>106</td></tr> <tr><td>0111111</td><td>63</td><td>1101011</td><td>107</td></tr> <tr><td>1000000</td><td>64</td><td>1101100</td><td>108</td></tr> <tr><td>1000001</td><td>65</td><td>1101101</td><td>109</td></tr> <tr><td>1000010</td><td>66</td><td>1101110</td><td>110</td></tr> <tr><td>1000011</td><td>67</td><td>1101111</td><td>111</td></tr> <tr><td>1000100</td><td>68</td><td>1110000</td><td>112</td></tr> <tr><td>1000101</td><td>69</td><td>1110001</td><td>113</td></tr> <tr><td>1000110</td><td>70</td><td>1110010</td><td>114</td></tr> <tr><td>1000111</td><td>71</td><td>1110011</td><td>115</td></tr> <tr><td>1001000</td><td>72</td><td>1110100</td><td>116</td></tr> <tr><td>1001001</td><td>73</td><td>1110101</td><td>117</td></tr> <tr><td>1001010</td><td>74</td><td>1110110</td><td>118</td></tr> <tr><td>1001011</td><td>75</td><td>1110111</td><td>119</td></tr> <tr><td>1001100</td><td>76</td><td>1111000</td><td>120</td></tr> <tr><td>1001101</td><td>77</td><td>1111001</td><td>121</td></tr> <tr><td>1001110</td><td>78</td><td>1111010</td><td>122</td></tr> <tr><td>1001111</td><td>79</td><td>1111011</td><td>123</td></tr> <tr><td>1010000</td><td>80</td><td>1111100</td><td>124</td></tr> <tr><td>1010001</td><td>81</td><td>1111101</td><td>125</td></tr> <tr><td>1010010</td><td>82</td><td>1111110</td><td>126</td></tr> <tr><td>1010011</td><td>83</td><td>1111111</td><td>127</td></tr> </tbody> </table>		RTNB[6:0]	Frame Rate	RTNB[6:0]	Frame Rate	0101000	40	1010100	84	0101001	41	1010101	85	0101010	42	1010110	86	0101011	43	1010111	87	0101100	44	1011000	88	0101101	45	1011001	89	0101110	46	1011010	90	0101111	47	1011011	91	0110000	48	1011100	92	0110001	49	1011101	93	0110010	50	1011110	94	0110011	51	1011111	95	0110100	52	1100000	96	0110101	53	1100001	97	0110110	54	1100010	98	0110111	55	1100011	99	0111000	56	1100100	100	0111001	57	1100101	101	0111010	58	1100110	102	0111011	59	1100111	103	0111100	60	1101000	104	0111101	61	1101001	105	0111110	62	1101010	106	0111111	63	1101011	107	1000000	64	1101100	108	1000001	65	1101101	109	1000010	66	1101110	110	1000011	67	1101111	111	1000100	68	1110000	112	1000101	69	1110001	113	1000110	70	1110010	114	1000111	71	1110011	115	1001000	72	1110100	116	1001001	73	1110101	117	1001010	74	1110110	118	1001011	75	1110111	119	1001100	76	1111000	120	1001101	77	1111001	121	1001110	78	1111010	122	1001111	79	1111011	123	1010000	80	1111100	124	1010001	81	1111101	125	1010010	82	1111110	126	1010011	83	1111111	127
	RTNB[6:0]	Frame Rate	RTNB[6:0]	Frame Rate																																																																																																																																																																																		
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	0101001	41	1010101	85																																																																																																																																																																																		
	0101010	42	1010110	86																																																																																																																																																																																		
	0101011	43	1010111	87																																																																																																																																																																																		
	0101100	44	1011000	88																																																																																																																																																																																		
	0101101	45	1011001	89																																																																																																																																																																																		
	0101110	46	1011010	90																																																																																																																																																																																		
	0101111	47	1011011	91																																																																																																																																																																																		
	0110000	48	1011100	92																																																																																																																																																																																		
	0110001	49	1011101	93																																																																																																																																																																																		
	0110010	50	1011110	94																																																																																																																																																																																		
	0110011	51	1011111	95																																																																																																																																																																																		
	0110100	52	1100000	96																																																																																																																																																																																		
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	0110110	54	1100010	98																																																																																																																																																																																		
	0110111	55	1100011	99																																																																																																																																																																																		
	0111000	56	1100100	100																																																																																																																																																																																		
	0111001	57	1100101	101																																																																																																																																																																																		
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0111101	61	1101001	105																																																																																																																																																																																			
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1000000	64	1101100	108																																																																																																																																																																																			
1000001	65	1101101	109																																																																																																																																																																																			
1000010	66	1101110	110																																																																																																																																																																																			
1000011	67	1101111	111																																																																																																																																																																																			
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1000101	69	1110001	113																																																																																																																																																																																			
1000110	70	1110010	114																																																																																																																																																																																			
1000111	71	1110011	115																																																																																																																																																																																			
1001000	72	1110100	116																																																																																																																																																																																			
1001001	73	1110101	117																																																																																																																																																																																			
1001010	74	1110110	118																																																																																																																																																																																			
1001011	75	1110111	119																																																																																																																																																																																			
1001100	76	1111000	120																																																																																																																																																																																			
1001101	77	1111001	121																																																																																																																																																																																			
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1010011	83	1111111	127																																																																																																																																																																																			
<p><b>Note: OSC output fre. Is 1.2MHz, FPA=02H and BPA=02H</b></p>																																																																																																																																																																																						

# ST7787

	FPB[4:0]		Timing	BPB[4:0]		Timing
		00000	0	0 line	00000	0
	00001	1	1 line	00001	1	1 line
	00010	2	2 lines	00010	2	2 lines
	00011	3	3 lines	00011	3	3 lines
	00100	4	4 lines	00100	4	4 lines
	00101	5	5 lines	00101	5	5 lines
	00110	6	6 lines	00110	6	6 lines
	00111	7	7 lines	00111	7	7 lines
	01000	8	8 lines	01000	8	8 lines
	01001	9	9 lines	01001	9	9 lines
	01010	10	10 lines	01010	10	10 lines
	01011	11	11 lines	01011	11	11 lines
	01100	12	12 lines	01100	12	12 lines
	01101	13	13 lines	01101	13	13 lines
	01110	14	14 lines	01110	14	14 lines
	01111	15	15 lines	01111	15	15 lines
	10000	16	16 lines	10000	16	16 lines
	10001	17	17 lines	10001	17	17 lines
	10010	18	18 lines	10010	18	18 lines
	10011	19	19 lines	10011	19	19 lines
	10100	20	20 lines	10100	20	20 lines
	10101	21	21 lines	10101	21	21 lines
	10110	22	22 lines	10110	22	22 lines
	10111	23	23 lines	10111	23	23 lines
	11000	24	24 lines	11000	24	24 lines
	11001	25	25 lines	11001	25	25 lines
	11010	26	26 lines	11010	26	26 lines
	11011	27	27 lines	11011	27	27 lines
	11100	28	28 lines	11100	28	28 lines
	11101	29	29 lines	11101	29	29 lines
	11110	30	30 lines	11110	30	30 lines
	11111	31	31 lines	11111	31	31 lines

Restriction	-If this register not using the register need be reserved.
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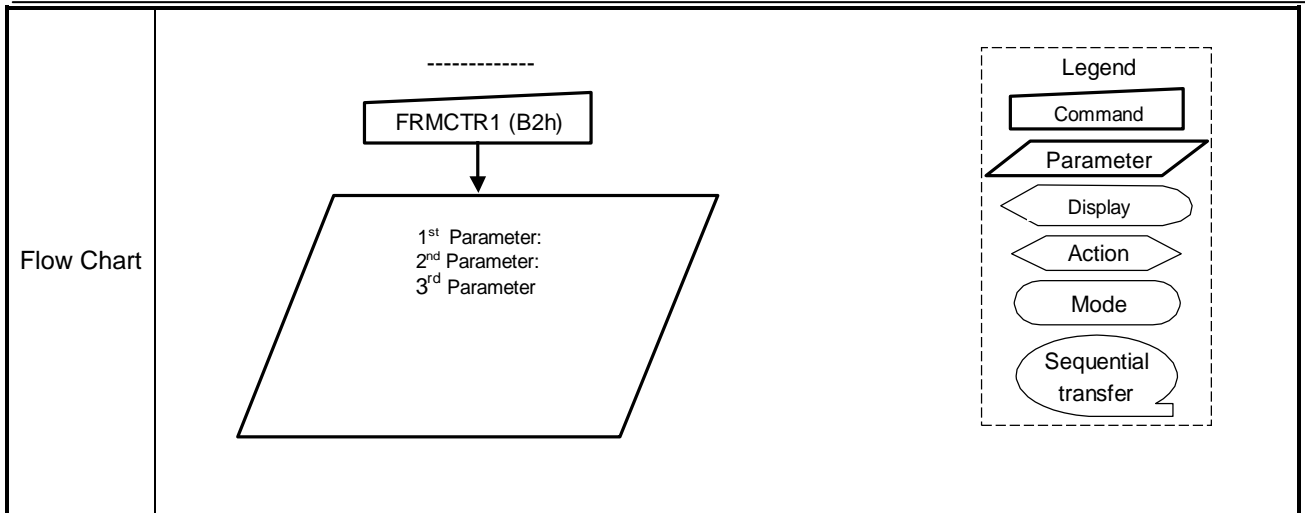
  

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes

Default	Status	Default Value		
		RTNB	FPB	BPB
	Power On Sequence	38H	02H	02H
	S/W Reset	38H	02H	02H
	H/W Reset	38H	02H	02H

# ST7787



## 10.2.3 FRMCTR3 (B3h): Frame Rate Control (In Partial mode/ full colors)

B3H		FRMCTR3 (Frame Rate Control)											(Code)
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
FRMCTR3	0	↑	1	-	1	0	1	1	0	0	1	1	(B3h)
1 <sup>st</sup> Parameter	1	↑	1	-	-	RTNC[6]	RTNC[5]	RTNC[4]	RTNC[3]	RTNC[2]	RTNC[1]	RTNC[0]	-
2 <sup>nd</sup> Parameter	1	↑	1	-	-	-	-	FPC[4]	FPC[3]	FPC[2]	FPC[1]	FPC[0]	-
3 <sup>rd</sup> Parameter	1	↑	1	-	-	-	-	BPC[4]	BPC[3]	BPC[2]	BPC[1]	BPC[0]	-
4 <sup>th</sup> Parameter	1	↑	1	-	---	RTND[6]	RTND[5]	RTND[4]	RTND[3]	RTND[2]	RTND[1]	RTND[0]	-
5 <sup>th</sup> Parameter	1	↑	1	-	-	-	-	FPD[4]	FPD[3]	FPD[2]	FPD[1]	FPD[0]	-
6 <sup>th</sup> Parameter	1	↑	1	-	-	-	-	BPD[4]	BPD[3]	BPD[2]	BPD[1]	BPD[0]	-

NOTE: "-- Don't care

- Set the frame frequency of the Partial mode/ full colors.
- When the display is frame inversion the frame frequency need to meet 65Hz ±5% in this mode.
- When the display is line inversion the frame frequency need to meet 70Hz ±5% in this mode.

OSC

$$\text{Frame rate(Hz)} = \frac{\text{OSC}}{(\text{RTNA}+2) * (320+\text{FPA}+\text{BPA})}$$

Description

RTNC[6:0]		Frame Rate	RTNC[6:0]		Frame Rate
0101000	40	87	1010100	84	42
0101001	41	85	1010101	85	41
0101010	42	83	1010110	86	41
0101011	43	81	1010111	87	40
0101100	44	79	1011000	88	40
0101101	45	77	1011001	89	39
0101110	46	76	1011010	90	39
0101111	47	74	1011011	91	39
0110000	48	73	1011100	92	38
0110001	49	71	1011101	93	38
0110010	50	70	1011110	94	37
0110011	51	68	1011111	95	37
0110100	52	67	1100000	96	36
0110101	53	66	1100001	97	36
0110110	54	65	1100010	98	36
0110111	55	63	1100011	99	35
0111000	56	62	1100100	100	35
0111001	57	61	1100101	101	35
0111010	58	60	1100110	102	34
0111011	59	59	1100111	103	34
0111100	60	58	1101000	104	34
0111101	61	57	1101001	105	33
0111110	62	56	1101010	106	33
0111111	63	55	1101011	107	33
1000000	64	54	1101100	108	32
1000001	65	54	1101101	109	32
1000010	66	53	1101110	110	32
1000011	67	52	1101111	111	32
1000100	68	51	1110000	112	31
1000101	69	51	1110001	113	31
1000110	70	50	1110010	114	31
1000111	71	49	1110011	115	30
1001000	72	49	1110100	116	30
1001001	73	48	1110101	117	30
1001010	74	47	1110110	118	30
1001011	75	47	1110111	119	29
1001100	76	46	1111000	120	29
1001101	77	45	1111001	121	29
1001110	78	45	1111010	122	29
1001111	79	44	1111011	123	28
1010000	80	44	1111100	124	28
1010001	81	43	1111101	125	28
1010010	82	43	1111110	126	28
1010011	83	42	1111111	127	28



Note: OSC output fre. Is 1.2MHz, FPA=02H and BPA=02H

RTND[6:0]		Frame Rate	RTND[6:0]		Frame Rate
0101000	40	867	1010100	84	42
0101001	41	85	1010101	85	41
0101010	42	83	1010110	86	41
0101011	43	81	1010111	87	40
0101100	44	79	1011000	88	40
0101101	45	77	1011001	89	39
0101110	46	75	1011010	90	39
0101111	47	74	1011011	91	38
0110000	48	72	1011100	92	38
0110001	49	71	1011101	93	38
0110010	50	69	1011110	94	37
0110011	51	68	1011111	95	37
0110100	52	67	1100000	96	36
0110101	53	66	1100001	97	36
0110110	54	64	1100010	98	36
0110111	55	63	1100011	99	35
0111000	56	62	1100100	100	35
0111001	57	61	1100101	101	35
0111010	58	60	1100110	102	34
0111011	59	59	1100111	103	34
0111100	60	58	1101000	104	34
0111101	61	57	1101001	105	33
0111110	62	56	1101010	106	33
0111111	63	55	1101011	107	33
1000000	64	55	1101100	108	32
1000001	65	54	1101101	109	32
1000010	66	53	1101110	110	32
1000011	67	52	1101111	111	32
1000100	68	51	1110000	112	31
1000101	69	51	1110001	113	31
1000110	70	50	1110010	114	31
1000111	71	49	1110011	115	30
1001000	72	49	1110100	116	30
1001001	73	48	1110101	117	30
1001010	74	47	1110110	118	30
1001011	75	47	1110111	119	29
1001100	76	46	1111000	120	29
1001101	77	45	1111001	121	29
1001110	78	45	1111010	122	29
1001111	79	44	1111011	123	28
1010000	80	44	1111100	124	28
1010001	81	43	1111101	125	28
1010010	82	43	1111110	126	28
1010011	83	42	1111111	127	28

Note: OSC output fre. Is 1.2MHz, FPA=02H and BPA=02H

Restriction -If this register not using the register need be reserved.

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes

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Status	Default Value					
	RTNC	FPC	BPC	RTND	FPD	BPD
Power On Sequence	36h	02h	02h	38h	02h	02h
S/W Reset	36h	02h	02h	38h	02h	02h
H/W Reset	36h	02h	02h	38h	02h	02h

Flow Chart

```

graph TD
    A[FRMCTR1 (B3h)] --> B[1st Parameter:  
2nd Parameter:  
3rd Parameter:  
. . .  
6th Parameter:]
    
```

Legend

- Command
- Parameter
- Display
- Action
- Mode
- Sequential transfer

## 10.2.5 INVCTR (B4h): Display Inversion Control

B4H	INVCTR (Display Inversion Control)												(Code)
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
INVCTR	0	↑	1	-	1	0	1	1	0	1	0	0	(B4h)
1 <sup>st</sup> Parameter	1	↑	1	-	0	0	0	0	0	NLA	NLB	NLC	02h

NOTE: “-“ Don't care

Description	-Display Inversion mode control					
	-NLA: Inversion setting in full colors normal mode (Normal mode on)					
	<b>NLA</b>	<b>Line Inversion</b>				
	0	Frame Inversion				
	1					
	-NLB: Inversion setting in Idle mode (Idle mode on)					
Restriction	<b>NLB</b>	<b>Line Inversion</b>				
	0	Frame Inversion				
	1					
	-NLC: Inversion setting in full colors partial mode (Partial mode on / Idle mode off)					
	<b>NLC</b>	<b>Line Inversion</b>				
	0	Frame Inversion				
1						
Register Availability	-If this register not using the register need be reserved.					
Default	Status		Availability			
	Normal Mode On, Idle Mode Off, Sleep Out		Yes			
	Normal Mode On, Idle Mode On, Sleep Out		Yes			
	Partial Mode On, Idle Mode Off, Sleep Out		Yes			
	Partial Mode On, Idle Mode On, Sleep Out		Yes			
Sleep In		Yes				
Flow Chart	Status		Default Value			
			NLA	NLB	NLC	B4h
	Power On Sequence		0d	1d	0d	02h
	S/W Reset		0d	1d	0d	02h
H/W Reset		0d	1d	0d	02h	
Flow Chart						<p>Legend</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>

## 10.2.6 RGBBPCTR (B5h): RGB Interface Blanking Porch setting

B5H	RGBPSET (RGB Interface Blanking Porch setting)												(Code)
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RGBBPCTR	0	↑	1	-	1	0	1	1	0	1	0	1	(B5h)
1 <sup>st</sup> Parameter	1	↑	1	-	---	---	---	---	VFP[3]	VFP[2]	VFP[1]	VFP[0]	-
2 <sup>nd</sup> Parameter	1	↑	1	-	---	---	---	---	VBP[3]	VBP[2]	VBP[1]	VBP[0]	-
3 <sup>rd</sup> Parameter	1	↑	1		---	---	---	---	HFP[3]	HFP[2]	HFP[1]	HFP[0]	
4 <sup>th</sup> Parameter	1	↑	1		---	---	---	---	HBP[3]	HBP[2]	HBP[1]	HBP[0]	

NOTE: "-- Don't care

Description	-Set the blanking porch in the RGB interface -The detail settings are designed by driver maker.			
Restriction	-If this register not using the register need be reserved.			
Register Availability	Status		Availability	
	Normal Mode On, Idle Mode Off, Sleep Out		Yes	
	Normal Mode On, Idle Mode On, Sleep Out		Yes	
	Partial Mode On, Idle Mode Off, Sleep Out		Yes	
	Partial Mode On, Idle Mode On, Sleep Out		Yes	
Sleep In		Yes		
Default	Status	Default Value		
		VFP[3:0]	VBP[3:0]	HFP[3:0]
	Power On Sequence	00H	02H	09H
	S/W Reset	00H	02H	09H
H/W Reset	00H	02H	09H	
Flow Chart	<p style="text-align: center;">-----</p> <div style="text-align: center;"> <pre> graph TD     A[RGBBPCTR1 (B5h)] --&gt; B[1st Parameter]     A --&gt; C[2nd Parameter]     A --&gt; D[3rd Parameter]     A --&gt; E[4th Parameter]             </pre> </div>			<p>Legend</p> <ul style="list-style-type: none"> <li> Command</li> <li> Parameter</li> <li> Display</li> <li> Action</li> <li> Mode</li> <li> Sequential transfer</li> </ul>

## 10.2.7 DISSET5 (B6h): Display Function set 5

B6H	DISSET (Display Function set 5)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DISSET5	0	↑	1	-	1	0	1	1	0	1	1	0	(B6h)
1 <sup>st</sup> Parameterr	1	↑	1	-	---	---	NO1	NO0	STD1	STD0	EQ1	EQ0	02h
2 <sup>nd</sup> Paramete	1	↑	1	-	---	---	---	---	PTG1	PTG0	PT1	PT0	02h

NOTE: "-- Don't care

Description	-1 <sup>st</sup> parameter: Set output waveform relation.				
	-NO[1:0]: Set the amount of non-overlap of the gate output				
	<b>NO[1:0]</b>	<b>Amount of non-overlap of the gate output</b>			
		Refer the Internal oscillator			
		Refer the PCLK			
	00	0			
		2 clock cycle			
		8 clock cycle			
	01	1			
		4 clock cycle			
	16 clock cycle				
10	2				
	8 clock cycle				
	32 clock cycle				
11	3				
	10 clock cycle				
	40 clock cycle				
-SDT[1:0]: Set delay amount from gate signal falling edge of the source output.					
<b>SDT[1:0]</b>	<b>Amount of non-overlap of the gate output</b>				
	Refer the Internal oscillator				
	Refer the PCLK				
00	0				
	1 clock cycle				
	4 clock cycle				
01	1				
	2 clock cycle				
	8 clock cycle				
10	2				
	3 clock cycle				
	12 clock cycle				
11	3				
	4 clock cycle				
	16 clock cycle				
-EQ[1:0]: Set the Equalizing period					
<b>EQ[1:0]</b>	<b>Amount of non-overlap of the gate output</b>				
	Refer the Internal oscillator				
	Refer the PCLK				
00	0				
	0 clock cycle				
	0 clock cycle				
01	1				
	4 clock cycle				
	16 clock cycle				
10	2				
	6 clock cycle				
	24 clock cycle				
11	3				
	8 clock cycle				
	32 clock cycle				
-2 <sup>nd</sup> parameter: Set the output waveform in non-display area.					
-PTG[1:0]: Determine gate output in a non-display area in the partial mode					
<b>PTG[1:0]</b>	<b>Gate output in a non-display area</b>				
00	0				
	Normal scan				
01	1				
	Fix on VGL				
10	2				
	Fix on VGL				
11	3				
	Fix on VGL				
-PT[1:0]: Determine Source /VCOM output in a non-display area in the partial mode					
<b>PT[1:0]</b>	<b>Source output on non-display area</b>	<b>VCOM output on non-display area</b>			
	Positive	Negative	Positive	Negative	
00	0	V63	V0	VCOML	VCOMH
01	1	V0	V63	VCOML	VCOMH
10	2	AGND	AGND	AGND	AGND
11	3	Hi-z	Hi-z	AGND	AGND
Restriction	-If this register not using the register need be reserved.				

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Register Availability	Status		Availability			
	Normal Mode On, Idle Mode Off, Sleep Out		Yes			
	Normal Mode On, Idle Mode On, Sleep Out		Yes			
	Partial Mode On, Idle Mode Off, Sleep Out		Yes			
	Partial Mode On, Idle Mode On, Sleep Out		Yes			
Sleep In		Yes				
Default	Status		Default Value			
		NO[1:0]	STD[1:0]	EQ[1:0]	PTG[1:0]	PT[1:0]
	Power On Sequence	00	00	10	00	10
	S/W Reset	00	00	10	00	10
H/W Reset	00	00	10	00	10	
Flow Chart	<p style="text-align: center;">-----</p> <p style="text-align: center;">DISSET5 (B6h)</p> <p style="text-align: center;">↓</p> <div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 0 auto;"> <p style="text-align: center;">1<sup>st</sup> Parameter NO[1:0], STD[1:0], EQ[1:0] 2<sup>nd</sup> Parameter: PTG[1:0], PT[1:0]</p> </div> <div style="border: 1px dashed black; padding: 10px; width: fit-content; margin: 10px auto;"> <p style="text-align: center;">Legend</p> <ul style="list-style-type: none"> <li style="margin-bottom: 5px;">Command</li> <li style="margin-bottom: 5px;">Parameter</li> <li style="margin-bottom: 5px;">Display</li> <li style="margin-bottom: 5px;">Action</li> <li style="margin-bottom: 5px;">Mode</li> <li style="margin-bottom: 5px;">Sequential transfer</li> </ul> </div>					

## 10.2.8 VSYNCOUT (BCh):

BCh	VSYNCOUT													
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)	
VSYNCOUT	0	↑	1	-	1	0	1	1	1	1	1	0	0	(BCh)
1 <sup>st</sup> Parameter	No Parameter													

NOTE: “-“ Don't care

**Description**

This command comes off external VSYNC a display synchronous.

Operation shifts to an internal synchronous mode by the VSYNCOUT command while external VSYNC is synchronizing. VSYNCOUT command is recognized frame synchronously. The shift operation becomes the same for the VSYNCOUT command issued within the range of the inside of the figure.

**Restriction**

-If this register not using the register need be reserved.

**Register Availability**

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

**Default**

Status	Default Value
Power On Sequence	OFF
S/W Reset	OFF
H/W Reset	OFF

**Flow Chart**

**Legend**

- Command
- Parameter
- Display
- Action
- Mode
- Sequential transfer

## 10.2.9 VSYNCIN (BDh):

BDH	VSYNCIN													
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)	
VSYNCOUT	0	↑	1	-	1	0	1	1	1	1	1	0	1	(BDh)
1 <sup>st</sup> Parameter	No Parameter													

NOTE: “-“ Don't care

Description	<p>-The frame to which the command is input finishes sending data by an internal vertical synchronizing signal. Afterward, an external vertical synchronizing signal is waiting for at the rest period. The operation after that becomes external synchronous. Operation enters the rest period when the transmission of data ends for one frame while the external is synchronizing.</p> <p><b>wait:</b> Synchronous waiting period. Operation is external VSYNC perceives “L” level of the VSYNC signal and internal operate and after synchronization t, scans the display for one frame. External VSYNC signal through TE pin. Operation enters the synchronous waiting period again when the display sacanning ends.</p>												
Restriction	-If this register not using the register need be reserved.												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>OFF</td> </tr> <tr> <td>S/W Reset</td> <td>OFF</td> </tr> <tr> <td>H/W Reset</td> <td>OFF</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	OFF	S/W Reset	OFF	H/W Reset	OFF				
Status	Default Value												
Power On Sequence	OFF												
S/W Reset	OFF												
H/W Reset	OFF												
Flow Chart	<div style="border: 1px dashed black; padding: 5px; margin-top: 10px;"> <p>Legend</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul> </div>												

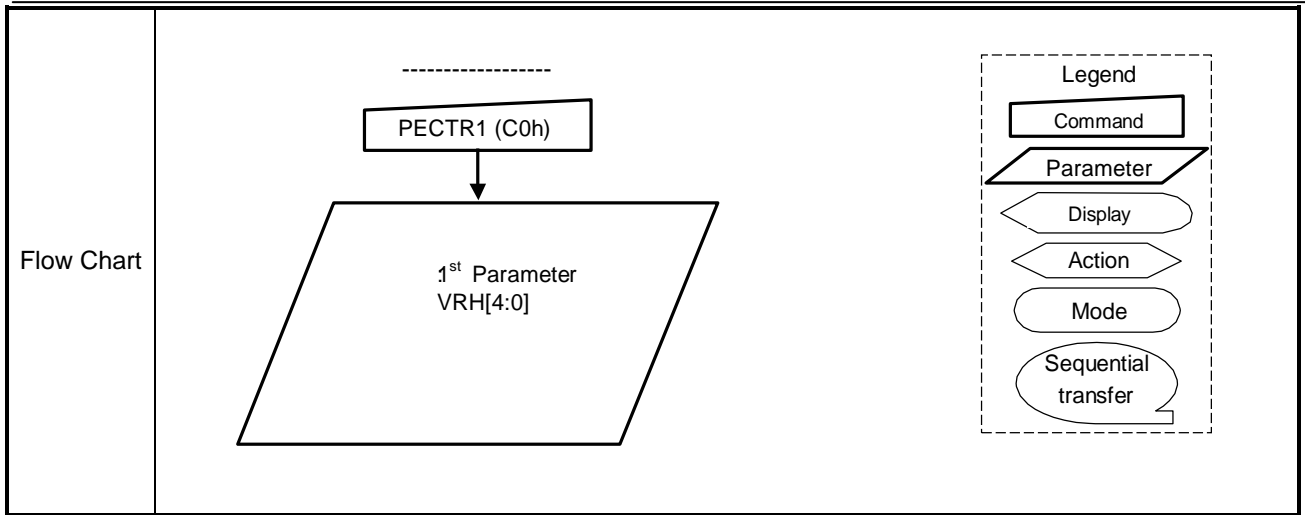


## 10.2.10 PWCTR1 (C0h): Power Control 1

C0H	PWCTR1 (Power Control 1)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWCTR1	0	↑	1	-	1	1	0	0	0	0	0	0	(C0h)
1 <sup>st</sup> Parameter	1	↑	1	-	0	0	0	VRH4	VRH3	VRH2	VRH1	VRH0	

NOTE: "-" Don't care

Description	-Set the GVDD and voltage													
	<b>VRH[4:0]</b>	<b>GVDD</b>												
	00000	0 5.00												
	00001	1 4.75												
	00010	2 4.70												
	00011	3 4.65												
	00100	4 4.60												
	00101	5 4.55												
	00110	6 4.50												
	00111	7 4.45												
	01000	8 4.40												
	01001	9 4.35												
	01010	10 4.30												
	01011	11 4.25												
	01100	12 4.20												
	01101	13 4.15												
	01110	14 4.10												
	01111	15 4.05												
	10000	16 4.00												
	10001	17 3.95												
	10010	18 3.90												
	10011	19 3.85												
	10100	20 3.80												
	10101	21 3.75												
	10110	22 3.70												
	10111	23 3.65												
	11000	24 3.60												
	11001	25 3.55												
	11010	26 3.50												
	11011	27 3.45												
	11100	28 3.40												
	11101	29 3.35												
11110	30 3.25													
11111	31 3.00													
Restriction	-If this register not using the register need be reserved. -The deviation value of GVDD between with Measurement and Specification: <b>Max &lt;=50mV</b> -The deviation value of VCI1 between with Measurement and Specification: <b>Max &lt;= 1%</b>													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td></td> <td>LCM1, LCM0 = "01" TR LC Type</td> </tr> <tr> <td></td> <td>VRH[4:0]</td> </tr> <tr> <td>Power On Sequence</td> <td>10000</td> </tr> <tr> <td>S/W Reset</td> <td>10000</td> </tr> <tr> <td>H/W Reset</td> <td>10000</td> </tr> </tbody> </table>		Status	Default Value		LCM1, LCM0 = "01" TR LC Type		VRH[4:0]	Power On Sequence	10000	S/W Reset	10000	H/W Reset	10000
Status	Default Value													
	LCM1, LCM0 = "01" TR LC Type													
	VRH[4:0]													
Power On Sequence	10000													
S/W Reset	10000													
H/W Reset	10000													



## 10.2.11 PWCTR2 (C1h): Power Control 2

C1H	PWCTR2 (Power Control 2)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWCTR2	0	↑	1	-	1	1	0	0	0	0	0	1	(C1h)
1 <sup>st</sup> Parameter	1	↑	1	-	VGH3	VGH2	VGH1	VGH0	VGL3	VGL2	VGL1	VGL0	
2 <sup>nd</sup> Parameter	1	↑	1	-	--	--	--	--	--	GOT2	GOT1	GOT0	

NOTE: "-" Don't care

Description	-Set the AVDD, VCL, VGH and VGL supply power level																																																																													
	<table border="1"> <thead> <tr> <th>VGH[2:0]/VGL[2:0]</th> <th>VGH</th> <th>VGL</th> </tr> </thead> <tbody> <tr><td>0000</td><td>0</td><td>X</td></tr> <tr><td>0001</td><td>1</td><td>X</td></tr> <tr><td>0010</td><td>2</td><td>X</td></tr> <tr><td>0011</td><td>3</td><td>X</td></tr> <tr><td>0100</td><td>4</td><td>X</td></tr> <tr><td>0101</td><td>5</td><td>12</td></tr> <tr><td>0110</td><td>6</td><td>12.5</td></tr> <tr><td>0111</td><td>7</td><td>13.0</td></tr> <tr><td>1000</td><td>8</td><td>13.5</td></tr> <tr><td>1001</td><td>9</td><td>14.0</td></tr> <tr><td>1010</td><td>10</td><td>14.5</td></tr> <tr><td>1011</td><td>11</td><td>15.0</td></tr> <tr><td>1100</td><td>12</td><td>15.5</td></tr> <tr><td>1101</td><td>13</td><td>16.0</td></tr> <tr><td>1110</td><td>14</td><td>16.5</td></tr> <tr><td>1111</td><td>15</td><td>x</td></tr> </tbody> </table> <p>Unit(V)</p> <p>GOT [2:0]: Define VGH2 level period.</p> <table border="1"> <thead> <tr> <th>GOT[2:0]</th> <th>UC mode OSC clk</th> <th>RGB pixel clk</th> </tr> </thead> <tbody> <tr><td>000</td><td>0</td><td>0</td></tr> <tr><td>001</td><td>4</td><td>16</td></tr> <tr><td>010</td><td>6</td><td>24</td></tr> <tr><td>011</td><td>9</td><td>36</td></tr> <tr><td>100</td><td>11</td><td>44</td></tr> <tr><td>101</td><td>14</td><td>56</td></tr> <tr><td>110</td><td>16</td><td>64</td></tr> <tr><td>111</td><td>19</td><td>76</td></tr> </tbody> </table> <p>Note: When VCI1=2.5V, VDD=2.5V, Set-up cycle 1 effective=95%, Set-up cycle 2 effective=98%,</p>	VGH[2:0]/VGL[2:0]	VGH	VGL	0000	0	X	0001	1	X	0010	2	X	0011	3	X	0100	4	X	0101	5	12	0110	6	12.5	0111	7	13.0	1000	8	13.5	1001	9	14.0	1010	10	14.5	1011	11	15.0	1100	12	15.5	1101	13	16.0	1110	14	16.5	1111	15	x	GOT[2:0]	UC mode OSC clk	RGB pixel clk	000	0	0	001	4	16	010	6	24	011	9	36	100	11	44	101	14	56	110	16	64	111	19
VGH[2:0]/VGL[2:0]	VGH	VGL																																																																												
0000	0	X																																																																												
0001	1	X																																																																												
0010	2	X																																																																												
0011	3	X																																																																												
0100	4	X																																																																												
0101	5	12																																																																												
0110	6	12.5																																																																												
0111	7	13.0																																																																												
1000	8	13.5																																																																												
1001	9	14.0																																																																												
1010	10	14.5																																																																												
1011	11	15.0																																																																												
1100	12	15.5																																																																												
1101	13	16.0																																																																												
1110	14	16.5																																																																												
1111	15	x																																																																												
GOT[2:0]	UC mode OSC clk	RGB pixel clk																																																																												
000	0	0																																																																												
001	4	16																																																																												
010	6	24																																																																												
011	9	36																																																																												
100	11	44																																																																												
101	14	56																																																																												
110	16	64																																																																												
111	19	76																																																																												
Restriction	-If this register not using the register need be reserved. -The deviation value of VGH/ VGL between with Measurement and Specification: <b>Max: VGH-VGL&lt;=1V</b> -VGH-VGL <= 32V																																																																													

# ST7787

Register Availability	Status		Availability	
	Normal Mode On, Idle Mode Off, Sleep Out		Yes	
	Normal Mode On, Idle Mode On, Sleep Out		Yes	
	Partial Mode On, Idle Mode Off, Sleep Out		Yes	
	Partial Mode On, Idle Mode On, Sleep Out		Yes	
	Sleep In		Yes	
Default	Status		Default Value	
		GOT[2:0]	VGH[3:0]	VGL[3:0]
	Power On Sequence	00h	C0h	80h
	S/W Reset	00h	C0h	80h
	H/W Reset	00h	C0h	80h
Flow Chart	<pre> graph TD     A[PWCTR2 (C1h)] --&gt; B[1st Parameter 2nd Parameter]     </pre> <p>Legend</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>			

## 10.2.12 PWCTR3 (C2h): Power Control 3 (in Normal mode/ Full colors)

C2H	PWCTR3 (Power Control 3)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWCTR3	0	↑	1	-	1	1	0	0	0	0	1	0	(C2h)
1 <sup>st</sup> Parameter	1	↑	1	-	0	0	0	0	0	APA2	APA1	APA0	
2 <sup>nd</sup> Parameter	1	↑	1	-	STEP1A_SEL3	STEP1A_SEL2	STEP1A_SEL1	STEP1A_SEL0	0	STEP2A_SEL2	STEP2A_SEL1	STEP2A_SEL0	
3 <sup>rd</sup> Parameter	1	↑	1	-	1	LDO5_SEL2	LDO5_SEL1	LDO5_SEL0	---	STEP4A_SEL2	STEP4A_SEL1	STEP4A_SEL0	
4 <sup>th</sup> Parameter	1	↑	1	-	-	STEP1AP_SEL2	STEP1AP_SEL1	STEP1AP_SEL0	---	STEP2PA_SEL2	STEP2PA_SEL1	STEP2PA_SEL0	
5 <sup>th</sup> Parameter	1	↑	1	-	-	-	-	-	-	STEP4PA_SEL2	STEP4PA_SEL1	STEP4PA_SEL0	

NOTE: “-“ Don't care

Description	<p>-Set the amount of current in Operational amplifier in normal mode/full colors.                  -Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.</p>				
	<b>APA[2:0]</b>		<b>Amount of Current in Operational Amplifier</b>		
	000	0	Operation of the operational amplifier stops		
	001	1	Small		
	010	2	Medium Low		
	011	3	Medium		
	100	4	Medium High		
	101	5	Large		
	110	6	Reserved		
	111	7	Reserved		
	<p>-Set the Booster circuit Step-up cycle in Normal mode/ full colors.</p>				
	<b>Step1A_SEL[3:0]</b>		<b>Step-up cycle in Booster circuit 1</b>		
	0000	0	OSC/2048		
	0001	1	OSC/1024		
	0010	2	OSC/512		
0011	3	OSC/128			
0100	4	OSC/64			
0101	5	OSC/16			
0110	6	OSC/8			
0111	7	OSC/4			
1000	8	OSC/2048			
1001	9	OSC/1024			
1010	10	OSC/512			
1011	11	OSC/128			
1100	12	OSC/64			
1101	13	OSC/16			
1110	14	OSC/8			
1111	15	OSC/4			
<b>LDO5 [2:0]</b>		<b>C1S(V)</b>			
000	0	4.5			
001	1	4.6			
010	2	4.7			
011	3	4.8			
100	4	4.9			
101	5	5.0			
110	6	5.1			
111	7	X			
Unit(V)					
<p>Unit:KHz                  Note:While Step1A_SEL3 setting to '0', the charge pump circuit is selected to "Single mode". On the contrary to "Dual mode".</p>					
<b>Step2A_SEL[2:0]</b>		<b>Step-up cycle in Booster circuit 2</b>	<b>Step4A_SEL[2:0]</b>	<b>Step-up cycle in Booster circuit 4</b>	
000	0	OSC/2048	000	0	OSC/2048
001	1	OSC/1024	001	1	OSC/1024
010	2	OSC/512	010	2	OSC/512
011	3	OSC/128	011	3	OSC/128
100	4	OSC/64	100	4	OSC/64
101	5	OSC/16	101	5	OSC/16
110	6	OSC/8	110	6	OSC/8
111	7	OSC/4	111	7	OSC/4
Unit:KHz					

1. Set the Booster circuit Step-up cycle during porch area in Normal mode/ full colors.

Step1PA_SEL[2:0]		Step-up cycle in Booster circuit 1	Step2PA_SEL[2:0]		Step-up cycle in Booster circuit 2
000	0	OSC/2048	000	0	OSC/2048
001	1	OSC/1024	001	1	OSC/1024
010	2	OSC/512	010	2	OSC/512
011	3	OSC/128	011	3	OSC/128
100	4	OSC/64	100	4	OSC/64
101	5	OSC/16	101	5	OSC/16
110	6	OSC/8	110	6	OSC/8
111	7	OSC/4	111	7	OSC/4

Unit:KHz

Step4PA_SEL[2:0]		Step-up cycle in Booster circuit 4
000	0	OSC/2048
001	1	OSC/1024
010	2	OSC/512
011	3	OSC/128
100	4	OSC/64
101	5	OSC/16
110	6	OSC/8
111	7	OSC/4

Unit:KHz

Note: BCLK is Clock frequency for Booster circuit

Restriction -If some parameter of the register not use the register need to be reserved.

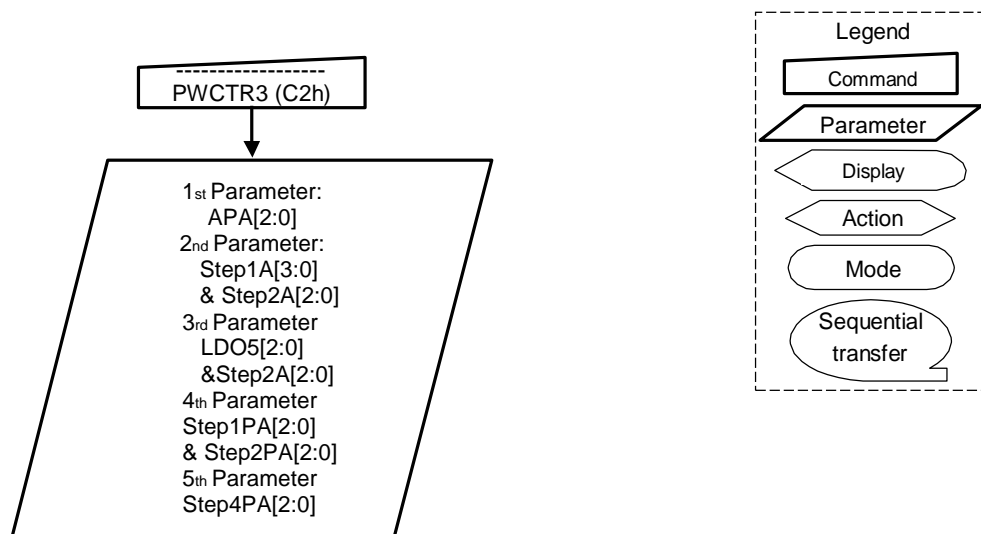
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value							
	APA[2:0]	Step1A_SEL[3:0]	Step2A_SEL[2:0]	Ste4A_SEL[2:0]	LDO5_SEL[2:0]	Step1PA_SEL[3:0]	Step2PA_SEL[2:0]	Ste4PA_SEL[2:0]
Power On Sequence	01h	0Bh	03h	03h	00h	00h	00h	00h
S/W Reset	01h	0Bh	03h	03h	00h	00h	00h	00h
H/W Reset	01h	0Bh	03h	03h	00h	00h	00h	00h

Flow Chart



## 10.2.13 PWCTR4 (C3h): Power Control 4 (in Idle mode/ 8-colors)

C3H	PWCTR4 (Power Control 4)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWCTR4	0	↑	1	-	1	1	0	0	0	0	1	1	(C3h)
1 <sup>st</sup> Parameter	1	↑	1	-	0	0	0	0	0	APB2	APB1	APB0	
2 <sup>nd</sup> Parameter	1	↑	1	-	STEP1B_SEL3	STEP1B_SEL2	STEP1B_SEL1	STEP1B_SEL0	0	STEP2B_SEL2	STEP2B_SEL1	STEP2B_SEL0	
3 <sup>rd</sup> Parameter	1	↑	1							STEP4B_SEL2	STEP4B_SEL1	STEP4B_SEL0	
4 <sup>th</sup> Parameter	1	↑	1			STEP1PB_SEL2	STEP1PB_SEL1	STEP1PB_SEL0		STEP2PB_SEL2	STEP2PB_SEL1	STEP2PB_SEL0	
5 <sup>th</sup> Parameter	1	↑	1							STEP4PB_SEL2	STEP4PB_SEL1	STEP4PB_SEL0	

NOTE: “-“ Don't care

Description	<p>-Set the amount of current in Operational amplifier in Idle mode/8 colors.                  -Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.</p>				
	<b>APB[2:0]</b>		<b>Amount of Current in Operational Amplifier</b>		
	000	0	Operation of the operational amplifier stops		
	001	1	Small		
	010	2	Medium Low		
	011	3	Medium		
	100	4	Medium High		
	101	5	Large		
	110	6	Reserved		
	111	7	Reserved		
	<p>-Set the Booster circuit Step-up cycle in Idle mode/8 colors.</p>				
	<b>Step1B_SEL[3:0]</b>		<b>Step-up cycle in Booster circuit 1</b>		
	0000	0	OSC/2048		
	0001	1	OSC/1024		
	0010	2	OSC/512		
0011	3	OSC/128			
0100	4	OSC/64			
0101	5	OSC/16			
0110	6	OSC/8			
0111	7	OSC/4			
1000	8	OSC/2048			
1001	9	OSC/1024			
1010	10	OSC/512			
1011	11	OSC/128			
1100	12	OSC/64			
1101	13	OSC/16			
1110	14	OSC/8			
1111	15	OSC/4			
<p>Unit:KHz                  Note:While Step1B_SEL3 setting to '0', the charge pump circuit is selected to "Single mode". On the contrary to "Dual mode".</p>					
<b>Step2B_SEL[2:0]</b>		<b>Step-up cycle in Booster circuit 2</b>	<b>Step4B_SEL[2:0]</b>	<b>Step-up cycle in Booster circuit 4</b>	
000	0	OSC/1024	000	0	OSC/2048
001	1	OSC/2048	001	1	OSC/1024
010	2	OSC/1024	010	2	OSC/512
011	3	OSC/512	011	3	OSC/128
100	4	OSC/128	100	4	OSC/64
101	5	OSC/64	101	5	OSC/16
110	6	OSC/16	110	6	OSC/8
111	7	OSC/8	111	7	OSC/4

1. Set the Booster circuit Step-up cycle during porch area in Idle mode.

Step1PB_SEL[2:0]		Step-up cycle in Booster circuit 1	Step2PB_SEL[2:0]		Step-up cycle in Booster circuit 2
000	0	OSC/2048	000	0	OSC/2048
001	1	OSC/1024	001	1	OSC/1024
010	2	OSC/512	010	2	OSC/512
011	3	OSC/128	011	3	OSC/128
100	4	OSC/64	100	4	OSC/64
101	5	OSC/16	101	5	OSC/16
110	6	OSC/8	110	6	OSC/8
111	7	OSC/4	111	7	OSC/4

Unit:KHz

Step4PB_SEL[2:0]		Step-up cycle in Booster circuit 4
000	0	OSC/2048
001	1	OSC/1024
010	2	OSC/512
011	3	OSC/128
100	4	OSC/64
101	5	OSC/16
110	6	OSC/8
111	7	OSC/4

Unit:KHz

Note: BCLK is Clock frequency for Booster circuit

Restriction -If some parameter of the register not use the register need to be reserved.

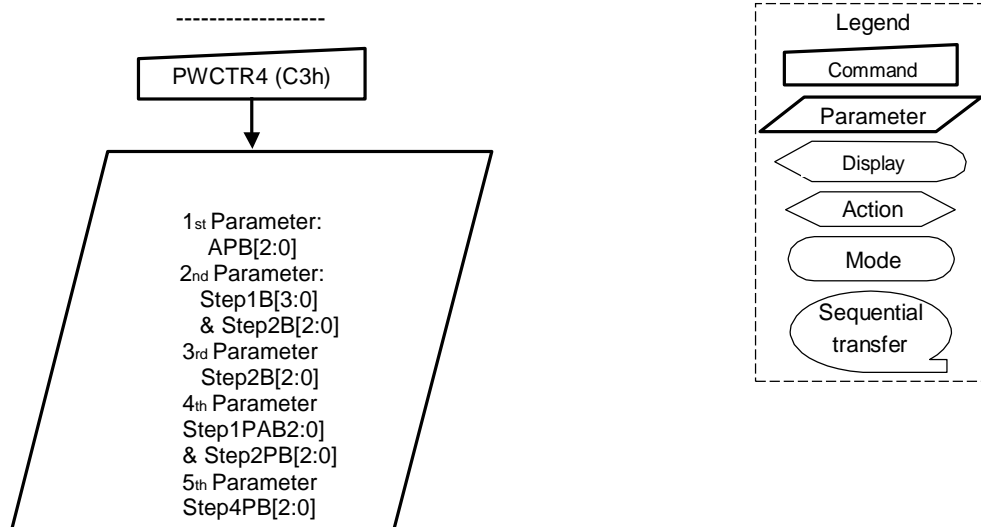
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value						
	APB[2:0]	Step1B_SEL[3:0]	Step2B_SEL[2:0]	Ste4B_SEL[2:0]	Step1PB_SEL[3:0]	Step2PB_SEL[2:0]	Ste4PB_SEL[2:0]
Power On Sequence	01h	00h	00h	00h	00h	00h	00h
S/W Reset	01h	00h	00h	00h	00h	00h	00h
H/W Reset	01h	00h	00h	00h	00h	00h	00h

Flow Chart





## 10.2.14 PWCTR5 (C4h): Power Control 5 (in Partial mode/ full-colors)

C4H	PWCTR5 (Power Control 5)												(Code)
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWCTR5	0	↑	1	-	1	1	0	0	0	1	0	0	(C4h)
1 <sup>st</sup> Parameter	1	↑	1	-	0	0	0	0	0	APC2	APC1	APC0	
2 <sup>nd</sup> Parameter	1	↑	1	-	STEP1C_SEL3	STEP1C_SEL2	STEP1C_SEL1	STEP1C_SEL0	0	STEP2C_SEL2	STEP2C_SEL1	STEP2C_SEL0	00h
3 <sup>rd</sup> Parameter	1	↑	1	-	-	--	-	-	-	STEP4C_SEL2	STEP4C_SEL1	STEP4C_SEL0	
4 <sup>th</sup> Parameter	1	↑	1	-	-	STEP1PC_SEL2	STEP1PC_SEL1	STEP1PC_SEL0	-	STEP2PC_SEL2	STEP2PC_SEL1	STEP2PC_SEL0	
5 <sup>th</sup> Parameter	1	↑	1	-	-	-	-	-	-	STEP4PC_SEL2	STEP4PC_SEL1	STEP4PC_SEL0	

NOTE: “-“ Don't care

Description	-Set the amount of current in Operational amplifier in Partial mode/ full-colors.		
	-Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.		
	<b>APC[2:0]</b>	<b>Amount of Current in Operational Amplifier</b>	
	000	0 Operation of the operational amplifier stops	
	001	1 Small	
	010	2 Medium Low	
	011	3 Medium	
	100	4 Medium High	
	101	5 Large	
	110	6 Reserved	
	111	7 Reserved	
	-Set the Booster circuit Step-up cycle in Partial mode/ full-colors.		
	Note: BCLK is Clock frequency for Booster circuit		
	<b>Step1C_SEL[3:0]</b>	<b>Step-up cycle in Booster circuit 1</b>	
	0000	0 OSC/2048	
0001	1 OSC/1024		
0010	2 OSC/512		
0011	3 OSC/128		
0100	4 OSC/64		
0101	5 OSC/16		
0110	6 OSC/8		
0111	7 OSC/4		
1000	8 OSC/2048		
1001	9 OSC/1024		
1010	10 OSC/512		
1011	11 OSC/128		
1100	12 OSC/64		
1101	13 OSC/16		
1110	14 OSC/8		
1111	15 OSC/4		
Unit:KHz			
Note: While Step1B_SEL3 setting to '0', the charge pump circuit is selected to "Single mode". On the contrary to "Dual mode".			
<b>Step2C_SEL[2:0]</b>	<b>Step-up cycle in Booster circuit 2</b>	<b>Step4C_SEL[2:0]</b>	<b>Step-up cycle in Booster circuit 4</b>
000	0 OSC/2048	000	0 OSC/2048
001	1 OSC/1024	001	1 OSC/1024
010	2 OSC/512	010	2 OSC/512
011	3 OSC/128	011	3 OSC/128
100	4 OSC/64	100	4 OSC/64
101	5 OSC/16	101	5 OSC/16
110	6 OSC/8	110	6 OSC/8
111	7 OSC/4	111	7 OSC/4

1. Set the Booster circuit Step-up cycle during porch area in Partial mode/ full-colors.	<table border="1"> <thead> <tr> <th colspan="2">Step1PC_SEL[2:0]</th> <th>Step-up cycle in Booster circuit 1</th> <th colspan="2">Step2PC_SEL[2:0]</th> <th>Step-up cycle in Booster circuit 2</th> </tr> </thead> <tbody> <tr><td>000</td><td>0</td><td>OSC/2048</td><td>000</td><td>0</td><td>OSC/2048</td></tr> <tr><td>001</td><td>1</td><td>OSC/1024</td><td>001</td><td>1</td><td>OSC/1024</td></tr> <tr><td>010</td><td>2</td><td>OSC/512</td><td>010</td><td>2</td><td>OSC/512</td></tr> <tr><td>011</td><td>3</td><td>OSC/128</td><td>011</td><td>3</td><td>OSC/128</td></tr> <tr><td>100</td><td>4</td><td>OSC/64</td><td>100</td><td>4</td><td>OSC/64</td></tr> <tr><td>101</td><td>5</td><td>OSC/16</td><td>101</td><td>5</td><td>OSC/16</td></tr> <tr><td>110</td><td>6</td><td>OSC/8</td><td>110</td><td>6</td><td>OSC/8</td></tr> <tr><td>111</td><td>7</td><td>OSC/4</td><td>111</td><td>7</td><td>OSC/4</td></tr> </tbody> </table>						Step1PC_SEL[2:0]		Step-up cycle in Booster circuit 1	Step2PC_SEL[2:0]		Step-up cycle in Booster circuit 2	000	0	OSC/2048	000	0	OSC/2048	001	1	OSC/1024	001	1	OSC/1024	010	2	OSC/512	010	2	OSC/512	011	3	OSC/128	011	3	OSC/128	100	4	OSC/64	100	4	OSC/64	101	5	OSC/16	101	5	OSC/16	110	6	OSC/8	110	6	OSC/8	111	7	OSC/4	111	7	OSC/4
	Step1PC_SEL[2:0]		Step-up cycle in Booster circuit 1	Step2PC_SEL[2:0]		Step-up cycle in Booster circuit 2																																																						
	000	0	OSC/2048	000	0	OSC/2048																																																						
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<table border="1"> <thead> <tr> <th colspan="2">Step4PC_SEL[2:0]</th> <th>Step-up cycle in Booster circuit 4</th> </tr> </thead> <tbody> <tr><td>000</td><td>0</td><td>OSC/2048</td></tr> <tr><td>001</td><td>1</td><td>OSC/1024</td></tr> <tr><td>010</td><td>2</td><td>OSC/512</td></tr> <tr><td>011</td><td>3</td><td>OSC/128</td></tr> <tr><td>100</td><td>4</td><td>OSC/64</td></tr> <tr><td>101</td><td>5</td><td>OSC/16</td></tr> <tr><td>110</td><td>6</td><td>OSC/8</td></tr> <tr><td>111</td><td>7</td><td>OSC/4</td></tr> </tbody> </table>						Step4PC_SEL[2:0]		Step-up cycle in Booster circuit 4	000	0	OSC/2048	001	1	OSC/1024	010	2	OSC/512	011	3	OSC/128	100	4	OSC/64	101	5	OSC/16	110	6	OSC/8	111	7	OSC/4																												
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Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="7">Default Value</th> </tr> <tr> <th>APC[2:0]</th> <th>Step1C_SEL[3:0]</th> <th>Step2C_SEL[2:0]</th> <th>Ste4C_SEL[2:0]</th> <th>Step1PC_SEL[3:0]</th> <th>Step2PC_SEL[2:0]</th> <th>Ste4PC_SEL[2:0]</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>01h</td> <td>0Bh</td> <td>03h</td> <td>03h</td> <td>00h</td> <td>00h</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>01h</td> <td>0Bh</td> <td>03h</td> <td>03h</td> <td>00h</td> <td>00h</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>01h</td> <td>0Bh</td> <td>03h</td> <td>03h</td> <td>00h</td> <td>00h</td> <td>00h</td> </tr> </tbody> </table>						Status	Default Value							APC[2:0]	Step1C_SEL[3:0]	Step2C_SEL[2:0]	Ste4C_SEL[2:0]	Step1PC_SEL[3:0]	Step2PC_SEL[2:0]	Ste4PC_SEL[2:0]	Power On Sequence	01h	0Bh	03h	03h	00h	00h	00h	S/W Reset	01h	0Bh	03h	03h	00h	00h	00h	H/W Reset	01h	0Bh	03h	03h	00h	00h	00h															
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S/W Reset	01h	0Bh	03h	03h	00h	00h	00h																																																					
H/W Reset	01h	0Bh	03h	03h	00h	00h	00h																																																					
Flow Chart	<div style="display: flex; align-items: center;"> <div style="flex: 1;"> <p style="text-align: center;">-----</p> <div style="border: 1px solid black; width: fit-content; margin: 0 auto; padding: 5px;">PWCTR4 (C4h)</div> <p style="text-align: center;">↓</p> <div style="border: 1px solid black; width: 200px; height: 150px; margin: 0 auto; padding: 10px;"> <p>1<sup>st</sup> Parameter: APB[2:0]</p> <p>2<sup>nd</sup> Parameter: Step1B[3:0] &amp; Step2B[2:0]</p> <p>3<sup>rd</sup> Parameter Step2B[2:0]</p> <p>4<sup>th</sup> Parameter Step1PAB[2:0] &amp; Step2PB[2:0]</p> <p>5<sup>th</sup> Parameter Step4PB[2:0]</p> </div> </div> <div style="flex: 0.5; border: 1px dashed black; padding: 5px; margin-left: 20px;"> <p style="text-align: center;">Legend</p> <div style="display: flex; flex-direction: column; gap: 5px;"> <div style="border: 1px solid black; width: 50px; height: 15px; margin: 0 auto;"></div> <div style="border: 1px solid black; width: 50px; height: 15px; transform: rotate(-15deg); margin: 0 auto;"></div> <div style="border: 1px solid black; width: 50px; height: 15px; border-radius: 10px; margin: 0 auto;"></div> <div style="border: 1px solid black; width: 50px; height: 15px; border-radius: 10px; margin: 0 auto;"></div> <div style="border: 1px solid black; width: 50px; height: 15px; border-radius: 10px; margin: 0 auto;"></div> <div style="border: 1px solid black; width: 50px; height: 15px; border-radius: 10px; margin: 0 auto;"></div> </div> </div> </div>																																																											

## 10.2.15 VMCTR1 (C5h): VCOM Control 1

C5H	VMCTR1 (VCOM Control 1)												(Code)
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VMCTR1	0	↑	1	-	1	1	0	0	0	1	0	1	(C5h)
1 <sup>st</sup> Parameter	1	↑	1	-	0	VMH_R6	VMH_R5	VMH_R4	VMH_R3	VMH_R2	VMH_R1	VMH_R0	
2 <sup>nd</sup> Parameter	1	↑	1	-	0	VMH_IDMON6	VMH_IDMON5	VMH_IDMON4	VMH_IDMON3	VMH_IDMON2	VMH_IDMON1	VMH_IDMON0	
3 <sup>rd</sup> Parameter	1	↑	1	-	nVM0	---	----	----	----	----	----	----	

NOTE: "-- Don't care

Description	-Set VCOMH Voltage in normal mode/full colors.											
	VMH[6:0]	VCOMH	VMH[6:0]	VCOMH	VMH[6:0]	VCOMH	VMH[6:0]	VCOMH	VMH[6:0]	VCOMH	VMH[6:0]	VCOMH
	0000000	0	2.500	0011011	27	3.175	0110110	54	3.850	1010001	81	4.525
	0000001	1	2.525	0011100	28	3.200	0110111	55	3.875	1010010	82	4.550
	0000010	2	2.550	0011101	29	3.225	0111000	56	3.900	1010011	83	4.575
	0000011	3	2.575	0011110	30	3.250	0111001	57	3.925	1010100	84	4.600
	0000100	4	2.600	0011111	31	3.275	0111010	58	3.950	1010101	85	4.625
	0000101	5	2.625	0100000	32	3.300	0111011	59	3.975	1010110	86	4.650
	0000110	6	2.650	0100001	33	3.325	0111100	60	4.000	1010111	87	4.675
	0000111	7	2.675	0100010	34	3.350	0111101	61	4.025	1011000	88	4.700
	0001000	8	2.700	0100011	35	3.375	0111110	62	4.050	1011001	89	4.725
	0001001	9	2.725	0100100	36	3.400	0111111	63	4.075	1011010	90	4.750
	0001010	10	2.750	0100101	37	3.425	1000000	64	4.100	1011011	91	4.775
	0001011	11	2.775	0100110	38	3.450	1000001	65	4.125	1011100	92	4.800
	0001100	12	2.800	0100111	39	3.475	1000010	66	4.150	1011101	93	4.825
	0001101	13	2.825	0101000	40	3.500	1000011	67	4.175	1011110	94	4.850
	0001110	14	2.850	0101001	41	3.525	1000100	68	4.200	1011111	95	4.875
	0001111	15	2.875	0101010	42	3.550	1000101	69	4.225	1100000	96	4.900
	0010000	16	2.900	0101011	43	3.575	1000110	70	4.250	1100001	97	4.925
	0010001	17	2.925	0101100	44	3.600	1000111	71	4.275	1100010	98	4.950
	0010010	18	2.950	0101101	45	3.625	1001000	72	4.300	1100011	99	4.975
	0010011	19	2.975	0101110	46	3.650	1001001	73	4.325	1100100	100	5.000
	0010100	20	3.000	0101111	47	3.675	1001010	74	4.350	1100101	101	Not Permitted
	0010101	21	3.025	0110000	48	3.700	1001011	75	4.375			
	0010110	22	3.050	0110001	49	3.725	1001100	76	4.400	1111111	127	
	0010111	23	3.075	0110010	50	3.750	1001101	77	4.425			
	0011000	24	3.100	0110011	51	3.775	1001110	78	4.450			
	0011001	25	3.125	0110100	52	3.800	1001111	79	4.475			
	0010110	26	3.150	0110101	53	3.825	1010000	80	4.500			
	-When the VCOM circuit use VCOMH + VCOMAC											
	-The VCOML is generated from VCOMH-VCOMAC											
	-VcomH voltage also can be adjusted by VMH_IDOMON[6:0] register in Idle mode/8 colors.											
	VMH_IDOMON[6:0]	VCOMH	VMH_IDOMON[6:0]	VCOMH	VMH_IDOMON[6:0]	VCOMH	VMH_IDOMON[6:0]	VCOMH	VMH_IDOMON[6:0]	VCOMH	VMH_IDOMON[6:0]	VCOMH
	0000000	0	2.500	0011011	27	3.175	0110110	54	3.850	1010001	81	4.525
	0000001	1	2.525	0011100	28	3.200	0110111	55	3.875	1010010	82	4.550
	0000010	2	2.550	0011101	29	3.225	0111000	56	3.900	1010011	83	4.575
	0000011	3	2.575	0011110	30	3.250	0111001	57	3.925	1010100	84	4.600
	0000100	4	2.600	0011111	31	3.275	0111010	58	3.950	1010101	85	4.625
	0000101	5	2.625	0100000	32	3.300	0111011	59	3.975	1010110	86	4.650
	0000110	6	2.650	0100001	33	3.325	0111100	60	4.000	1010111	87	4.675
	0000111	7	2.675	0100010	34	3.350	0111101	61	4.025	1011000	88	4.700
	0001000	8	2.700	0100011	35	3.375	0111110	62	4.050	1011001	89	4.725
	0001001	9	2.725	0100100	36	3.400	0111111	63	4.075	1011010	90	4.750
	0001010	10	2.750	0100101	37	3.425	1000000	64	4.100	1011011	91	4.775
	0001011	11	2.775	0100110	38	3.450	1000001	65	4.125	1011100	92	4.800
	0001100	12	2.800	0100111	39	3.475	1000010	66	4.150	1011101	93	4.825
	0001101	13	2.825	0101000	40	3.500	1000011	67	4.175	1011110	94	4.850
	0001110	14	2.850	0101001	41	3.525	1000100	68	4.200	1011111	95	4.875
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	0010000	16	2.900	0101011	43	3.575	1000110	70	4.250	1100001	97	4.925
	0010001	17	2.925	0101100	44	3.600	1000111	71	4.275	1100010	98	4.950
	0010010	18	2.950	0101101	45	3.625	1001000	72	4.300	1100011	99	4.975
	0010011	19	2.975	0101110	46	3.650	1001001	73	4.325	1100100	100	5.000
	0010100	20	3.000	0101111	47	3.675	1001010	74	4.350	1100101	101	Not Permitted
	0010101	21	3.025	0110000	48	3.700	1001011	75	4.375			
	0010110	22	3.050	0110001	49	3.725	1001100	76	4.400	1111111	127	

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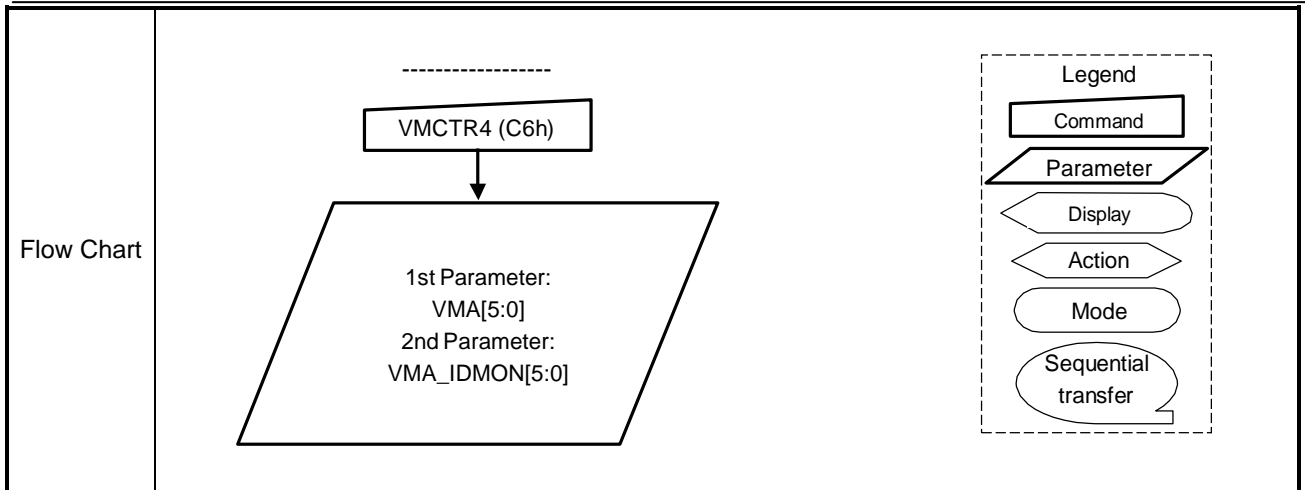
	0010111	23	3.075	0110010	50	3.750	1001101	77	4.425															
	0011000	24	3.100	0110011	51	3.775	1001110	78	4.450															
	0011001	25	3.125	0110100	52	3.800	1001111	79	4.475															
	0011010	26	3.150	0110101	53	3.825	1010000	80	4.500															
	-Set VCOMH Voltage in normal mode/full colors. -When nVM0=1, VcomH voltage can be adjusted by VMH_R[6:0] register. -When nVM0=0, VcomH program will be setted by OTP register value.																							
Restriction	-If this register not using the register need be reserved. -The deviation value of VCOMH/VCOML between with Measurement and Specification: <b>Max&lt;=30mV</b> -The deviation value of VCOMAC between with Measurement and Specification: <b>Max &lt;=50mV</b>																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes		
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In	Yes																							
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="2">Default Value</th> </tr> <tr> <th>nVM0=0, VMH_R[6:0]</th> <th>nVM0=0, VMH_COLOR8M[6:0]</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>28h</td> <td>28h</td> </tr> <tr> <td>S/W Reset</td> <td>28h</td> <td>28h</td> </tr> <tr> <td>H/W Reset</td> <td>28h</td> <td>28h</td> </tr> </tbody> </table>										Status	Default Value		nVM0=0, VMH_R[6:0]	nVM0=0, VMH_COLOR8M[6:0]	Power On Sequence	28h	28h	S/W Reset	28h	28h	H/W Reset	28h	28h
Status	Default Value																							
	nVM0=0, VMH_R[6:0]	nVM0=0, VMH_COLOR8M[6:0]																						
Power On Sequence	28h	28h																						
S/W Reset	28h	28h																						
H/W Reset	28h	28h																						
Flow Chart	<div style="display: flex; align-items: center; justify-content: center;"> <div style="text-align: center; margin-right: 20px;"> <div style="border: 1px solid black; padding: 5px; width: fit-content;">PWCTR4 (C5h)</div> <div style="margin: 5px 0;">↓</div> <div style="border: 1px solid black; padding: 10px; width: 200px; height: 100px; display: flex; flex-direction: column; justify-content: center; align-items: center;"> <div style="margin-bottom: 5px;">1st Parameter: VMH_R[6:0]</div> <div style="margin-bottom: 5px;">2nd Parameter: VMH_COLOR8M[6:0]</div> <div style="margin-bottom: 5px;">3<sup>rd</sup> Parameter nVM0</div> </div> </div> <div style="border: 1px dashed black; padding: 10px; width: 150px;"> <p style="text-align: center; margin: 0;">Legend</p> <div style="margin-bottom: 5px;"><span style="border: 1px solid black; padding: 2px 5px; display: inline-block; width: 20px; height: 10px;"></span> Command</div> <div style="margin-bottom: 5px;"><span style="border: 1px solid black; padding: 2px 5px; display: inline-block; width: 20px; height: 10px; transform: rotate(-45deg);"></span> Parameter</div> <div style="margin-bottom: 5px;"><span style="border: 1px solid black; padding: 2px 5px; display: inline-block; width: 20px; height: 10px; border-radius: 5px;"></span> Display</div> <div style="margin-bottom: 5px;"><span style="border: 1px solid black; padding: 2px 5px; display: inline-block; width: 20px; height: 10px; border-radius: 5px;"></span> Action</div> <div style="margin-bottom: 5px;"><span style="border: 1px solid black; padding: 2px 5px; display: inline-block; width: 20px; height: 10px; border-radius: 5px;"></span> Mode</div> <div style="margin-bottom: 5px;"><span style="border: 1px solid black; padding: 2px 5px; display: inline-block; width: 20px; height: 10px; border-radius: 5px;"></span> Sequential transfer</div> </div> </div>																							

## 10.2.16 VMCTR2 (C6h): VCOM Control 2

C6H	VMCTR2 (VCOM Control 2)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VMCTR2	0	↑	1	-	1	1	0	0	0	1	1	0	(C6h)
1 <sup>st</sup> Parameter	1	↑	1	-	0	0	VMA5	VMA4	VMA3	VMA2	VMA1	VMA0	
2 <sup>nd</sup> Parameter	1	↑	1	-	0	0	VMA_IDMON5	VMA_IDMON4	VMA_IDMON3	VMA_IDMON2	VMA_IDMON1	VMA_IDMON0	

NOTE: "-" Don't care

Description	-Set VCOMAC Voltage in normal mode/full colors.													
	<b>VMA[5:0]</b>	<b>VCOMAC</b>	<b>VMA[5:0]</b>	<b>VCOMAC</b>	<b>VMA[5:0]</b>	<b>VCOMAC</b>	<b>VMA[5:0]</b>	<b>VCOMAC</b>	<b>VMA[5:0]</b>	<b>VCOMAC</b>				
	000000	0	4.000	010000	16	4.800	100000	32	5.600					
	000001	1	4.050	010001	17	4.850	100001	33	5.650					
	000010	2	4.100	010010	18	4.900	100010	34	5.700					
	000011	3	4.150	010011	19	4.950	100011	35	5.750					
	000100	4	4.200	010100	20	5.000	100100	36	5.800					
	000101	5	4.250	010101	21	5.050	100101	37	5.850					
	000110	6	4.300	010110	22	5.100	100110	38	5.900					
	000111	7	4.350	010111	23	5.150	100111	39	5.950					
	001000	8	4.400	011000	24	5.200	101000	40	6.000					
	001001	9	4.450	011001	25	5.250	101001	41		Not Permitted				
	001010	10	4.500	011010	26	5.300								
	001011	11	4.550	011011	27	5.350	111111	63						
	001100	12	4.600	011100	28	5.400								
	001101	13	4.650	011101	29	5.450								
	001110	14	4.700	011110	30	5.500								
	001111	15	4.750	011111	31	5.550								
	Description	-Set VCOMAC Voltage in Idle mode/8 colors.												
		<b>VMA_IDMON[5:0]</b>	<b>VCOMAC</b>	<b>VMA_IDMON[5:0]</b>	<b>VCOMAC</b>	<b>VMA_IDMON[5:0]</b>	<b>VCOMAC</b>	<b>VMA_IDMON[5:0]</b>	<b>VCOMAC</b>	<b>VMA_IDMON[5:0]</b>	<b>VCOMAC</b>			
		000000	0	4.000	010000	16	4.800	100000	32	5.600				
		000001	1	4.050	010001	17	4.850	100001	33	5.650				
		000010	2	4.100	010010	18	4.900	100010	34	5.700				
		000011	3	4.150	010011	19	4.950	100011	35	5.750				
		000100	4	4.200	010100	20	5.000	100100	36	5.800				
000101		5	4.250	010101	21	5.050	100101	37	5.850					
000110		6	4.300	010110	22	5.100	100110	38	5.900					
000111		7	4.350	010111	23	5.150	100111	39	5.950					
001000		8	4.400	011000	24	5.200	101000	40	6.000					
001001		9	4.450	011001	25	5.250	101001	41		Not Permitted				
001010		10	4.500	011010	26	5.300								
001011		11	4.550	011011	27	5.350	111111	63						
001100		12	4.600	011100	28	5.400								
001101		13	4.650	011101	29	5.450								
001110		14	4.700	011110	30	5.500								
001111		15	4.750	011111	31	5.550								
Restriction		-If this register not use the register need be reserved. -The deviation value of VCOMAC between with Measurement and Specification: <b>Max &lt;=50mV</b>												
Register Availability		Status						Availability						
		Normal Mode On, Idle Mode Off, Sleep Out						Yes						
		Normal Mode On, Idle Mode On, Sleep Out						Yes						
		Partial Mode On, Idle Mode Off, Sleep Out						Yes						
		Partial Mode On, Idle Mode On, Sleep Out						Yes						
		Sleep In						Yes						
Default	Status			Default Value										
				LCM1, LCM0 = "01" TR LC Type VMA[6:0]						LCM1, LCM0 = "01" TR LC Type VMA_IDMON[5:0]				
	Power On Sequence			06h						00h				
	S/W Reset			06h						00h				
H/W Reset			06h						00h					



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## 10.2.17 WRID1 (D0h): OTP ID1 set LCM version code

D0H	OTP ID1 set LCM version code												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
OTP-read	0	↑	1	-	1	1	0	1	0	0	0	0	(D0h)
1 <sup>st</sup> Parameter	1	↑	1	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	

Description	-OTP ID1 set the LCM version code													
Restriction	-If this register not using the register need be reserved. -After adjust the C5H command(VcomH voltage) and C6H command(VcomAC voltage), VPP connect 7.5V.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Ooff, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode Off, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>No</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Ooff, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode Off, Idle Mode On, Sleep Out	Yes	Sleep In	No
Status	Availability													
Normal Mode On, Idle Mode Ooff, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode Off, Idle Mode On, Sleep Out	Yes													
Sleep In	No													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>N/A</td> </tr> <tr> <td>S/W Reset</td> <td>N/A</td> </tr> <tr> <td>H/W Reset</td> <td>N/A</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	N/A	S/W Reset	N/A	H/W Reset	N/A				
Status	Default Value													
Power On Sequence	N/A													
S/W Reset	N/A													
H/W Reset	N/A													
Flow Chart	<pre> graph TD     A[MTP_Load (D0H)] --&gt; B[/1st Parameter/]     </pre>													

## 10.2.18 WRID2 (D1h): OTP ID2 set LCM version code

D1H	OTP ID2 set LCM version code												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
OTP-read	0	↑	1	-	1	1	0	1	0	0	0	1	(D1h)
1 <sup>st</sup> Parameter	1	↑	1	-	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	

Description	-OTP ID2 set the LCM version code													
Restriction	-If this register not using the register need be reserved. -After adjust the C5H command(VcomH voltage) and C6H command(VcomAC voltage), Vpp connect 7.5V.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Ooff, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode Off, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>No</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Ooff, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode Off, Idle Mode On, Sleep Out	Yes	Sleep In	No
Status	Availability													
Normal Mode On, Idle Mode Ooff, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode Off, Idle Mode On, Sleep Out	Yes													
Sleep In	No													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>N/A</td> </tr> <tr> <td>S/W Reset</td> <td>N/A</td> </tr> <tr> <td>H/W Reset</td> <td>N/A</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	N/A	S/W Reset	N/A	H/W Reset	N/A				
Status	Default Value													
Power On Sequence	N/A													
S/W Reset	N/A													
H/W Reset	N/A													
Flow Chart	<pre> graph TD     A[MTP_Load (D1H)] --&gt; B[/1st Parameter/]     </pre> <p><b>Legend</b></p> <ul style="list-style-type: none"> <li>Command: Rectangle</li> <li>Parameter: Parallelogram</li> <li>Display: Arrow pointing right</li> <li>Action: Arrow pointing left</li> <li>Mode: Oval</li> <li>Sequential transfer: Oval with arrow</li> </ul>													



D2H	OTP ID3 set LCM version code												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
OTP-read	0	↑	1	-	1	1	0	1	0	0	1	0	(D2h)
1 <sup>st</sup> Parameter	1	↑	1	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	

Description	-OTP ID3 set the project code													
Restriction	-If this register not using the register need be reserved. -After adjust the C5H command(VcomH voltage) and C6H command(VcomAC voltage), VPP connect 7.5V.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Ooff, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode Off, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>No</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Ooff, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode Off, Idle Mode On, Sleep Out	Yes	Sleep In	No
Status	Availability													
Normal Mode On, Idle Mode Ooff, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode Off, Idle Mode On, Sleep Out	Yes													
Sleep In	No													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>N/A</td> </tr> <tr> <td>S/W Reset</td> <td>N/A</td> </tr> <tr> <td>H/W Reset</td> <td>N/A</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	N/A	S/W Reset	N/A	H/W Reset	N/A				
Status	Default Value													
Power On Sequence	N/A													
S/W Reset	N/A													
H/W Reset	N/A													
Flow Chart	<pre> graph TD     A[MTP_Load (D2H)] --&gt; B[/1st Parameter/]     </pre> <p>Legend</p> <ul style="list-style-type: none"> <li>Command: Rectangle</li> <li>Parameter: Parallelogram</li> <li>Display: Pointed rectangle</li> <li>Action: Arrow</li> <li>Mode: Oval</li> <li>Sequential transfer: Oval with arrow</li> </ul>													

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## 10.2.20 OTP-Load (Deh): OTP read command

DEH	OTP-Load												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
OTP-read	0	↑	1	-	1	1	0	1	1	1	1	0	(Deh)
1 <sup>st</sup> Parameter	1	↑	1	-	0	1	1	1	0	1	0	1	(75H)

Description	-Read OTP value After OTP programming, IC will download the OTP value. If you change the VcomH register, you can execute Deh command to re-download OTP.													
Restriction	-If this register not using the register need be reserved.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Ooff, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode Off, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>No</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Ooff, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode Off, Idle Mode On, Sleep Out	Yes	Sleep In	No
Status	Availability													
Normal Mode On, Idle Mode Ooff, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode Off, Idle Mode On, Sleep Out	Yes													
Sleep In	No													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>75h</td> </tr> <tr> <td>S/W Reset</td> <td>75h</td> </tr> <tr> <td>H/W Reset</td> <td>75h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	75h	S/W Reset	75h	H/W Reset	75h				
Status	Default Value													
Power On Sequence	75h													
S/W Reset	75h													
H/W Reset	75h													
Flow Chart	<pre> graph TD     A[MTP_Load (DEH)] --&gt; B[/1st Parameter: 75H/]     </pre> <p>Legend</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>													

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## 10.2.21 OTP-Prog (DFh): OTP Programing command

DFH	OTP-Prog												(Code)
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	
OTP-read	0	↑	1	-	1	1	0	1	1	1	1	0	(DFh)
1 <sup>st</sup> Parameter	1	↑	1	-	0	1	1	1	0	1	0	1	(CAH)
2 <sup>nd</sup> Parameter	1	↑	1	-	0	0	0	0	0	0	0	0	(00H)
3 <sup>rd</sup> Parameter	1	↑	1	-	1	0	1	0	1	0	1	0	(AAH)
4 <sup>rd</sup> Parameter	1	↑	1	-	1	0	1	0	0	1	0	1	(A5H)
5 <sup>rd</sup> Parameter	1	↑	1	-	0	1	0	1	1	0	1	0	(5AH)

Description	- OTP download -Set the VcomH voltage in normal mode/full colors and Idle mode/8 colors. -Set the VcomAC voltage in normal mode/full colors and Idle mode/8 colors.													
Restriction	-If this register not using the register need be reserved. -After adjust the C5H command(VcomH voltage) and C6H command(VcomAC voltage), VPP connect 7.5V.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Ooff, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode Off, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>No</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Ooff, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode Off, Idle Mode On, Sleep Out	Yes	Sleep In	No
Status	Availability													
Normal Mode On, Idle Mode Ooff, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode Off, Idle Mode On, Sleep Out	Yes													
Sleep In	No													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>No change</td> </tr> <tr> <td>S/W Reset</td> <td>No change</td> </tr> <tr> <td>H/W Reset</td> <td>No change</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	No change	S/W Reset	No change	H/W Reset	No change				
Status	Default Value													
Power On Sequence	No change													
S/W Reset	No change													
H/W Reset	No change													
Flow Chart	<div style="display: flex; align-items: center;"> <div style="flex: 1;"> <pre> graph TD     A[MTP_Prog (DFH)] --&gt; B[/1st Parameter: CAH 2nd Parameter: 00H 3rd Parameter: AAH 4th Parameter: A5H 5th Parameter: 5AH/]                     </pre> </div> <div style="flex: 1; border: 1px dashed black; padding: 5px;"> <p>Legend</p> <ul style="list-style-type: none"> <li>Command: [ ]</li> <li>Parameter: / /</li> <li>Display: &lt; &gt;</li> <li>Action: &lt; &gt;</li> <li>Mode: ( )</li> <li>Sequential transfer: ( )</li> </ul> </div> </div>													

## 10.2.22 GMCTRP1 (E0h): Gamma ('+'polarity) Correction Characteristics Setting

E0H	GMCTRP0 (Gamma '+'polarity Correction Characteristics Setting)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GMCTRP1	0	-↑	1	-	1	1	1	0	0	0	0	0	(E0h)
1 <sup>st</sup> Parameter	1	-↑	1	-	MVA_EN	-	-	-	RFP0[3]	RFP0[2]	RFP0[1]	RFP0[0]	
2 <sup>nd</sup> Parameter	1	-↑	1	-	-	-	-	-	PKP0[3]	PKP0[2]	PKP0[1]	PKP0[0]	
3 <sup>rd</sup> Parameter	1	-↑	1	-	-	-	-	PKP1[4]	PKP1[3]	PKP1[2]	PKP1[1]	PKP1[0]	
4 <sup>th</sup> Parameter	1	-↑	1	-	-	-	-	PKP2[4]	PKP2[3]	PKP2[2]	PKP2[1]	PKP2[0]	
5 <sup>th</sup> Parameter	1	-↑	1	-	-	-	-	PKP3[4]	PKP3[3]	PKP3[2]	PKP3[1]	PKP3[0]	
6 <sup>th</sup> Parameter	1	-↑	1	-	-	-	-	PKP4[4]	PKP4[3]	PKP4[2]	PKP4[1]	PKP4[0]	
7 <sup>th</sup> Parameter	1	-↑	1	-	-	-	-	PKP5[4]	PKP5[3]	PKP5[2]	PKP5[1]	PKP5[0]	
8 <sup>th</sup> Parameter	1	-↑	1	-	-	-	-	PKP6[4]	PKP6[3]	PKP6[2]	PKP6[1]	PKP6[0]	
9 <sup>th</sup> Parameter	1	-↑	1	-	-	-	-	PKP7[4]	PKP7[3]	PKP7[2]	PKP7[1]	PKP7[0]	
10 <sup>th</sup> Parameter	1	-↑	1	-	-	-	-	-	PKP8[3]	PKP8[2]	PKP8[1]	PKP8[0]	
11 <sup>th</sup> Parameter	1	-↑	1	-	-	-	-	-	RFP1[3]	RFP1[2]	RFP1[1]	RFP1[0]	
12 <sup>th</sup> Parameter	1	-↑	1	-	-	-	-	-	-	OSP1[2]	OSP1[1]	OSP1[0]	
13 <sup>th</sup> Parameter	1	-↑	1	-	-	-	-	OSP0[4]	OSP0[3]	OSP0[2]	OSP0[1]	OSP0[0]	

Description	Register Group	Negative Polarity	Set-up Contents
	High level adjustment		RFP0[3:0]
Mid level adjustment		PKP0[3:0]	The voltage of grayscale number 3 is selected by the 16 to 1 selector
		PKP1[4:0]	The voltage of grayscale number 6 is selected by the 32 to 1 selector
		PKP2[4:0]	The voltage of grayscale number 11 is selected by the 32 to 1 selector
		PKP3[4:0]	The voltage of grayscale number 20 is selected by the 32 to 1 selector
		PKP4[4:0]	The voltage of grayscale number 31 is selected by the 32 to 1 selector
		PKP5[4:0]	The voltage of grayscale number 43 is selected by the 32 to 1 selector
		PKP6[4:0]	The voltage of grayscale number 52 is selected by the 32 to 1 selector
		PKP7[4:0]	The voltage of grayscale number 57 is selected by the 32 to 1 selector
		PKP8[3:0]	The voltage of grayscale number 60 is selected by the 16 to 1 selector
		RFP1[3:0]	The voltage of grayscale number 1 is selected by the 16 to 1 selector
		OSP1[2:0]	The voltage of grayscale number 62 is selected by the 7 to 1 selector
Low level adjustment		OSP0[4:0]	Variable resistor VRLP
-When MVA_EN=1, The Gamma correction select to MVA type -When MVA_EN=0, The Gamma correction don't select to MVA type			
Restriction	-		
Register Availability	Status		Availability
	Normal Mode On, Idle Mode Off, Sleep Out		Yes
	Normal Mode On, Idle Mode On, Sleep Out		Yes
	Partial Mode On, Idle Mode Off, Sleep Out		Yes
	Partial Mode On, Idle Mode On, Sleep Out		Yes
Sleep In		Yes	

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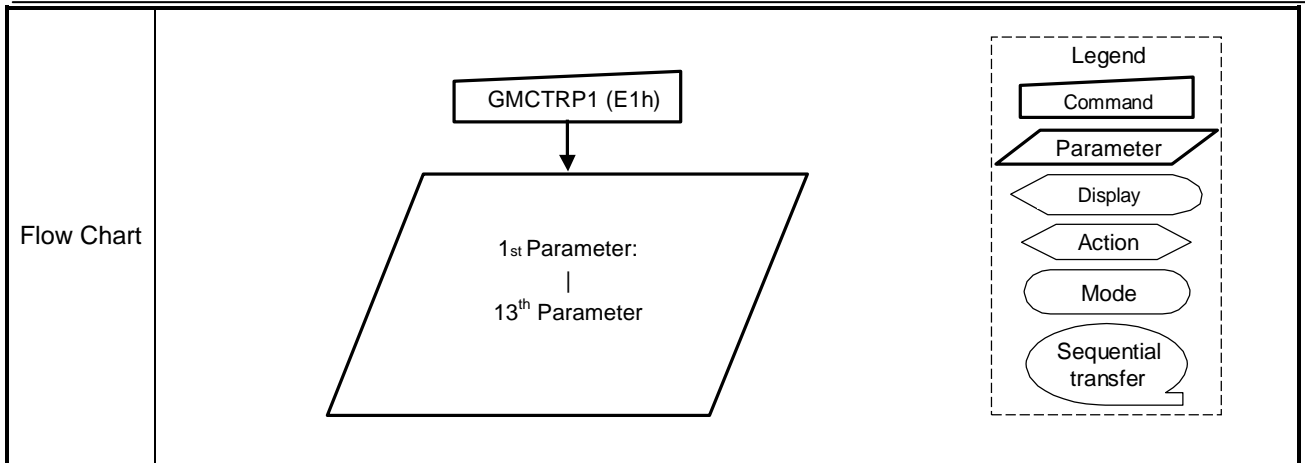
Default	Status	Default Value
	Power On Sequence	Not Fixed
	S/W Reset	Not Fixed
	H/W Reset	Not Fixed
Flow Chart	<pre> graph TD     A[GMCTRP1 (E0h)] --&gt; B[/1st Parameter:   13th Parameter/]     </pre>	
	<p style="text-align: center;">Legend</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>	

## 10.2.23 GMCTR1 (E1h): Gamma ('-' polarity) Correction Characteristics Setting

E1H	GMCTR0 (Gamma '+' polarity Correction Characteristics Setting)												(Code)
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GMCTR1	0	-↑	1	-	1	1	1	0	0	0	0	0	(E1h)
1 <sup>st</sup> Parameter	1	-↑	1	-	-	-	-	-	RFN0[3]	RFN0[2]	RFN0[1]	RFN0[0]	
2 <sup>nd</sup> Parameter	1	-↑	1	-	-	-	-	-	PKN0[3]	PKN0[2]	PKN0[1]	PKN0[0]	
3 <sup>rd</sup> Parameter	1	-↑	1	-	-	-	-	PKN1[4]	PKN1[3]	PKN1[2]	PKN1[1]	PKN1[0]	
4 <sup>th</sup> Parameter	1	-↑	1	-	-	-	-	PKN2[4]	PKN2[3]	PKN2[2]	PKN2[1]	PKN2[0]	
5 <sup>th</sup> Parameter	1	-↑	1	-	-	-	-	PKN3[4]	PKN3[3]	PKN3[2]	PKN3[1]	PKN3[0]	
6 <sup>th</sup> Parameter	1	-↑	1	-	-	-	-	PKN4[4]	PKN4[3]	PKN4[2]	PKN4[1]	PKN4[0]	
7 <sup>th</sup> Parameter	1	-↑	1	-	-	-	-	PKN5[4]	PKN5[3]	PKN5[2]	PKN5[1]	PKN5[0]	
8 <sup>th</sup> Parameter	1	-↑	1	-	-	-	-	PKN6[4]	PKN6[3]	PKN6[2]	PKN6[1]	PKN6[0]	
9 <sup>th</sup> Parameter	1	-↑	1	-	-	-	-	PKN7[4]	PKN7[3]	PKN7[2]	PKN7[1]	PKN7[0]	
10 <sup>th</sup> Parameter	1	-↑	1	-	-	-	-	-	PKN8[3]	PKN8[2]	PKN8[1]	PKN8[0]	
11 <sup>th</sup> Parameter	1	-↑	1	-	-	-	-	-	RFN1[3]	RFN1[2]	RFN1[1]	RFN1[0]	
12 <sup>th</sup> Parameter	1	-↑	1	-	-	-	-	-	-	OSN1[2]	OSN1[1]	OSN1[0]	
13 <sup>th</sup> Parameter	1	-↑	1	-	-	-	-	OSN0[4]	OSN0[3]	OSN0[2]	OSN0[1]	OSN0[0]	

Description	Register Group	Negative Polarity	Set-up Contents
	High level adjustment		RFN0[3:0]
Mid level adjustment		PKN0[3:0]	The voltage of grayscale number 3 is selected by the 16to 1 selector
		PKN1[4:0]	The voltage of grayscale number 6 is selected by the 32 to 1 selector
		PKP2[4:0]	The voltage of grayscale number 11 is selected by the 32 to 1 selector
		PKN3[4:0]	The voltage of grayscale number 20 is selected by the 32 to 1 selector
		PKN4[4:0]	The voltage of grayscale number 31 is selected by the 32 to 1 selector
		PKN5[4:0]	The voltage of grayscale number 43 is selected by the 32 to 1 selector
		PKN6[4:0]	The voltage of grayscale number 52 is selected by the 32 to 1 selector
		PKN7[4:0]	The voltage of grayscale number 57 is selected by the 64 to 1 selector
		PKN8[3:0]	The voltage of grayscale number 60 is selected by the 16 to 1 selector
		RFN1[3:0]	The voltage of grayscale number 1 is selected by the 16 to 1 selector
		OSN1[2:0]	The voltage of grayscale number 62 is selected by the 7 to 1 selector
Low level adjustment		OSN0[4:0]	Variable resistor VRLN
Restriction	-		
Register Availability	Status		Availability
	Normal Mode On, Idle Mode Off, Sleep Out		Yes
	Normal Mode On, Idle Mode On, Sleep Out		Yes
	Partial Mode On, Idle Mode Off, Sleep Out		Yes
	Partial Mode On, Idle Mode On, Sleep Out		Yes
Sleep In		Yes	
Default	Status		Default Value
	Power On Sequence		Not Fixed
	S/W Reset		Not Fixed
	H/W Reset		Not Fixed

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## 10.2.24 Vcom\_multi\_mode (FBh):

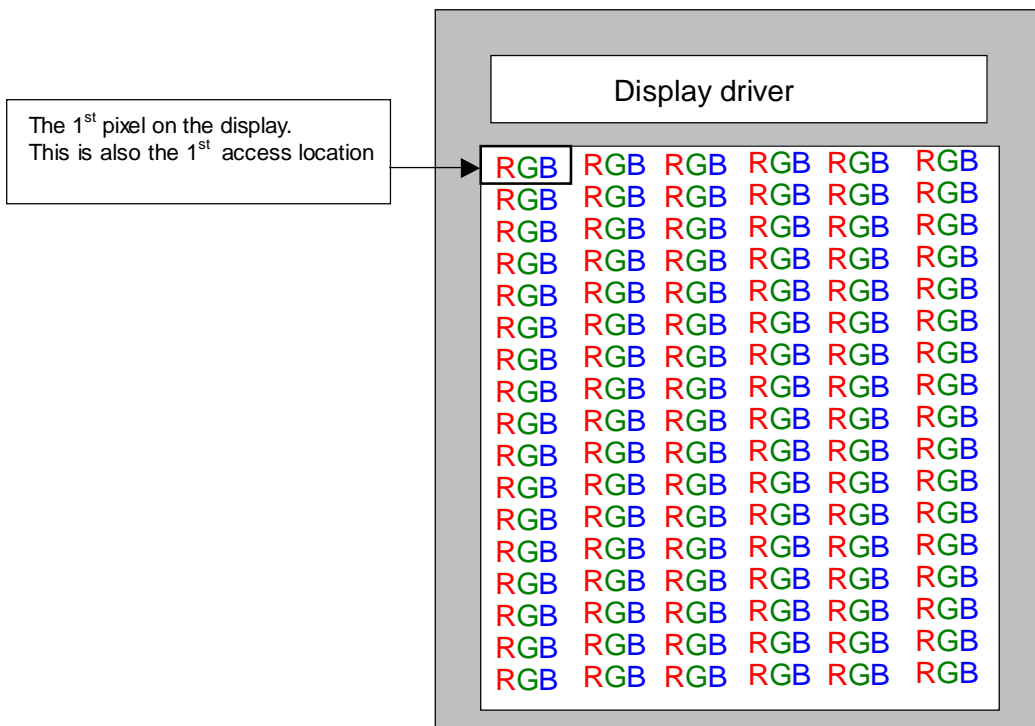
DEH		OTP-Load											
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Vcom_multi_mode	0	↑	1	-	1	1	1	1	1	0	1	1	(FBh)
1 <sup>st</sup> Parameter	1	↑	1	-	0	1	Vcom_multi_mode	1	1	1	1	1	

Description	-Vcom_multi_mode For power saving, please set the Vcom_multi_mode=1.												
Restriction	-If this register not using the register need be reserved.												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Ooff, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode Off, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>No</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Ooff, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode Off, Idle Mode On, Sleep Out	Yes	Sleep In	No
Status	Availability												
Normal Mode On, Idle Mode Ooff, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode Off, Idle Mode On, Sleep Out	Yes												
Sleep In	No												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>7Fh</td> </tr> <tr> <td>S/W Reset</td> <td>7Fh</td> </tr> <tr> <td>H/W Reset</td> <td>7Fh</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	7Fh	S/W Reset	7Fh	H/W Reset	7Fh				
Status	Default Value												
Power On Sequence	7Fh												
S/W Reset	7Fh												
H/W Reset	7Fh												
Flow Chart	<p>The flow chart shows a rectangular box labeled 'MTP_Load (FBH)' with an arrow pointing down to a parallelogram box labeled '1st Parameter: 7FH'. To the right is a legend box containing: Command (rectangle), Parameter (parallelogram), Display (oval), Action (diamond), Mode (rounded rectangle), and Sequential transfer (oval with a tail).</p>												



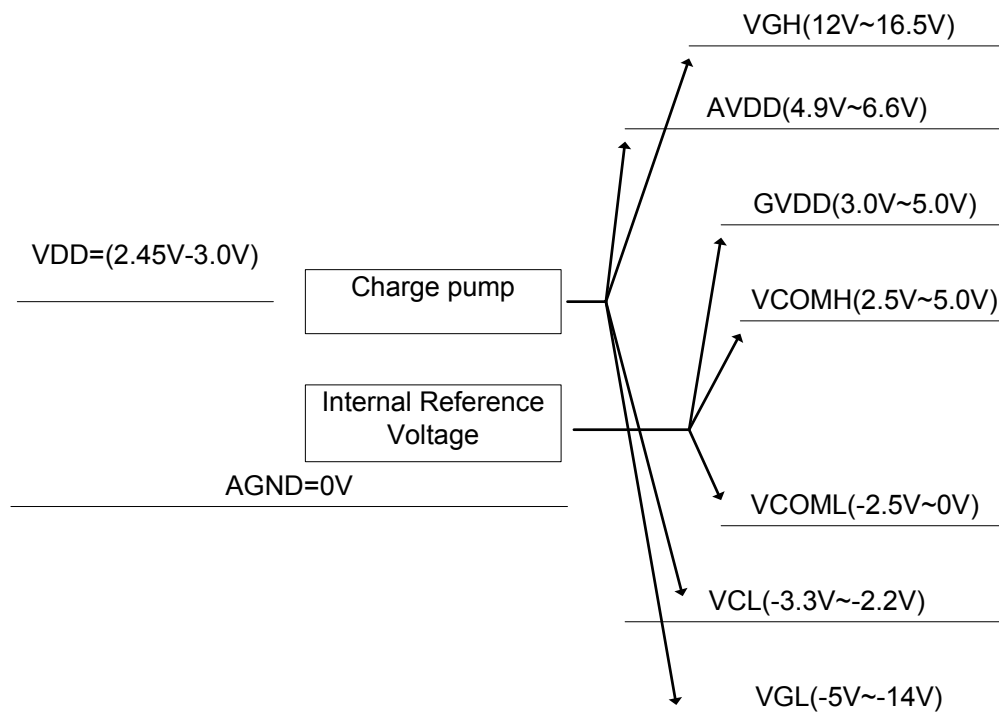
## 11. Display Module Default Position

The default position of the display is always as follow, when MADCTL's (36h) parameter is 00h.



## 12. Power structure

### 12.1. Driver IC Operating voltages Specification



#### Remark

1. AVDD supply to all power source (exclude VGH, VGL)
2. Source output range: 0.1V ~ AVDD-0.1V
3. Linear Range: 0.2V ~ AVDD-0.2V  
(For all output voltage, but exclude VGH, VGL)
4. Above operating voltages is min range.

12.2 Power Booster Circuit

12.2.1 VCI1 generate from VDD regulator

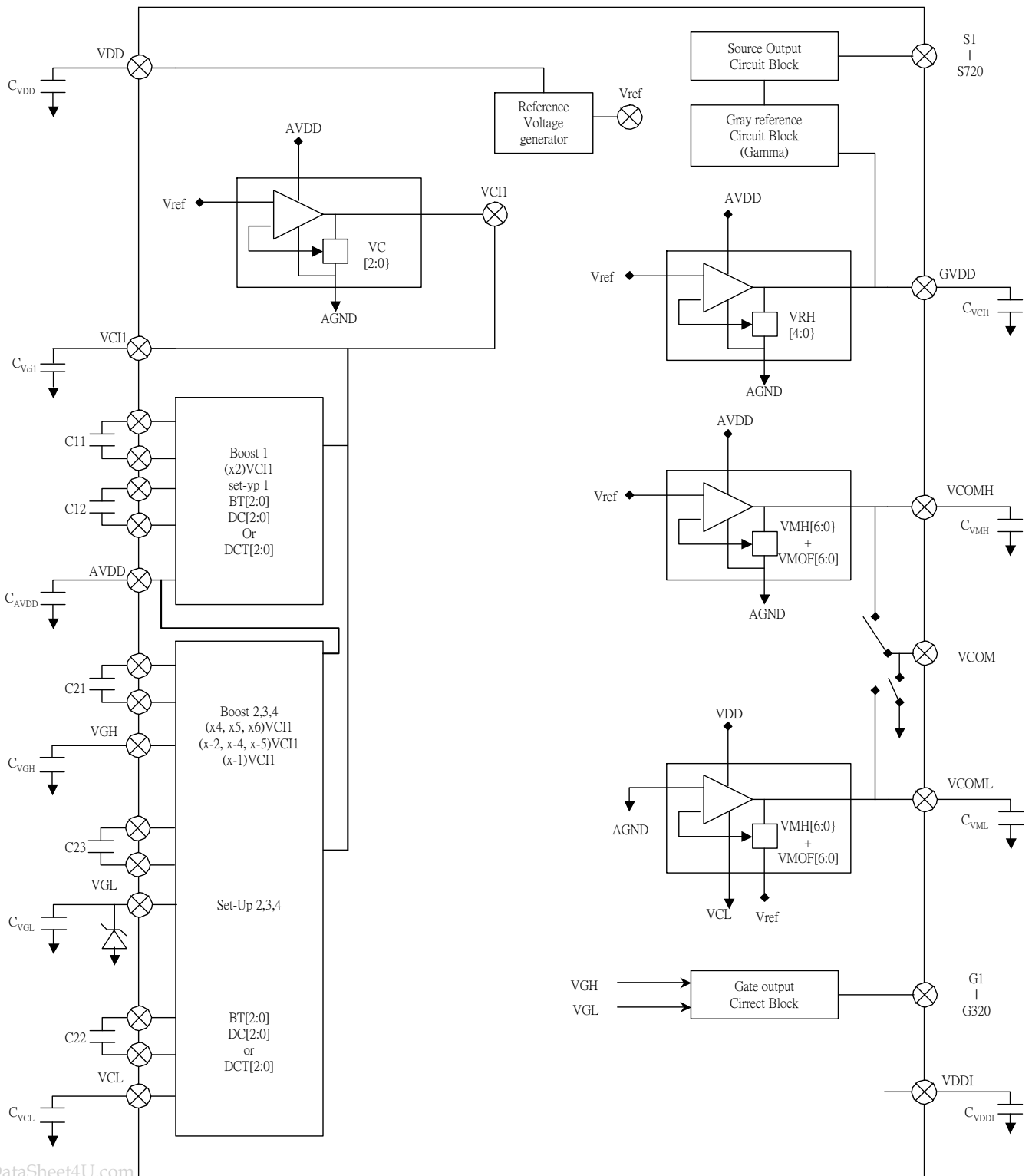


Fig. 12.2.1 Power Booster Structure (1)

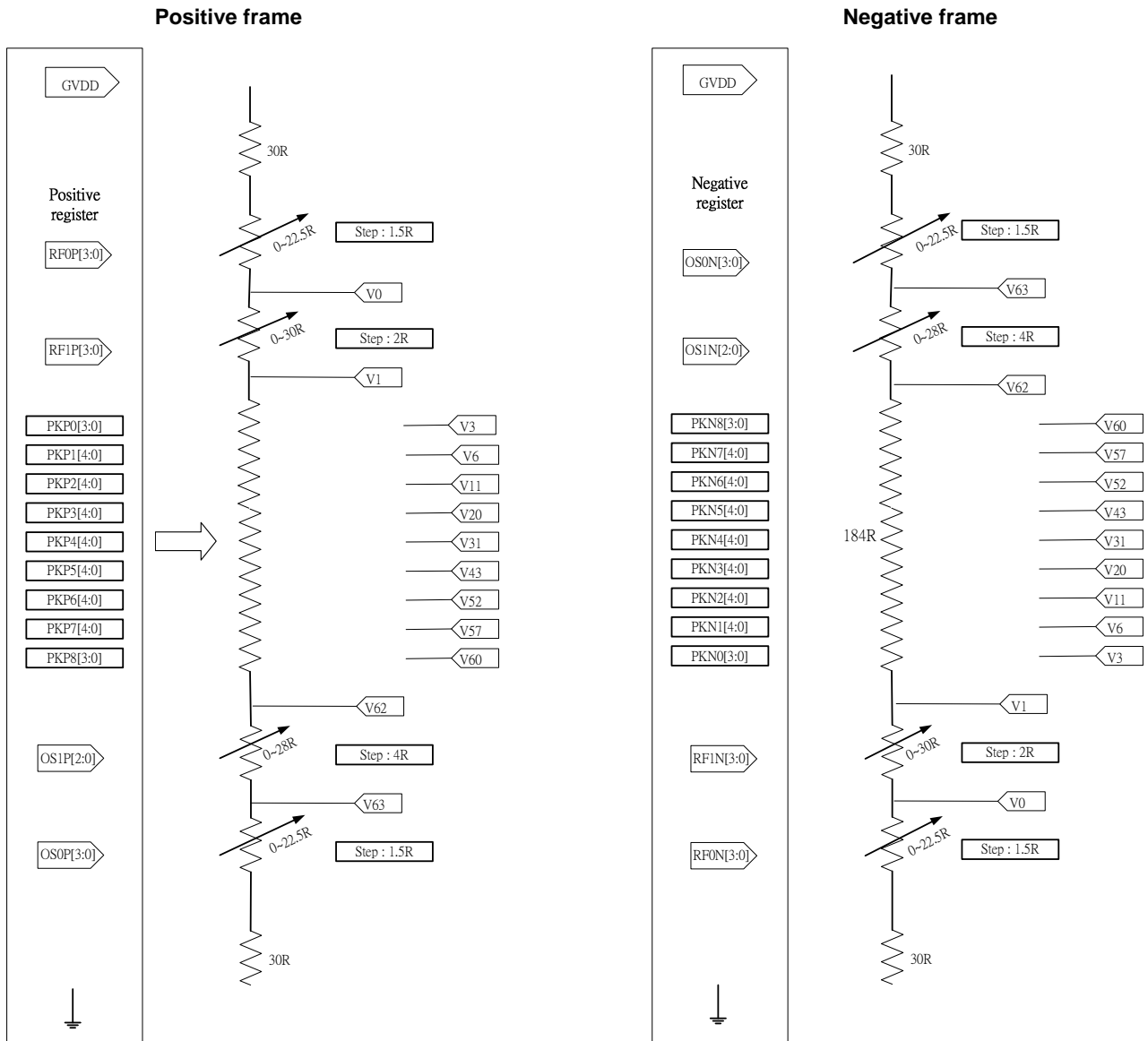
## 12.2.2 EXTERNAL COMPONENTS CONNECTION

Pad Name	Connection	Rated (Min) Voltage	Typical capacitance value
VDDI	VDDI (Logic Power)	10.0V	1.0 uF
VDD	VDD (Analog Power)	10.0V	1.0 uF
VCC	Connect to Capacitor (Max 3V): VCC -----  ----- GND	10.0V	1.0 uF
AGND	Analog ground (Connect to GND)		
DGND	Digital ground (Connect to GND)		
C23P, C23N	Connect to Capacitor: C23P -----  -----C23N	25.0V	1.0 uF
C22P, C22N	Connect to Capacitor: C22P -----  -----C22N	25.0V	1.0 uF
C21P, C22N	Connect to Capacitor: C21P -----  -----C21N	10.0V	1.0 uF
C12P, C12N	Connect to Capacitor: C12P -----  -----C12N	10.0V	1.0 uF
C11P, C11N	Connect to Capacitor: C11P -----  -----C11N	10.0V	1.0 uF
AVDD	Connect to Capacitor: AVDD -----  ----- GND	10.0V	1.0 uF
VC11	Connect to Capacitor: AVDD -----  ----- GND	10.0V	1.0 uF
VGH	Connect to Capacitor: VGH -----  ----- GND	25.0V	1.0 uF
VGL	Connect to Capacitor: VGL -----  ----- GND	25.0V	1.0 uF
VCL	Connect to Capacitor: VCL -----  ----- GND	10.0V	1.0 uF
VREF	Connect to Capacitor: VREF -----  ----- GND	10.0V	1.0 uF
GVDD	Connect to Capacitor: GVDD -----  ----- GND	10.0V	1.0 uF
VCOMH	Connect to Capacitor: VCOMH-----  ----- GND	10.0V	1.0 uF
VCOML	Connect to Capacitor: VCOML -----  ----- GND	10.0V	1.0 uF
VC1S	Connect to Capacitor: VC1S -----  ----- GND	10V	1.0uF
VGL	Connect to Schottky diode: VGL -----. ----- GND	30V	Schottky diode

13. Gamma structure

13.1 STRUCTURE OF GRAYSCALE AMPLIFIER

The structure of grayscale amplifier is shown as below. 13 voltage levels (VIN0-VIN12) between GVDD and VGS are determined by the high/ mid/ low level adjustment registers. Each mid-adjustment level is split into 64 levels again by the internal ladder resistor network. As a result, grayscale amplifier generates 64 voltage levels ranging from V0 to V63 and outputs one of 64 levels.



## 13.2 Gamma Voltage Formula (Positive/ Negative Polarity)

Grayscale	Voltage Formula(Positive)	Voltage Formula(Negative)
0	VIN0	VINN 0
1	VINP1	VINN 1
2	$V1-(V1-V3)*(16/30)$	$V1-(V1-V3)*(17/30)$
3	VIN2	VINN 2
4	$V3-(V3-V6)*(21/60)$	$V3-(V3-V6)*(12/30)$
5	$V3-(V3-V6)*(41/60)$	$V3-(V3-V6)*(22/30)$
6	VINP3	VINN 3
7	$V6-(V6-V11)*(13/60)$	$V6-(V6-V11)*(9/40)$
8	$V6-(V6-V11)*(26/60)$	$V6-(V6-V11)*(17/40)$
9	$V6-(V6-V11)*(38/60)$	$V6-(V6-V11)*(25/40)$
10	$V6-(V6-V11)*(49/60)$	$V6-(V6-V11)*(33/40)$
11	VINP4	VINN 4
12	$V11-(V11-V20)*(8/60)$	$V11-(V11-V20)*(4/36)$
13	$V11-(V11-V20)*(16/60)$	$V11-(V11-V20)*(8/36)$
14	$V11-(V11-V20)*(24/60)$	$V11-(V11-V20)*(12/36)$
15	$V11-(V11-V20)*(31/60)$	$V11-(V11-V20)*(16/36)$
16	$V11-(V11-V20)*(38/60)$	$V11-(V11-V20)*(20/36)$
17	$V11-(V11-V20)*(44/60)$	$V11-(V11-V20)*(24/36)$
18	$V11-(V11-V20)*(50/60)$	$V11-(V11-V20)*(28/36)$
19	$V11-(V11-V20)*(55/60)$	$V11-(V11-V20)*(32/36)$
20	VINP5	VINN 5
21	$V20-(V20-V31)*(6/60)$	$V20-(V20-V32)*(5/60)$
22	$V20-(V20-V31)*(12/60)$	$V20-(V20-V32)*(10/60)$
23	$V20-(V20-V31)*(18/60)$	$V20-(V20-V32)*(15/60)$
24	$V20-(V20-V31)*(24/60)$	$V20-(V20-V32)*(20/60)$
25	$V20-(V20-V31)*(30/60)$	$V20-(V20-V32)*(25/60)$
26	$V20-(V20-V31)*(35/60)$	$V20-(V20-V32)*(30/60)$
27	$V20-(V20-V31)*(40/60)$	$V20-(V20-V32)*(35/60)$
28	$V20-(V20-V31)*(45/60)$	$V20-(V20-V32)*(40/60)$
29	$V20-(V20-V31)*(50/60)$	$V20-(V20-V32)*(45/60)$
30	$V20-(V20-V31)*(55/60)$	$V20-(V20-V32)*(50/60)$
31	VINP6	VINN 6
32	$V31-(V31-V43)*(5/60)$	$V32-(V32-V43)*(5/60)$
33	$V31-(V31-V43)*(10/60)$	$V32-(V32-V43)*(10/60)$
34	$V31-(V31-V43)*(15/60)$	$V32-(V32-V43)*(15/60)$
35	$V31-(V31-V43)*(20/60)$	$V32-(V32-V43)*(20/60)$
36	$V31-(V31-V43)*(25/60)$	$V32-(V32-V43)*(25/60)$
37	$V31-(V31-V43)*(30/60)$	$V32-(V32-V43)*(30/60)$
38	$V31-(V31-V43)*(35/60)$	$V32-(V32-V43)*(36/60)$
39	$V31-(V31-V43)*(40/60)$	$V32-(V32-V43)*(42/60)$
40	$V31-(V31-V43)*(45/60)$	$V32-(V32-V43)*(48/60)$
41	$V31-(V31-V43)*(55/60)$	$V31-(V31-V43)*(48/60)$
42	$V31-(V31-V43)*(60/60)$	$V31-(V31-V43)*(54/60)$
43	VINP7	VINN 7
44	$V43-(V43-V52)*(2/18)$	$V43-(V43-V52)*(5/60)$
45	$V43-(V43-V52)*(4/18)$	$V43-(V43-V52)*(10/60)$
46	$V43-(V43-V52)*(6/18)$	$V43-(V43-V52)*(16/60)$
47	$V43-(V43-V52)*(8/18)$	$V43-(V43-V52)*(22/60)$
48	$V43-(V43-V52)*(10/18)$	$V43-(V43-V52)*(29/60)$
49	$V43-(V43-V52)*(12/18)$	$V43-(V43-V52)*(36/60)$
50	$V43-(V43-V52)*(14/18)$	$V43-(V43-V52)*(44/60)$
51	$V43-(V43-V52)*(16/18)$	$V43-(V43-V52)*(52/60)$
52	VINP8	VINN 8
53	$V52-(V52-V57)*(7/40)$	$V52-(V52-V57)*(11/60)$
54	$V52-(V52-V57)*(15/40)$	$V52-(V52-V57)*(22/60)$

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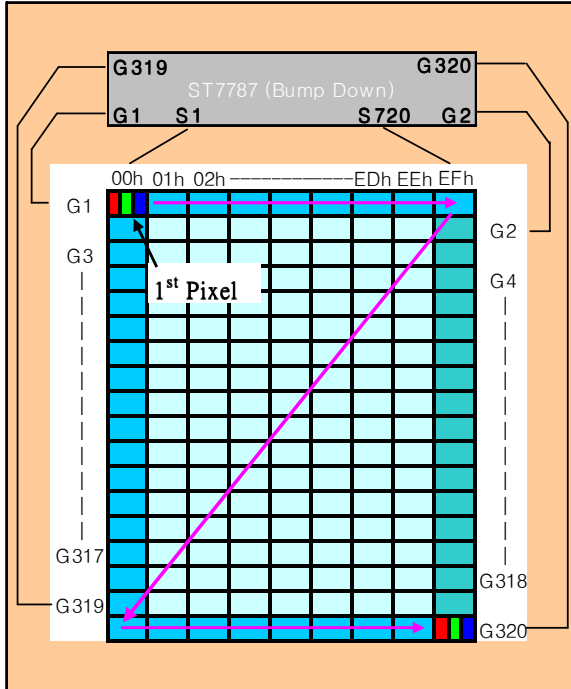
55	V52-(V52-V57)*(23/40)	V52-(V52-V57)*(34/60)
56	V52-(V52-V57)*(31/40)	V52-(V52-V57)*(47/60)
57	VINP9	VINN 9
58	V57-(V57-V60)*(8/30)	V57-(V57-V60)*(19/60)
59	V57-(V57-V60)*(18/30)	V57-(V57-V60)*(39/60)
60	VINP10	VINN 10
61	V60-(V60-V62)*(13/30)	V60-(V60-V62)*(14/30)
62	VINP11	VINN 11
63	VINP12	VINN12

## 14. Example Connection with Panel direction and Different Resolution

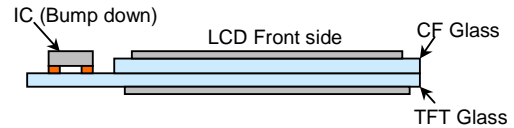
### 14.1 Application of connection with panel direction

Case 1: (This is default case)

- 1<sup>st</sup> Pixel is at *Left Top* of the panel
- RGB filter order = **RGB**

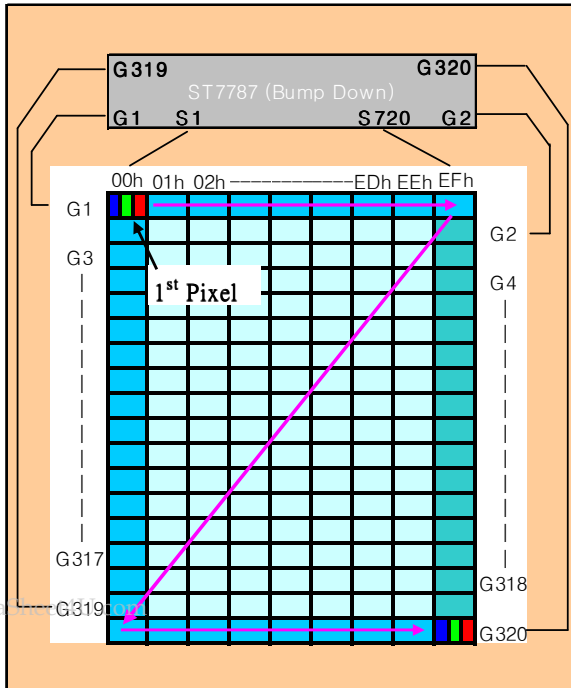


- Direction default setting (H/W)
  - SMX = '0'
  - SMY = '0'
  - SRGB = '0'
  - S1 = Filter **R**
  - S2 = Filter **G**
  - S3 = Filter **B**
- Display direction control (S/W)
  - X-Mirror control by MX
  - Y-Mirror control by MY
  - XY-Exchange control by MV



Case 2:

- 1<sup>st</sup> Pixel is at *Left Top* of the panel
- RGB filter order = **BGR**



- Direction default setting (H/W)
  - SMX = '0'
  - SMY = '0'
  - SRGB = '1'
  - S1 = Filter **B**
  - S2 = Filter **G**
  - S3 = Filter **R**
- Display direction control (S/W)
  - X-Mirror control by MX
  - Y-Mirror control by MY
  - XY-Exchange control by MV

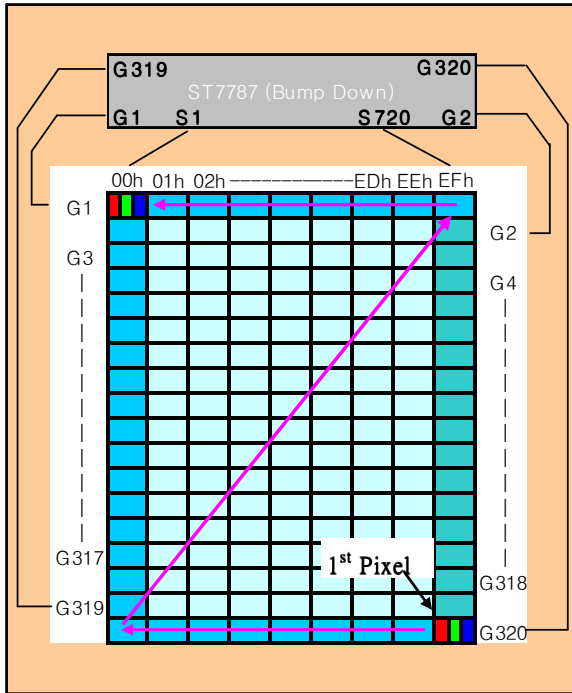




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Case 3:

- 1<sup>st</sup> Pixel is at *Right Bottom* of the panel
- RGB filter order = **RGB**



- Direction default setting (H/W)

SMX = '1'

SMY = '1'

SRGB = '0'

S1 = Filter **R**

S2 = Filter **G**

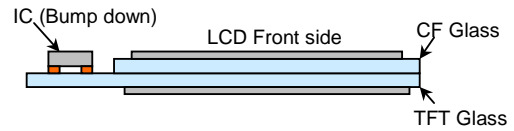
S3 = Filter **B**

- Display direction control (S/W)

- X-Mirror control by MX

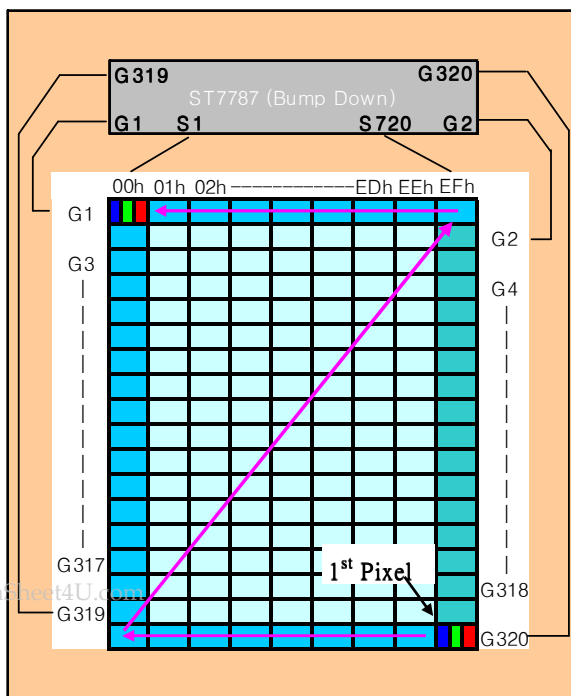
- Y-Mirror control by MY

- XY-Exchange control by MV



Case 4:

- 1<sup>st</sup> Pixel is at *Right Bottom* of the panel
- RGB filter order = **BGR**



- Direction default setting (H/W)

SMX = '1'

SMY = '1'

SRGB = '1'

S1 = Filter **B**

S2 = Filter **G**

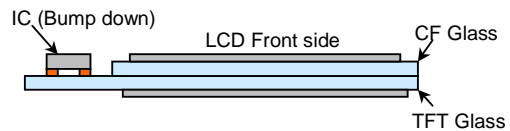
S3 = Filter **R**

- Display direction control (S/W)

- X-Mirror control by MX

- Y-Mirror control by MY

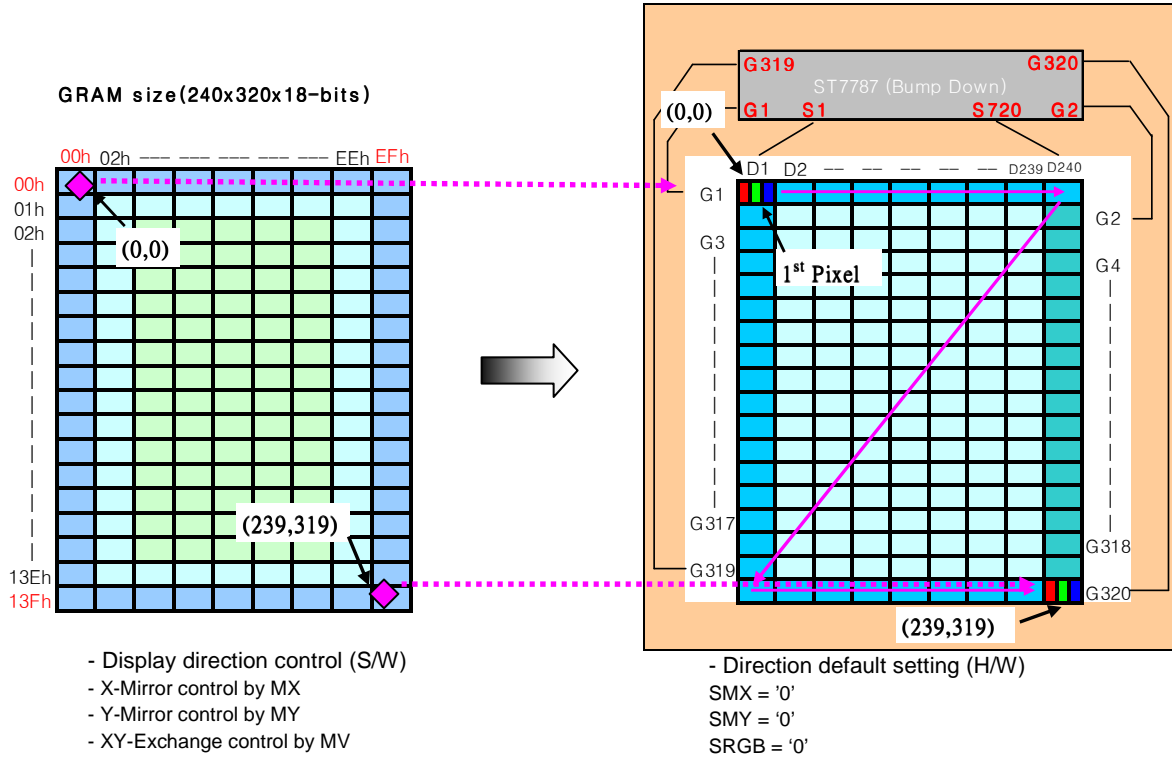
- XY-Exchange control by MV



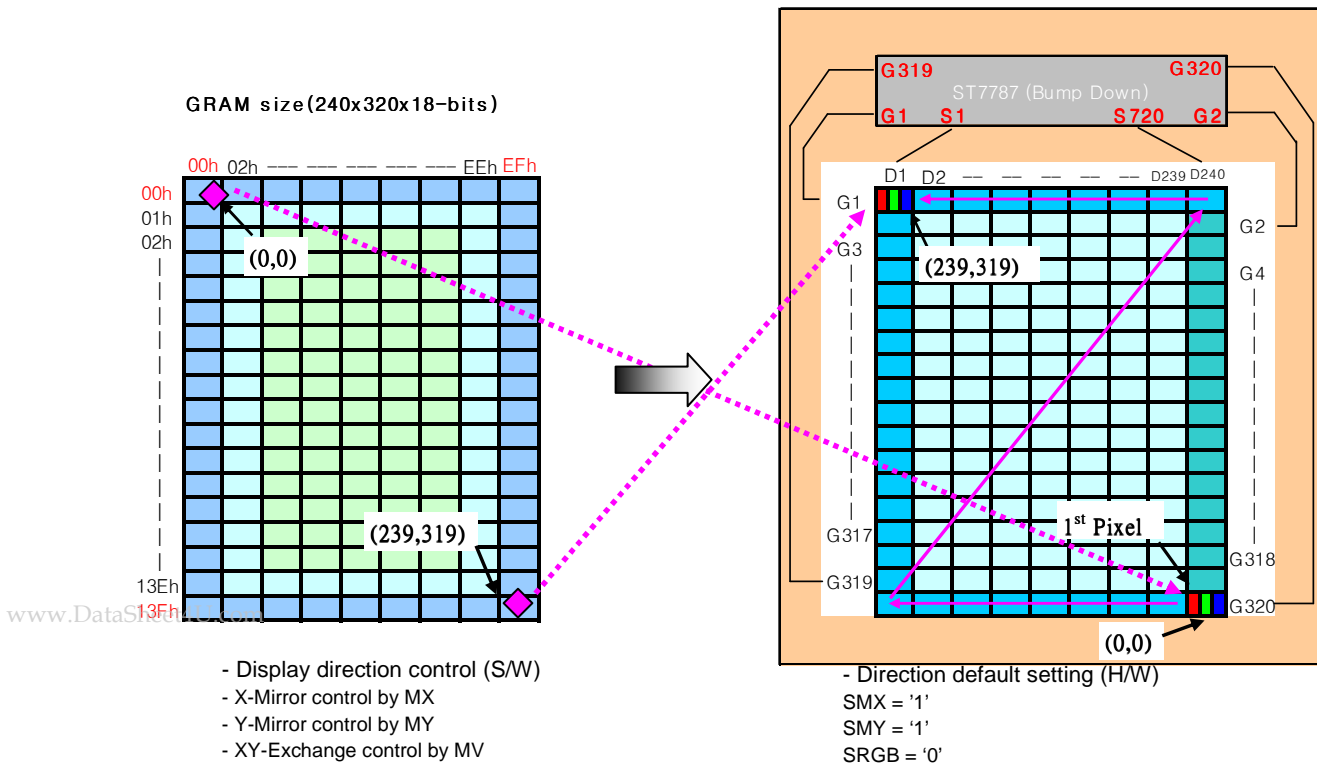
## 14.2 Application of connection with Different resolution

RAM size=240 x 320 x 18-bits (Used)  
 Display size = 240 RGB x 320

1). Example for SMX=SMY='0'



2). Example for SMX=SMY='1'



## 14.3 MicroProcessor Interface applications

### 14.3.1 8080-Series MCU + SPI Interface (RCM = '00', P68='0', IM2='1')

#### 14.3.1.1 8080-Series MCU Interface for 8-bits data bus (IM1, IM0="00")

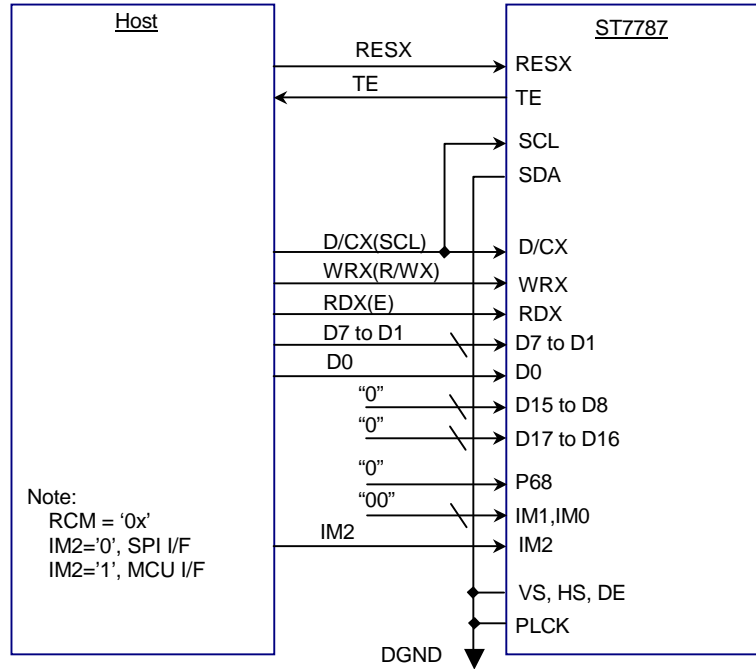


Fig. 14.3.1.1 8080-Series MCU Interface for 8-bits data bus

#### 14.3.1.2 8080-Series MCU Interface for 16-bits data bus (IM1, IM0="01")

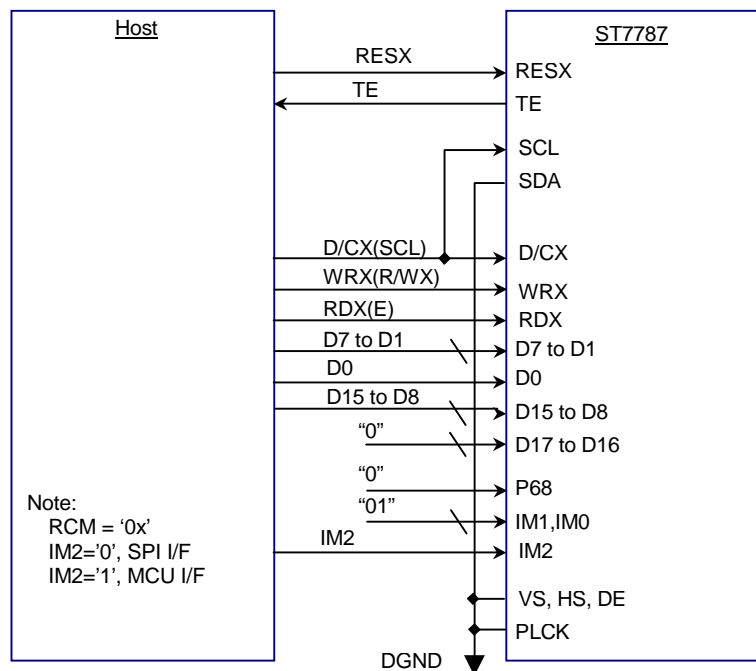


Fig. 14.3.1.2 8080-Series MCU Interface for 16-bits data bus

## 14.3.1.3 8080-Series MCU Interface for 9-bits data bus (IM1, IM0="10")

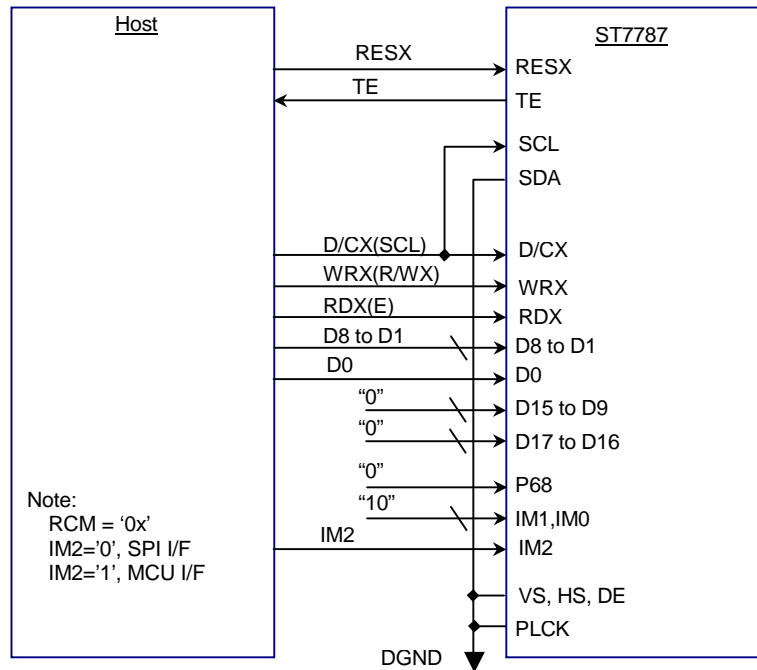


Fig. 14.3.1.3 8080-Series MCU Interface for 9-bits data bus

## 14.3.1.4 8080-Series MCU Interface for 18-bits data bus (IM1, IM0="11")

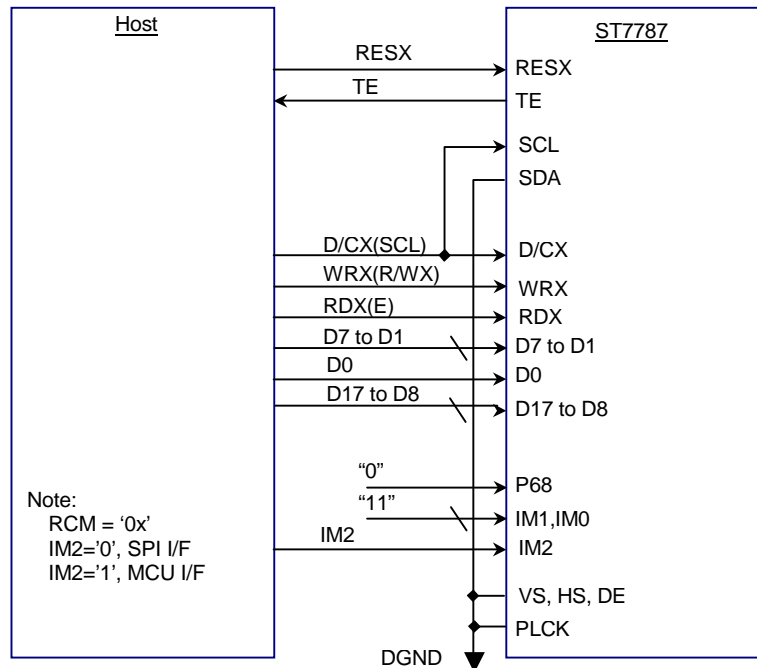


Fig. 14.3.1.4 8080-Series MCU Interface for 18-bits data bus

## 14.3.2 6800-Series MCU + SPI Interface (RCM = '00', P68='1', IM2='1')

### 14.3.2.1 6800-Series MCU Interface for 8-bits data bus (IM1, IM0="00")

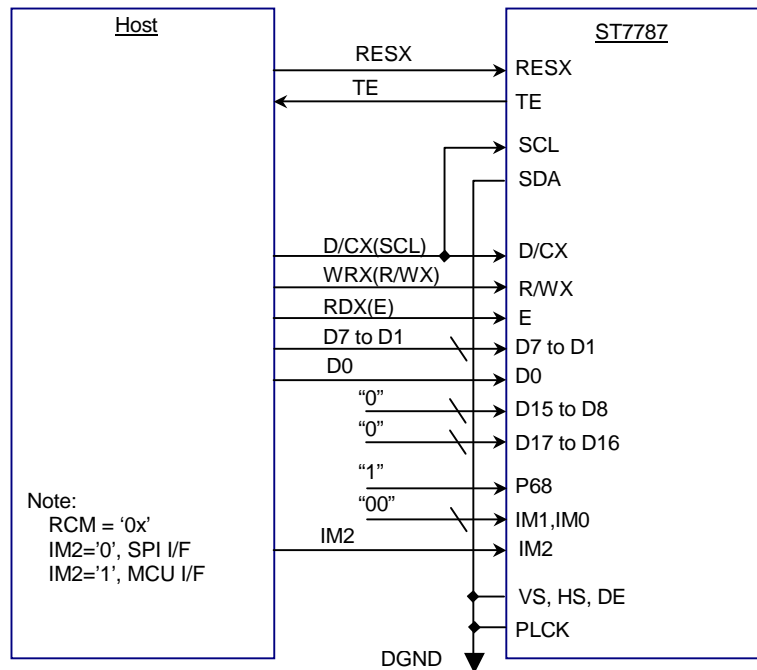


Fig. 14.3.2.1 6800-Series MCU Interface for 8-bits data bus

### 14.3.2.2 6800-Series MCU Interface for 16-bits data bus (IM1, IM0="01")

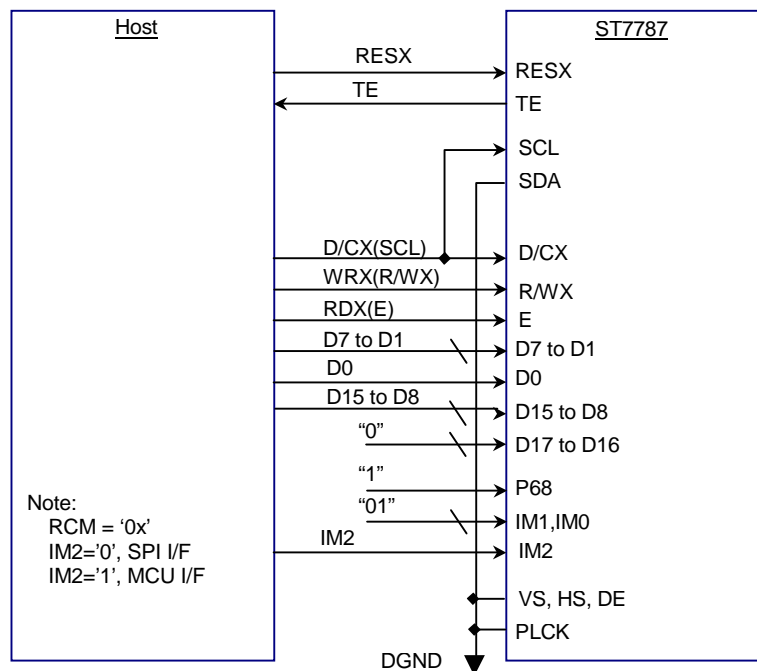


Fig. 14.3.2.2 6800-Series MCU Interface for 16-bits data bus

## 14.3.2.3 6800-Series MCU Interface for 9-bits data bus (IM1, IM0="10")

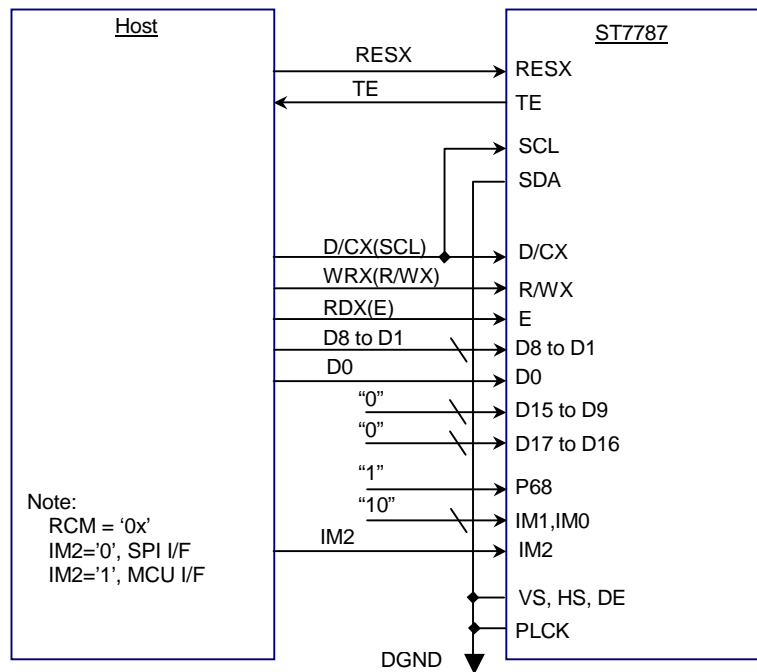


Fig. 14.3.2.3 6800-Series MCU Interface for 9-bits data bus

## 14.3.2.4 6800-Series MCU Interface for 18-bits data bus (IM1, IM0="11")

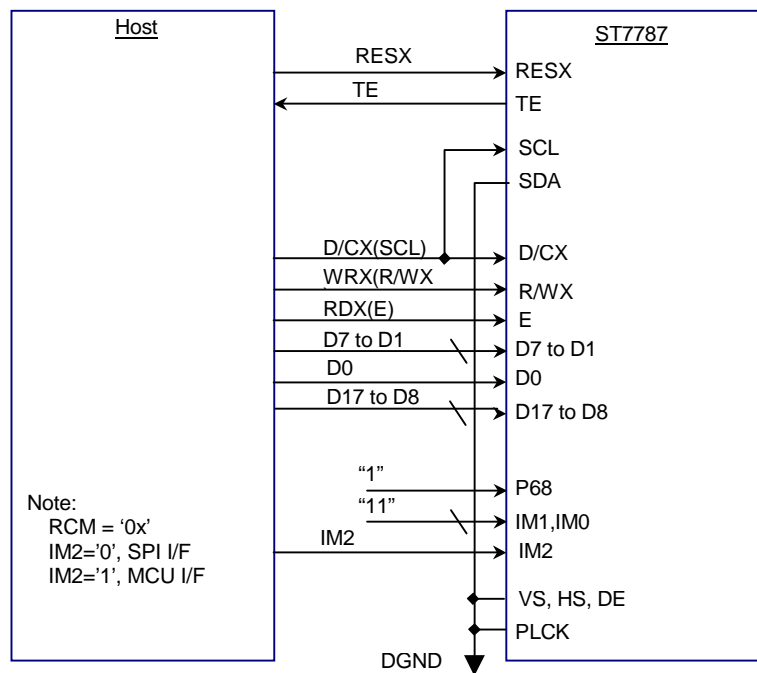


Fig. 14.3.2.4 6800-Series MCU Interface for 18-bits data bus

## 14.3.3 RGB Interface (RCM = '1')

### 14.3.3.1 RGBInterface for 6-bits Data Width

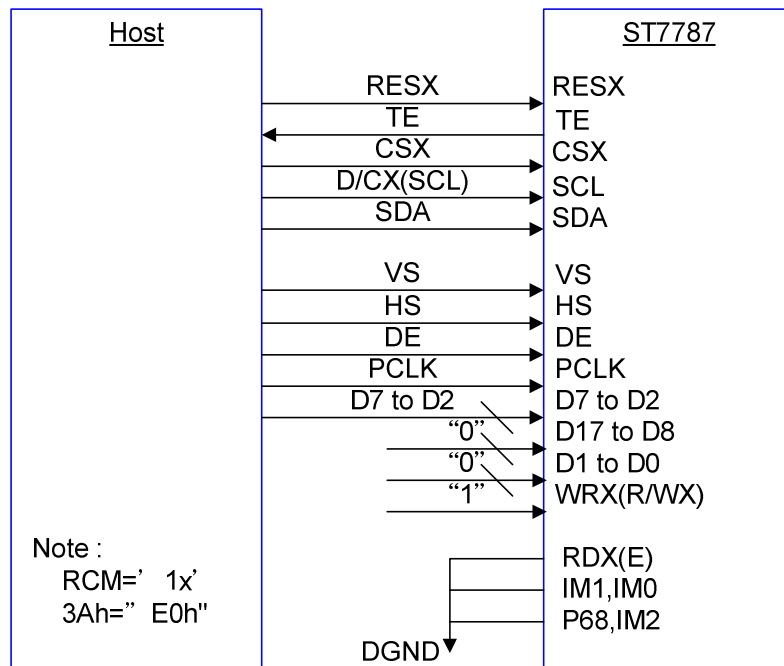


Fig. 14.3.3.1 RGB Interface for 6-bits data width

### 14.3.3.2 RGBInterface for 16-bits Data Width

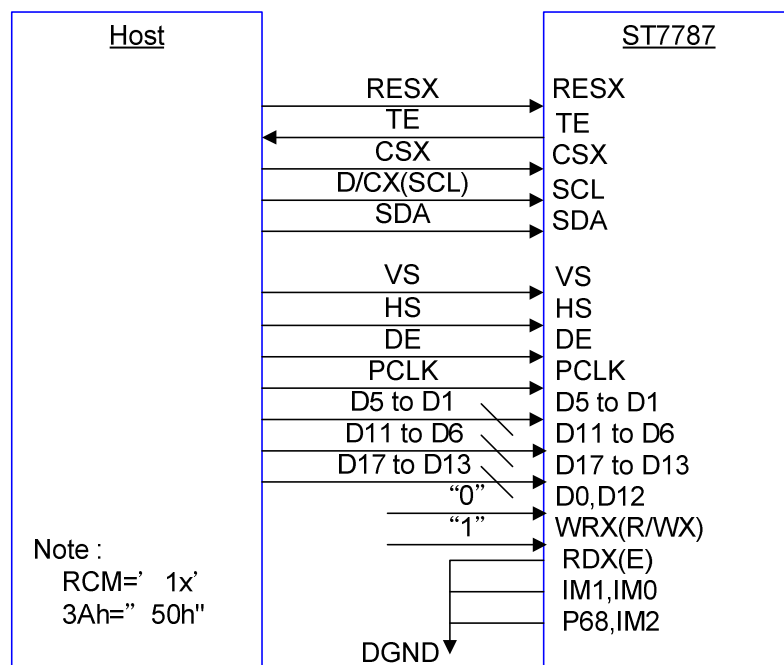


Fig. 14.3.3.2 RGB Interface for 16-bits data width

## 14.3.3.3 RGB Interface for 18-bits Data Width

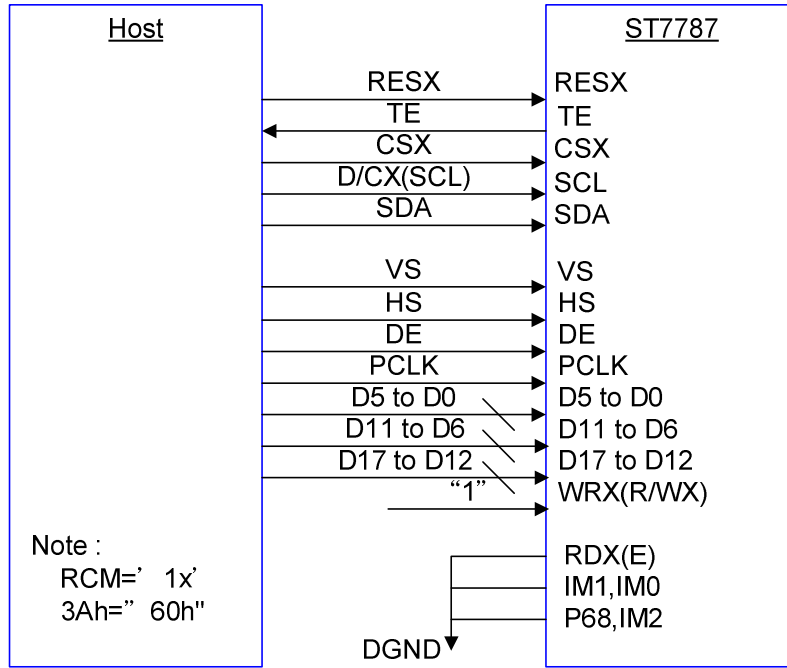


Fig. 14.3.3.3 RGB Interface for 18-bits data width



# ST7787

## 11. Revise History

ST7787 Serial Specification Revision History			
Version	Date	Description	Page
0.5B	2007/02/06	Add timing value	
1.0	2007/3/2	Modify Power on and off sequence	
1.0	2007/3/2	Add FBH command	
1.1	2007/06/14	Modify the operation temperature range Modify the command 3Ah Modify gamma structure	P2 P157 P206
1.2	2007/9/6	Removed the description of 4-line	P22
1.3	2007/9/11	Modify 3SPI Interface description Modify "RAMHD" typo to "RAMRD" Modify VIPF[3:0] typo	P34 P142 P157
1.4	2007/10/2	Modify the description of power on/off sequence(9.15) Remove table 9.17.3.1 reset input timing(9.17.3) Modify the figure of reset timing (9.17.3) Modify the waiting time of SWReset to 120ms(10.1.2) Modify the waiting time of SLPout to 120ms(10.1.12)	P91 P96 P96 P111 P124
1.5	2007/11/26	Modify the description of command E0h & E1h Modify power consumption IDDI (Unit) Modify operation temperature range Modify RGB Interface application circuit	P196, P198 P29 P27~P30, P32~33 P215~216
1.6	2008/3/6	Modify Power On Sequence on RGB Mode 2 from VDDI→VDD to VDD→VDDI(9.9.6.4) Modify Power OFF Sequence on RGB Mode 2 from VDDI→VDD to VDD→VDDI(9.9.6.5)	P73 P74
1.7	2009/4/18	Modify WRX level on RGB mode from VDDI or DGND to VDDI only Modify SCL signal on SPI mode during proch area from clock to Hi level	P22,P215,P216  P40,P44