# SGS-THOMSON MICROELECTRONICS

ST9036

## 16K ROM HCMOS MCU
WITH RAM AND A/D CONVERTER

- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes

- Minimum instruction cycle time : 500ns (12MHz internal)

- Internal Memory :
  ROM   16Kbytes
  RAM   256 bytes
  224 general purpose registers available as RAM, accumulators or index registers (register file)

- 80-pin PQFP package for ST9036Q

- 68-lead PLCC package for ST9036C

- 56-pin shrink DIP package for ST9036B

- DMA controller, Interrupt handler and Serial Peripheral Interface as standard features

- Up to 56 fully programmable I/O pins

- Up to 8 external plus 1 non-maskable interrupts

- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer

- Two 16 bit Multifunction Timers, each with an 8 bit prescaler and 13 operating modes

- 8 channel 8 bit Analog to Digital Converter, with Analog Watchdogs and external references

- Serial Communications Interface with asynchronous and synchronous capability

- Rich Instruction Set and 14 Addressing modes

- Division-by-Zero trap generation

- Versatile development tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators

- Real Time Operating System

- Windowed and One Time Programmable EPROM parts available for prototyping and pre-production development phases

- Pin to pin compatible with ST9030 and ST9040
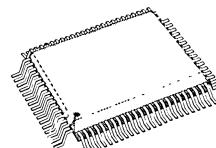
PQFP80
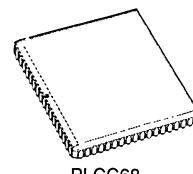
PLCC68
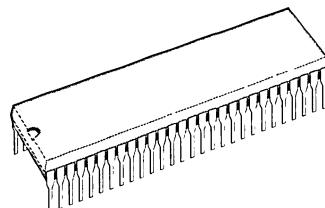
PSDIP56

(Ordering Information at the end of the Datasheet)

ST9036

Figure 1. 80 Pin PQFP Package

VR0A1649
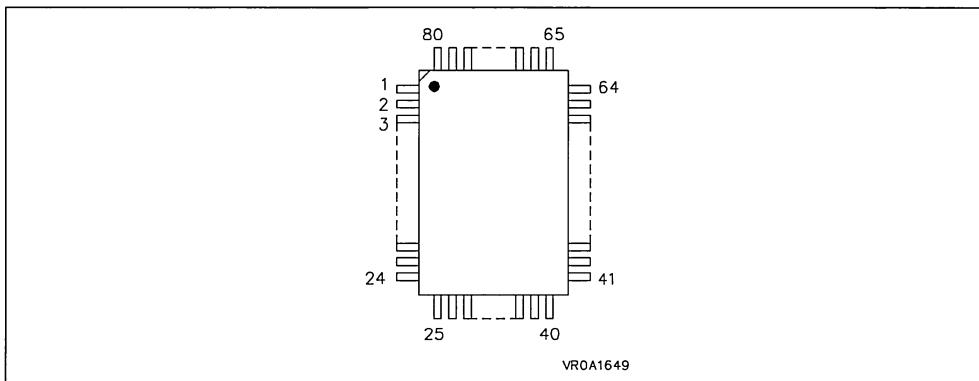
Table 1. ST9036Q Pin Description

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	AV$_{SS}$	25	P34/T1INA	64	P20/NMI	80	AV$_{DD}$
2	AV$_{SS}$	26	P33/T0OUTB	63	NC	79	NC
3	NC	27	P32/T0INB	62	V$_{SS}$	78	P47/AIN7
4	P44/AIN4	28	P31/T0OUTA	61	P70/SIN	77	P46/AIN6
5	P57	29	P30/P/$\overline{D}$/T0INA	60	P71/SOUT	76	P45/AIN5
6	P56	30	A15	59	P72/INT4/TXCLK /CLKOUT	75	P43/AIN3
7	P55	31	A14			74	P42/AIN2
8	P54	32	NC	58	P73/INT5 /RXCLK/ADTRG	73	P41/AIN1
9	INT7	33	A13			72	P40/AIN0
10	INT0	34	A12	57	P74/P/$\overline{D}$/INT6	71	P27/RRDY5
11	P53	35	A11	56	P75/$\overline{WAIT}$	70	P26/INT3 /$\overline{RDSTB5}$/P/$\overline{D}$
12	NC	36	A10	55	P76/WDOUT /$\overline{BUSREQ}$		
13	P52	37	A9			69	P25/WRRDY5
14	P51	38	A8	54	P77/WDIN /$\overline{BUSACK}$	68	P24/INT1 /$\overline{WRSTB5}$
15	P50	39	P00/A0/D0				
16	OSCOUT	40	P01/A1/D1	53	R/$\overline{W}$	67	P23/SDO
17	V$_{SS}$			52	NC	66	P22/INT2/SCK
18	V$_{SS}$			51	$\overline{DS}$	65	P21/SDI/P/$\overline{D}$
19	NC			50	$\overline{AS}$		
20	OSCIN			49	NC		
21	$\overline{RESET}$			48	V$_{DD}$		
22	P37/T1OUTB			47	V$_{DD}$		
23	P36/T1INB			46	P07/A7/D7		
24	P35/T1OUTA			45	P06/A6/D6		
				44	P05/A5/D5		
				43	P04/A4/D4		
				42	P03/A3/D3		
				41	P02/A2/D2		

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Figure 2. 68 Pin PLCC Package
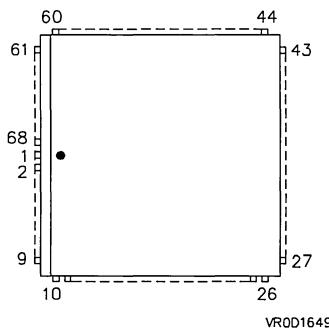
Table 2. ST9036C Pin Description

Pin	Name	Pin	Name	Pin	Name	Pin	Name
61	P44/AIN4	10	P35/T1OUTA	43	P70/SIN	60	AV$_{SS}$
62	P57	11	P34/T1INA	42	P71/SOUT	59	AV$_{DD}$
63	P56	12	P33/T0OUTB	41	P72/CLKOUT /TXCLK/INT4	58	P47/AIN7
64	P55	13	P32/T0INB			57	P46/AIN6
65	P54	14	P31/T0OUTA	40	P73/ADTRG /RXCLK/INT5	56	P45/AIN5
66	INT7	15	P30/P/$\overline{D}$/T0INA			55	P43/AIN3
67	INT0	16	P17/A15	39	P74/P/$\overline{D}$/INT6	54	P42/AIN2
68	P53	17	P16/A14	38	$\overline{P75/WAIT}$	53	P41/AIN1
● 1	P52	18	P15/A13	37	P76/WDOUT /BUSREQ	52	P40/AIN0
2	P51	19	P14/A12			51	P27/RRDY5
3	P50	20	P13/A11	36	P77/WDIN /BUSACK	50	P26/INT3 /RDSTB5/P/$\overline{D}$
4	OSCOUT	21	P12/A10	35	R/$\overline{W}$		
5	V$_{SS}$	22	P11/A9	34	$\overline{DS}$	49	P25/WRRDY5
6	OSCIN	23	P10/A8	33	$\overline{AS}$	48	P24/INT1 /WRSTB5
7	$\overline{RESET}$	24	P00/A0/D0	32	V$_{DD}$		
8	P37/T1OUTB	25	P01/A1/D1	31	P07/A7/D7	47	P23/SDO
9	P36/T1INB	26	P02/A2/D2	30	P06/A6/D6	46	P22/INT2/SCK
				29	P05/A5/D5	45	P21/SDI/P/$\overline{D}$
				28	P04/A4/D4	44	P20/NMI
				27	P03/A3/D3		

Figure 1b. 56 Pin Shrink DIP Pinout
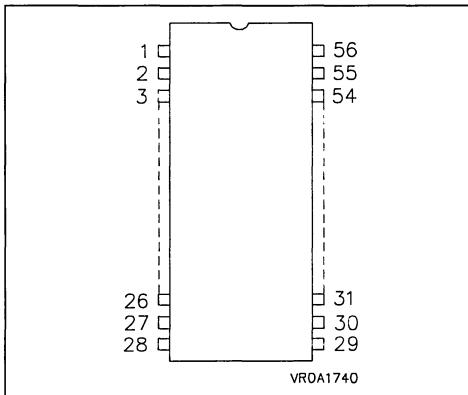
Table 3. ST9036B Pin Description

Pin	Pin name	Pin	Pin name
1	P42/AIN2	56	P41/AIN1
2	P43/AIN3	55	P40/AIN0
3	P45/AIN5	54	P23/SDO
4	P46/AIN6	53	P22/INT2/SCK
5	P47/AIN7	52	P21/SDI/P.$\overline{\text{D}}$
6	AVDD	51	P20/NMI
7	AVSS	50	P70/SIN
8	P44/AIN4	49	P71/SOUT
9	P57	48	P72/CLKOUT TXCLK/INT4
10	P56		
11	P55	47	P73/ADTRG RXCLK/INT5
12	P54		
13	P53	46	P76/$\overline{\text{WDOUT}}$/$\overline{\text{BUSREQ}}$
14	P52	45	P77/WDIN/BUSACK
15	OSCOUT	44	R/$\overline{\text{W}}$
16	Vss	43	DS
17	OSCIN	42	$\overline{\text{AS}}$
18	$\overline{\text{RESET}}$	41	VDD
19	P37/T1OUTB	40	Vss
20	P36/T1INB	39	P07/A7/D7
21	NC	38	P06/A6/D6
22	P35/T1OUTA	37	P05/A5/D5
23	P34/T1INA	36	P04/A4/D4
24	P33/T0OUTB	35	P03/A3/D3
25	P32/T0INB	34	P02/A2/D2
26	P31/T0OUTA	33	P01/A1/D1
27	P30/P/D/T0INA	32	P00/A0/D0
28	P13/A11	31	P10/A8
		30	P11/A9
		29	P12/A10

1.1 GENERAL DESCRIPTION

The ST9036 is a ROM member of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The ST9036 EPROM peripheral and functional actions are fully compatible throughout the ST903x/4x family. This datasheet will thus provide only information specific to this ROM device.

THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST9030 ROM-BASED DEVICE FOR FURTHER DETAILS.

The nucleus of the ST9036 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-bus, I^2C-bus and IM-bus Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set. The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST9036 with up to 56 I/O lines dedicated to digital Input/Output. These lines are grouped into up to seven 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, an address/data bus for interfacing external memory, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.

Three basic memory spaces are available to support this wide range of configurations: Program Memory (internal and external), Data Memory (internal and external) and the Register File, which includes the control and status registers of the on-chip peripherals.

Two 16 bit MultiFunction Timers, each with an 8 bit Prescaler and 13 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer. In addition there is an 8 channel Analog to Digital Converter with integral sample and hold, fast 11µs conversion time and 8 bit resolution. An Analog Watchdog feature is included for two input channels.

Completing the device is a full duplex Serial Communications Interface with an integral 110 to 375,000 baud rate generator, asynchronous and 1.5Mbyte/s synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

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1.2 PIN DESCRIPTION

AS. *Address Strobe (output, active low, 3-state).* Address Strobe is pulsed low once at the beginning of each memory cycle. The rising edge of $\overline{AS}$ indicates that address, Read/Write (R/$\overline{W}$), and Data Memory signals are valid for program or data memory transfers. Under program control, $\overline{AS}$ can be placed in a high-impedance state along with Port 0 and Port 1, Data Strobe ($\overline{DS}$) and R/$\overline{W}$.

DS. *Data Strobe (output, active low, 3-state).* Data Strobe provides the timing for data movement to or from Port 0 for each memory transfer. During a write cycle, data out is valid at the leading edge of $\overline{DS}$. During a read cycle, Data In must be valid prior to the trailing edge of $\overline{DS}$. When the ST9036 accesses on-chip memory, $\overline{DS}$ is held high during the whole memory cycle. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and R/$\overline{W}$.

R/$\overline{W}$. *Read/Write (output, 3-state).* Read/Write determines the direction of data transfer for external memory transactions. R/$\overline{W}$ is low when writing to external program or data memory, and high for all other transactions. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and $\overline{DS}$.

RESET. *Reset (input, active low).* The ST9 is initialised by the Reset signal. With the deactivation of $\overline{RESET}$, program execution begins from the Program memory location pointed to by the vector contained in program memory locations 00h and 01h.

INT0, INT7. External interrupts (input, active on rising or falling edge). External interrupt inputs 0 and 7 respectively. INT0 channel may also be used for the timer watchdog interrupt.

OSCIN, OSCOUT. *Oscillator (input and output).* These pins connect a parallel-resonant crystal (24MHz maximum), or an external source to the on-chip clock oscillator and buffer. OSCIN is the input of the oscillator inverter and internal clock generator; OSCOUT is the output of the oscillator inverter.

AV$_{DD}$. Analog V$_{DD}$ of the Analog to Digital Converter.

AV$_{SS}$. Analog V$_{SS}$ of the Analog to Digital Converter. *Must be tied to V$_{SS}$.*

V$_{DD}$. Main Power Supply Voltage (5V $\pm$ 10%)

V$_{SS}$. Digital Circuit Ground.

P0.0-P0.7, P1.0-P1.7, P2.0-P2.7 P3.0-P3.7, P4.0-P4.7, P5.0-P5.7, P7.0-P7.7 *I/O Port Lines (Input/Output, TTL or CMOS compatible).* 56 lines grouped into I/O ports of 8 bits, bit programmable under program control as general purpose I/O or as alternate functions.

1.2.1 I/O Port Alternate Functions

Each pin of the I/O ports of the ST9036 may assume software programmable Alternative Functions as shown in the Pin Configuration Drawings. Table 1-4 shows the Functions allocated to each I/O Port pins and a summary of packages for which they are available.

Figure 3. ST9036 Block Diagram

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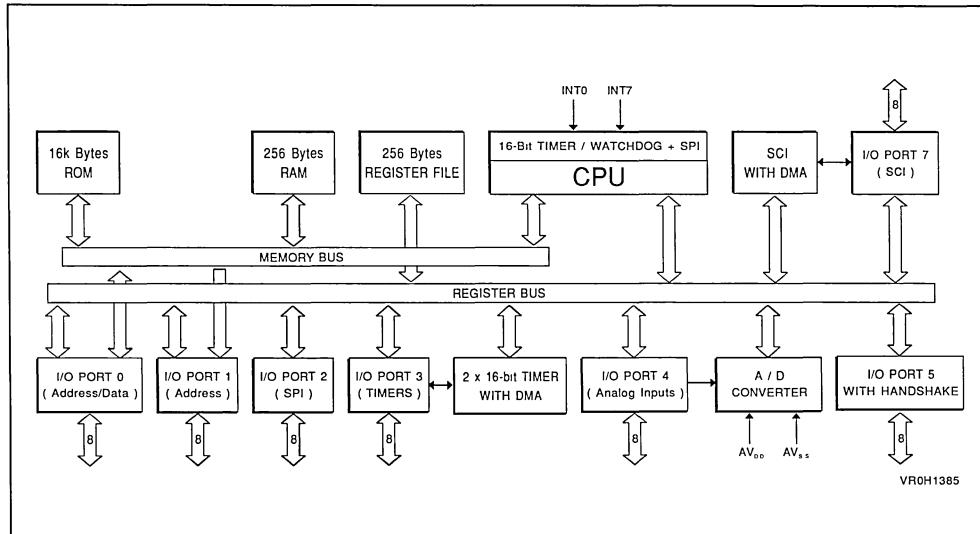
PIN DESCRIPTION (Continued)

Table 4. ST9036 I/O Port Alternate Function Summary

I/O PORT	Name	Function	Alternate Function	Pin Assignment		
Port. bit				PLCC	PQFP	PSDIP
P0.0	A0/D0	I/O	Address/Data bit 0 mux	24	39	32
P0.1	A1/D1	I/O	Address/Data bit 1 mux	25	40	33
P0.2	A2/D2	I/O	Address/Data bit 2 mux	26	41	34
P0.3	A3/D3	I/O	Address/Data bit 3 mux	27	42	35
P0.4	A4/D4	I/O	Address/Data bit 4 mux	28	43	36
P0.5	A5/D5	I/O	Address/Data bit 5 mux	29	44	37
P0.6	A6/D6	I/O	Address/Data bit 6 mux	30	45	38
P0.7	A7/D7	I/O	Address/Data bit 7 mux	31	46	39
P1.0	A8	O	Address bit 8	23	38	31
P1.1	A9	O	Address bit 9	22	37	30
P1.2	A10	O	Address bit 10	21	36	29
P1.3	A11	O	Address bit 11	20	35	28
P1.4	A12	O	Address bit 12	19	34	
P1.5	A13	O	Address bit 13	18	33	
P1.6	A14	O	Address bit 14	17	31	
P1.7	A15	O	Address bit 15	16	30	
P2.0	NMI	I	Non-Maskable Interrupt	44	64	51
P2.0	ROMless	I	ROMless Select (Mask option)	44	64	51
P2.1	P/$\overline{D}$	O	Program/Data Space Select	45	65	
P2.1	SDI	I	SPI Serial Data Out	45	65	52
P2.2	INT2	I	External Interrupt 2	46	66	53
P2.2	SCK	O	SPI Serial Clock	46	66	53
P2.3	SDO	O	SPI Serial Data In	47	67	54
P2.4	INT1	I	External Interrupt 1	48	68	
P2.4	$\overline{WRSTB5}$	I	Handshake Write Strobe P5	48	68	
P2.5	WRRDY5	O	Handshake Write Ready P5	49	69	
P2.6	INT3	I	External Interrupt 3	50	70	
P2.6	$\overline{RDSTB5}$	I	Handshake Read Strobe P5	50	70	
P2.6	P/$\overline{D}$	O	Program/Data Space Select	50	70	
P2.7	RDRDY5	O	Handshake Read Ready P5	51	71	
P3.0	T0INA	I	MF Timer 0 Input A	15	29	27
P3.0	P/$\overline{D}$	O	Program/Data Space Select	15	29	27
P3.1	T0OUTA	O	MF Timer 0 Output A	14	28	26
P3.2	T0INB	I	MF Timer 0 Input B	13	27	25
P3.3	T0OUTB	O	MF Timer 0 Output B	12	26	24
P3.4	T1INA	I	MF Timer 1 Input A	11	25	23

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PIN DESCRIPTION (Continued)

Table 4. ST9036 I/O Port Alternate Function Summary(Continued)

I/O PORT	Name	Function	Alternate Function	Pin Assignment		
Port. bit				**PLCC**	**PQFP**	**PSDIP**
P3.5	T1OUTA	O	MF Timer 1 Output A	10	24	22
P3.6	T1INB	I	MF Timer 1 Input B	9	23	20
P3.7	T1OUTB	O	MF Timer 1 Output B	8	22	19
P4.0	AIN0	I	A/D Analog Input 0	52	72	55
P4.1	AIN1	I	A/D Analog Input 1	53	73	56
P4.2	AIN2	I	A/D Analog Input 2	54	74	1
P4.3	AIN3	I	A/D Analog Input 3	55	75	2
P4.4	AIN4	I	A/D Analog Input 4	61	4	8
P4.5	AIN5	I	A/D Analog Input 5	56	76	3
P4.6	AIN6	I	A/D Analog Input 6	57	77	4
P4.7	AIN7	I	A/D Analog Input 7	58	78	5
P5.0		I/O	I/O Handshake Port 5	3	15	
P5.1		I/O	I/O Handshake Port 5	2	14	
P5.2		I/O	I/O Handshake Port 5	1	13	14
P5.3		I/O	I/O Handshake Port 5	68	11	13
P5.4		I/O	I/O Handshake Port 5	65	8	12
P5.5		I/O	I/O Handshake Port 5	64	7	11
P5.6		I/O	I/O Handshake Port 5	63	6	10
P5.7		I/O	I/O Handshake Port 5	62	5	9
P7.0	SIN	I	SCI Serial Input	43	61	50
P7.1	SOUT	O	SCI Serial Output	42	60	49
P7.1	ROMless	I	ROMless Select (Mask option)	42	60	49
P7.2	INT4	I	External Interrupt 4	41	59	48
P7.2	TXCLK	I	SCI Transmit Clock Input	41	59	48
P7.2	CLKOUT	O	SCI Byte Sync Clock Output	41	59	48
P7.3	INT5	I	External Interrupt 5	40	58	47
P7.3	RXCLK	I	SCI Receive Clock Input	40	58	47
P7.3	ADTRG	I	A/D Conversion Trigger	40	58	47
P7.4	INT6	I	External Interrupt 6	39	57	
P7.4	P/$\overline{\text{D}}$	O	Program/Data Space Select	39	57	
P7.5	$\overline{\text{WAIT}}$	I	External Wait Input	38	56	
P7.6	WDOUT	O	T/WD Output	37	55	46
P7.6	$\overline{\text{BUSREQ}}$	I	External Bus Request	37	55	46
P7.7	WDIN	I	T/WD Input	36	54	45
P7.7	$\overline{\text{BUSACK}}$	O	External Bus Acknowledge	36	54	45

1.3 MEMORY

1.3.1 INTRODUCTION

The memory of the ST9 is divided into two spaces:

- Data memory with up to 64K (65536) bytes
- Program memory with up to 64K (65536) bytes

Thus, there is a total of 128K bytes of addressable memory space.

The 16K bytes of on-chip ROM memory of the ST9036 are selected at memory addresses 0 through 3FFFh (hexadecimal) in the PROGRAM space. The data space includes 256 bytes of on-chip RAM at address 200h through 2FFh.

Off-chip memory, addressed using the multiplexed address and data buses (Ports 0 and 1) may be divided into the Program and Data spaces by the external decoding of the Program/Data select pin (P/$\overline{D}$) available as an Alternate function output, allowing the full 127.5K byte memory

The first 512 bytes of the data space are not accessible.

Figure 1-4. Memory Map

ROM

PROGRAM SPACE

65535 — FFFF

16384 — 1FFF

0000 — 0000

INTERNAL   EXTERNAL

RAM

NOT ACCESS'BLE

DATA SPACE

65535 — FFFF

768 — 02FF

512 — 01FF

0000 — 0000

INTERNAL   EXTERNAL

VR01996G

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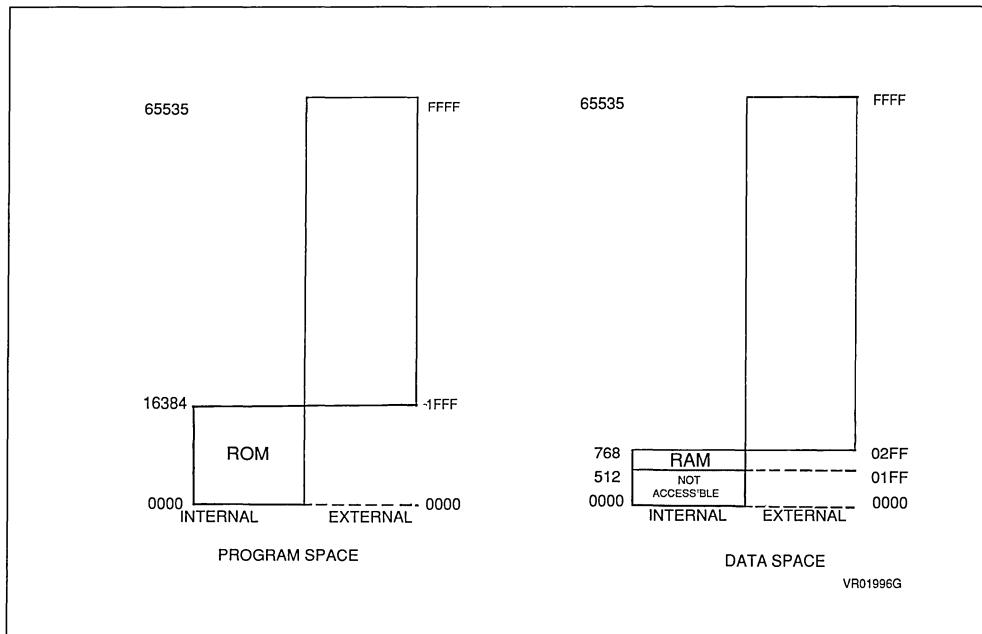
AC ELECTRICAL CHARACTERISTICS
(V_{DD} = 5V ± 10% T_A = – 40 °C to + 85°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
I_{DD}	Run Mode Current no CPUCLK prescale, Clock divide by 2	24MHz, Note 1			50	mA
I_{DP2}	Run Mode Current Prescale by 2 Clock divide by 2	24MHz, Note 1			30	mA
I_{WFI}	WFI Mode Current no CPUCLK prescale, Clock divide by 2	24MHz, Note 1			20	mA
I_{HALT}	HALT Mode Current	24MHz, Note 1			100	μA

Note 1: All I/O Ports are configured in Bidirectional Weak Pull-up Mode with no DC load, External Clock pin (OSCIN) is driven by square wave external clock. No peripheral working.

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68-Pin Plastic Leadless Chip Carrier

VR001534
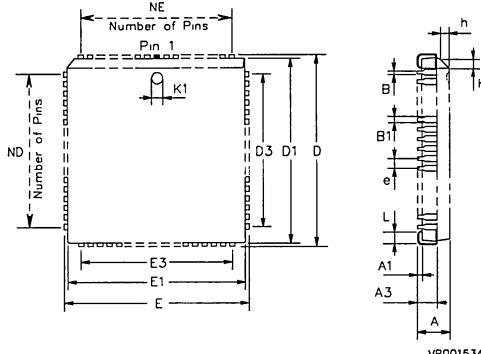
Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	4.20		5 08	0.165		0 200
A1	0.51			0.020		
A3	2 29		3 30	0.090		0 130
B	-	-	-	-	-	-
B1	-	-	-	-	-	-
D	25 02		25 27	0 985		0 995
D1	24 13		24 33	0.950		0 958
D3		20 32			0 800	
E	25 02		25 27	0.985		0 995
E1	24 13		24 33	0 950		0 958
E3		20 32			0 800	
K1	-	-	-	-	-	-
h						
e		1 27			0.050	
Number of Pins						
N	64					
ND	16					
NE	16					

56-Pin Plastic Shrink Dual-In-line Package, 600 Mil Width

VR001725
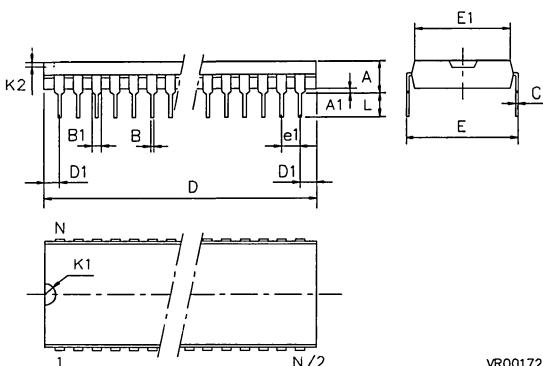
Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5 08			0 200
A1	0.51			0 020		
B	0.35		0 59	0 014		0.023
B1	0 75		1 42	0 030		0 056
C	0 20		0 36	0 008		0 014
D		52.12			2 052	
D1	–	–	–	–	–	–
E			18 54			0 730
E1		13 72				0.540
K1	–	–	–	–	–	–
K2	–	–	–	–	–	–
L	2 54		3 81	100		0 150
e1		1 78			0 070	
Number of Pins						
N	56					

ORDERING INFORMATION

Sales Type	Frequency	Temperature Range	Package
ST9036Q1/XX			PQFP80
ST9036C1/XX		0°C to + 70°C	PLCC68
ST9036B1/XX	24MHz		PSDIP56
ST9036C6/XX		-40°C to + 85°C	PLCC68
ST9036B6/XX			PSDIP56

Note: "XX" is the ROM code identifier that is allocated by SGS-THOMSON after receipt of all required options and the related ROM file.

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ST9036 STANDARD OPTION LIST

Please copy this page (enlarge if possible) and complete ALL sections.
Send the form, with the ROM code image required, to your local SGS-THOMSON sales office.

Customer Company : [... ....]
Company Address : [............... ....]
[............. . ...]
Telephone : [...... ....]
FAX : [......................]
Contact : [........... ....] Telephone (Direct) : [.... ....]

Please confirm characteristics of device :
Device   ST9036

Package   [ ] PQFP80   [ ] PLCC68   [ ] PSDIP56

Temperature Range   [ ] -40°C to +85°C   [ ] 0°C to +70°C

Special Marking   [ ] No
                     [ ] Yes   14 characters   [| | | | | | | | | | | | | |]
                     Authorized characters are letters, digits, '.', '-', '/' and spaces only.
Please consult your local SGS-THOMSON sales office for other marking details if required.
Notes :

ROMless Option (Consult text)
                     [ ] No
                     [ ] Yes   Port Bit   [ ] P7.1   [ ] P2.0

Code :   [ ] EPROM (27128, 27256)
                     [ ] HEX format files on IBM-PC® compatible disk
                        filename : [....................]

Confirmation :   [ ] Code checked with EPROM device in application

Yearly Quantity forecast :   [. ....] k units
- for a period of :   [.........................] years

Preferred Production start dates : [.....................] (YY/MM/DD)

Customer Signature :
Date :