

**ROMLESS HCMOS MCU
WITH EEPROM, RAM AND A/D CONVERTER**

- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time:500ns (12MHz internal)
- ROMless to allow maximum external memory flexibility
- Internal Memory :
 - RAM 256 bytes
 - EEPROM 512 bytes224 general purpose registers available as RAM, accumulators or index pointers (register file)
- 80-pin Plastic Quad Flat Pack Package for ST90R40Q
- 68-lead Plastic Leaded Chip Carrier package for ST90R40C
- DMA controller, Interrupt handler and Serial Peripheral Interface as standard features
- 40 fully programmable I/O pins
- Up to 8 external plus 1 non-maskable interrupts
- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- Two 16 bit Multifunction Timers, each with an 8 bit prescaler and 13 operating modes
- 8 channel 8 bit Analog to Digital Converter, with Analog Watchdogs and external references
- Serial Communications Interface with asynchronous and synchronous capability
- Rich Instruction Set and 14 Addressing modes
- Division-by-Zero trap generation
- Versatile development tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators
- Real Time Operating System
- Compatible with ST9040 16K ROM device (also available in windowed and One Time Programmable EPROM packages)

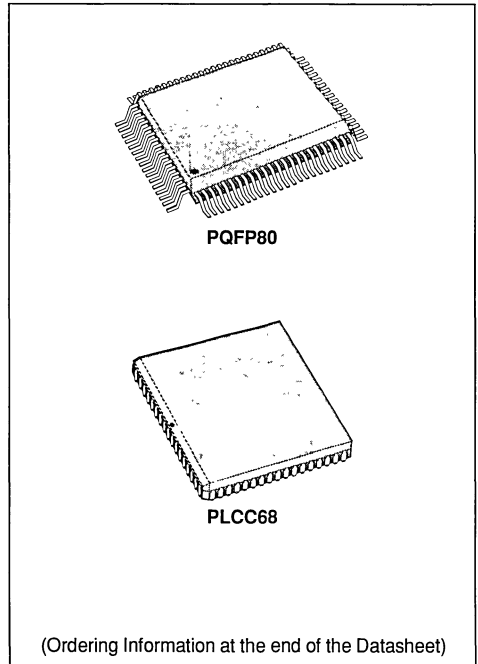


Figure 1. 80 Pin PQFP Package

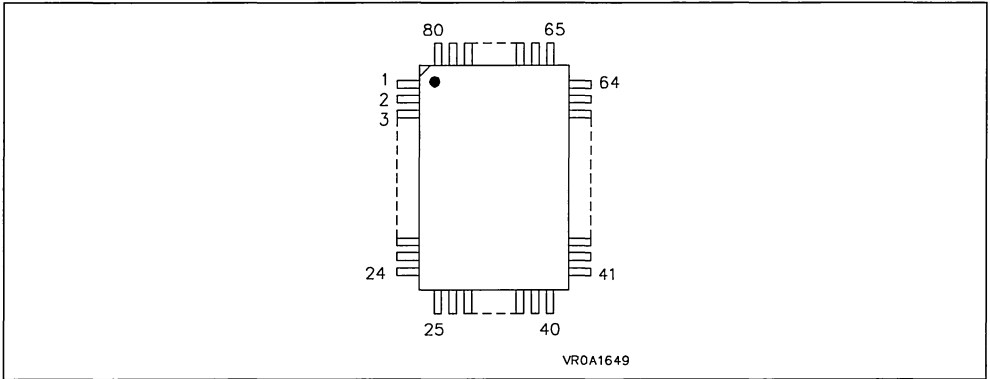


Table 1. ST90R40Q Pin Description

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	AV _{SS}	25	P34/T1INA	64	P20/NMI	80	AV _{DD}
2	AV _{SS}	26	P33/T0OUTB	63	NC	79	NC
3	NC	27	P32/T0INB	62	V _{SS}	78	P47/AIN7
4	P44/AIN4	28	P31/T0OUTA	61	P70/SIN	77	P46/AIN6
5	P57	29	P30/P/D/T0INA	60	P71/SOUT	76	P45/AIN5
6	P56	30	A15	59	P72/INT4/TXCLK /CLKOUT	75	P43/AIN3
7	P55	31	A14	58	P73/INT5 /RXCLK/ADTRG	74	P42/AIN2
8	P54	32	NC	57	P74/P/D/INT6	73	P41/AIN1
9	INT7	33	A13	56	P75/WAIT	72	P40/AIN0
10	INT0	34	A12	55	P76/WDOU /BUSREQ	71	P27/RRDY5
11	P53	35	A11	54	P77/WDIN /BUSACK	70	P26/INT3 /RDSTB5/P/D
12	NC	36	A10	53	R/W	69	P25/WRRDY5
13	P52	37	A9	52	NC	68	P24/INT1 /WRSTB5
14	P51	38	A8	51	DS	67	P23/SDO
15	P50	39	A0/D0	50	AS	66	P22/INT2/SCK
16	OSCOU	40	A1/D1	49	NC	65	P21/SDI/P/D
17	V _{SS}			48	V _{DD}		
18	V _{SS}			47	V _{DD}		
19	NC			46	A7/D7		
20	OSCIN			45	A6/D6		
21	RESET			44	A5/D5		
22	P37/T1OUTB			43	A4/D4		
23	P36/T1INB			42	A3/D3		
24	P35/T1OUTA			41	A2/D2		

Figure 2. 68 Pin PLCC Package

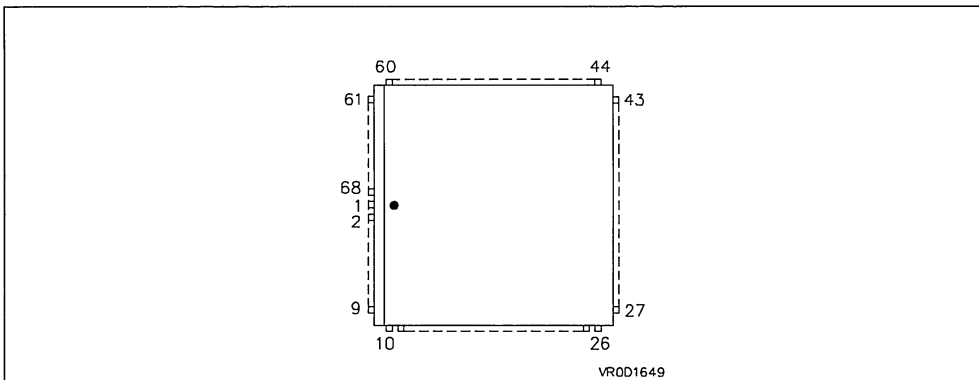


Table 2. ST90R40C Pin Description

Pin	Name	Pin	Name	Pin	Name	Pin	Name
61	P44/Ain4	10	P35/T1OUTA	43	P70/SIN	60	AV _{SS}
62	P57	11	P34/T1INA	42	P71/SOUT	59	AV _{DD}
63	P56	12	P33/T0OUTB	41	P72/CLKOUT /TXCLK/INT4	58	P47/Ain7
64	P55	13	P32/T0INB			57	P46/Ain6
65	P54	14	P31/T0OUTA	40	P73/ADTRG /RXCLK/INT5	56	P45/Ain5
66	INT7	15	P30/P/D/T0INA			55	P43/Ain3
67	INT0	16	A15	39	P74/P/D/INT6	54	P42/Ain2
68	P53	17	A14	38	P75/WAIT	53	P41/Ain1
● 1	P52	18	A13	37	P76/WDOOUT /BUSREQ	52	P40/Ain0
2	P51	19	A12			51	P27/RRDY5
3	P50	20	A11	36	P77/WDIN /BUSACK	50	P26/INT3 /RDSTB5/P/D
4	OSCOUT	21	A10			49	P25/WRRDY5
5	V _{SS}	22	A9	35	R/W	48	P24/INT1 /WRSTB5
6	OSCIN	23	A8	34	DS		
7	RESET	24	A0/D0	33	AS	46	P22/INT2/SCK
8	P37/T1OUTB	25	A1/D1	32	V _{DD}	45	P21/SDI/P/D
9	P36/T1INB	26	A2/D2	31	A7/D7	44	P20/NMI
				30	A6/D6		
				29	A5/D5		
				28	A4/D4		
				27	A3/D3		

1.1 GENERAL DESCRIPTION

The ST90R40 is a ROMLESS member of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The ROMLESS part may be used for the prototyping and pre-production phases of development, and offers the maximum in program flexibility in production systems.

The ST90R40 is fully compatible with the ST9040 ROM version and this datasheet will thus provide only information specific to the ROMLESS device.

THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST9040 ROM-BASED DEVICE.

The ROMLESS ST90R40 can be configured as a microcontroller able to manage external memory, or as a parallel processing element in a system with other processors and peripheral controllers.

The nucleus of the ST90R40 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-BUS, I²C-bus and IM-bus Interface, plus two

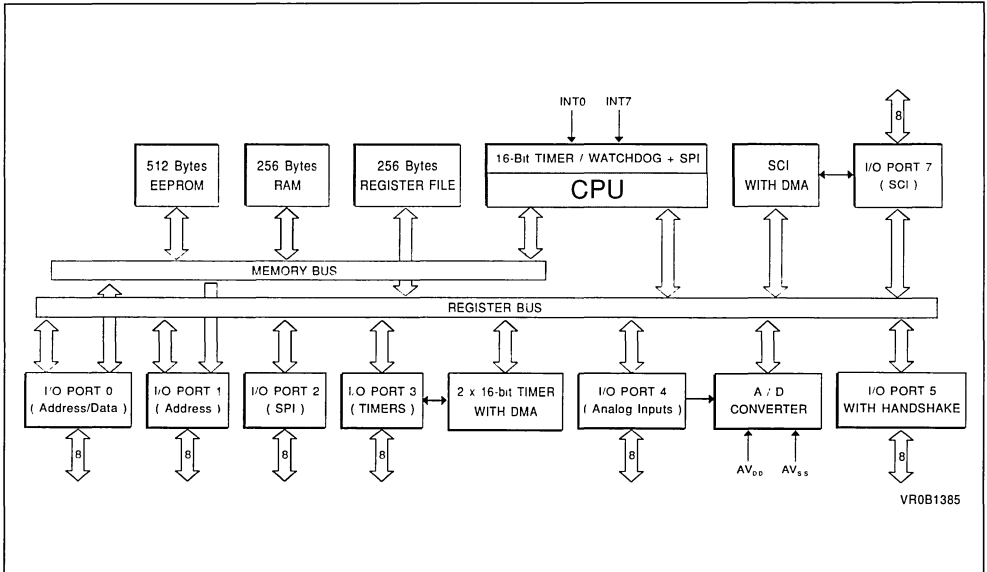
8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST90R40 with up to 56 I/O lines dedicated to memory addressing or digital Input/Output. These lines are grouped into up to seven 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing and status signals, address lines, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.

Three memory spaces are available: Program Memory (external), Data Memory (internal and external) and the Register File, which includes the control and status registers of the on-chip peripherals.

Two 16 bit MultiFunction Timers, each with an 8 bit Prescaler and 13 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer.

Figure 3. Block Diagram



GENERAL DESCRIPTION (Continued)

In addition there is an 8 channel Analog to Digital Converter with integral sample and hold, fast 1 μ s conversion time and 8 bit resolution. An Analog Watchdog feature is included for two input channels.

1.2 PIN DESCRIPTION

\overline{AS} . *Address Strobe (output, active low, 3-state).* Address Strobe is pulsed low once at the beginning of each memory cycle. The rising edge of \overline{AS} indicates that address, Read/Write (R/W), and Data Memory signals are valid for program or data memory transfers. Under program control, \overline{AS} can be placed in a high-impedance state along with Port 0 and Port 1, Data Strobe (\overline{DS}) and R/W.

\overline{DS} . *Data Strobe (output, active low, 3-state).* Data Strobe provides the timing for data movement to or from Port 0 for each memory transfer. During a write cycle, data out is valid at the leading edge of \overline{DS} . During a read cycle, Data In must be valid prior to the trailing edge of \overline{DS} . When the ST90R40 accesses on-chip Data memory, \overline{DS} is held high during the whole memory cycle. It can be placed in a high impedance state along with Port 0, Port 1, \overline{AS} and R/W.

R/W. *Read/Write (output, 3-state).* Read/Write determines the direction of data transfer for memory transactions. R/W is low when writing to program or data memory, and high for all other transactions. It can be placed in a high impedance state along with Port 0, Port 1, \overline{AS} and \overline{DS} .

RESET. *Reset (input, active low).* The ST9 is initialised by the Reset signal. With the deactivation of RESET, program execution begins from the Program memory location pointed to by the vector contained in program memory locations 00h and 01h.

Completing the device is a full duplex Serial Communications Interface with an integral 110 to 375000 baud rate generator, asynchronous and 1.5Mbyte/s synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

OSCIN, OSCOUT. *Oscillator (input and output).* These pins connect a parallel-resonant crystal (24MHz maximum), or an external source to the on-chip clock oscillator and buffer. OSCIN is the input of the oscillator inverter and internal clock generator; OSCOUT is the output of the oscillator inverter.

AV_{DD} . Analog V_{DD} of the Analog to Digital Converter.

AV_{SS} . Analog V_{SS} of the Analog to Digital Converter. *Must be tied to V_{SS} .*

V_{DD} . Main Power Supply Voltage ($5V \pm 10\%$)

V_{SS} . Digital Circuit Ground.

AD0-AD7, (P0.0-P0.7) *Address/Data Lines (Input/Output, TTL or CMOS compatible).* 8 lines providing a multiplexed address and data bus, under control of the \overline{AS} and \overline{DS} timing signals.

A8-A15 *Address Lines (Output, TTL or CMOS compatible).* 8 lines providing non-multiplexing address bus, under control of the \overline{AS} and \overline{DS} timing signals.

P2.0-P2.7 P3.0-P3.7, P4.0-P4.7, P5.0-P5.7, P7.0-P7.7 *I/O Port Lines (Input/Output, TTL or CMOS compatible).* 40 lines grouped into I/O ports of 8 bits, bit programmable under program control as general purpose I/O or as Alternate functions (see next section).

1.2.1 I/O PORT ALTERNATE FUNCTIONS

Each pin of the I/O ports of the ST90R40 may assume software programmable Alternative Functions as shown in the Pin Configuration Drawings. Table 3 shows the Functions allocated to each I/O Port pins.

PIN DESCRIPTION (Continued)

Table 3. I/O Port Alternate Function Summary

I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin Assignment	
				PQFP80	PLCC68
P0.0	A0/D0	I/O	Address/Data bit 0 mux	39	24
P0.1	A1/D1	I/O	Address/Data bit 1 mux	40	25
P0.2	A2/D2	I/O	Address/Data bit 2 mux	41	26
P0.3	A3/D3	I/O	Address/Data bit 3 mux	42	27
P0.4	A4/D4	I/O	Address/Data bit 4 mux	43	28
P0.5	A5/D5	I/O	Address/Data bit 5 mux	44	29
P0.6	A6/D6	I/O	Address/Data bit 6 mux	45	30
P0.7	A7/D7	I/O	Address/Data bit 7 mux	46	31
P1.0	A8	O	Address bit 8	38	23
P1.1	A9	O	Address bit 9	37	22
P1.2	A10	O	Address bit 10	36	21
P1.3	A11	O	Address bit 11	35	20
P1.4	A12	O	Address bit 12	34	19
P1.5	A13	O	Address bit 13	33	18
P1.6	A14	O	Address bit 14	31	17
P1.7	A15	O	Address bit 15	30	16
P2.0	NMI	I	Non-Maskable Interrupt	64	44
P2.1	P/D	O	Program/Data Space Select	65	45
P2.1	SDI	I	SPI Serial Data Out	65	45
P2.2	INT2	I	External Interrupt 2	66	46
P2.2	SCK	O	SPI Serial Clock	66	46
P2.3	SDO	O	SPI Serial Data In	67	47
P2.4	INT1	I	External Interrupt 1	68	48
P2.4	WRSTB5	O	Handshake Write Strobe P5	68	48
P2.5	WRRDY5	I	Handshake Write Ready P5	69	49
P2.6	INT3	I	External Interrupt 3	70	50
P2.6	RDSTB5	I	Handshake Read Strobe P5	70	50
P2.6	P/D	O	Program/Data Space Select	70	50
P2.7	RDRDY5	O	Handshake Read Ready P5	71	51
P3.0	T0INA	I	MF Timer 0 Input A	29	15
P3.0	P/D	O	Program/Data Space Select	29	15
P3.1	T0OUTA	O	MF Timer 0 Output A	28	14
P3.2	T0INB	I	MF Timer 0 Input B	27	13
P3.3	T0OUTB	O	MF Timer 0 Output B	26	12
P3.4	T1INA	I	MF Timer 1 Input A	25	11

PIN DESCRIPTION (Continued)

Table 3. I/O Port Alternate Function Summary (Continued)

I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin Assignment	
				PQFP80	PLCC68
P3.5	T1OUTA	O	MF Timer 1 Output A	24	10
P3.6	T1INB	I	MF Timer 1 Input B	23	9
P3.7	T1OUTB	O	MF Timer 1 Output B	22	8
P4.0	Ain0	I	A/D Analog Input 0	72	52
P4.1	Ain1	I	A/D Analog Input 1	73	53
P4.2	Ain2	I	A/D Analog Input 2	74	54
P4.3	Ain3	I	A/D Analog Input 3	75	55
P4.4	Ain4	I	A/D Analog Input 4	4	61
P4.5	Ain5	I	A/D Analog Input 5	76	56
P4.6	Ain6	I	A/D Analog Input 6	77	57
P4.7	Ain7	I	A/D Analog Input 7	78	58
P5.0		I/O	I/O Handshake Port 5	15	3
P5.1		I/O	I/O Handshake Port 5	14	2
P5.2		I/O	I/O Handshake Port 5	13	1
P5.3		I/O	I/O Handshake Port 5	11	68
P5.4		I/O	I/O Handshake Port 5	8	65
P5.5		I/O	I/O Handshake Port 5	7	64
P5.6		I/O	I/O Handshake Port 5	6	63
P5.7		I/O	I/O Handshake Port 5	5	62
P7.0	SIN	I	SCI Serial Input	61	43
P7.1	SOUT	O	SCI Serial Output	60	42
P7.2	INT4	I	External Interrupt 4	59	41
P7.2	TXCLK	I	SCI Transmit Clock Input	59	41
P7.2	CLKOUT	O	SCI Byte Sync Clock Output	59	41
P7.3	INT5	I	External Interrupt 5	58	40
P7.3	RXCLK	I	SCI Receive Clock Input	58	40
P7.3	ADTRG	I	A/D Conversion Trigger	58	40
P7.4	INT6	I	External Interrupt 6	57	39
P7.4	P/D	O	Program/Data Space Select	57	39
P7.5	WAIT	I	External Wait Input	56	38
P7.6	WDOUT	O	T/WD Output	55	37
P7.6	BUSREQ	I	External Bus Request	55	37
P7.7	WDIN	I	T/WD Input	54	36
P7.7	BUSACK	O	External Bus Acknowledge	54	36

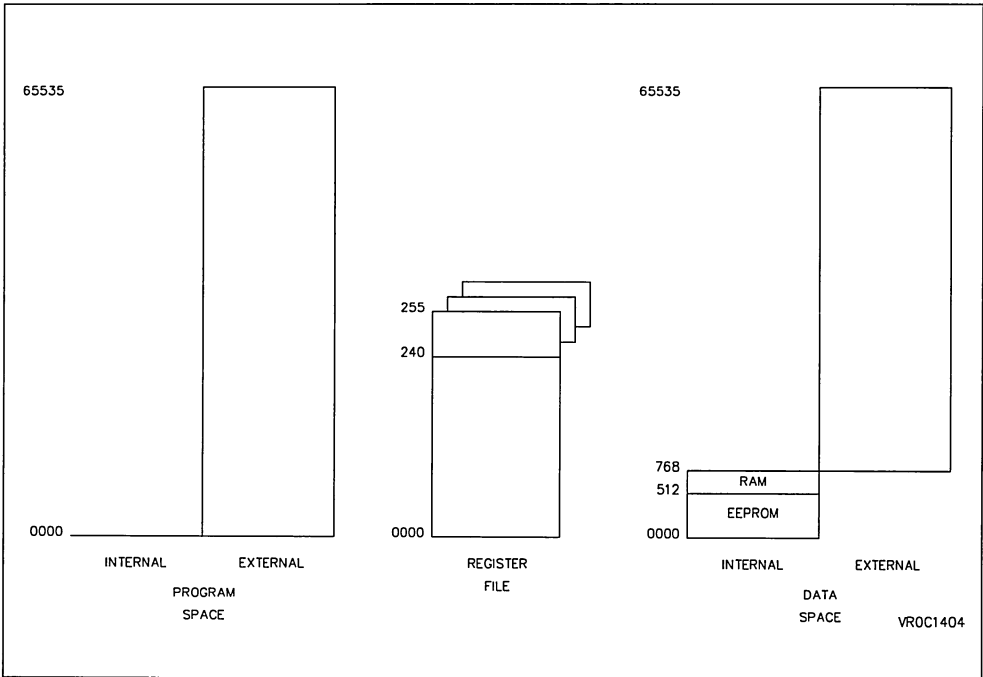
1.3 MEMORY

The memory of the ST90R40 is functionally divided into two areas, the Register File and Memory. The Memory may optionally be divided into two spaces, each having a maximum of 65,536 bytes. The two memory spaces are separated by function, one space for Program code, the other for Data. The ST90R40 addresses all program memory in the external PROGRAM space. The DATA space includes the 512 bytes of on-chip EEPROM at addresses 0 through 1FFh and the 256 bytes of

on-chip RAM memory at addresses 200h through 2FFh.

The External Memory spaces are addressed using the multiplexed address and data buses on Ports 0 and 1. Data Memory may be decoded externally by using the P/D Alternate Function output. The on-chip general purpose (GP) Registers may be used as RAM memory.

Figure 4. Memory Spaces



ORDERING INFORMATION

Sales Type	Frequency	Temperature Range	Package
ST90R40C6	24MHz	-40°C to + 85°C	PLCC68
ST90R40Q1		0 °C to + 70 °C	PQFP80