STA027

SBC CODEC

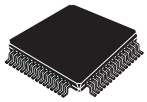
PRODUCT PREVIEW

Features

- Fully Integrated SBC Encoder And Decoder
- Operating Modes:
  - SBC encoder mode (PCM In/Serial Output)
    - PCM input: 16, 32, 44.1, 48kHz
    - Channel Mode: Mono, Dual,
    - Stereo
    - Subbands: 4 OR 8
    - Allocation Methods:
    - Loudness/SNR
  - SBC Decoder Mode
    - Serial Input
    - PCM Output: 16, 32, 44.1, 48kHz
- Digital Volume
- Bass & Treble Control
- Serial Bitstream Input/output Interface up to 2Mbit/s
- Easy Programmable ADC Input Interface
- Serial PCM Output Interface (I^2S and other Formats)
- PLL for Internal Clock and for Output PCM Clock Generation
- I^2C Control Bus
- Low Power 2.4V CMOS Technology with 3.3V Tolerant and Capable I/O

Applications

- bluetooth AV Applications
- DVD Wirless Speaker Options



TQFP64

- Wireless Audio Dongle
- PC Wireless Speakers
- Generic Compressed Audio LinkS
- Wireless Headphone/Headsets

Description

STA027 is a fully integrated SBC codec targeting wireless audio transmission such as DVD rear channels wireless speakers, USB dongle, PC wireless speakers. The device is fully controllable through a standard I^2C bus.

Compression Engine

SBC

The SBC Subband Coding engine can be used when high quality audio is required in wireless applications (such as Bluetooth). SBC is an audio coding system specially designed for Bluetooth AV applications to obtain high quality audio at medium bit rates, and having a low computational complexity. SBC uses 4 or 8 subbands, adaptive bit allocation algorithm, and simple adaptive block PCM quantizers..

Order codes

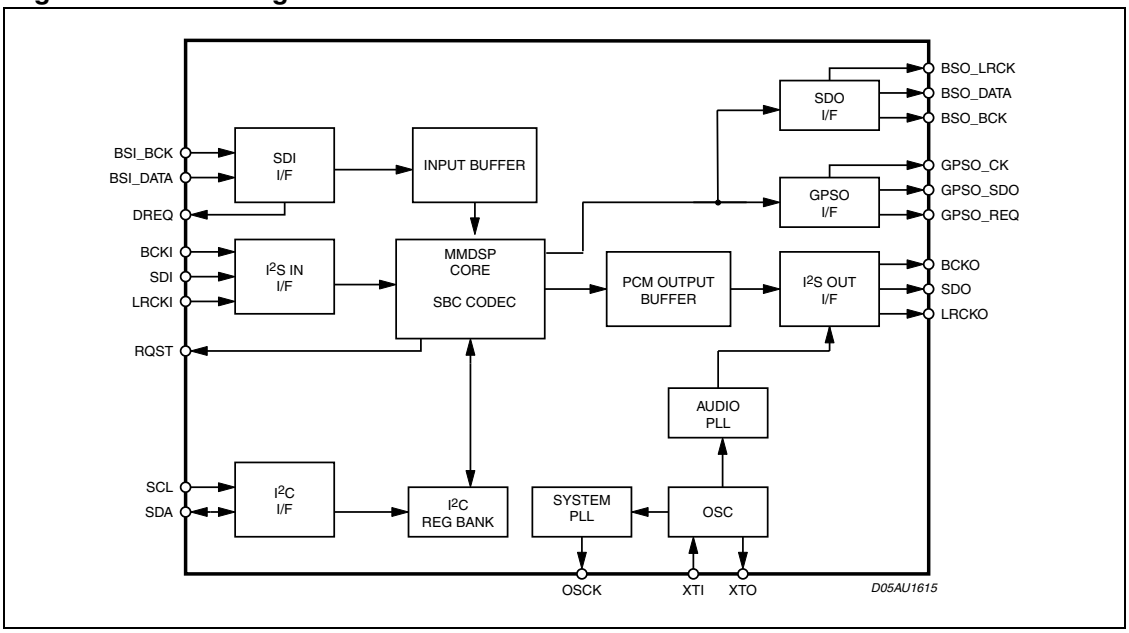
Part number	Package	Packing
STA027	TQFP64	Tube

Contents

1 Typical application circuit and block diagram

1.1 Block diagram

Figure 1. Block diagram



1.2 Typical bluetooth wireless audio application

Figure 2. Transmitter block diagram

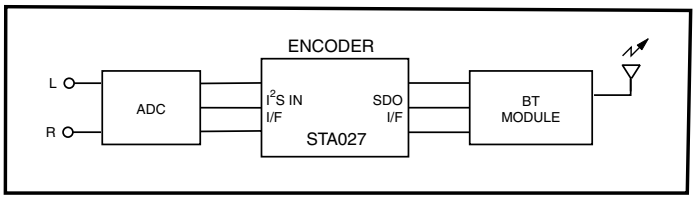
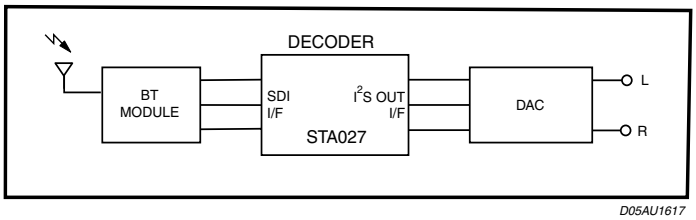


Figure 3. Receiver block diagram



Note: for Bluetooth chipset please refer to following device: SLTLC2416, STLC2150, STLC2500. For ADC and DAC solutions please refer to following devices: STW5094, STW5095, TDA7535.

2 Pins description and connection diagram

2.1 Pin description

Table 1. pin description

PIN	Pin Name	Type	Description	Source/Dest
SDO interface				
1	BSO_LRCK	I	DSP Interface left/right Clock	From DSP
2	BSO_BCK	I	DSP interface serial data	From DSP
3	BSO_DATA	I	DSP interface bit clock	From DSP
SDI interface				
4	DREQ	O	Bitstream data request	To MCU
7	BSI_LRCK	I	Bitstream interface left/right Clock	From MCU
8	BSI_BCK	I	Bitstream interface clock	From MCU
9	BSI_DATA	I	Bitstream interface serial data	From MCU
PCM IN interface				
12	LRCKI	I	ADC left/right Clock	From ADC
13	BCKI	I	ADC bit clock	From ADC
14	SDI	I	ADC serial data	From ADC
PCM OUT interface				
19	OSCK	O	DAC oversampling clock	To DAC/ADC
20	LRCKO	O	DAC Interface left/right Clock	To DAC
21	BCKO	O	DAC bit clock	To DAC
22	SDO	O	DAC serial data	To DAC
GPSO interface				
54	GPSO_SDO	O	GPSO serial data	To MCU
55	GPSO_CK	I	GPSO bit clock	From MCU
56	GPSO_REQ	O	GPSO request signal	To MCU
GPIO interface				
26	IODATA0	I/O	GPIODATA0	
27	IODATA1	I/O	GPIODATA1	
28	IODATA2	I/O	GPIODATA2	
31	IODATA3	I/O	GPIODATA3	
32	IODATA4	I/O	GPIODATA4	
33	IODATA5	I/O	GPIODATA5	

Table 1. pin description

PIN	Pin Name	Type	Description	Source/Dest
34	IODATA6	I/O	GPIODATA6	
35	IODATA7	I/O	GPIODATA7	
44	IODATA8	I/O	GPIODATA8	
45	IODATA9	I/O	GPIODATA9	
46	IODATA10	I/O	GPIODATA10	
47	IODATA11	I/O	GPIODATA11	
48	IODATA12	I/O	GPIODATA12	
49	IODATA13	I/O	GPIODATA13	
50	IODATA14	I/O	GPIODATA14	
51	IODATA15	I/O	GPIODATA15	
HANDSHAKE SIGNALS				
59	RQST	O	I^2C data signal	To MCU
60	STB	I	Strobe signal	From MCU
I^2C LINK				
63	SCL	I	I^2C clock signal	From MCU
64	SDA	I/O	I^2C data signal	To MCU
MISCELLANEOUS				
15	-RESET	I	Reset	
16	-TESTEN	I	Reserved for test purpose	
17	XTI	I	Oscillator input	
18	XTO	O	Oscillator output	
25	CLKOUT	O	Buffered output clock	
38	FILT1		PLL external filter	
40	FILT0	I	PLL external filter	
POWER SUPPLY				
5	VDD_1		Digital supply (2.5V Power Supply)	
6	VSS_1		Ground	
10	VDD_2		Digital supply (2.5V Power Supply)	
11	VSS_2		Ground	
23	VCC_1		Digital supply (3.3V Power Supply)	
24	VSS_3		Ground	
29	VDD_3		Digital supply (2.5V Power Supply)	
30	VSS_4		Ground	

Table 1. pin description

PIN	Pin Name	Type	Description	Source/Dest
36	VDD_4		Digital supply (2.5V Power Supply)	
37	VSS_5		Ground	
39	PLL_VCC		Digital supply (2.5V Power Supply)	
41	PLL_GND		Ground	
42	VCC_2		Digital supply (3.3V Power Supply)	
43	VSS_6		Ground	
52	VSS_7		Ground	
53	VDD_5		Digital supply (2.5V Power Supply)	
57	VSS_8		Ground	
58	VCC_3		Digital supply (3.3V Power Supply)	
61	VSS_9		Ground	
62	VDD_6		Digital supply (2.5V Power Supply)	

Figure 4.

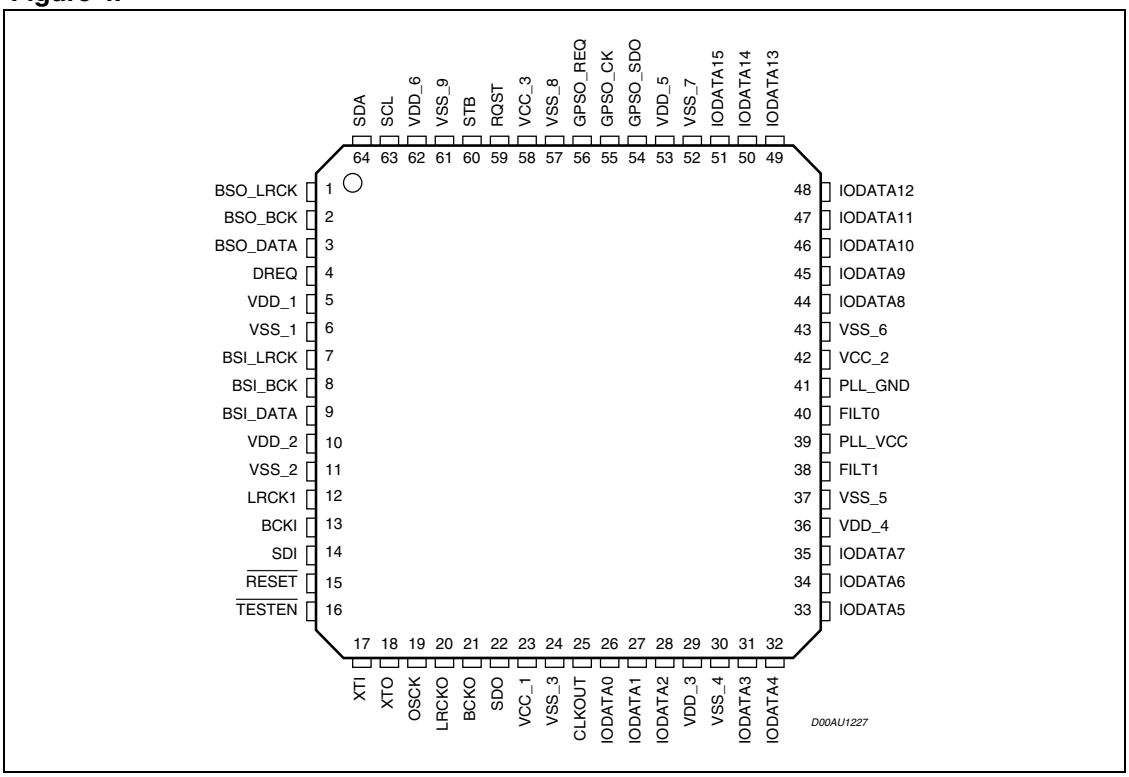


Table 2. Thermal Data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal resistance Junction to Ambient	85	°C/W

3 Electrical Specification

3.1 Absolute maximum ratings

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DD}	Digital Power Supply at 2.5V (nominal)	-0.5 to 3.3	V
V_{CC}	Digital Power Supply at 3.3V (nominal)	-0.5 to 4	V
P_{LL}-V_{CC}	Analog Supply Voltage at 2.5V (nominal)	-0.5 to 3.3	V
V_{IH}/V_{IL}	Voltage on input pins (3.3V pads)	-0.5 to V_{CC} +0.5	V
T_{stg}	Storage Temperature	-40 to +150	°C
T_{op}	Operative ambient temp	-40 to +85(*)	°C
T_j	Operating Junction Temperature	-40 to 125	°C

3.2 Electrical characteristics

(T_{amb} = 25°C; R_g = 50Ω unless otherwise specified)

Table 4. DC Operating Conditions

Symbol	Parameter	Value	Unit
V_{DD}	Power Supply Voltage	2.5 ± 0.25	V
V_{CC}	Power Supply Voltage	3.3 ± 0.3	V
PLL_V_{CC}	Power Supply Voltage	2.5 ± 0.25	V

Table 5. General Interface Electrical Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Note
I_{IL}	Low Level Input CurrentWithout pull-up device	V_i = 0V	-10		10	µA	1
I_{IH}	High Level Input CurrentWithout pull-up device	$V_i = V_{DD}$	-10		10	µA	1
V_{esd}	Electrostatic Protection	Leakage < 1µA	2000			V	2

Note: 1 The leakage currents are generally very small, < 1nA. The value given here is a maximum that can occur after an electrostatic stress on the pin.

2 Human Body Model.

Table 6. DC electrical characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Note
V_{IL}	Low Level Input Voltage				$0.2*V_{CC}$	V	
V_{IH}	High Level Input Voltage		$0.8*V_{CC}$			V	
V_{ol}	Low Level Output Voltage	I_{ol} = Xma			0.4V	V	1, 2
V_{oh}	High Level Output Voltage		$0.85*V_{CC}$			V	1, 2

Note: 1 Takes into account 200mV voltage drop in both supply lines.

2 X is the source/sink current under worst case conditions and is reflected in the name of the I/O cell according to the drive capability.

Table 7.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Note
I_{pu}	Pull-up current	V_i = 0V; pin numbers 7, 24 and 26	-25	-66	-125	µA	1
R_{pu}	Equivalent Pull-up Resistance			50		kΩ	

Note: 1 Min. condition: V_{DD} = 2.7V, 125°C Min process Max. condition: V_{DD} = 3.6V, -20°C Max.

Table 8. Power Dissipation

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Note
P_D	Power Dissipation@ V_{DD} = 2.4V	Sampling_freq ≤24 kHz		165		mW	
		Sampling_freq ≤32 kHz		170		mW	
		Sampling_freq ≤48 kHz		185		mW	

Note: power measurements refer to encoder mode.

4 Host register

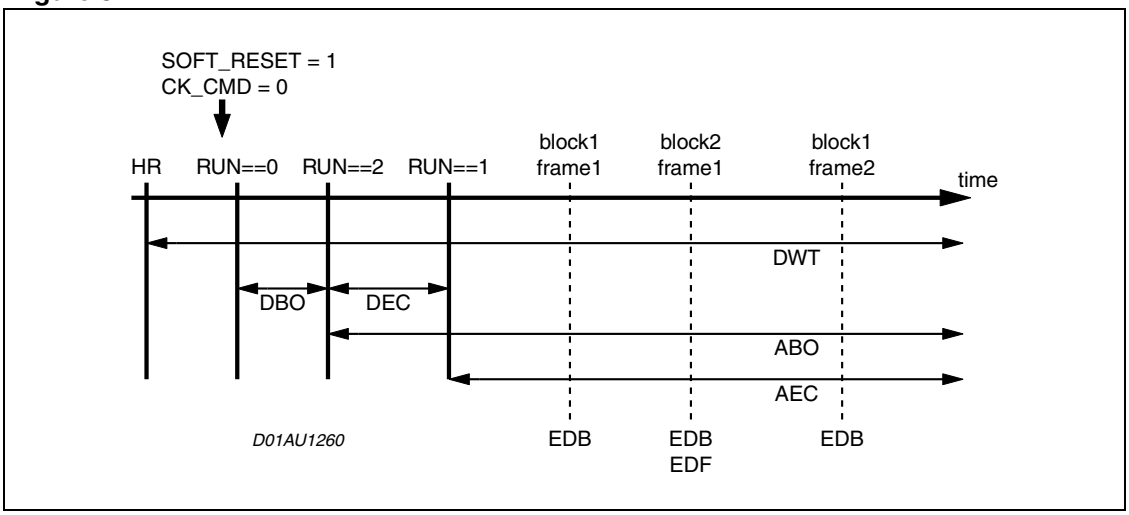
The following table gives a description of STA027 register list.

The STA027 device includes 256 I^2C registers. In this document, only the user-oriented registers are described. The undocumented registers are reserved or unused. These registers must never be accessed (in Read or in Write mode). The Read-Only registers must never be written

We can split the data flux in different time periods (see following diagram) meanwhile host registers can be read or written :

- DWT : During Whole Time (at any time during process).
- DEC : During External Config (period between RUN=2 and RUN=1).
- DBO : During Boot (period between RUN=0 and RUN=2).
- ABO : After BOot (period after RUN=1).
- AEC : After External Config (period after RUN=2).
- EDF : Every Decoded Frame (each time a frame has been decoded).
- EDB : Every Decoded Block (each time a block has been decoded).

Figure 5.



4.1 Register map

Table 9. register map by function

Register function	Hex	Dec	Name	Type	When
VERSION	0x00	0	VERSION	RO	DWT
	0x01	1	IDENT	RO	DWT
	0xD3	211	SOFT_VERSION	RO	DWT
PLL_AUDIO_CONFIGURATION	0xDC	220	PLL_AUDIO_PEL_192	RW	DEC
	0xDD	221	PLL_AUDIO_PEH_192	RW	DEC
	0xDE	222	PLL_AUDIO_NDIV_192	RW	DEC
	0xDF	223	PLL_AUDIO_XDIV_192	RW	DEC
	0xE0	224	PLL_AUDIO_MDIV_192	RW	DEC
	0xE1	225	PLL_AUDIO_PEL_176	RW	DEC
	0xE2	226	PLL_AUDIO_PEH_176	RW	DEC
	0xE3	227	PLL_AUDIO_NDIV_176	RW	DEC
	0xE4	228	PLL_AUDIO_XDIV_176	RW	DEC
	0xE5	229	PLL_AUDIO_MDIV_176	RW	DEC
PLL_SYSTEM_CONFIGURATION	0xE6	230	PLL_SYSTEM_PEL_50	RW	DEC
	0xE7	231	PLL_SYSTEM_PEH_50	RW	DEC
	0xE8	232	PLL_SYSTEM_NDIV_50	RW	DEC
	0xE9	233	PLL_SYSTEM_XDIV_50	RW	DEC
	0xEA	234	PLL_SYSTEM_MDIV_50	RW	DEC
	0xEB	235	PLL_SYSTEM_PEL_42_5	RW	DEC
	0xEC	236	PLL_SYSTEM_PEH_42_5	RW	DEC
	0xED	237	PLL_SYSTEM_NDIV_42_5	RW	DEC
	0xEE	238	PLL_SYSTEM_XDIV_42_5	RW	DEC
	0xEF	239	PLL_SYSTEM_MDIV_42_5	RW	DEC
I^2Sout_CONFIGURATION	0x66	102	OUTPUT_CONF	RW	DEC
	0x67	103	PCM_DIV	RW	DEC
	0x68	104	PCM_CONF	RW	DEC
	0x69	105	PCM_CROSS	RW	DEC
GPSO_CONFIGURATION	0x66	102	OUTPUT_CONF	RW	DEC
	0x6A	106	GPSO_CONF	RW	DEC
I^2Sin_CONFIGURATION	0x5A	90	INPUT_CONF	RW	DEC
	0x5B	91	I_AUDIO_CONFIG_1	RW	DEC
	0x5C	92	I_AUDIO_CONFIG_2	RW	DEC
	0x5D	93	I_AUDIO_CONFIG_3	RW	DEC

Table 9. register map by function

Register function	Hex	Dec	Name	Type	When
SDI_CONFIGURATION	0x59	89	POL_REQ	RW	DEC
	0x5A	90	INPUT_CONF	RW	DEC
	0x5B	91	I_AUDIO_CONFIG_1	RW	DEC
COMMAND	0x10	16	SOFT_RESET	WO	DWT
	0x3A	58	CK_CMD	WO	DBO
	0x55	85	DEC_SEL	RW	DEC
	0x56	86	RUN	RW	DEC
	0x52	82	CRC_IGNORE	RW	ABO
	0x53	83	MUTE	RW	ABO
	0x57	87	SKIP	RW	ABO
	0x58	88	PAUSE	RW	ABO
STATUS	0xCC	204	STATUS_MODE	RO	EDF
	0xCD	205	STATUS_CHAN_NB	RO	EDF
	0xCE	206	STATUS_SF	RO	EDF
	0x6F	111	STATUS_FE	RO	EDF
	0xD4	212	HEADER_1	RO	EDF
	0xD5	213	HEADER_2	RO	EDF
	0xD6	214	HEADER_3	RO	EDF
	0xD7	215	HEADER_4	RO	EDF
	0xD8	216	HEADER_5	RO	EDF
	0xD9	217	HEADER_6	RO	EDF
MIX_CONFIGURATION	0x7b	123	MIX_MODE	RW	ABO
	0x7c	124	MIX_DLA	RW	ABO
	0x7d	125	MIX_DLB	RW	ABO
	0x7e	126	MIX_DRA	RW	ABO
	0x7f	127	MIX_DRB	RW	ABO
TONE_CONFIGURATION	0x75	117	TONE_ON	RW	ABO
	0x76	118	TONE_FCUTH	RW	ABO
	0x77	119	TONE_FCUTL	RW	ABO
	0x78	120	TONE_GAINH	RW	ABO
	0x79	121	TONE_GAINL	RW	ABO
	0x7A	122	TONE_GAIN_ATTEN	RW	ABO

5 Register description

5.1 Version registers description

5.1.1 VERSION :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0x00 (0)

Type : RO - DWT

Software Reset : 0x10

Hardware Reset : 0x10

Description :

The VERSION register is Read-only and it is used to identify the IC on the application board.

5.1.2 IDENT :

b7	b6	b5	b4	b3	b2	b1	b0
1	0	1	0	1	1	0	0

Address : 0x01 (1)

Type : RO - DWT

Software Reset : 0xAC

Hardware Reset : 0xAC

Description :

IDENT is a read-only register and it is used to identify the IC on an application board. IDENT always has the value 0xAC.

5.1.3 SOFT_VERSION :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0xD3 (211)

Type : RO - DWT

Software Reset : X

Description :

The SOFT_VERSION register is Read-only and it is used to identify the software running on the IC.

5.2 PLL_AUDIO_CONFIGURATION registers description

5.2.1 PLL_AUDIO_PEL_192 :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0xDC (220)

Type : RW - DEC

Software Reset : 58

Description :

This register must contain a PEL value that enables the audio PLL to generate a frequency of ofact*192 kHz for the PCMCK.See table 1, 2 & 3.

ofact is the oversampling factor needed by the DAC (ofac==246 or ofac==384).

Default value at soft reset assume :

- ofact == 256
- external crystal provide a CRYCK running at 14.31818 MHz

5.2.2 PLL_AUDIO_PEH_192 :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0xDD (221)

Type : RW - DEC

Software Reset : 187

Description :

This register must contain a PEH value that enables the audio PLL to generate a frequency of ofact*192 kHz for the PCMCK.See table 1, 2 & 3.

Default value at soft reset assume :

- ofact == 256
- external crystal provide a CRYCK running at 14.31818 MHz

5.2.3 PLL_AUDIO_NDIV_192 :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0xDE (222)

Type : RW - DEC

Software Reset : 0

Description :

This register must contain a NDIV value that enables the audio PLL to generate a frequency of ofact*192 kHz for the PCMCK.See table 1, 2 & 3.

Default value at soft reset assume :

– ofact == 256
– external crystal provide a CRYCK running at 14.31818 MHz

5.2.4 PLL_AUDIO_XDIV_192 :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0xDF (223)

Type : RW - DEC

Software Reset : 3

Description :

This register must contain a XDIV value that enables the audio PLL to generate a frequency of ofact*192 kHz for the PCMCK.See table 1, 2 & 3.

Default value at soft reset assume :

– ofact == 256
– external crystal provide a CRYCK running at 14.31818 MHz

5.2.5 PLL_AUDIO_MDIV_192 :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0xE0 (224)

Type : RW - DEC

Software Reset : 12

Description :

This register must contain a MDIV value that enables the audio PLL to generate a frequency of ofact*192 kHz for the PCMCK.See table 1, 2 & 3.

Default value at soft reset assume :

– ofact == 256
– external crystal provide a CRYCK running at 14.31818 MHz

5.2.6 PLL_AUDIO_PEL_176 :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0xE1 (225)

Type : RW - DEC

Software Reset : 54

Description :

This register must contain a PEL value that enables the audio PLL to generate a frequency of ofact*176 kHz for the PCMCK.See table 1, 2 & 3.

Default value at soft reset assume :

- fact == 256
- external crystal provide a CRYCK running at 14.31818 MHz

5.2.7 PLL_AUDIO_PEH_176 :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0xE2 (226)

Type : RW - DEC

Software Reset : 118

Description :

This register must contain a PEH value that enables the audio PLL to generate a frequency of ofact*176 kHz for the PCMCK.See table 1, 2 & 3.

Default value at soft reset assume :

- ofact == 256
- external crystal provide a CRYCK running at 14.31818 MHz

5.2.8 PLL_AUDIO_NDIV_176 :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0xE3 (227)

Type : RW - DEC

Software Reset : 0

Description :

This register must contain a NDIV value that enables the audio PLL to generate a frequency of ofact*176 kHz for the PCMCK.See table 1, 2 & 3.

Default value at soft reset assume :

- ofact == 256
- external crystal provide a CRYCK running at 14.31818 MHz

5.2.9 PLL_AUDIO_XDIV_176 :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0xE4 (228)

Type : RW - DEC

Software Reset : 2

Description :

This register must contain a XDIV value that enables the audio PLL to generate a frequency of ofact*176 kHz for the PCMCK.See table 1, 2 & 3.

Default value at soft reset assume :

- ofact == 256
- external crystal provide a CRYCK running at 14.31818 MHz

5.2.10 PLL_AUDIO_MDIV_176 :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0xE5 (229)

Type : RW - DEC

Software Reset : 8

Description :

This register must contain a MDIV value that enables the audio PLL to generate a frequency of ofact*176 kHz for the PCMCK.See table 1,2 & 3.

Default value at soft reset assume :

- ofact == 256
- external crystal provide a CRYCK running at 14.31818 MHz

5.3 PLL_SYSTEM_CONFIGURATION registers description

5.3.1 PLL_SYSTEM_PEL_50 :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0xE6 (230)

Type : RW - DEC

Software Reset : 0

Description :

This register must contain a PEL value that enables the system PLL to generate a frequency of 50 MHz for the SYSCK. See table 4.

Default value at soft reset assume :

– external crystal provide a CRYCK running at 14.31818 MHz

5.3.2 PLL_SYSTEM_PEH_50 :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0xE7 (231)

Type : RW - DEC

Software Reset : 0

Description :

This register must contain a PEH value that enables the system PLL to generate a frequency of 50 MHz for the SYSCK. See table 4.

Default value at soft reset assume :

– external crystal provide a CRYCK running at 14.31818 MHz

5.3.3 PLL_SYSTEM_NDIV_50 :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0xE8 (232)

Type : RW - DEC

Software Reset : 0

Description :

This register must contain a NDIV value that enables the system PLL to generate a frequency of 50 MHz for the SYSCK. See table 4.

Default value at soft reset assume :

– external crystal provide a CRYCK running at 14.31818 MHz

5.3.4 PLL_SYSTEM_XDIV_50 :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0xE9 (233)

Type : RW - DEC

Software Reset : 1

Description :

This register must contain a XDIV value that enables the system PLL to generate a frequency of 50 MHZ for the SYSCK. See table 4.

Default value at soft reset assume :

– external crystal provide a CRYCK running at 14.31818 MHz

5.3.5 PLL_SYSTEM_MDIV_50 :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0xEA (234)

Type : RW - DEC

Software Reset : 13

Description :

This register must contain a MDIV value that enables the system PLL to generate a frequency of 50 MHz for the SYSCK. See table 4.

Default value at soft reset assume :

– external crystal provide a CRYCK running at 14.31818 MHz

5.3.6 PLL_SYSTEM_PEL_42_5

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0xE6 (230)

Type : RW - DEC

Software Reset : 126

Description :

This register must contain a PEL value that enables the system PLL to generate a frequency of 42.5 MHz for the SYSCK.See table 4.

Default value at soft reset assume :

– external crystal provide a CRYCK running at 14.31818 MHz

5.3.7 PLL_SYSTEM_PEH_42_5 :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0xE7 (231)

Type : RW - DEC

Software Reset : 223

Description :

This register must contain a PEH value that enables the system PLL to generate a frequency of 42.5 MHz for the SYSCK.See table 4.

Default value at soft reset assume :

– external crystal provide a CRYCK running at 14.31818 MHz

5.3.8 PLL_SYSTEM_NDIV_42_5 :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0xE8 (232)

Type : RW - DEC

Software Reset : 0

Description :

This register must contain a NDIV value that enables the system PLL to generate a frequency of 42.5 MHz for the SYSCK.See table 4.

Default value at soft reset assume :

– external crystal provide a CRYCK running at 14.31818 MHz

5.3.9 PLL_SYSTEM_XDIV_42_5 :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0xE9 (233)

Type : RW - DEC

Software Reset : 1

Description :

This register must contain a XDIV value that enables the system PLL to generate a frequency of 42.5 MHz for the SYSCK.See table 4.

Default value at soft reset assume :

– external crystal provide a CRYCK running at 14.31818 MHz

5.3.10 PLL_SYSTEM_MDIV_42_5 :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0xEA (234)

Type : RW - DEC

Software Reset : 10

Description :

This register must contain a MDIV value that enables the system PLL to generate a frequency of 42.5 MHz for the SYSCK.See table 4.

Default value at soft reset assume :

– external crystal provide a CRYCK running at 14.31818 MHz

5.4 I^2Sout_CONFIGURATION registers description

5.4.1 OUTPUT_CONF :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0x66 (102)

Type : RW - DEC

Software Reset : 0

Description :

If set to 1 enable the configurability of the PCM-BLOCK Output thanks to following registers, else disable this configurability and take embedded default configuration for PCM-BLOCK registers.

Note that this embedded default configuration can be retrieved by user thanks to following setting :

– PCM_DIV = 3;
– PCM_CONF = 0;
– PCM_CROSS = 0;

5.4.2 PCM_DIV :

b7	b6	b5	b4	b3	b2	b1	b0
0	0	DV5	DV4	DV3	DV2	DV1	DV0

Address : 0x67 (103)

Type : RW - DEC

Software Reset : 0

Description :

If OUTPUT_CONF == 1, configure the divider to generate the bit clock of the I^2Sout interface, called BCK0, from PCMCK. according the following relation : BCKO = PCMCK / 2 * (PCM_DIV+1)

5.4.3 PCM_CONF :

b7	b6	b5	b4	b3	b2	b1	b0
0	CO6	CO5	CO4	CO3	CO2	CO1	CO0

Address : 0x68 (104)

Type : RW - DEC

Software Reset : 0

Description :

If OUTPUT_CONF == 1, configure the I^2Sout interface according following table

Table 10. .

Bit fields	Comment
CO[1:0]	0 : 16 bits mode (16 slots transmitted). 1 : 18 bits mode (18 slots transmitted). 2 : 20 bits mode (20 slots transmitted). 3 : 24 bits mode (24 slots transmitted).
CO2	Polarity of BCKO : 0 : data are sent on the falling edge & stable on the rising). 1 : (data are sent on the rising edge & stable on the falling).
CO3	0 : I2S format is selected 1 : other format is selected
CO4	Polarity of LRCKO : 0 : low->right, high->left). 1 : low->left, high->right so compliant to I2S format).
CO5	0 : data are in the last BCKO cycles of LRCKO (right aligned data). 1 : data are in the first BCKO cycles of LRCKO (left aligned data).
CO6	0 : the transmission is LS bit first. 1 : the transmission is MS bit first.

5.4.4 PCM_CROSS :

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0	CR1	CR0

Address : 0x69 (105)

Type : RW - DEC

Software Reset : 0

Description :

If OUTPUT_CONF == 1, CR[1:0] is used to configure the output crossbar according following table

Table 11. .

CR1	CR0	Comment
0	0	Left channel is mapped on the left output. Right channel is mapped on the right output.
0	1	Left channel is duplicated on both output channels.
1	0	Right channel is duplicated on both output channels.
1	1	Right and left channels are toggled.

5.5 GPSO_CONFIGURATION registers description

5.5.1 OUTPUT_CONF :

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	X	0C2	OC1	OC0

Address : 0x66 (102)

Type : RW - DEC

Software Reset : 0

Description

Table 12.

Bit fields	Comment
OC0	Configuration of gpso : 0 : take embedded default configuration. 1 : configure gpso from register GPSO_CONF.

Table 12.

Bit fields	Comment
OC1	Use of block PCM to generate clocks (PCMCK, LRCK & BCK): 0 : no use. 1 : use it.
OC2	Configuration of PCM block: 0 : take embedded default configuration. 1 : configure PCM block from PCM_DIV & PCM_CONF registers.

Note: that embedded default configuration for GPSO can be retrieved by user thanks to following setting :

– GPSO_CONF = b00000011;

Note: that embedded default configuration for PCM block is described at previous chapter.

5.5.2 GPSO_CONF :

b7	b6	b5	b4	b3	b2	b1	b0
CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0

Address : 0x6A (106)

Type : RW - DEC

Software Reset : 0

Description :

If OUTPUT_CONF == 1, this register configure the GPSO interface

Table 13. .

Bit fields	Comment
CF0	Polarity of GPSO_CK : 0 : data provided on rising edge & stable on falling edge 1 : data provided on falling edge & stable on rising edge
CF1	Polarity of GPSO_REQ : 0 : data are valid when GPSO_REQ is high 1 : data are valid when GPSO_REQ is low
CF[7:2]	Reserved : to be set to 0.

5.6 I²Sin_CONFIGURATION registers description

5.6.1 INPUT_CONF :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0x5A (90)

Type : RW - DEC

Software Reset : 0

Description :

If set to 1 enable the configurability of the I²Sin Input thanks to following registers, else disable this configurability and take embedded default configuration for I2Sin registers.

Note that this embedded default configuration can be retrieved by user thanks to following setting :

- I_AUDIO_CONFIG_1 = b00000110;
- I_AUDIO_CONFIG_2 = b11100000;
- I_AUDIO_CONFIG_3 = b00000001;

5.6.2 I_AUDIO_CONFIG_1:

b7	b6	b5	b4	b3	b2	b1	b0
CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0

Address : 0x5B (91)

Type : RW - DEC

Software Reset : 0

Description :

If INPUT_CONF == 1, this register configure the I²Sin interface.

Table 14.

Bit fields	Comment
CF0	Relative synchro : 0 : synchro with first data bit 1 : synchro one bit before first data bit
CF1	Data reception configuration : 0 : LSB first 1 : MSB first
CF2	Polarity of bit clock BCK : 0 : data provided on falling edge & stable on rising edge. 1 : data provided on rising edge & stable on falling edge

Table 14.

Bit fields	Comment
CF3	Polarity of LR clock LRCK : 0 : negative 1 : positive
CF4	Start value of LRCK : combined with CF3, this bit enable user to determine left/right couple according to the following table.
CF[7:5]	Reserved : to be set to 0.

Table 15.

CF3	CF4	Left/Right couples
0	0	(data1/data2), (data3/data4),...
1	0	(data0/data1), (data2/data3),...
0	1	(data0/data1), (data2/data3),...
1	1	(data1/data2), (data3/data4),...

5.6.3 I_AUDIO_CONFIG_2 :

b7	b6	b5	b4	b3	b2	b1	b0
LR7	LR6	LR5	LR4	LR3	LR2	LR1	LR0

Address : 0x5C (92)

Type : RW - DEC

Software Reset : 0

Description :

See I_AUDIO_CONFIG_3 register description..

5.6.4 I_AUDIO_CONFIG_3 :

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0	LR9	LR8

Address : 0x5D (93)

Type : RW - DEC

Software Reset : 0

Description :

If INPUT_CONF == 1, this register is used to configure the phase of the LRCK of the I^2Sin.

Table 16.

Bit fields	Comment
LR[4:0]	Position of the data within the LRCK phase : - if CF1 = 0 (LSB), value must be set to[31 - SL[9:5] - bit position of the first bit of data within the LRCK phase]. - if CF1 = 1 (MSB), value must be set to bit position of the first bit of data within the LRCK phase. *Note: that range of value for this bit position is [0:31].*
LR[9:5]	Length-1 of the data. Max value is 31.
LR[15:10]	Reserved : to be set to 0

5.7 SDI_CONFIGURATION registers description

5.7.1 POL_REQ :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0x59 (89)

Type : WO - DEC

Software Reset : 0

Description :

This register manage the polarity of the data REQ signal DREQ of the BS input interface.

If set to 0, data are requested when REQ = 0.

If set to 1, data are requested when REQ = 1.

5.7.2 INPUT_CONF :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0x5A (90)

Type : RW - DEC

Software Reset : 0

Description :

If set to 1 enable the configurability of the BSB input interfaces in burst mode thanks to following register, else disable this configurability and take embedded default configuration.

Note that this embedded default configuration can be retrieved by user thanks to following setting :

– I_AUDIO_CONFIG1 = b00000000;// polarity choice

5.7.3 I_AUDIO_CONFIG_1 :

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0	0	CF0

Address : 0x5B (91)

Type : RW - DEC

Software Reset : 0

Description :

If INPUT_CONF == 1, this register is used to configure BSB bit clock

Table 17. .

Bit	Comment
CF0	Polarity of bit clock BS_BCK : 0 : data provided on falling edge & stable on rising edge. 1 : data provided on rising edge & stable on falling edge.

5.8 COMMAND registers description

5.8.1 SOFT_RESET :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0x10 (16)

Type : WO - DWT

Software Reset : 0

Description :

When user write 1 in this register, a soft reset occurs. The core command register and the interrupt register are cleared. The decoder goes into idle mode.

5.8.2 CK_CMD :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0x3A (58)

Type : WO - DBO

Software Reset : 1

Hardware Reset : 1

Description :

After a soft reset, user must write 0 in CK_CMD to run the core clock of the chip. This will begin the boot of the chip, and so get it out of its idle state.

5.8.3 DEC_SEL :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0x55 (85)

Type : RW - DEC

Software Reset : 0

Description :

This register select the encoder/decoder data flux according the mode written in following table

Table 18. .

Bit(7:0)	Mode
10	SINE (test mode chip alive)
18	SBC decoder
19	ADC/GPSO SBC encoder
21	SDI/GPSO SBC encoder
22	ADC/SDO SBC encoder
Note: available modes depends on patch code used	

5.8.4 RUN :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0x56 (86)

Type : RW - DEC

Software Reset : 0

Description :

- When a software reset occurs, register RUN is reset (value 0) by the dsp (see I).
- When boot routines are finished, the dsp write inside RUN register the value 2 : this is the start of the external configuration period (start of DEC : see I).
- When the external device wants to end the external configuration period, it must write the value 1 inside the register RUN: this is the run command that starts the decoding process (see I).

5.8.5 CRC_IGNORE :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0x52 (82)

Type : RW - ABO

Software Reset : 0

Description :

For decoders having CRC abilities (see each decoder configuration), if set to 0 enable the check of CRC, if set to 1 disable the check of the CRC.

5.8.6 MUTE :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0x53 (83)

Type : RW - ABO

Software Reset : 0

Description :

For decoders having MUTE abilities (see each decoder configuration), if set to 0 disable the mute of the decoder, if set to 1 enable the mute of the decoder. Note that during a MUTE the input stream keeps on entering.

5.8.7 SKIP :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0x57 (87)

Type : RW - ABO

Software Reset : 0

Description :

For data flux using USSB Input, if SKIP == n>2, decoder skip (n-1) out of n frames. Note that maximum value for n is 8, and if n==0 or n==1, no frames is skipped.

5.8.8 PAUSE :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0x58 (88)

Type : RW - ABO

Software Reset : 0

Description :

For decoders having PAUSE abilities (see each decoder configuration), if set to 0 disable the pause of the decoder, if set to 1 enable the pause of the decoder. Note that during a PAUSE the input stream is stopped.

5.9 STATUS registers description

5.9.1 STATUS_MODE :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0xCC (204)

Type : RO - EDF

Software Reset : 0

Description :

This register give the type of the currently decoded bitstream.

5.9.2 STATUS_CHANS_NB :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0xCD (205)

Type : RO - EDF

Software Reset : 0

Description :

This register gives the number of channel currently decoded.

5.9.3 STATUS_SF :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0xCE (206)

Type : RO - EDF

Software Reset : 0

Description :

This register gives the index of the sampling frequency of the stream currently decoded. Note that sampling frequency indexes are given by table 5

5.9.4 STATUS_FE :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0x6F (111)

Type : RO - AEC

Software Reset : 0

Description :

This register give the status of the synchronization process according following table.

Table 19.

Value	Level
0	Syncrho not started
1	Syncword found
2	Syncword search
3	Syncword hard to find

5.9.5 HEADER _n:

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0xD4 (212) to 0xD9 (217)

Type : RO - EDF

Software Reset : 0

Description :

This register give the nth byte of the header of the frame currently decoded

5.10 MIX_CONFIGURATION registers description

5.10.1 MIX_MODE:

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0x7B (123)

Type : RW - ABO

Software Reset : 2

Description :

This register selectes the mode of mix/volume control

Table 20. :

Value	Mode
0	diseable mix/volume control
1	volume control
2	mono to stereo (up-mix)
3	stereo to mono (down-mix)

5.10.2 MIX_DLA:

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0x7C (124)

Type : RW - ABO

Software Reset : 0

Description :

This register specifies the direct left attenuation (in dB).

5.10.3 MIX_DLB:

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0x7D (125)

Type : RW - ABO

Software Reset : 0

Description :

This register specifies the left attenuation (in dB) on rigth channel.

5.10.4 MIX_DRA:

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0x7E (126)

Type : RW - ABO

Software Reset : 0

Description :

This register specifies the direct right attenuation (in dB).

5.10.5 MIX_DRB:

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0x7F (127)

Type : RW - ABO

Software Reset : 0

Description :

This register specifies the rigth attenuation (in dB) on left channel.

5.11 TONE_CONFIGURATION registers description

5.11.1 TONE_ON:

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0x75 (117)

Type : RW - ABO

Software Reset : 0

Description :

This register enables/diseables (1/0) the tone control.

5.11.2 TONE_FCUTH :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0x76 (118)

Type : RW - ABO

Software Reset : 20

Description :

This register specifies the high cut frequency: fcut(in Hz)=(TONE_FCUTH+1)*50.

5.11.3 TONE_FCUTL :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0x77 (119)

Type : RW - ABO

Software Reset : 10

Description :

This register specifies the low cut frequency: fcut(in Hz) = (TONE_FCUTL+1)*10

5.11.4 TONE_GAINH :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0x78 (120)

Type : RW - ABO

Software Reset : 12

Description :

This register specifies the gain on high frequencies: gain(in Db)=(TONE_GAINH-12)*1.5

5.11.5 TONE_GAINL :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0x79 (121)

Type : RW - ABO

Software Reset : 12

Description :

This register specifies the gain on high frequencies: gain (in Db)=(TONE_GAINL-12)*1.5. Value of register from 0 to 24.

5.11.6 TONE_GAIN_ATTEN :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0x7A (122)

Type : RW - ABO

Software Reset : 0

Description :

This register specifies the attenuation on global spectrum: gain (in dB)=-TONE_GAIN_ATTEN*1.5. Value of register from 0 to 12.

6 TABLES

Table 21. values to configure audio PLL for ofact==256.

This table give values to configure the audio PLL according CRYCK so that to generate a PCMCK == 256*SF.

Register	CRYCK in MHz 10	CRYCK in MHz 14.31818	CRYCK in MHz 14.7456
PLL_AUDIO_PEL_192	42	58	85
PLL_AUDIO_PEH_192	169	187	85
PLL_AUDIO_NDIV_192	0	0	0
PLL_AUDIO_XDIV_192	3	3	0
PLL_AUDIO_MDIV_192	18	12	2
PLL_AUDIO_PEL_176	56	54	0
PLL_AUDIO_PEH_176	16	118	64
PLL_AUDIO_NDIV_176	0	0	0
PLL_AUDIO_XDIV_176	3	2	3
PLL_AUDIO_MDIV_176	17	8	11

Table 22. values to configure audio PLL for ofact==384

This table give values to configure the audio PLL according CRYCK so that to generate a PCMCK == 384*SF.

Register	CRYCK in MHz 10	CRYCK in MHz 14.31818	CRYCK in MHz 14.7456
PLL_AUDIO_PEL_192	224	108	0
PLL_AUDIO_PEH_192	190	76	0
PLL_AUDIO_NDIV_192	0	0	0
PLL_AUDIO_XDIV_192	1	1	1
PLL_AUDIO_MDIV_192	13	9	9
PLL_AUDIO_PEL_176	42	54	0
PLL_AUDIO_PEH_176	140	118	48
PLL_AUDIO_NDIV_176	0	0	0
PLL_AUDIO_XDIV_176	1	1	1
PLL_AUDIO_MDIV_176	12	8	8

Table 23. values to configure audio PLL for ofact==512.

This table give values to configure the audio PLL according CRYCK so that to generate a PCMCK == 512*SF.

Register	CRYCK in MHz 10	CRYCK in MHz 14.31818	CRYCK in MHz 14.7456
PLL_AUDIO_PEL_192	42	58	85
PLL_AUDIO_PEH_192	169	187	85
PLL_AUDIO_NDIV_192	0	0	0
PLL_AUDIO_XDIV_192	1	0	1
PLL_AUDIO_MDIV_192	18	5	12
PLL_AUDIO_PEL_176	56	157	0
PLL_AUDIO_PEH_176	16	157	64
PLL_AUDIO_NDIV_176	0	0	0
PLL_AUDIO_XDIV_176	1	1	1
PLL_AUDIO_MDIV_176	17	11	11

Table 24. values to configure system PLL for SYSCK.

This table give values to configure the system PLL according CRYCK so that to generate a SYSCK == 50MHz. or SYSCK == 42.5MHz.

Register	CRYCK in MHz 10	CRYCK in MHz 14.31818	CRYCK in MHz 14.7456
PLL_SYSTEM_PEL_50	162	0	28
PLL_SYSTEM_PEH_50	11	0	152
PLL_SYSTEM_NDIV_50	0	0	0
PLL_SYSTEM_XDIV_50	1	1	1
PLL_SYSTEM_MDIV_50	19	13	12
PLL_SYSTEM_PEL_42_5	0	126	100
PLL_SYSTEM_PEH_42_5	0	223	135
PLL_SYSTEM_NDIV_42_5	0	0	0
PLL_SYSTEM_XDIV_42_5	1	1	1
PLL_SYSTEM_MDIV_42_5	16	10	10

Table 25. index of the Sampling Frequency

Index	Frequency
0	48 kHz
1	44.1 kHz
2	32 kHz
4	96 kHz
5	88.2 kHz

Table 25. index of the Sampling Frequency

Index	Frequency
6	64 kHz
8	24 kHz
9	22.05 kHz
10	16 kHz
12	12 kHz
13	11.025 kHz
14	8 kHz
16	192 kHz
17	176.4 kHz
18	128 kHz
3, 7, 11, 15 or 19	illegal frequency

6.1 Notations

ABO : After BOot (see I).

AEC : After External Config (see I).

BCK: Bit ClocK

BSA: BitStream input interface in Audio mode.

BSB: BitStream input interface in Burst mode.

BS: BitStream input interface.

BYPASSA : decoder BYPASS an Audio stream.

CD : input interface for CD.

CK : ClocK.

CRYCK: CRYstal ClocK provided to the chip by an external crystal.

DBO : During BOot (see I).

DEC : During External Config (see I).

DWT : During Whole Time (see I).

EDB : Every Decoded Block (see I).

EDF : Every Decoded Frame (see I).

LRCK: Left Right ClocK for an I2S interface.

ofact: oversampling factor for PCMCK (PCMCK == ofact * SF).

PCMCK: PCM ClocK (can be generated by the audio PLL).

SF: Sampling Frequency.

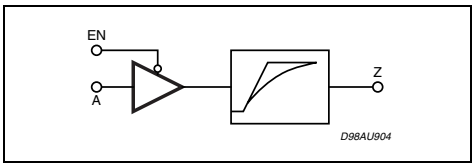
SYSCK: SYStem ClocK (clock of the core, can be generated by the system PLL).

X : don’t care.

7 I/O CELL DESCRIPTION

7.1 TTL Tristate Output Pad Buffer, 3V capable 4mA, with Slew Rate Control

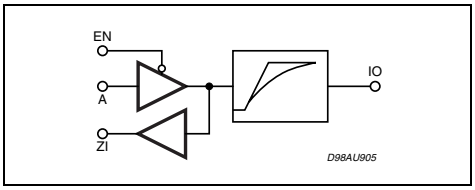
Pin numbers: 4, 18, 20, 21, 22, 25, 54, 56, 59



INPUT PIN	MAX LOAD
Z	100pF

7.2 TTL Schmitt Trigger Bidir Pad Buffer, 3V capable, 4mA, with Slew Rate Control

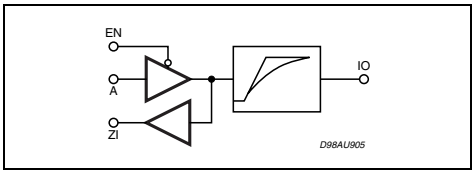
Pin numbers: 1, 2, 3, 7, 8, 9, 19



INPUT PIN	CAPACITANCE	OUTPUT PIN	MAX LOAD
IO	TBD	IO	100pF

7.3 TTL Schmitt Trigger Inpud Pad Buffer, 3V capable

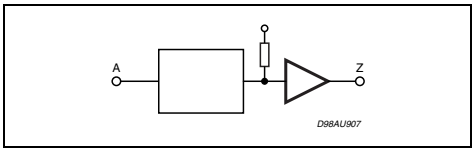
Pin numbers:17, 60, 63



INPUT PIN	CAPACITANCE
A	TBD

7.4 TTL Inpud Pad Buffer, 3V capable with Pull-Up

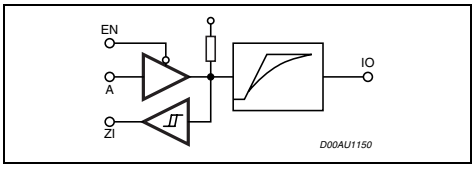
Pin numbers:15, 16



INPUT PIN	CAPACITANCE
A	TBD

7.5 TTL Schmitt Trigger Bidir Pad Buffer, with Pull-up, 4mA, with slew rate control / 3V capable

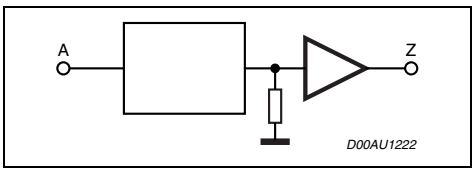
Pin numbers: 26, 27, 28, 31, 32, 33, 34, 35, 44, 45, 46, 47, 48, 49, 50, 51, 64



INPUT PIN	CAPACITANCE	OUTPUT PIN	MAX LOAD
IO	TBD	IO	100pF

7.6 TTL Input Pad Buffer, 3V capable, with pull down

Pin numbers: 12, 13, 14, 55



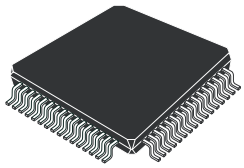
INPUT PIN	CAPACITANCE
A	TBD

8 Package Informations

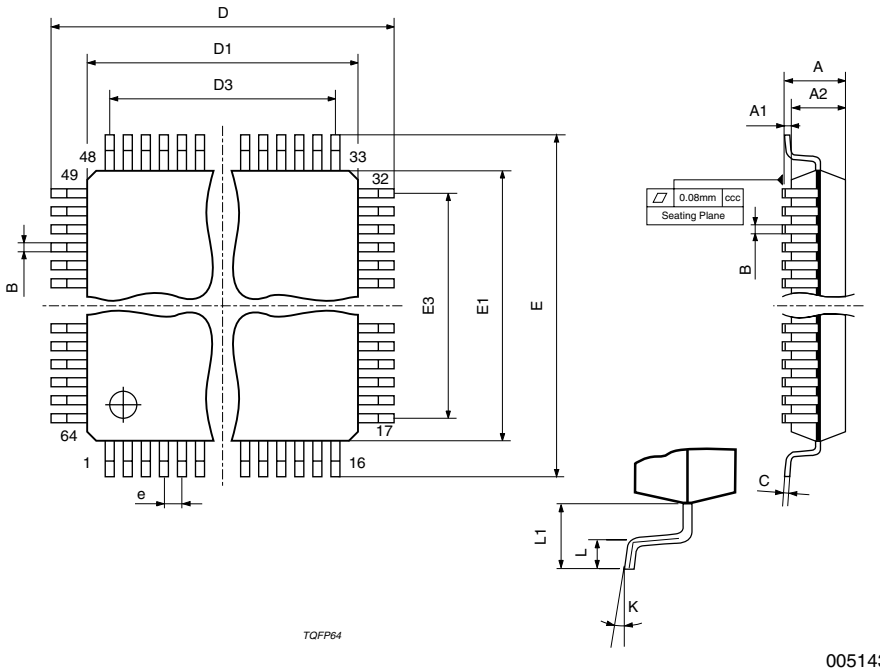
Figure 6. TQFP64 (10x10x1.4mm) Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.0066	0.0086	0.0106
C	0.09			0.0035		
D	11.80	12.00	12.20	0.464	0.472	0.480
D1	9.80	10.00	10.20	0.386	0.394	0.401
D3		7.50			0.295	
e		0.50			0.0197	
E	11.80	12.00	12.20	0.464	0.472	0.480
E1	9.80	10.00	10.20	0.386	0.394	0.401
E3		7.50			0.295	
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0393	
K	0˚ (min.), 3.5˚ (min.), 7˚(max.)					
ccc			0.080			0.0031

OUTLINE AND MECHANICAL DATA



TQFP64 (10 x 10 x 1.4mm)



9 Revision history

Date	Revision	Changes
1-sept-2005	1	Initial release.