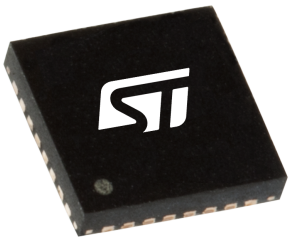
STA5635A

Datasheet

Automotive universal GNSS RF receiver



VFQFPN32L
(5x5x1.0 mm)

Features

- AEC-Q100 qualified
- Multi GNSS band support (L1/E1, L2C, L5/E5/E6/L6 and L band)
- Programmable IF bandwidth (7 or 13 MHz range)
- 1.62 V to 3.6 V supply voltage range
- Smart digital interface (JESD207-COMPATIBLE)
- Fractional-N synthesizer with embedded loop filter
- SPI interface for full programmability and interface to transmit L-band data bit
- 2 bit A/D converter
- Operating temperature range -40 °C ~ +105 °C
- CMOS040 technology
- VFQFPN 5x5x1.0 mm 32 leads package

Product status link
STA5635A

Product summary		
Order code	Package	Packing
STA5635A	VFQFPN32L 5x5x1.0 mm	Tray
STA5635ATR		Tape and reel

Description

The STA5635A is a fully integrated GNSS RF front-end able to support different bands (L1, L2, L5, L6 and L) thanks to a programmable and flexible RF-IF chain driven by a fractional PLL. In particular, G5RF is able to manage all the GNSS constellations available and planned in the next future like GPS, Galileo, Glonass, BeiDou, IRNSS and QZSS.

The RF_IF chain is followed by a 2-bit ADC able to convert the IF signal to sign (SIGN) and magnitude (MAG) bits. The MAG bit is internally used to control the variable gain amplifiers. The VGA gain can also be set via the SPI interface.

Additionally, the STA5635A is able to manage the L-band signal from 1525 to 1559 MHz, through a dedicated 10 bit ADC. In this case, the SPI interface is used to transmit raw L-band correction data to the host.

A digital interface, JESD207 compliant, is used to transmit GNSS data and clock to an external baseband.

The embedded fractional PLL allows supporting a wide range of reference clocks (the typical value is 26 MHz) and generates a sampling clock available for the baseband.

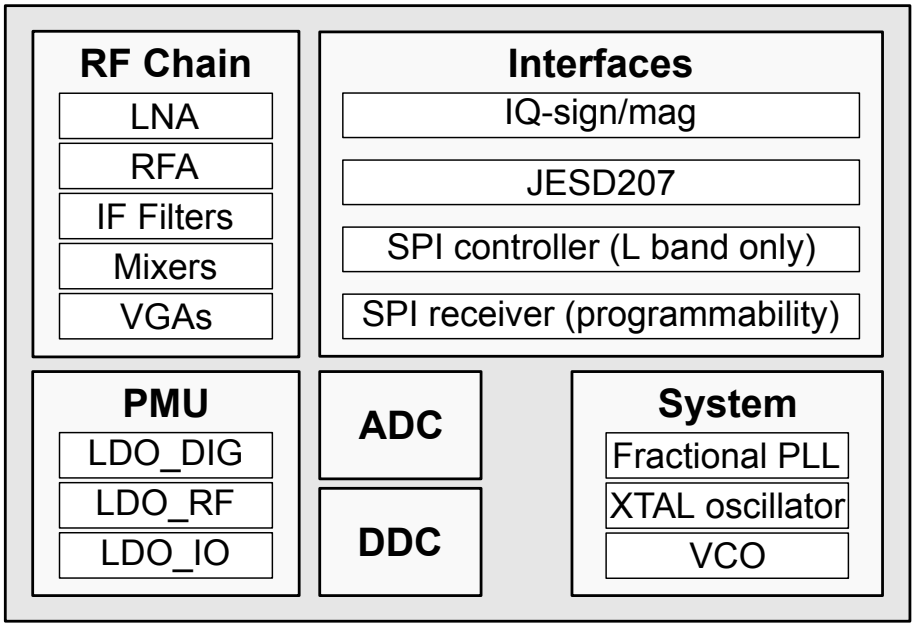
The STA5635A embeds two LDOs to supply at 1.1 V the analog and digital cores of the device facilitating requirements for external power supply. A third LDO can be turned-on to supply at 1.8 V external active components such as the TCXO.

The chip is manufactured in CMOS040nm technology and housed in a VFQFPN package.

1 Block diagram and pin description

1.1 Block diagram

Figure 1. **Block diagram**



1.2 Pin description

Figure 2. **Device pinout**

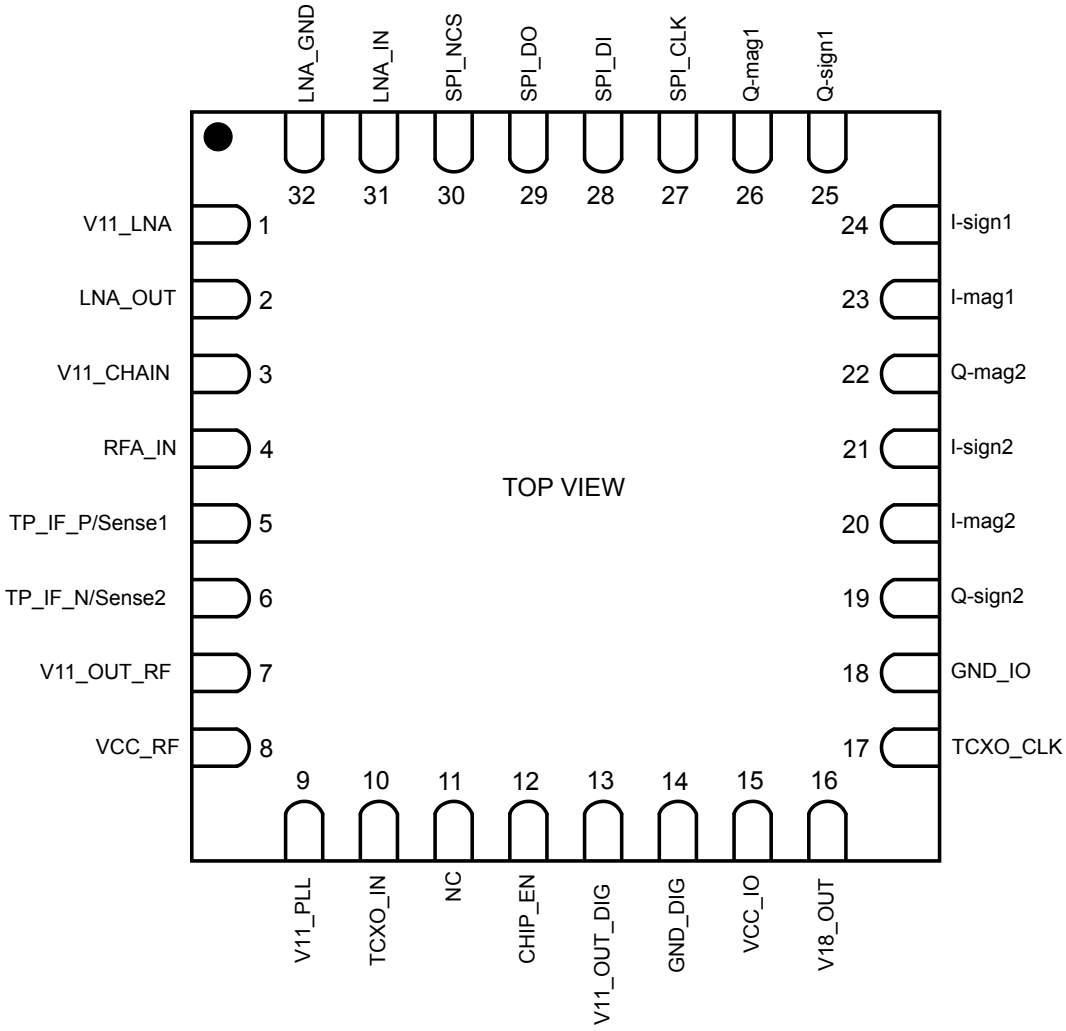


Table 1. **Pin function**

#	Name	Description	Supply domain	Type
1	V11_LNA	LNA power supply (1.1 V)	1.1 V	Supply
2	LNA_OUT	LNA output	1.1 V	Analog
3	V11_CHAIN	RF-IF chain power supply (1.1 V)	1.1 V	Supply
4	RFA_IN	RFA input, DC coupled	1.1 V	Analog
5	TP_IF_P/Sense1(1)	RF/IF receiver chain test positive output Antenna Sense1 input	1.8/3.3 V	Analog
6	TP_IF_N/Sense2(1)	RF/IF receiver chain test negative output Antenna Sense2 input	1.8/3.3 V	Analog
7	V11_OUT_RF	LDO RF output: supply (1.1 V) for RF section	1.1 V	Supply
8	VCC_RF	Voltage supply 1.62-3.6 V for LDO RF	1.8/3.3 V	Supply
9	V11_PLL	PLL power supply (1.1 V)	1.1 V	Supply
10	TCXO_IN	TCXO input (DC coupled)	1.1 V	Analog

#	Name	Description	Supply domain	Type
11	NC	Not connected	-	-
12	CHIP_EN	Enable for the whole chip	1.8/3.3 V	Digital
13	V11_OUT_DIG	LDO DIG output: power supply (1.1 V) for digital interface and IO ring	1.8/3.3 V	Supply
14	GND_DIG	Ground for digital	1.8/3.3 V	Ground
15	VCC_IO	Voltage supply 1.62-3.6 V for digital and IO LDOs	1.8/3.3 V	Supply
16	V18_OUT	LDO 1.8 V output: supply 1.8 V for external BOM	1.8/3.3 V	Supply
17	TCXO_CLK	TCXO buffered output at 1.1 V or at VCC_IO	1.8/3.3 V	Analog/Digital
18	GND_IO	I/Os ground	1.8/3.3 V	Ground
19	Q-sign2	Q-sign of secondary chain	1.8/3.3 V	Digital
20	I-mag2	I-mag of secondary chain	1.8/3.3 V	Digital
21	I-sign2	I-sign of secondary chain	1.8/3.3 V	Digital
22	Q-mag2	Q-mag of secondary chain	1.8/3.3 V	Digital
23	I-mag1	I-mag of main chain	1.8/3.3 V	Digital
24	I-sign1	I-sign of main chain	1.8/3.3 V	Digital
25	Q-sign1	Q-sign of main chain	1.8/3.3 V	Digital
26	Q-mag1[1]	Q-mag of main chain	1.8/3.3 V	Digital
27	SPI_CLK	Serial parallel interface clock	1.8/3.3 V	Digital
28	SPI_DI	Serial parallel interface data input	1.8/3.3 V	Digital
29	SPI_DO	Serial parallel interface data output	1.8/3.3 V	Digital
30	SPI_NCS	Serial parallel interface chip select	1.8/3.3 V	Digital
31	LNA_IN	LNA input, DC coupled	1.1 V	Analog
32	LNA_GND	Ground for LNA signal	1.1 V	Ground
EP	GND	Ground	-	Ground

1. *Selectable by SPI programming.*

1.3 I/O configurations

The digital I/O pins described in this section supports alternate functions. All the functions are described in the Table 2.

Table 2. Digital pin function

Main name	Description/function	Supply domain	Type
MCLK/Q_Sign2	Digital interface clock (clock decimator filter)	1.8/3.3 V	Digital
	Q-sign data of secondary main		
Enable/Q_Sign1	Enable for digital interface	1.8/3.3 V	Digital
	Q-sign data of main chain		
Q_Mag1	Q-mag data of main chain	1.8/3.3 V	Digital
D(0)/I_Sign1	I-sign and I-mag data of main chain	1.8/3.3 V	Digital
	I-sign data of main chain		
	Sign data real of main chain		
D(1)/I_Mag1	Q-sign and Q-mag data of main chain	1.8/3.3 V	Digital
	I-mag data of main chain		
	Mag data real of main chain		
D(2)/Q_Mag2	Q-mag data of secondary chain	1.8/3.3 V	Digital
	GNSS clock ($64f_0$)		
D(3)/I_Sign2	I-sign and I-mag data of secondary chain	1.8/3.3 V	Digital
	I-sign data of secondary chain		
	Sign data real of secondary chain		
D(4)/I_Mag2	Q-sign and Q-mag data of secondary chain	1.8/3.3 V	Digital
	I-mag data of secondary chain		
	Mag data real of secondary chain		
TCXO_CLK	TCXO output buffered signal at VCC_IO	1.8/3.3 V	Digital
	TCXO output buffered signal at 1V1		
	CLK $64f_0$ (out of H divider) at VCC_IO		
	MCLK at VCC_IO (clock decimator filter)		

The functionality of these pins can be configured by using SPI register #52.

2 Power management and start-up strategy

The 3.3 V (or 1.8 V) external supply voltage must be applied to the VCC_RF and VCC_IO pins. The CHIP_EN pin must be tied to the same supply voltage with and RC network (1 kΩ, 1 µF).

When the 3.3 V (or 1.8 V) external power supply is applied and the CHIP_EN is inactive (low state), the IC is in standby mode ensuring the minimum leakage only current consumption. When CHIP_EN is raised, the internal LDOs and the XTAL oscillator are turned ON and after all the rest of the device. As already pointed out, it is mandatory to delay the CHIP_EN rise (with an RC network) in respect to the main voltage supply rise to be sure that the internal LDOs are supplied before to enable them.

Figure 3. Power configuration

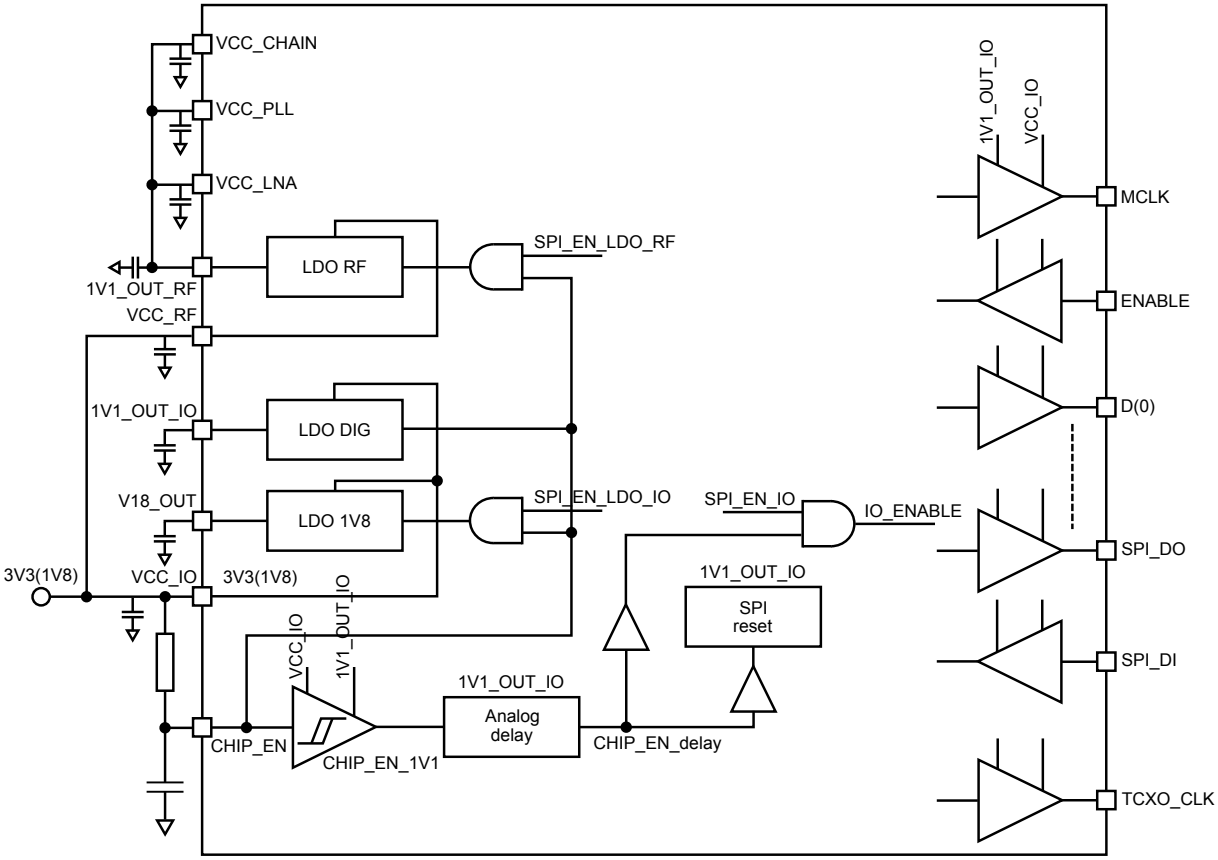
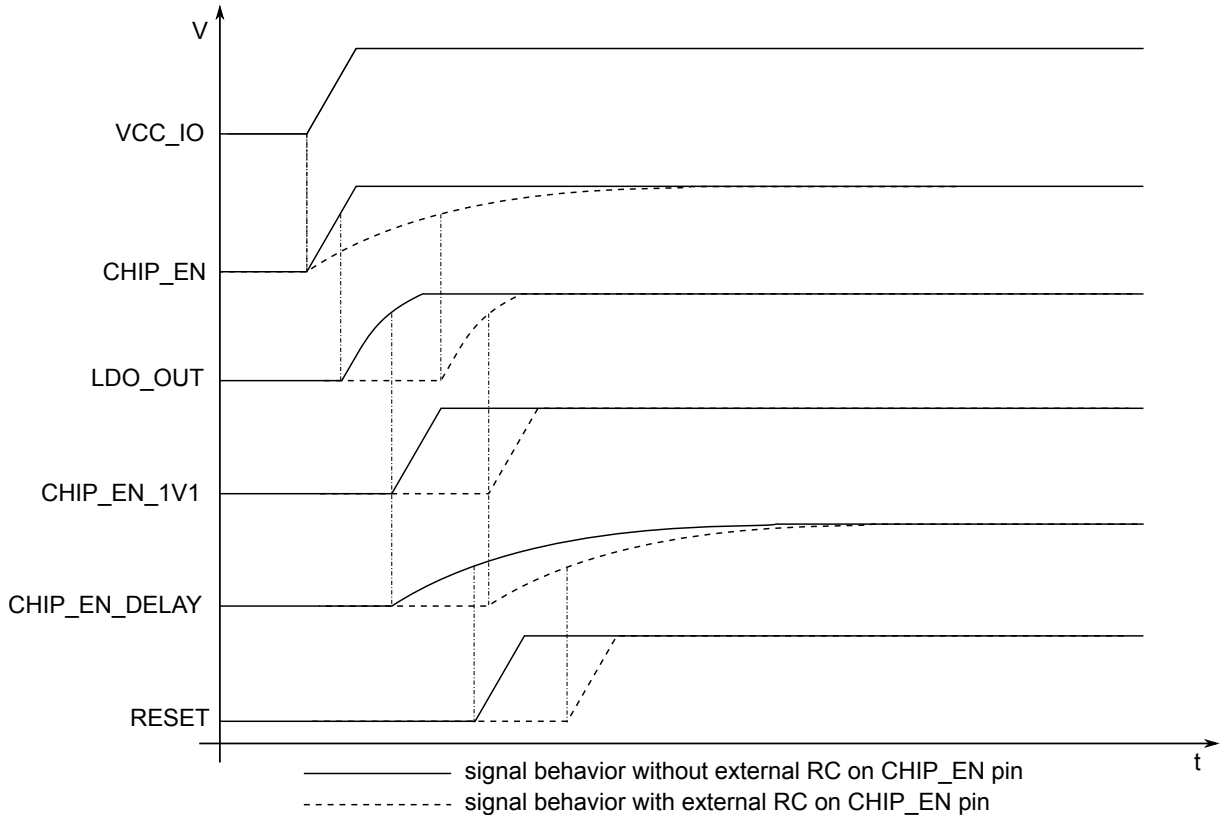


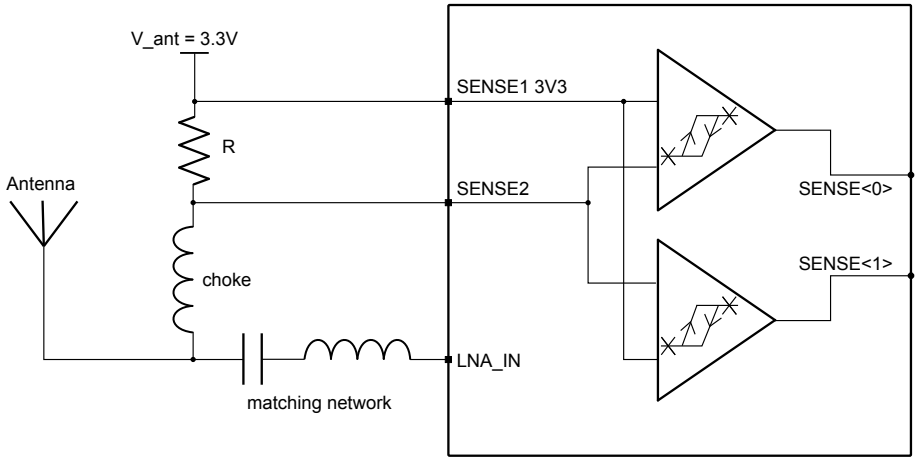
Figure 4. **Power-up strategy**



3 Antenna sensing

The Figure 5 shows an example of an antenna sensing circuit working with a 3.3 V antenna.

Figure 5. Antenna sensing configuration



The antenna status is monitored through the two SENSE bits transferred over the SPI interface and to the internal interrupt logic.

The following tables shows the antenna status current thresholds in case of R = 1.4 Ω and V_ant = 3.3 V in the case of rising and falling current.

Table 3. Thresholds when current is rising

Current from antenna (when current is rising)	SENSE <1>	SENSE <0>
I < 24 mA	0	0
24 ≤ I ≤ 62 mA	0	1
I > 62 mA	1	1

Table 4. Thresholds when current is falling

Current from antenna (when current is falling)	SENSE <1>	SENSE <0>
I > 53 mA	1	1
16 ≤ I ≤ 53 mA	0	1
I < 16 mA	0	0

4 Electrical specifications

4.1 Parameter conditions

Unless otherwise specified, all voltages are referred to GND.

4.2 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices.

The STA5635A parts are tested at T = -40 °C and T = +105 °C.

4.3 Typical values

Unless otherwise specified, typical data are based on T_{AMB} = +25 °C, VCC_RF = VCC_IO = 3.3 V, V11_OUT_RF = V11_OUT_DIG = 1.1 V and V18_OUT = 1.8 V.

4.4 Absolute maximum ratings

Table 5. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
VCC_RF	Supply voltages	-0.3	3.9	V
VCC_IO	Supply voltages	-0.3	3.9	V
V18_OUT	Supply voltages	-0.3	1.98	V
V11_OUT_RF	Supply voltages	-0.3	1.25	V
V11_OUT_DIG	Supply voltages	-0.3	1.25	V
V11_LNA V11_PLL V11_CHAIN	Supply voltages	-0.3	1.25	V
TJ	Junction operating temperature	-40	125	°C
TS	Storage temperature	-65	150	°C
ESDHBM	Electrostatic discharge - Human body model	-	2	kV
ESDCDM	Electrostatic discharge - Charge device model	-	250	V

4.5 Thermal data

Table 6. Thermal data

Symbol	Parameter	Value	Unit
T_{AMB}	Ambient operating temperature	-40 to +105	°C
TR_{JA}	Thermal resistance Junction-Ambient	40	°C/W

4.6 Electrical characteristics

Table 7. **Electrical characteristics**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
SUPPLY						
VCC_RF	Analog input voltage		1.62	3.3	3.6	V
VCC_IO	Voltage supply for IOs, LDO_1V8 and LDO_DIG	If IO pins are supplied at 3.3 V	3.0	3.3	3.6	V
		If IO pins are supplied at 1.8 V (LDO_1V8 must be turned-off)	1.62	1.8	1.98	
ICC	RF current consumption	V_{CC} = 1.1 V Main/Secondary chain ON	17	28	39	mA
ICC_STBY	Standby power consumption	All blocks OFF, only VCC_RF and VCC_IO supplied	-	4	6	µA
VOLTAGE REGULATOR						
LDO_RF	Regulator output voltage		1.0	1.1	1.2	V
LDO_DIG	Regulator output voltage		1.0	1.1	1.2	V
LDO_1V8	Regulator output voltage		1.62	1.8	1.98	V
LNA						
Gp	Power gain	L1 band	10.5	17	24	dB
		L2-L5 band	10.5	18	25	
NF	Noise figure(1)	L1 band	-	1.7	-	dB
		L2-L5 band	-	1.7	-	
$LNAP_{\_1dB}$	Input compression point		-15	-	-	dBm
RFA - MIXER - IF FILTER - VGA						
GpRFA	RFA voltage gain(1)	Max gain	-	20	-	dB
		Min gain	-	0	-	dB
GC	Conversion gain (from RFA in to ADC input)	VGA and RFA at max gain	60	82	90	dB
		VGA and RFA at min gain	12	26	38	
Δ_{VGA}	VGA dynamic range		35	48	60	dB
$P_{\_1dB}$	RF-IF-VGA input compression point	In band RFA max, VGA max	-	-105	-	dBm
		In band RFA max, VGA min	-	-55	-	dBm
NF_{RF-IF}	RF-IF-VGA noise figure(1)	VGA and RFA at max gain in L1-L2-L5-L band	-	5	-	dB
BW	-1dBhigh freq corner IF filter		-	13	-	MHz
ATT	Aliasing frequency rejection(1)	F = 52 MHz (corner #1)	20	-	-	dB
CRYSTAL OSCILLATOR - FRACTIONAL SYNTHESIZER - VCO						
F_{XTAL}	XTAL frequency		-	26	-	MHz
P_{XTAL_IN}	Reference input signal sensitivity(1)	XTAL_IN pin DC blocked requested. Without crystal XTAL_OUT load < 5 pF	-20	-	-	dBm
R_{DIV}	Reference divider range(1)		1	-	63	–
N_{DIV}	Loop divider range(1)		56	-	2047	–

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Frac	PLL fractionality		-	18	-	bit
F_{LO}	LO operating frequency		2300	-	3300	MHz
DIGITAL INPUT - OUTPUT DC						
VIH_1V8	CMOS input high level	V_{CC_IO} = 1.8 V	0.75 * VCC_IO	-	0.3 + V_{CC_IO}	V
VIL_1V8	CMOS input high level	V_{CC_IO} = 1.8 V	-0.3	-	0.25 * V_{CC_IO}	V
VIH_3V3	CMOS input high level	V_{CC_IO} = 3.3 V	2.5	-	0.3 + V_{CC_IO}	V
VIL_3V3	CMOS input high level	V_{CC_IO} = 3.3 V	-0.3	-	0.6	V
VOH	CMOS output high level		V_{CC_IO} - 0.4	-	-	V
VOL	CMOS output low level		-	-	0.4	V

1. *Not tested in production, specified by design.*

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 VFQFPN32 (5x5x1 mm) package information

Figure 6. VFQFPN32 (5x5x1 mm) package outline

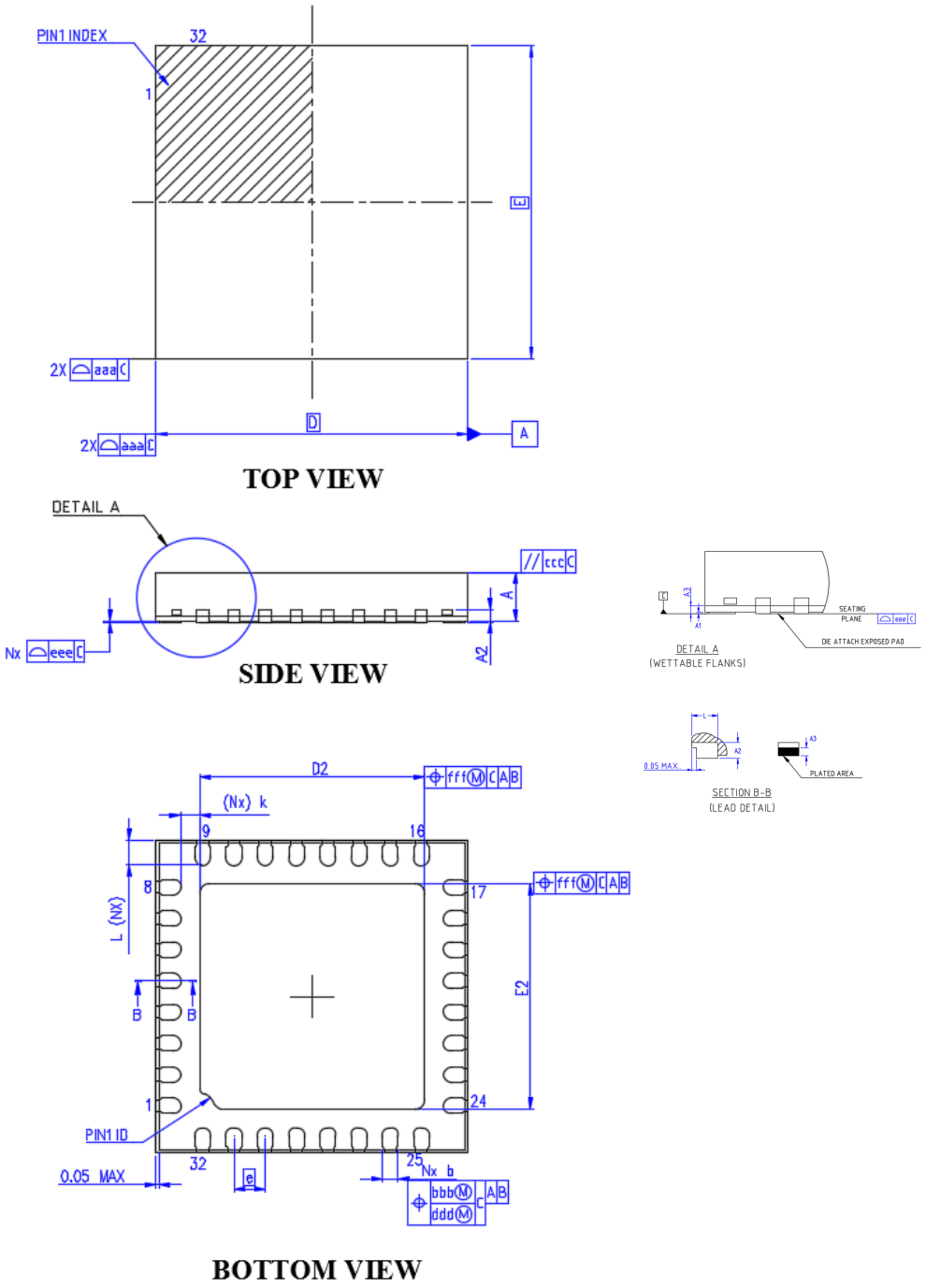


Table 8. **VFQFPN32 (5x5x1 mm) package mechanical data**

Ref.	Dimension (mm)			Note
	Min.	Typ.	Max.	
A	0.80	0.90	1.00	12
A1	0.00	-	0.05	9, 12
A2		0.2 REF.		-
A3	0.10	-	-	12
b	0.20	0.25	0.30	5, 6, 7, 12, 13
D		5.00 BSC		4, 12
D2	3.50	3.60	3.70	10, 12
e		0.50 BSC		12
E		5.00 BSC		4, 12
E2	3.50	3.60	3.70	10, 12
L	0.30	0.40	0.50	12, 13
k	0.20	-	-	-
N		32		8
Tolerance of form and position				
aaa		0.15		-
bbb		0.10		
ccc		0.10		
ddd		0.05		
eee		0.08		
fff		0.10		-
NOTE		112		-
REF		-		

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. All Dimensions are in millimeters
3. Terminal A1 identifier and terminal numbering convention shall conform to JEP95 SPP-002. Terminal A1 identifier must be located within the zone indicated on the outline drawing. Topside terminal A1 indicator may be a molded, or metalized feature. Optional indicator on bottom surface may be a molded, marked or metallized feature.
4. Outlines with “D” and “E” increments less than 0.5 mm should be registered as “stand alone” outlines. These outlines should use as many of the algorithms and dimensions states in the design standard as possible to insure predictability in manufacturing.
5. Dimension ‘b’ / ‘b1’ / ‘b2’ applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension ‘b’ / ‘b1’ / ‘b2’ should not be measured in that radius area.
6. Inner edge of corner terminals may be chamfered or rounded in order to achieve minimum gap “k”. This feature should not affect the terminal width “b” / ‘b1’ / ‘b2’, which is measured L/2 from the edge of the package body.
7. Exact shape of the leads at the edge of the package is optional.

8. “N” is the maximum number of terminal positions for the specified body size. Depopulation is allowed, but only under the following conditions.
   – Depopulation scheme must be consistent in each quadrant of the package.
   – Non-symmetric variations should be broken out as separate mechanical outline variations, including depopulation graphics.
9. A1 is defined as the distance from the seating plane to the lowest point on the package body (standoff).
10. Dimension D2 and E2 refer to exposed pad.
11. Tolerance of Form and Position.
12. Critical dimensions:
    12.1 A
    12.2 A1
    12.3 A3
    12.4 D and E
    12.5 B and L
    12.6 e
    12.7 D2 and E2
13. Dimensions “b” / ‘b1’ / ‘b2’ and “L” are measured at terminal plating surface.

Revision history

Table 9. **Document revision history**

Date	Version	Changes
26-Mar-2019	1	Initial release.
02-Dec-2020	2	RPN in production data. Updated *Figure 1*. Deleted old chapter 2, 3, 4, 5,and Appendix.
27-Feb-2024	3	Updated: • *Section Description*; • *Section 2: Power management and start-up strategy*; • *Section 3: Antenna sensing*; • *Section 4.6: Electrical characteristics*. Minor text changes.
17-Jun-2024	4	Updated: • Figure 3. Power configuration; • Section 5.1: VFQFPN32 (5x5x1 mm) package information. Minor text changes to improve readability.

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